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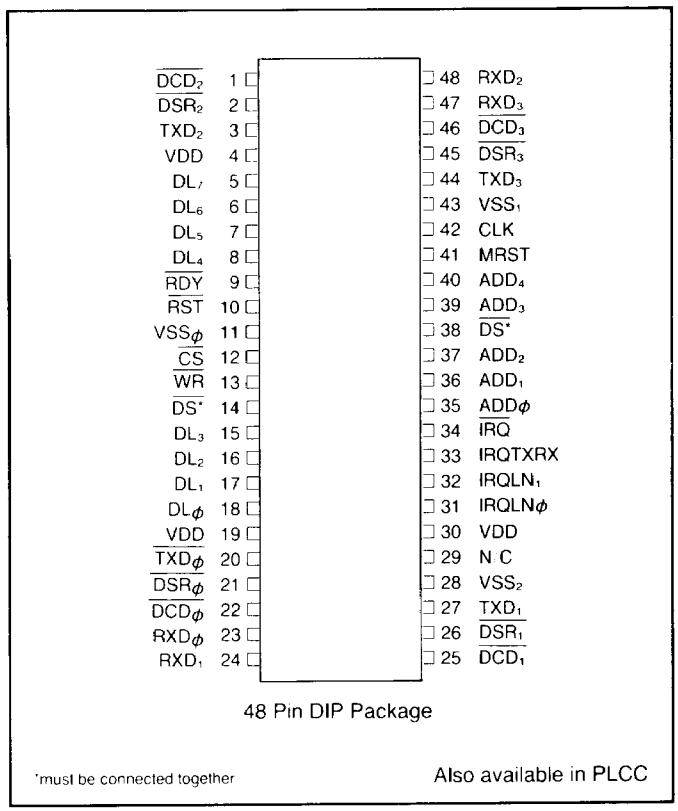
COM78804
PRELIMINARY

Four-channel Universal Asynchronous Receiver/Transmitter Quad UART

FEATURES

- ☐ Four independent full duplex serial data lines
- ☐ Programmable baud rates individually selectable for each line's transmitter/receiver (50 to 19,200 baud)
- ☐ Summary registers that allow a single read to detect a data set change or to determine the cause of an interrupt on any line
- ☐ Triple buffers for each receiver
- ☐ Device scanner mechanism that reports interrupt request due transmitter/receiver interrupts
- ☐ Independently programmable lines for interrupt-driven operation
- ☐ Modem status change detection for Data Set Ready (DSR) and Data Carrier Detect (DCD) signals
- ☐ Programmable interrupts for modem status changes
- ☐ Synchronizes critical read-only registers
- ☐ Single 5V Power Supply
- ☐ TTL Compatible

PIN CONFIGURATION



48 Pin DIP Package

*must be connected together

Also available in PLCC

GENERAL DESCRIPTION

The COM78804 Four-channel Asynchronous Receiver/Transmitter (Quad UART) is a VLSI device for new generations of asynchronous serial communication designs and for microcomputer systems. This device performs the basic operations necessary for simultaneous reception and transmission of asynchronous messages on four independent lines. Figure 1 is a functional block diagram of the COM78804 Quad UART.

90 RES Orig

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4795 SMC

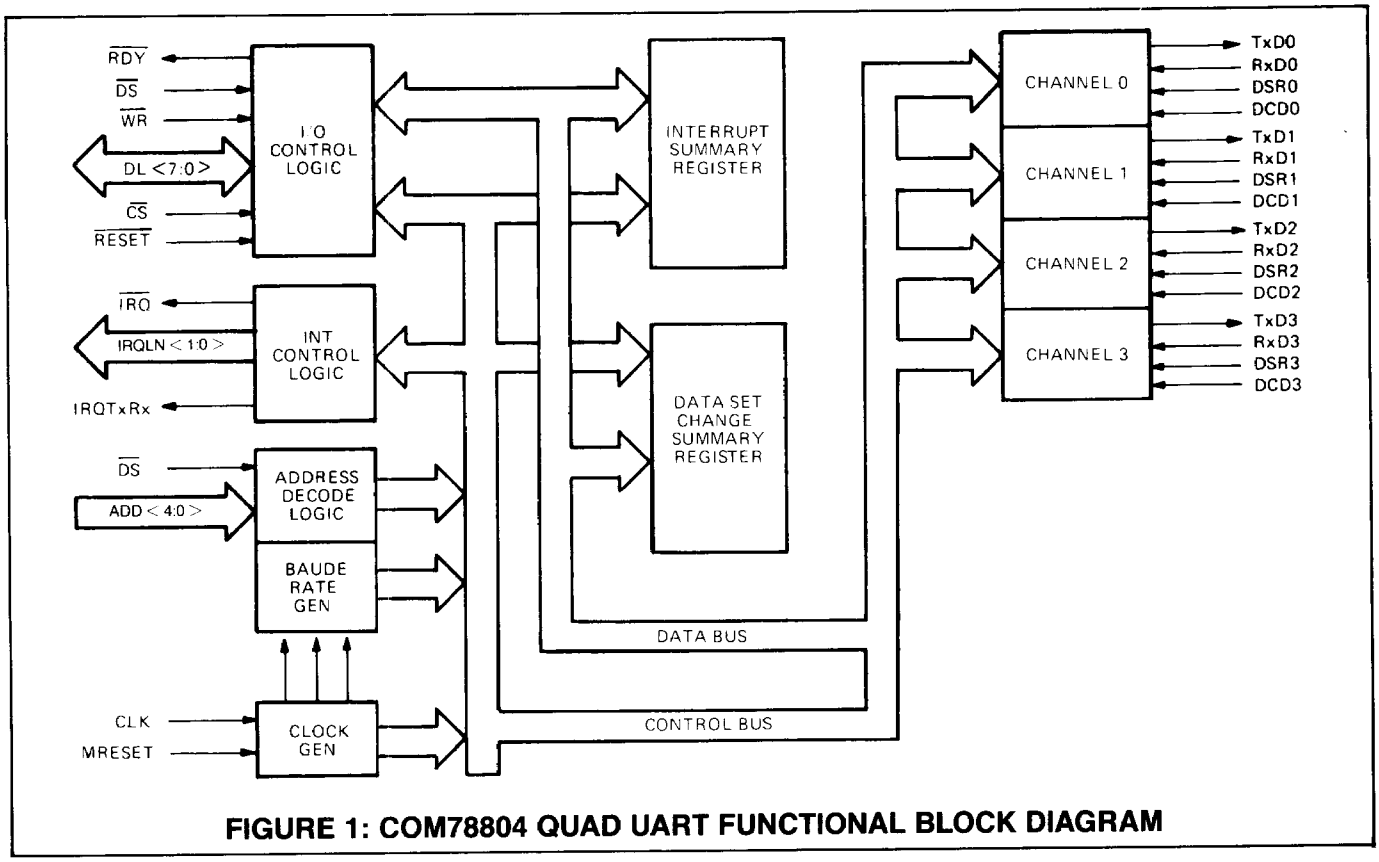


FIGURE 1: COM78804 QUAD UART FUNCTIONAL BLOCK DIAGRAM

TABLE 1–COM78804 PIN AND SIGNAL SUMMARY

Pin	Signal	Input/Output	Definition/Function
5-8,15-18	DL<7:0>	input/output	Data lines <7:0>–Receives and transmits the parallel data.
35-37,39,40	ADD<4:0>	input	Address<4:0>–Selects the internal registers in the Quad UART.
12	$\overline{CS}$	input	Chip select–Activates the Quad UART to receive and transmit data over the DL<7:0> lines.
14,38	$\overline{DS}$	input	Data strobe–Receives timing information for data transfers.
13	$\overline{WR}$	input	Write–Specifies direction of data transfer on the DL<7:0> lines.
9	$\overline{RDY}$	output	Ready–Indicates when the Quad UART is ready to participate in data transfer cycles.
10	$\overline{RESET}$	input	Reset–Initializes the internal logic.
41	MRESET	input	Manufacturing reset–For manufacturing use.
42	CLK	input	Clock–Clock input for timing.
2,21,26,45	$\overline{DSR}$<3:0>	inputs	Data set ready–Monitor data set ready (DSR) signals from modems.
1,22,25,46	$\overline{DCD}$<3:0>	inputs	Data set carrier detect–Monitor data set carrier detect (DCD) signals from modems.
34	$\overline{IRQ}$	output	Interrupt request–Requests a processor interrupt.
31,32	IRQLN<1:0>	output	Interrupt request line number–Indicates the line number of originating interrupt request.
33	IRQTxRx	output	Interrupt request transmit/receive–Indicates whether an interrupt request is for transmitting or receiving data.
3,20,27,44	TxD<3:0>	outputs	Transmit data–Provides asynchronous bit-serial data output streams.
23,24,47,48	RxD<3:0>	outputs	Receive data–Accepts asynchronous bit-serial data input streams.
4,19,30	V_{DD}	input	Voltage–Power supply voltage +5 Vdc.
11,28,43	V_{SS}	input	Ground–Ground reference

DATA AND ADDRESS

Data lines (DL<7:0>)–These lines are used for the parallel transmission and reception of data between the CPU and the Quad UART. The receivers are active when the data strobe ($\overline{DS}$) signal is asserted. The output drivers are active only when the chip select ($\overline{CS}$) signal is asserted, the data strobe ($\overline{DS}$) signal is asserted, and the write ($\overline{WR}$) signal is deasserted. The drivers will become inactive (high-impedance) within 50 nanoseconds when one or more of the following occurs: the chip select ($\overline{CS}$) signal is deasserted, the data strobe ($\overline{DS}$) signal is deasserted, or the write ($\overline{WR}$) signal is asserted.

Address (ADD<4:0>)–These lines select which Quad UART internal register is accessible through the data I/O lines (DL<7:0>) when the data strobe ($\overline{DS}$) and chip select ($\overline{CS}$) signals are asserted. Table 2 lists the addresses corresponding to each register. The receiver buffer and transmitter holding register for each line have the same address. When the ($\overline{WR}$) signal is deasserted, the address accesses the receiver buffer register and when asserted, it accesses the transmitter holding register.

TABLE 2–COM78804 REGISTERS ADDRESS SELECTION

ADD Line* <4>	<3>	<2>	<1>	<0>	Read/Write	Register
0	0	0	0	0	Read	Line 0 Receiver Buffer
0	0	0	0	0	Write	Line 0 Transmitter Holding
0	0	0	0	1	Read	Line 0 Status
0	0	0	1	0	Read/Write	Line 0 Mode Registers 1,2
0	0	0	1	1	Read/Write	Line 0 Command
0	1	0	0	0	Read	Line 1 Receiver Buffer
0	1	0	0	0	Write	Line 1 Transmitter Holding
0	1	0	0	1	Read	Line 1 Status
0	1	0	1	0	Read/Write	Line 1 Mode Register 1,2
0	1	0	1	1	Read/Write	LIne 1 Command
1	0	0	0	0	Read	Line 2 Receiver Buffer
1	0	0	0	0	Write	Line 2 Transmitter Holding
1	0	0	0	1	Read	Line 2 Status
1	0	0	1	0	Read/Write	Line 2 Mode Register 1,2
1	0	0	1	1	Read/Write	Line 2 Command
1	1	0	0	0	Read	Line 3 Receiver Buffer
1	1	0	0	0	Write	Line 3 Transmitter Holding
1	1	0	0	1	Read	Line 3 Status
1	1	0	1	0	Read/Write	Line 3 Mode Register 1,2
1	1	0	1	1	Read/Write	Line 3 Command
X	X	1	0	0	Read	Interrupt Summary
X	X	1	0	1	Read	Data Set Change Summary

*X = Either 0 or 1.

BUS TRANSACTION CONTROL

Chip select ($\overline{CS}$)–This signal is asserted to permit data transfers through the DL<7:0> lines to or from the internal registers. Data transfer is controlled by the data strobe ($\overline{DS}$) signal and write ($\overline{WR}$) signal.

Data strobe ($\overline{DS}$)– This input receives timing information for data transfers. During a write cycle, the CPU asserts the data strobe signal when valid output data is available and deasserts the data strobe signal before the data is removed. During a read cycle, the CPU asserts the data strobe signal and the Quad UART transfers the valid data. When the data strobe signal is deasserted, the DL<7:0> lines become a high impedance.

Write ($\overline{WR}$)–The write ($\overline{WR}$) signal specifies the direction of data transfer on the DL<7:0> pins. If the $\overline{WR}$ signal is asserted during a data transfer (the $\overline{CS}$ and $\overline{DS}$ signals asserted), the Quad UART is receiving data from DL<7:0>. If the $\overline{WR}$ signal is deasserted during a write data transfer, the Quad UART is driving data onto the DL<7:0> lines.

INTERRUPT REQUEST

Interrupt request $\overline{IRQ}$–The $\overline{IRQ}$ pin is an open drain output. The integral interrupt scanner asserts the IRQ signal when it has detected an interrupt condition on one of the four serial data lines.

Interrupt Request transmit/receive (IRQTxRx)—This signal indicates when the interrupt scanner in the Quad UART stops and asserts $\overline{IRQ}$ because of a transmitter interrupt condition (the IRQTxRx signal is asserted) or because of a receiver interrupt condition (the IRQTxRx signal is deasserted). The signal is valid only while $\overline{IRQ}$ is asserted. The state of IRQTxRx signal also appears as bit 0 of the interrupt summary register.

Interrupt request line number (IRQLN<1:0>)–These lines indicate the line number at which the Quad UART interrupt scanner stopped and asserted the interrupt request ($\overline{IRQ}$) signal. The number on these lines is valid only while the $\overline{IRQ}$ signal is asserted. Line IRQLN<1> is the high-order bit and the IRQLN<0> line is the low-order bit. The

state of these signals also appears as bits in the interrupt summary register: IRQLN<1> as bit 2, and IRQLN<0> as bit 1. Table 3 shows the line numbers corresponding to settings of IRQLN<1:0>.

TABLE 3–COM78804 INTERRUPT REQUEST LINE ASSIGNMENTS

IRQ Line <1>	IRQ Line <0>	Line
0	0	0
0	1	1
1	0	2
1	1	3

SERIAL DATA

Transmit data (TxD<3:0>)–These outputs transmit the asynchronous bit-serial data streams. They remain at a high level when no data is being transmitted and a low level when the TxBRK bit in the associated line's command register is set.

Receive data (RxD<3:0>)–These lines accept asynchronous bit-serial data streams. The input signals must remain in the high state for at least one-half bit time before a high-to-low transition is recognized. (A high-to-low transition is required to signal the beginning of a "start" bit and initiate data reception).

MODEM SIGNALS

Data set ready ($\overline{DSR}$<3:0>)–These four input pins, one for each serial data line on the COM78804, are typically connected via intervening level converters to the data set ready outputs of modems. A TTL low at a $\overline{DSR}$ pin causes the DSR bit (bit 7) in the corresponding line's status register to be asserted. A TTL high at a $\overline{DSR}$ pin causes the DSR bit in the corresponding line's status register to be deasserted. A change of this input from high-to-low, or low-to-high, causes the assertion of the data set change (DSCHNG) bit that corresponds to this line in the data set change summary register. Changes from one state to the other and back again that occur within one microsecond may not be detected.

Carrier detect (DCD<3:0>)–These four input pins, one for each serial data line of the Quad UART, are typically connected through intervening level converters to the received line signal detect (also called carrier detect) outputs of modems. A TTL low at a $\overline{DCD}$ pin causes the DCD bit of the corresponding line's status register to be deasserted. A change of this input from high-to-low, or low-to-high, causes the assertion of the data set change (DSCHNG) bit corresponding to this line in the data set change summary register. Changes from one state to the other and back again that occur within one microsecond may not be detected.

GENERAL CONTROL SIGNALS

Ready ($\overline{RDY}$)–The $\overline{RDY}$ pin is an open drain output. Upon detecting a negative transition of chip select ($\overline{CS}$), the Quad UART asserts the $\overline{RDY}$ signal to indicate readiness to take part in data transfer cycles. The $\overline{RDY}$ signal deasserts after the trailing edge of $\overline{CS}$.

Reset ($\overline{RESET}$)–When the $\overline{RESET}$ input in asserted, the TxD<3:0> lines are asserted and all internal status bits listed in the "Architecture Summary" discussion are cleared.

Manufacturing reset (MRESET)–This signal is for manufacturing use only and the input should be connected to ground for normal operation.

MISCELLANEOUS SIGNALS

Clock in (CLK)–All baud rates and internal clocks are derived from this input. Normal operating frequency is 4.9152 MHz ±0.1 percent and duty cycle is 50 percent ±5 percent.

POWER AND GROUND

Voltage (V_{DD})–Power supply 5 Vdc

Ground (V_{SS})–Ground reference

ARCHITECTURE SUMMARY

The Quad UART functions as a serial-to-parallel, parallel-to-serial converter/controller. It can be programmed by a microprocessor to provide different characteristics for each of its four serial data lines (stop bits, parity, character length, split baud rates, etc.)

Each serial line functions the same as a one-line UART-type device thereby reducing the number of chips and conserving space on communication devices that require multiple communications lines.

An integral interrupt scanner checks for device interrupt conditions on the four lines. Its scanning algorithm gives priority to receivers over transmitters. The scanner can also check for interrupts resulting from changes in modem control signals $\overline{DSR}$ and $\overline{DCD}$.

Line-specific Registers

Each of the four serial data lines in the Quad UART has a set of registers for buffering data into and out of the line and for external control of the line's characteristics. These registers are selected for access by setting the appropriate address on lines ADD<4:0>. Lines ADD<4:3> select one of the four data lines. Lines ADD<2:0> select the specific register for that line. Refer to Table 2 for the register address assignments.

Receiver buffer register–Each line's receiver consists of a character assembly register and a two-entry FIFO that is the receiver buffer register. When the RxEN bit in a line's command register is set, received characters are moved automatically into the line's receiver buffer as soon as they have been deserialized from the associated communications line. When there are characters in this FIFO, the RxRDY bit is set in the status register for the line.

The assertion of the RxRDY signal for a line that already has the RxIE bit of its command register set causes the interrupt scanner logic to stop and generate an interrupt condition (the $\overline{IRQ}$ signal is asserted). When the receiver buffer is read, the interrupt condition is cleared (the $\overline{IRQ}$ signal is deasserted) and the interrupt scanner resumes operation.

If there is another entry in a line's FIFO, the RxRDY bit remains asserted. When the interrupt scanner reaches this line again, the assertion of RxRDY causes the scanner to halt and assert the $\overline{IRQ}$ again.

Asserting the $\overline{RESET}$ signal or clearing the RxEN bit initializes the receiver logic of Quad UART. The RxRDY flag is cleared and the receiver buffer register outputs become undefined. Any data in the FIFO at that time is lost.

Transmitter holding register–Each line has a writable transmitter holding register. When the TxEN bit in the line's command register is set, characters are moved automatically from the output of this register into the transmitter serialization logic whenever the serialization logic becomes idle.

When this register is empty, the TxRDY bit in the line's status register is set. If the transmitter interrupt enable (TxIE) bit in the line's command register is also set, the interrupt scanner logic halts and generates an interrupt condition. If

a character is then loaded into the register, the interrupt is cleared and the scanner resumes operation.

Assertion of the $\overline{\text{RESET}}$ signal initializes the transmitter logic of the Quad UART. The TxRDY flag is cleared and the transmitter holding register's contents are lost. The transmitter enable (TxEN) bit in the line's command register is also cleared by $\overline{\text{RESET}}$. If at the end of the reset process, the TxEN is reasserted and TxRDY bit is reasserted. Software clearing of TxEN alone produces results different from the full $\overline{\text{RESET}}$ in that the transmitter holding register's contents are not lost; they are transmitted when TxEN is set again.

Status register–Each line has a read-only status register that provides information about the current state of the given line. This register indicates a line's readiness for transmission or reception of data and flags error conditions in its bit fields. Figure 3 shows the format of the status register. Table 3 lists the flag bits in each status register.

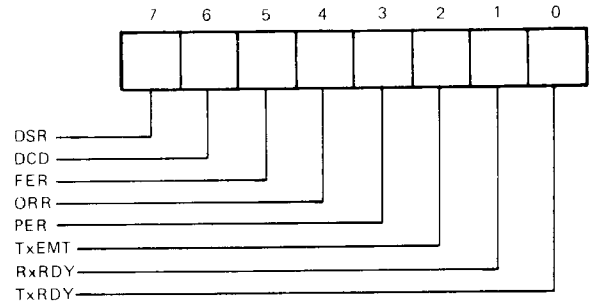


FIGURE 3: COM78804 STATUS REGISTERS (LINE 0-3) FORMAT

TABLE 4–COM78804 STATUS REGISTER (LINES 0-3) DESCRIPTION

Bit	Description
7	DSR (Data set ready)–This bit is the inverted state of the $\overline{\text{DSR}}$ line.
6	DCD (Data set carrier detect)–This bit is the inverted state of the $\overline{\text{DCD}}$ line.
5	FER (Frame error)–Set when the received character currently displayed in the receiver buffer register was not framed by a stop bit. Only the first stop bit is checked to determine that a framing error exists. Subsequent reading of the receiver buffer register that indicates all zeros (including the parity bit, if any) can be interpreted as a Break condition. This bit is cleared by clearing RxEN (bit 2) of the command register, by asserting the $\overline{\text{RESET}}$ input, or by setting the reset error RERR (bit 4) of the command register.
4	ORR (Overrun error)–Set when the character in the receiver buffer register was not read before another character was received. Cleared by clearing RxEN (bit 2) of the command register, by asserting the $\overline{\text{RESET}}$ input, or by setting reset error RERR (bit 4) of the command register.
3	PER (Parity error)–If parity is enabled and this bit is set, the received character in the receiver buffer register has an incorrect parity bit. This bit is cleared by clearing RxEN (bit 2) of the command register, by asserting the $\overline{\text{RESET}}$ input, by setting reset error RERR (bit 2) of the command register, or by reading the current character in the receiver buffer register.
2	TxEMT (Transmitter empty)–Set when the transmitter serialization logic for the associated line has completed transmission of a character, and no new character has been loaded into the transmitter holding register. Cleared by loading the transmitter holding register, by clearing TxEN (0) of the command register, or by asserting the $\overline{\text{RESET}}$ input.
1	RxRDY (Receiver buffer ready)–When set, a character has been loaded into the FIFO buffer from the deserialization logic. Cleared by reading the receiver buffer register, by clearing RxEN (bit 2) in the command register, or by asserting the $\overline{\text{RESET}}$ input.
0	TxRDY (Transmitter holding register ready)—When set, this bit indicates that the transmitter holding register is empty. Cleared when the program has loaded a character into the transmitter holding register, when the transmitter for this line is disabled by clearing TxEN (bit 0) in the command register, or by asserting the $\overline{\text{RESET}}$ input. This bit is initially set when the transmitter logic is enabled by the setting of TxEN (bit 0) and the transmitter holding register is empty. This bit is not set when the automatic echo or remote loopback modes are programmed. Data can be overwritten if a consecutive write is performed while TxRDY is cleared.

Mode registers 1 and 2—These read/write registers control the attributes (including parity, character length, and line speed) of the communications line.

Each of the four communications lines has two of these registers, both accessed by the same address on ADD<4:0>. Successive access operations (either read or write, in any combination) alternate between the two registers at that address by use of an internal pointer. The first operation addresses mode register 1, the next address mode register 2, and another after that would recycle the pointer to mode register 1. The pointer is reset to point to mode register 1 by $\overline{\text{RESET}}$ or by a read of the command register for this line. These registers should not be accessed by bit-oriented instructions that do read/modify/write cycles such as the PDP-11 BIS, BIC, and BIT instructions.

Figure 4 shows the format of mode registers 1 and Table 5 describes the function of the register information.

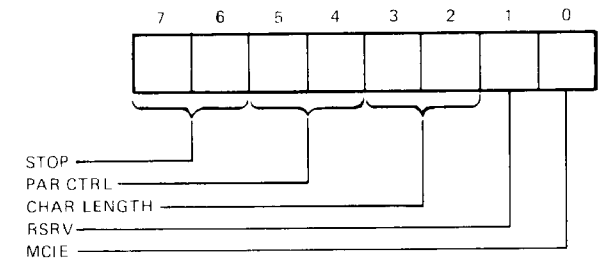


FIGURE 4–COM78804 MODE REGISTERS 1 (LINE 0-3) FORMAT

TABLE 5–COM78804 MODE REGISTER 1 (LINES 0-3) DESCRIPTION

Bit	Description
7,6	STOP–These bits determine the number of stop bits that are appended to the transmitted characters as follows. These bits are cleared by asserting the RESET input. **Bits** **Stop Bits** **7** **6** 0 0 Invalid 0 1 1.0 1 0 1.5 1 1 2.0
5,4	PAR CTRL (Parity control)–These bits determine parity as follows and are cleared by asserting the RESET input. X = either 1 or 0. **Bits** **Parity Type** **5** **4** 1 1 Even 0 1 Odd X 0 Disabled
3,2	CHAR LENGTH (Character length)–These bits determine the length (excluding start bit, parity, and stop bits) of the characters received and sent. Received characters of less than 8 bits are "right aligned" in the receiver buffer with unused high-order bits equal to zero. Parity bits are not shown in the receiver buffer. The character length bits are cleared by asserting the RESET input. The character length bits are defined as follows: **Bit** **Bit Length** **3** **2** 0 0 5 0 1 6 1 0 7 1 1 8
1	RSRV (Reserved and cleared by asserting the RESET input.)
0	MCIE (Modem control interrupt enable)–When set and RxIE (bit 5) of the command register is set, the modem control interrupts are enabled. Refer to the Interrupt Scanner and Interrupt Handling information. Cleared by asserting the RESET input.

Figure 5 shows the format of mode registers 2 and Table 5 indicates the baud rate selections of the register. Bits 7 through 4 of the mode register 2 control the transmitter baud rate and bits 3 through 0 control the receiver baud rate. These registers are cleared by asserting RESET input.

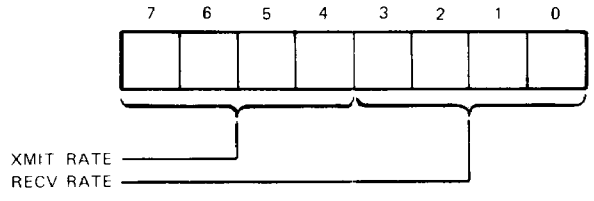


FIGURE 5–COM78804 MODE REGISTERS 2 (LINE 0-3) FORMAT

Command register–These read/write registers control various functions on the selected line. Figure 6 shows the format of the command registers and Table 6 describes the function of the register information.

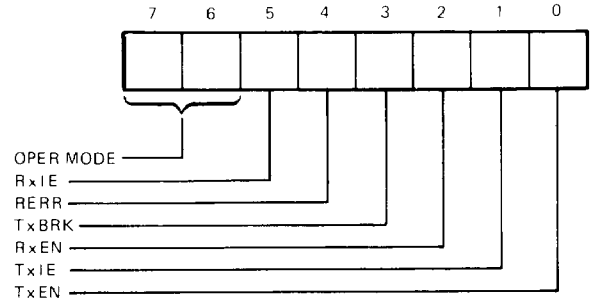


FIGURE 6–COM78804 COMMAND REGISTERS (LINE 0-3) FORMAT

TABLE 6–COM78804 MODE REGISTER 2 (LINES 0-3) DESCRIPTION

Bit	Description
7:0	XMIT RATE/RECV RATE (Transmitter/Receiver Rate)–Selects the baud rate of the transmitter (bits 7:4) and receiver (bits 3:0) as follows:

Transmitter Bits				Receiver Bits				Nominal	Actual	Error*
7	6	5	4	3	2	1	0	Rate	Rate	(percent)
0	0	0	0	0	0	0	0	50	same	—
0	0	0	1	0	0	0	1	75	same	—
0	0	1	0	0	0	1	0	110	109.09	0.826
0	0	1	1	0	0	1	1	134.5	133.33	0.867
0	1	0	0	0	1	0	0	150	same	—
0	1	0	1	0	1	0	1	300	same	—
0	1	1	0	0	1	1	0	600	same	—
0	1	1	1	0	1	1	1	1200	same	—
1	0	0	0	1	0	0	0	1800	1745.45	3.03
1	0	0	1	1	0	0	1	2000	2021.05	1.05
1	0	1	0	1	0	1	0	2400	same	—
1	0	1	1	1	0	1	1	3600	3490.91	3.03
1	1	0	0	1	1	0	0	4800	same	—
1	1	0	1	1	1	0	1	7200	6981.81	3.03
1	1	1	0	1	1	1	0	9600	same	—
1	1	1	1	1	1	1	1	19200	same	—

*The frequency of the clock input (CLK) is 4.9152 MHz. The clock input may vary by 0.1 percent. This variance results in an error that must be added to the error listed.

TABLE 7–COM78804 COMMAND REGISTER (LINES 0-3) DESCRIPTION

Bit	Description
7,6	OPER MODE (Operating mode)–These bits control the operating mode of the channel as follows. These bits are cleared by asserting the RESET input.

Bit		Operating Mode
7	6	
0	0	Normal operation
0	1	Automatic echo
1	0	Local loopback
1	1	Remote loopback

5	RxIE (Receiver interrupt enable)–When set, the RxRDY flag (bit 1) of the status register for this line will generate an interrupt.
4	RERR (Reset error)–When set, this bit clears the framing error, overrun error, and parity error of the status register associated with this line. This bit is cleared by asserting the RESET input (not self-clearing).
3	TxBRK (Transmit break)–When set, this bit forces the appropriate TxD<3:0> line to the spacing state at the conclusion of the character presently being transmitted. When the program clears this bit, normal operation is restored, and any character pending in the transmitter holding register is moved into the serialization logic and transmitted. The minimum break length obtainable is twice the character length plus 1 bit time. The maximum break length depends on the amount of time between the program setting and clearing this bit, but is an integral number of bit times. This bit is cleared by asserting the RESET input.
2	RxEN (Receiver enable)–When set, this bit enables the receiver logic. When cleared, it stops the assembling of the received character, clears all receiver error bits and the RxRDY (bit 1) of the status register, clears any receiver interrupt conditions associated with this line, and initializes all receiver logic. This bit is cleared by asserting the RESET input.
1	TxIE (Transmit interrupt enable)–When set, the state of the associated TxRDY flag (bit 0) of the status register is made available to the interrupt scanner logic. When the interrupt scanner logic scans this line, it determines if the TxRDY flag is asserted and generates an interrupt by asserting the IRQ signal.
0	TxEN (Transmitter enable)–When set, this bit enables the transmitter logic. When cleared, it inhibits the serialization of the characters that follow but the serialization of the current character is completed. It also clears the TxRDY flag (bit 0) of the status register, clears any transmitter interrupt conditions associated with this line, and initializes all transmitter logic except that associated with the transmitter holding register. The character in the transmitter holding register is retained so that XON/XOFF situations can be properly processed. This bit is cleared by asserting the RESET input.

Bits 5 through 0 enable the line's receiver and transmitter, enable handling of interrupts, initiate the transmission of break characters, and reset error bits for the line. Refer to "Interrupt Scanner" and "Interrupt Handling" paragraphs for detailed interrupt information. Bits 7 and 6 control the operating mode of the line. The four modes that can be set are:

- ☐ Normal operation–The serial data received is assembled in the receiver logic and transferred in parallel to the receiver buffer register. (The RxEN bit must be set.) Data to be transmitted is loaded in parallel into the transmitter holding register, then automatically transferred into the transmitter logic and serialized for transmission. (The TxEN bit must be set.)

- ☐ Automatic echo–The serial data received is assembled into parallel in the receiver logic (the RxEN bit must be set) and transferred to the receiver buffer register. Arriving serial data is also routed to the line's TxD<n> pin for serial output. TxEN is ignored and the transmitter logic is disabled. TxRDY flags and TxEMT indications are cleared. No transmitter interrupts are generated.
- ☐ Local loopback–The serial data from the RxD<n> input is ignored and the receiver serial input receives data from the transmitter serial output. The data is assembled into parallel form in the receiver logic (the RxEN bit must be set) and transferred to the receiver buffer register where it can be read by the program. Data to be transmitted to the receiver is loaded in parallel form into the transmitter holding register from which it is automatically moved into the transmitter logic and serialized for transmission. (The TxEN bit must be set.) The transmission goes only to the receiver serial input; the TxD<n> output is held high. As in normal operation, transmission and reception baud rates are controlled by the transmitter speed and receiver speed entries in mode register 2.
- ☐ Remote loopback–The serial data received on the RxD<n> line is returned to the TxD<n> line without further action. No data is received or transmitted. The RxRDY, TxRDY, and TxEMT flags are disabled. The TxEN and RxEN bits of the command register are held cleared, causing the transmitter and receiver logic to be disabled.

SUMMARY REGISTERS

The Quad UART contains two registers that summarize the current status of all four serial data lines, making it possible to determine that a line's status has changed with a single read operation. These registers are selected for access by setting the appropriate address on pins ADD <2:0>. Because the registers are shared by four serial lines, the line-selection bits (ADD <4:3>) are ignored when these registers are accessed. Refer to "Interrupt Scanner and Interrupt Handling" for detailed interrupt information.

Interrupt summary register–This read-only register indicates that a transmitter or receiver interrupt condition has occurred, and indicates the line number that generated the interrupt. Figure 7 shows the format of the interrupt summary register and Table 8 describes register information.

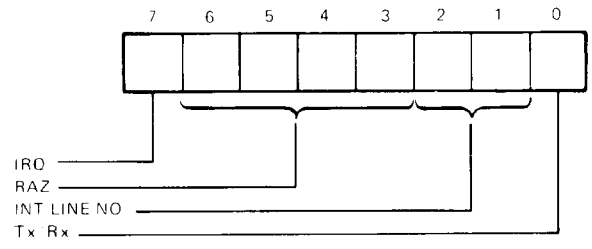


FIGURE 7–COM78804 INTERRUPT SUMMARY REGISTER FORMAT

TABLE 8–COM78804 INTERRUPT SUMMARY REGISTER DESCRIPTION

Bit	Description
7	IRQ (Interrupt request)–When set, this bit indicates that the interrupt scanner has found an interrupting condition among the four serial lines of the Quad UART. These conditions also result in the Quad UART asserting the $\overline{IRQ}$ signal.
6:4	RAZ (Read as zero)–Not used
3:1*	INT LINE NO (Interrupting line number)–These bits indicate the line number upon which an interrupting condition was found. These bits correspond to the IRQLN <1:0> signals–bit 2 = IRQLN<1>, and bit 1 = IRQLN<0>. Refer to Table 3.
0*	$\overline{Tx}/\overline{Rx}$ (Transmit/receive)–This bit indicates whether the interrupting condition was caused by a transmitter ($\overline{Tx}/\overline{Rx}$ equals 1) or a receiver ($\overline{Tx}/\overline{Rx}$ equals 0). This bit corresponds to the IRQTxRx signal of the Quad UART and is set when IRQTxRx is asserted.

*Bits 3-0 above represent the outputs of a free-running counter and are valid only when bit 7 is set.

Data set change summary register–When the $\overline{DSR}$ or $\overline{DCD}$ inputs that are associated with a line change state, the bit corresponding to that line in this read-only register is set. The current state of the $\overline{DSR}$ and $\overline{DCD}$ inputs can then be obtained from that line's status register. If the state of a line changes twice within one microsecond, the change in state may not be detected. Figure 8 shows the format of the data set change summary register.

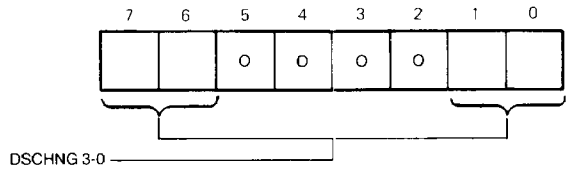


FIGURE 8–COM78804 DATA SET CHANGE SUMMARY REGISTER FORMAT

When the MCIE bit in a line's mode register 1 is set and RxIE is also set, the modem control interrupts are enabled for that line. If DSCHNG for that line is then set, the interrupt scanner will halt and assert the $\overline{IRQ}$ signal. The data set change summary register bits are cleared by writing a 1 into the bit position. A program that uses this register should read and save a copy of its contents. The copy can then be written back to the register to clear the bits that were set. The system interrupts should be disabled and writeback should directly follow the read operation.

Assertion of the $\overline{RESET}$ signal disables and initializes the data set change logic. When the $\overline{RESET}$ signal is deasserted, future changes in $\overline{DSR}$ and $\overline{DCD}$ are reported as they occur.

INTERRUPT SCANNER AND INTERRUPT HANDLING

The interrupt scanner sequentially checks each line for a receive interrupt and then checks each one in the same order for a transmitter interrupt. If the scanner detects an interrupt condition, it stops and the $\overline{IRQ}$ signal is asserted. An interrupt must be serviced by software or no other interrupt request can be posted.

The scanner determines that a line has a receiver interrupt if the line's receiver buffer is ready and receiver interrupts are enabled for that line (RxRDY and RxIE = 1) or either of the line's modem status signals has changed state and both receiver and modem control interrupts are enabled for that line (DSCHNG and RxIE and MCIE = 1).

The scanner determines that a line has a transmitter interrupt if the line's transmitter holding the register is empty and transmitter interrupts are enabled for that line (TxRDY and TxIE = 1).

When the scanner detects an interrupt, it reports the line number on the IRQ<1:0> lines. The IRQTxRx signal is asserted for a transmitter interrupt and deasserted for a receiver interrupt. The appropriate bits are also updated in the interrupt summary register. The $\overline{IRQ}$ line is deasserted and the scanner is restarted for each of the following three types of interrupt conditions.

- ☐ Reading the receiver buffer or resetting the RxIE bit of the interrupting line for the first type of receiver interrupt previously described.
- ☐ Resetting the MCIE, RxIE, or DSCHNG bit of the interrupting line for the second type of receiver interrupt previously described.
- ☐ Loading the transmitter holding register or resetting the TxIE bit of the interrupting line for transmitter interrupts.

If the scanner was originally stopped by a receiver interrupt condition, the scanner resumes sequential operation from where it stopped, thus providing receivers with equal priority. If the scanner was stopped by a transmitter condition, the scanner restarts from position 0 (line 0's receiver), thus giving receivers priority over transmitters.

EDGE-TRIGGERED AND LEVEL-TRIGGERED INTERRUPT SYTSTEMS

If the interrupt system of the Quad UART is used only for generating interrupts for the RxRDY and/or TxRDY flags, the $\overline{IRQ}$ line can be connected to a processor having either edge-triggered or level-triggered interrupt capability. If the modem control interrupts are being used (MCIE in mode register 1 = 1), the $\overline{IRQ}$ line can be connected only to a processor that uses level-triggered interrupts.

MODEM HANDLING

The TxEMT (transmitter empty) bit of the status register is typically used to indicate when a program can disable the transmission medium, as when deasserting the request-to-send line of a modem. A typical program will load the last character for transmission and then monitor the TxEMT bit of the status register.

The assertion of the TxEMT bit to indicate the transmission is complete may occur a substantial time after the loading of the last character. After the last character is loaded, one character is in the transmitter holding register and one character is in the serialization logic. Therefore, it will be two character times before the transmission process is completed. Waiting for the TxRDY signal to assert before monitoring the TxEMT status shortens this by one character time because the TxRDY status bit indicates that there are no characters in the transmitter holding register. The times involved are calculated by taking the reciprocal of the baud rate being used, multiplying by the number of bits per character (a starter bit–5,6,7, or 8 data bits; plus parity bit if enabled; and 1,1.5, or 2 stop bits), and multiplying by either two characters or one, depending on when TxEMT monitoring begins.

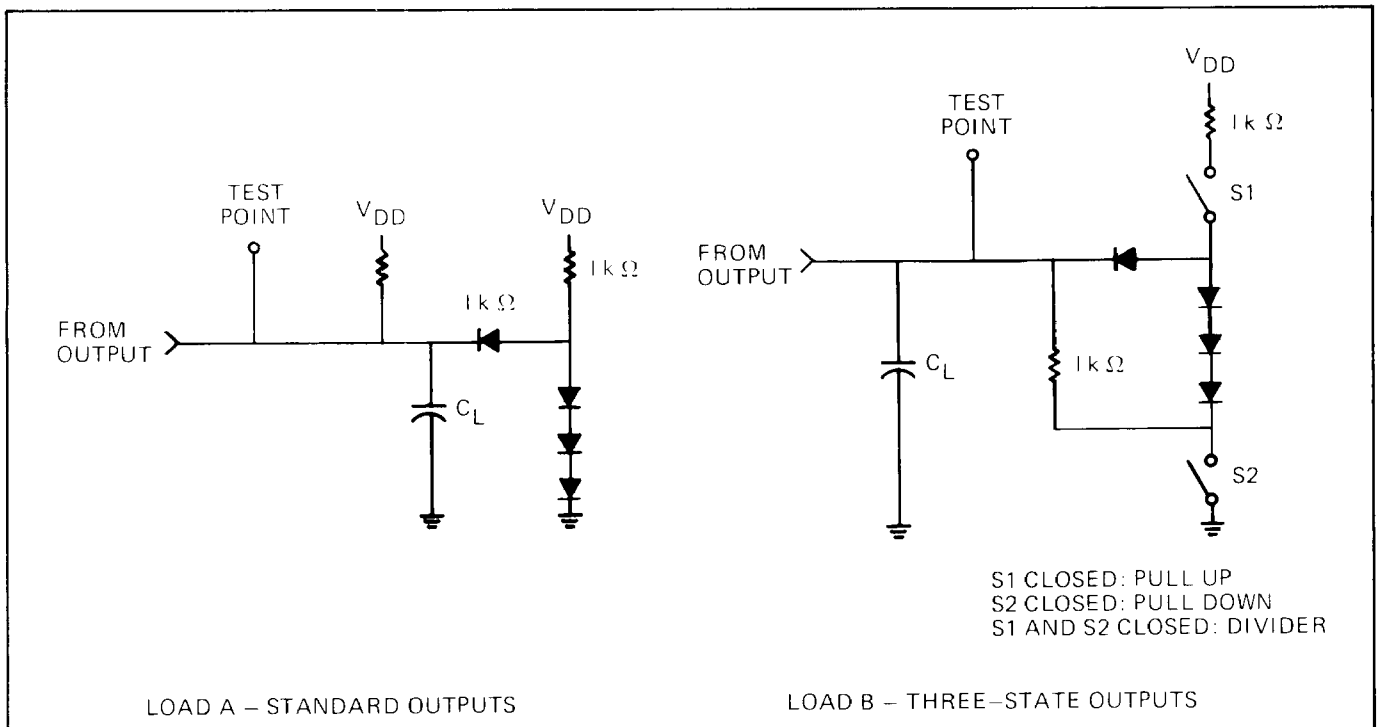


FIGURE 9–COM78804 OUTPUT LOAD CIRCUITS

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55° to +125°C
Lead Temperature (soldering, 10 sec.)	+300°C
Positive Voltage on any I/O Pin, with respect to ground	+0.7V
Negative Voltage on any I/O Pin, with respect to ground	−0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +5 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that a clamp circuit be used.

TABLE 9–COM78804

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Requirements Min.	Typ.	Max.	Units
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage	V_{DD} = Min. I_{OH} = 3.5 mA for DL<7:0> I_{DH} = 2.0 mA for all remaining output except $\overline{IRQ}$ and $\overline{RDY}$	2.4			V
V_{OL}	Low-level output voltage	V_{DD} = Min. I_{OL} = 5.5 mA for DL<7:0> I_{OL} = 3.5 mA for all remaining outputs			0.4	V
I_{IH}	Input current at maximum input voltage	V_{DD} = Max. $V_I = V_{DD}$(Max.)			10	µA
I_{IL}	Input current at miminum input voltage	V_{DD} = Max. V_I = 0.0V			−10	µA
I_{OS}[1]	Short-circuit output current for DL<7:0> all remaining outputs except $\overline{IRQ}$ and $\overline{RDY}$	V_{DD} = Max.	−50 −30		−180 −110	mA mA
I_{OZL}[2]	Three-state output current	V_{DD} = Max. V_O = 0.4V			10	µA
I_{OZH}[2]	Three-state output current	V_{DD} = Max. V_O = 2.4V			10	A
I_{DD}	Supply current	V_{DD} = Max. T_A = 0°		100		mA
C_{in}	Input capacitance				4	pF
C_{IO}[3]	Input/output capacitance				5	pF

[1]No more than one ouput should be short circuited at a time, and the duration of the short should not exceed 1 second.
[2]All three-state output drivers are wired in an I/O configuration. The parameters include the driver and input receiver leakage currents.
[3]The parameters include the capacitive loads of the output driver and the input receiver.

TIMING PARAMETERS

Figure 10 shows the signal timing for a read cycle to transfer information from the Quad UART to the processor. Figure 11 shows the signal timing for a write cycle to transfer information from the processor to the Quad UART. Table 11 lists the timing parameters for the read and write cycles.

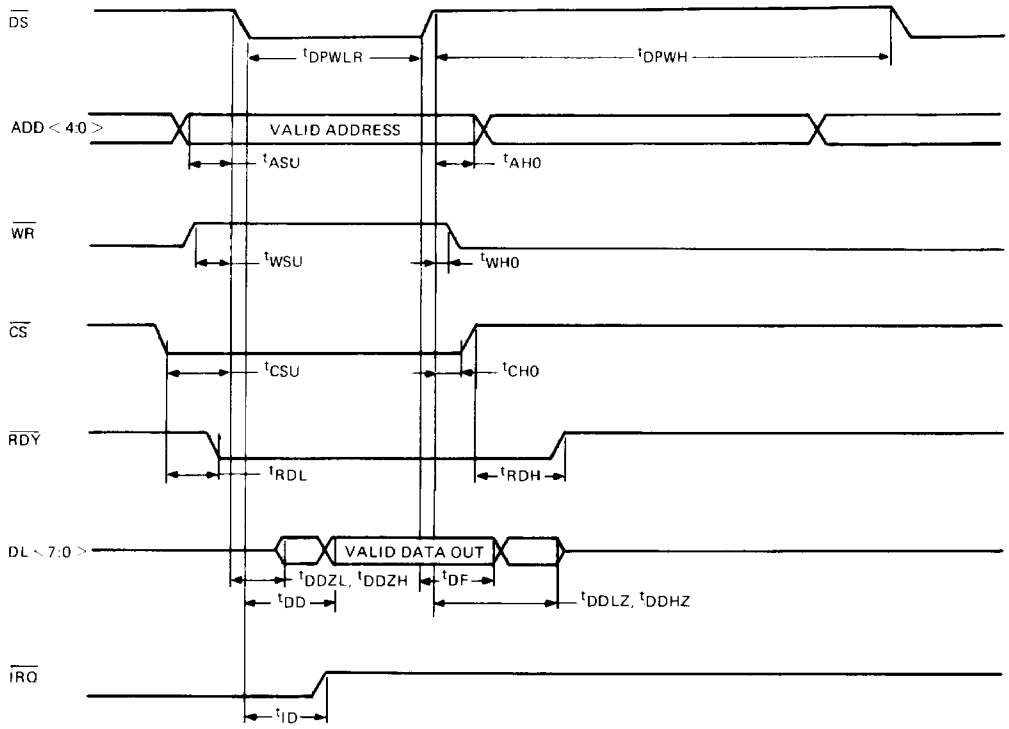


FIGURE 10–COM78804 BUS READ CYCLE TIMING

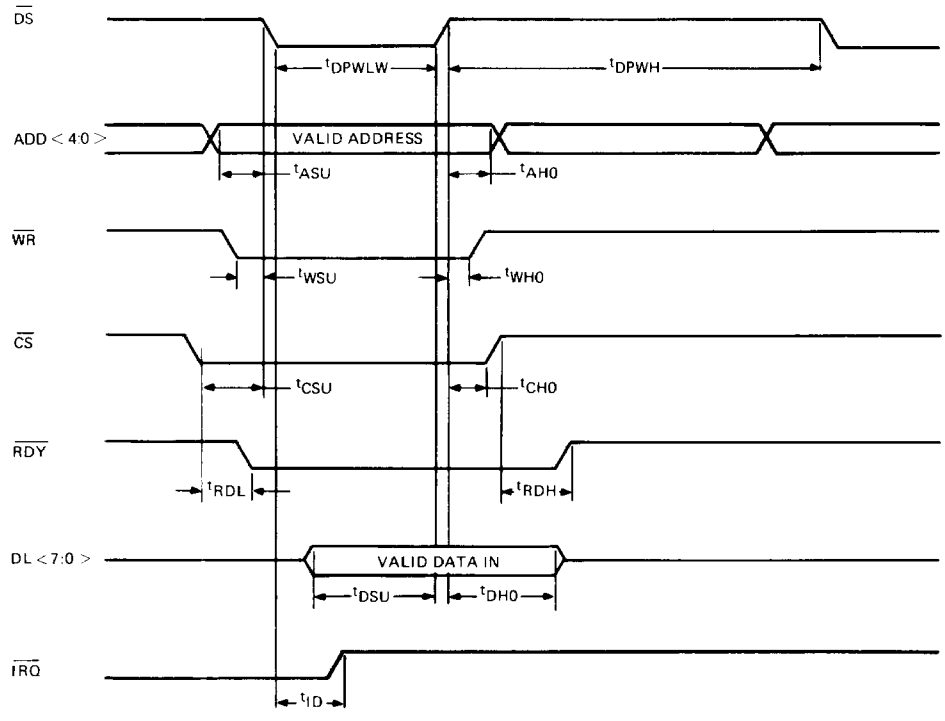


FIGURE 11–COM78804 BUS WRITE CYCLE TIMING

TABLE 10–COM78804 BUS READ AND WRITE TIMING PARAMETERS

Symbol	Definition	Requirements (ns) Min.	Max.	Load Circuit[1]
t_{AHO}	Hold time of a valid ADD <4:0> to a valid high level of $\overline{DS}$.	10		
t_{ASU}	Setup time of a valid ADD <4:0> to the falling edge of $\overline{DS}$.	30		
t_{CHO}	Hold time of a valid low level of $\overline{CS}$ to a valid high level of $\overline{DS}$.	10		
t_{CSU}	Setup time of a valid low level of $\overline{CS}$ to the falling edge of $\overline{DS}$.	30		
t_{DD}	Propagation delay of a valid low level on $\overline{DS}$ (if $\overline{CS}$ is low and $\overline{WR}$ is high) to valid high or low data on DL <7:0>.	165		$C_L = 150$ pF
t_{DDLZ}[2]	Propagation delay of a valid high level on $\overline{DS}$ (if $\overline{CS}$ is low and $\overline{WR}$ is high) to DL <7:0> output drivers disabled. t_{DDLZ} t_{DDHZ} t_{DDLZ} t_{DDHZ} t_{DDLZ} t_{DDHZ}		 50 50 60 60 65 65	 $C_L = 50$pF $C_L = 50$pF $C_L = 100$pF $C_L = 100$pF $C_L = 150$pF $C_L = 150$pF
t_{DDZL}	Propagation delay of a valid low level on $\overline{DS}$ (if $\overline{CS}$ is low and $\overline{WR}$ is high) to DL <7:0> output driver enabled. t_{DDZL} t_{DDZH}	 0	 165 165	 $C_L = 150$pF $C_L = 150$pF
t_{DF}	Hold time provided during a read cycle by Quad UART of valid high or low data on DL <7:0> after the rising edge of $\overline{DS}$.	0		
t_{DHO}	Hold time of a valid DL <7:0> to a valid high level of $\overline{DS}$.	30		
t_{DPWH}	Pulse width high of $\overline{DS}$.	450		
t_{DPWLR}	Pulse width low of $\overline{DS}$ when $\overline{WR}$ is high (read operation). Refer to timing parameter t_{DPWLW} also.	180	10,000	
t_{DPWLW}	Pulse width low of $\overline{DS}$ when $\overline{WR}$ is low (write operation). Refer to timing parameter t_{DPWLR} also.	130	10,000	
t_{DSU}	Setup time of a valid DL <7:0> to the falling edge of $\overline{DS}$.	0		
t_{ID}[3]	Propagation delay of a valid low level on $\overline{DS}$ (if $\overline{CS}$ is low) to a high level on $\overline{IRQ}$.		635	$C_L = 50$pF
t_{RDH}[4]	Propagation delay of a valid high level of $\overline{CS}$ to a valid high level on $\overline{RDY}$.		210	$C_L = 50$pF
t_{RDL}	Propagation delay of a valid low level on $\overline{CS}$ to a valid low level on $\overline{RDY}$.		90	$C_L = 50$pF
t_{WHO}	Hold time of a valid high or low level of $\overline{WR}$ to a valid high level of $\overline{DS}$.	10		
t_{WSU}	Setup time of a valid high or low level of $\overline{WR}$ to the falling edge of $\overline{DS}$.	30		

[1]Refer to Figure 9 for the load circuits used with these measurements.
[2]The t_{DDLZ} and t_{DDHZ} parameters are measured with $C_L = 150$ pF. The values of t_{DDLZ} and t_{DDHZ} for $C_L = 50$pF and $C_L = 100$ pF have been derived for user convenience.
[3]Total rise time depends on internal delay plus the pullup delay introduced by the external resistor being used. The t_{ID} parameter can be calculated by the following: $t_{ID} = 500 + RC_L$ where R = value of the resistor that connects to capacitor C_L in load A, Figure 9.
[4]Total rise time depends on internal delay plus the pullup delay introduced by the external resistor being used. The t_{RDH} parameter can be calculated by the following: $t_{RDH} = 75 + RC_L$ where R = value of the resistor that connects to capacitor C_L in load A, Figure 9.

Figure 12 shows the signal timing for the clock input, interrupt timing, effect of the $\overline{RESET}$ input on data strobe, data set carrier detect (DCD) and data set ready (DSR) input timing, and the transmit data output timing. Table 11 lists the timing parameters for Figure 12.

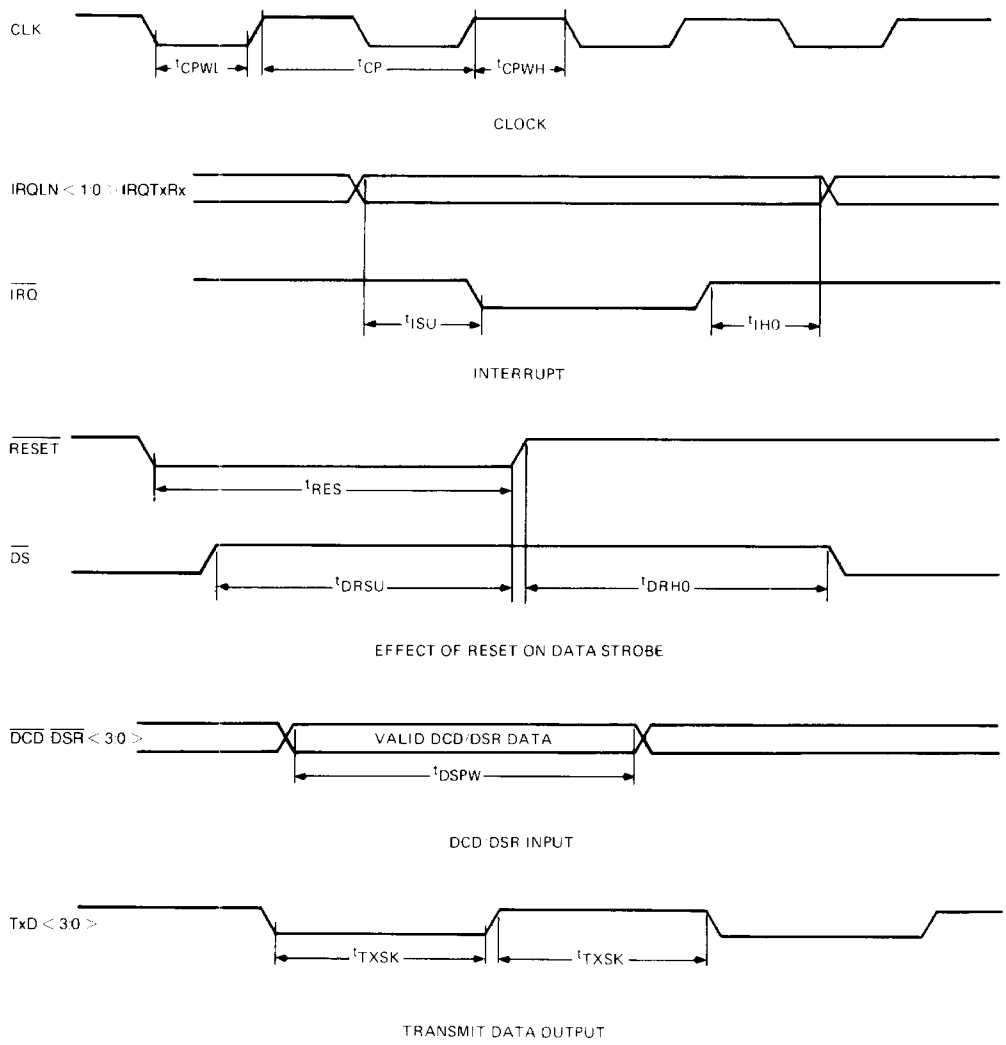


FIGURE 12–COM78804 MISCELLANEOUS SIGNAL TIMING

TABLE 11–MISCELLANEOUS WRITE TIMING PARAMETERS

Symbol	Definition	Requirements (ns) Min.	Load Circuit*
t_{CP}	Period of CLK.	203.45 (4.9152 MHz)	
t_{CPWH}	Pulse width high of CLK.	95	
t_{CPWL}	Pulse width low of CLK.	95	
t_{DRHO}	Hold time of a valid high level of $\overline{DS}$ to a valid high level of $\overline{RESET}$.	1,000	
t_{DRSU}	Setup time of a valid high level of $\overline{DS}$ to the rising edge of $\overline{RESET}$.	900	
t_{DSPW}	Pulse width high or low of DCD <3:0> and DSR <3:0>.	1,000	
t_{IHO}	Hold time provided by Quad UART from a valid IRQLN <1:0> and IRQTxRx to a valid high level of IRQ.	100	$C_L = 50pF$
t_{ISU}	Setup time provided by Quad UART from a valid IRQLN <1:0> and IRQTxRx to a valid low level of $\overline{IRQ}$.	100	$C_L = 50pF$
t_{RES}	Pulse width low of $\overline{RESET}$.	1,000	
t_{TXSK}	Pulse width high or low provided by Quad UART on the TxD <3:0> lines. At each baud rate, the actual pulse widths provided vary by t_{TXSK}. This timing parameter should be used to determine cumulative reception/transmission errors.	250	$C_L = 50pF$

*Refer to Figure 9 for the load circuits used with these measurements.

Figure 13 shows the input and output voltage waveforms for the propagation delay and setup and hold measurements. Figure 14 shows the waveforms for the three-state outputs measurement.

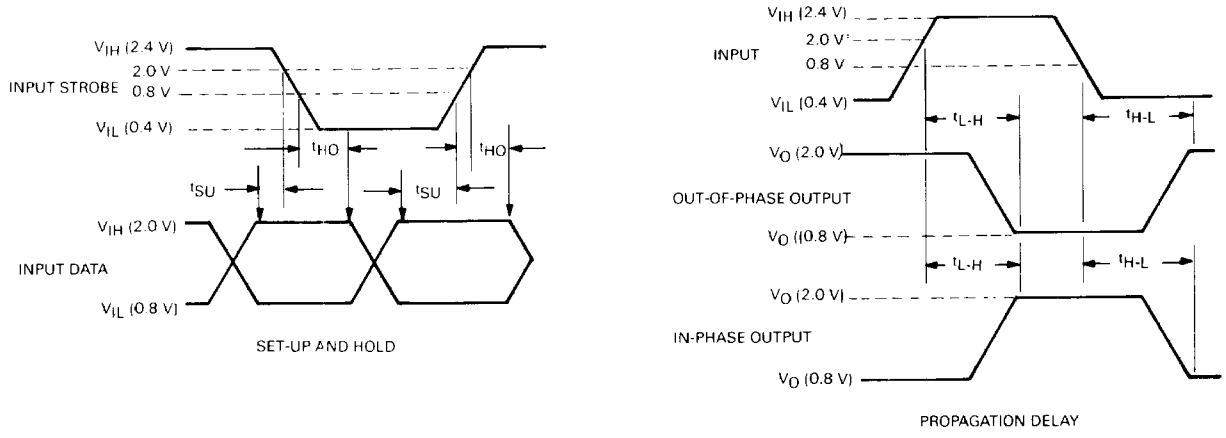
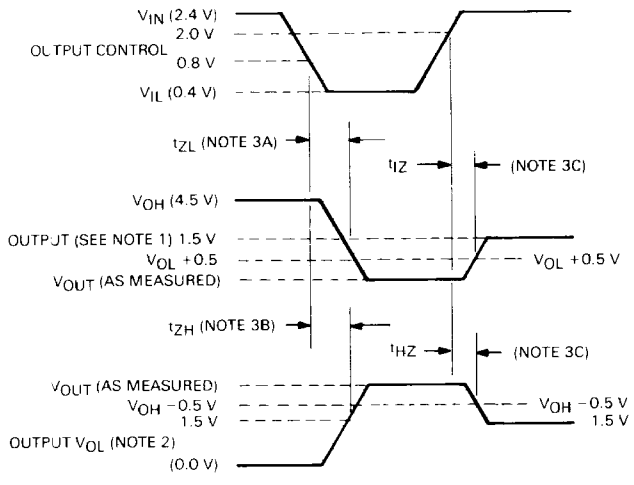


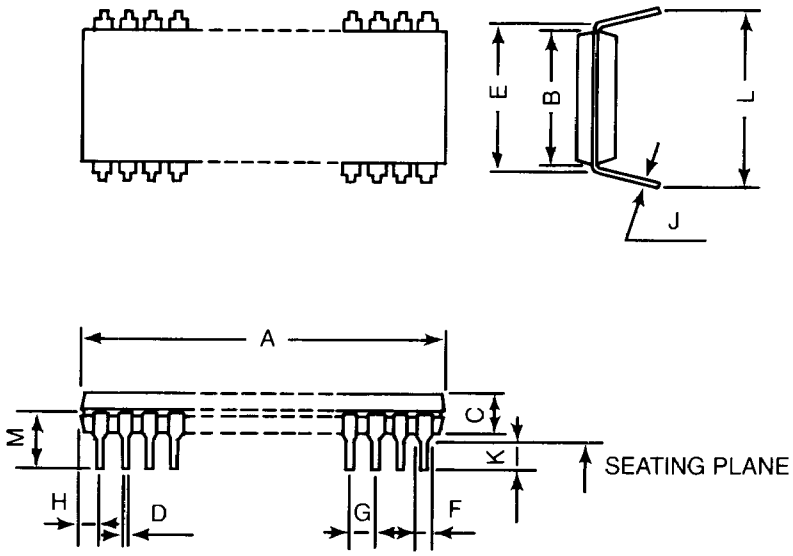
FIGURE 13–COM78804 PROPAGATION DELAY AND SETUP AND HOLD VOLTAGE WAVEFORMS



NOTES:
1. INTERNAL CONDITIONS ARE SUCH THAT THE OUTPUT IS LOW EXCEPT WHEN DISABLED BY THE OUTPUT CONTROL.
2. INTERNAL CONDITIONS ARE SUCH THAT THE OUTPUT IS HIGH EXCEPT WHEN DISABLED BY THE OUTPUT CONTROL.
3. REFER TO FIGURE 9. A = S1 CLOSED, B = S2 CLOSED, C = S1 AND S2 CLOSED.

FIGURE 14–COM78804 THREE-STATE OUTPUT VOLTAGE WAVEFORMS

48 LEAD PLASTIC DIP
PACKAGE OUTLINE



A	2.437 - 2.457
B	0.520 - 0.550
C	0.145 - 0.155
D	0.016 - 0.021
E	0.520 - 0.630
F	0.048 - 0.060
G	0.090 - 0.110
H	0.065 - 0.090
J	0.007 - 0.014
K	0.120 - 0.140
L	0.610 - 0.675
M	0.210 - 0.250