

DM74LS299

8-Input Universal Shift/Storage Register with Common Parallel I/O Pins

General Description

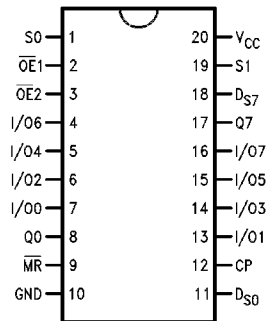
The ^{LS}299 is an 8-bit universal shift/storage register with 3-STATE outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Separate outputs are provided for flip-flops Q0 and Q7 to allow easy cascading. A separate active LOW Master Reset is used to reset the register.

Features

- Common I/O for reduced pin count
- Four operation modes: shift left, shift right, load and store
- Separate shift right serial input and shift left serial input for easy cascading
- 3-STATE outputs for bus oriented applications

Connection Diagram

Dual-In-Line Package



DS009827-1

Order Number DM54LS299E, DM54LS299J, DM54LS299W,
DM74LS299WM or DM74LS299N
See Package Number E20A, J20A, M20B, N20A or W20A

Pin Names	Description
CP	Clock Pulse Input (Active Rising Edge)
D _{S0}	Serial Data Input for Right Shift
D _{S7}	Serial Data Input for Left Shift
S0, S1	Mode Select Inputs
MR	Asynchronous Master Reset Input (Active LOW)
OE1, OE2	3-STATE Output Enable Inputs (Active LOW)
I/O0–I/O7	Parallel Data Inputs or 3-STATE Parallel Outputs
Q0–Q7	Serial Outputs

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V	DM54	-55°C to +125°C
Input Voltage	7V	DM74LS	0°C to +70°C
Operating Free Air Temperature Range		Storage Temperature Range	-65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM54LS299			DM74LS299			Units
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			2			V
V _{IL}	Low Level Input Voltage			0.7			0.8	V
I _{OH}	High Level Output Current	Q0, Q7		-0.4			-0.4	mA
		I/O0-I/O7		-2.6			-2.6	mA
I _{OL}	Low Level Output Current	Q0, Q7		4			8	mA
		I/O0-I/O7		12			24	mA
T _A	Free Air Operating Temperature	-55		125	0		70	°C
t _s (H)	Setup Time HIGH or LOW	24			24			ns
t _s (L)	S0 or S1 to CP	24			24			ns
t _h (H)	Hold Time HIGH or LOW	5			0			ns
t _h (L)	S0 or S1 to CP	5			0			ns
t _s (H)	Setup Time HIGH or LOW	15			10			ns
t _s (L)	I/O _n , D _{S0} , D _{S7} to CP	15			10			ns
t _h (H)	Hold Time HIGH or LOW	5			0			ns
t _h (L)	I/O _n , D _{S0} , D _{S7} to CP	5			0			ns
t _w (H)	CP Pulse Width HIGH or LOW	15			15			ns
t _w (L)		15			15			ns
t _w (L)	MR Pulse Width LOW	15			15			ns
t _{rec}	Recovery Time	10			10			ns
	MR to CP							

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units	
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = -18 mA			-1.5	V	
V _{OH}	High Level Output Voltage	V _{CC} = Min, I _{OH} = Max	DM54	2.5		V	
		V _{IL} = Max	Q0, Q7	DM74	2.7		3.4
			I/O0-I/O7		2.4		
V _{OL}	Low Level Output Voltage	V _{CC} = Min, I _{OL} = Max	DM54		0.4	V	
		V _{IH} = Min	DM74		0.35		0.5
		I _{OL} = 4 mA, V _{CC} = Min	DM74		0.25		0.4
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 10V (DM54)	Inputs		0.1	mA	
		V _I = 7V (DM74)	Sn		0.2	mA	
I _{IH}	High Level Input Current	V _{CC} = Max, V _I = 2.7V	Sn		40	μA	
			Inputs		20	μA	
I _{IL}	Low Level Input Current	V _{CC} = Max, V _I = 0.4V	Sn		-0.8	mA	
			Inputs		-0.4	mA	

Electrical Characteristics (Continued)

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units	
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 3)	Q_0, Q_7	-20		-100	mA
			$I/O_0-I/O_7$	-30		-130	
I_{CC}	Supply Current	$V_{CC} = \text{Max}, \overline{OE} = 4.5V$			60	mA	
I_{OZH}	3-STATE Output Off Current High	$V_{CC} = \text{Max}$ $V_O = 2.7V$			40	μA	
I_{OZL}	3-STATE Output Off Current Low	$V_{CC} = \text{Max}$ $V_O = 0.4V$			-400	μA	

Note 2: All typicals are at $V_{CC} = 5V, T_A = 25^\circ C$.

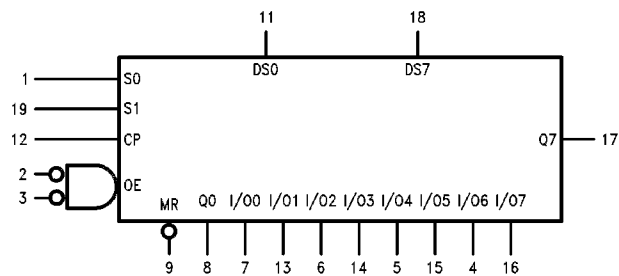
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

$V_{CC} = +5.0V, T_A = +25^\circ C$ (See Section 1 for waveforms and load configurations)

Symbol	Parameter	$R_L = 2\text{ k}\Omega$ $C_L = 15\text{ pF}$		Units
		Min	Max	
f_{max}	Maximum Input Frequency	35		MHz
t_{PLH}	Propagation Delay		26	ns
t_{PHL}	CP to Q_0 or Q_7		28	
t_{PLH}	Propagation Delay		25	ns
t_{PHL}	CP to I/O_n		35	
t_{PHL}	Propagation Delay \overline{MR} to Q_0 or Q_7		28	ns
t_{PHL}	Propagation Delay \overline{MR} to I/O_n		35	ns
t_{PZH}	Output Enable Time		18	ns
t_{PZL}			25	
t_{PHZ}	Output Disable Time		15	ns
t_{PLZ}			20	

Logic Symbol



DS006827-2

$V_{CC} = \text{Pin } 20$
 $GND = \text{Pin } 10$

Functional Description

The 'LS299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by the S0 and S1, as shown in the Mode Select Table. All flip-flop outputs are brought out through 3-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q0 and Q7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on \overline{MR} overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either $\overline{OE1}$ or $\overline{OE2}$ disables the 3-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-STATE buffers are also disabled by HIGH signals on both S0 and S1 in preparation for a parallel load operation.

Mode Select Table

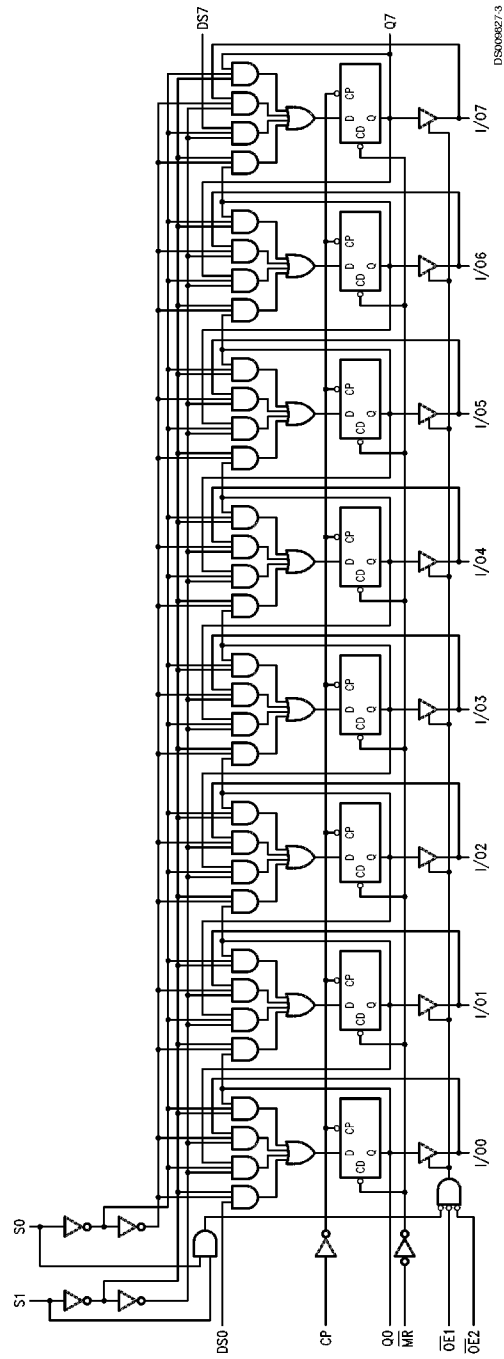
Inputs				Response
\overline{MR}	S1	S0	CP	
L	X	X	X	Asynchronous Reset; Q0–Q7 = LOW
H	H	H	↘	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	↘	Shift Right; $D_{S0} \rightarrow Q0$, $Q0 \rightarrow Q1$, etc.
H	H	L	↘	Shift Left; $D_{S7} \rightarrow Q7$, $Q7 \rightarrow Q6$, etc.
H	L	L	X	Hold

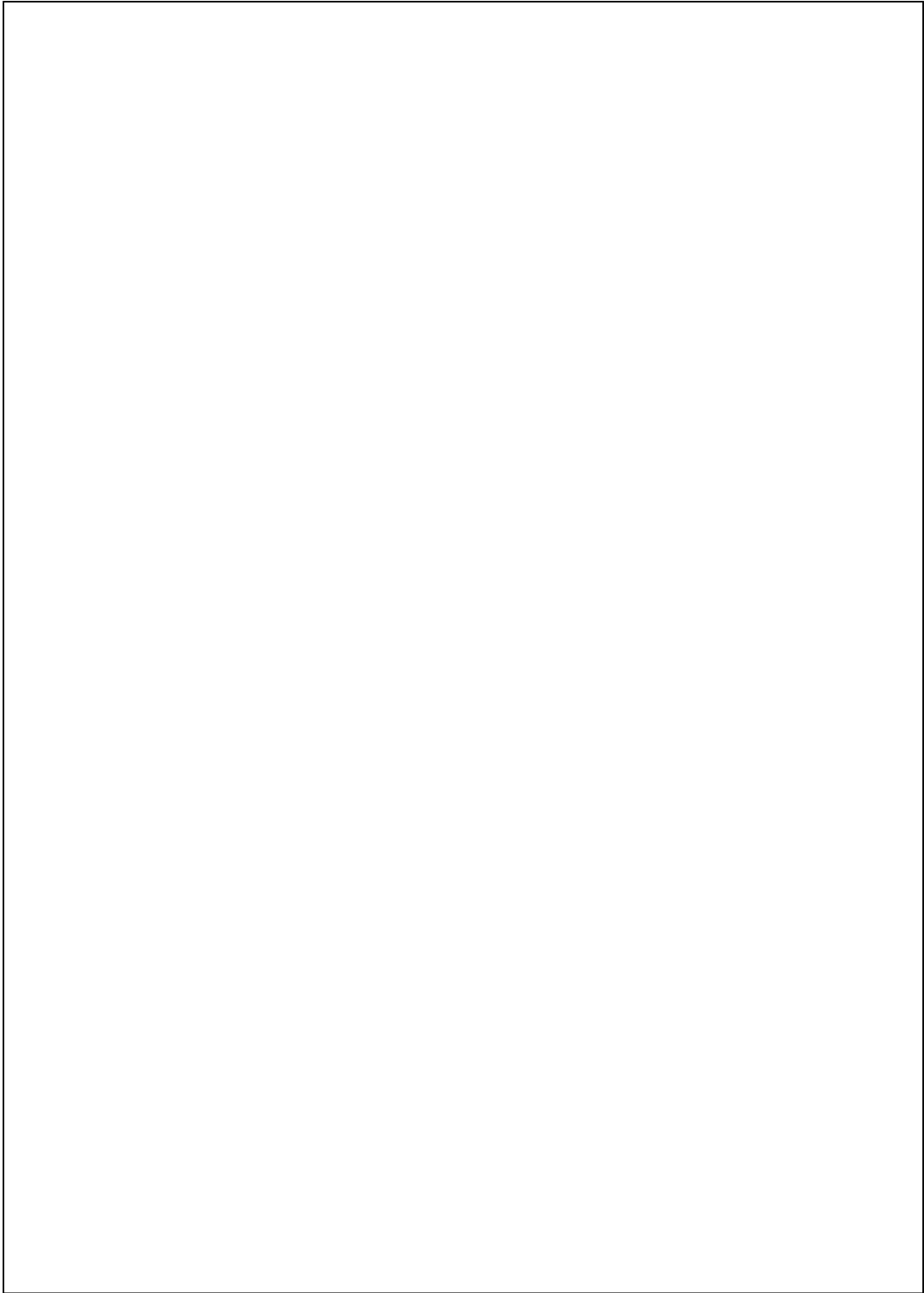
H = HIGH Voltage Level

L = LOW Voltage Level

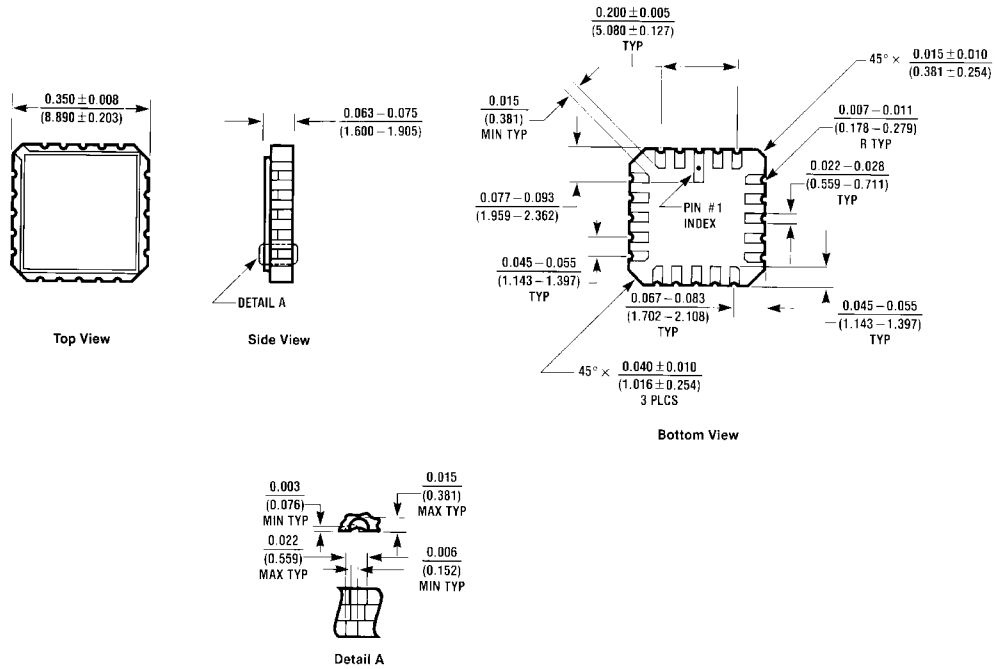
X = Immaterial

Logic Diagram





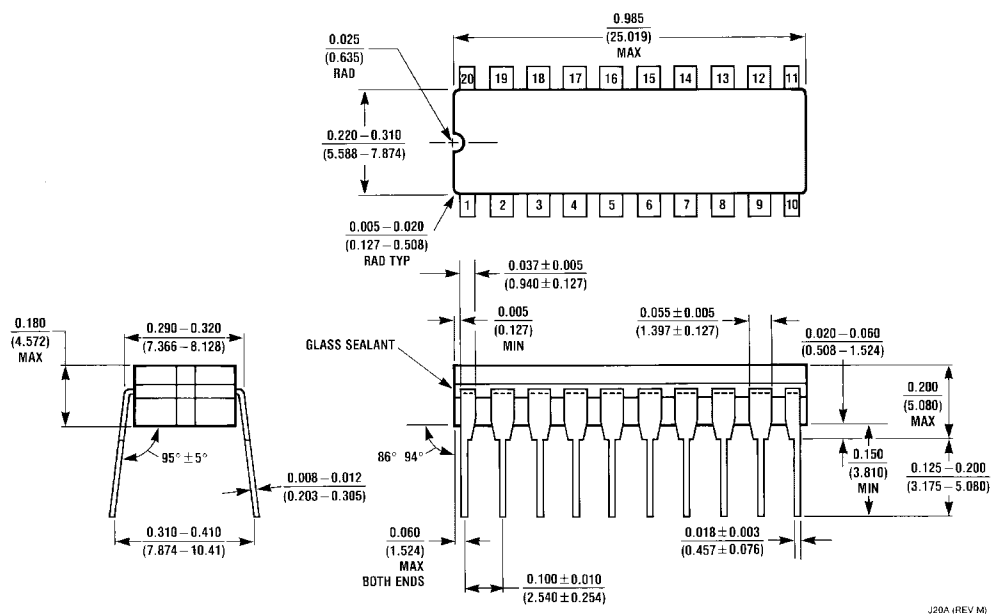
Physical Dimensions inches (millimeters) unless otherwise noted



L20A (REV D)

Ceramic Leadless Chip Carrier Package (E)
Order Number DM54LS299E
Package Number E20A

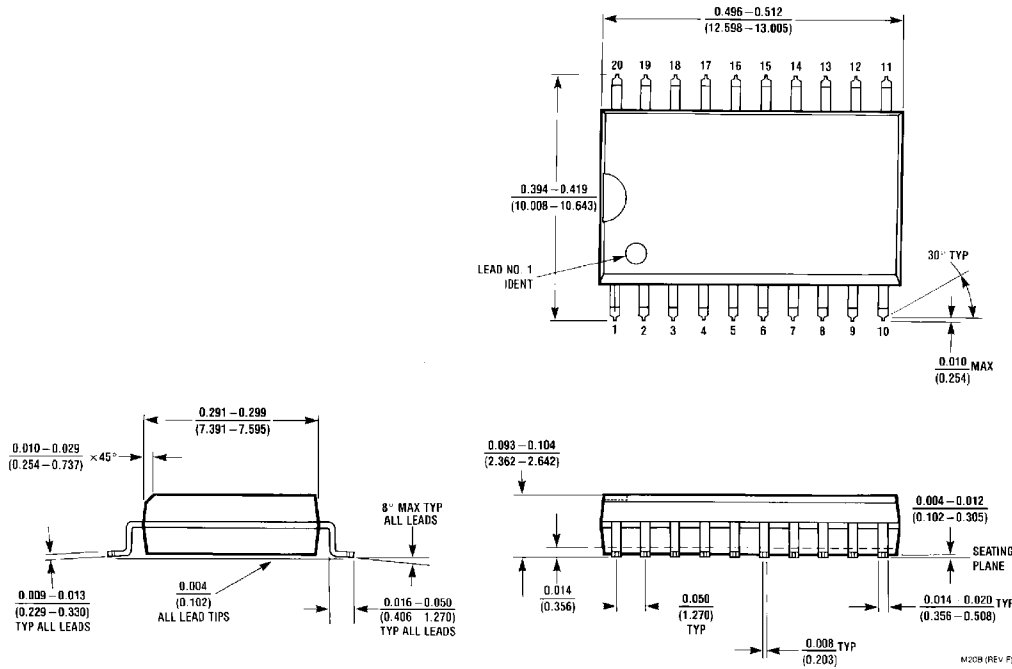
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



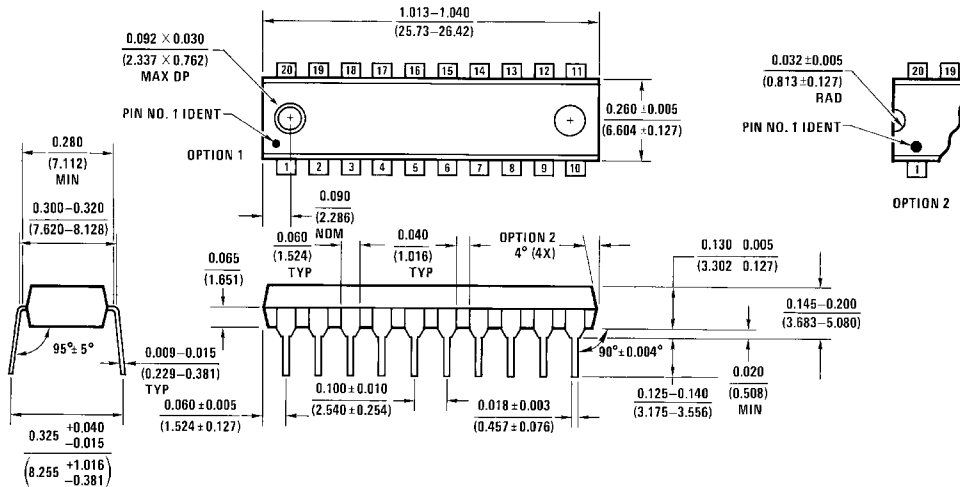
20-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS299J
Package Number J20A

J20A (REV M)

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

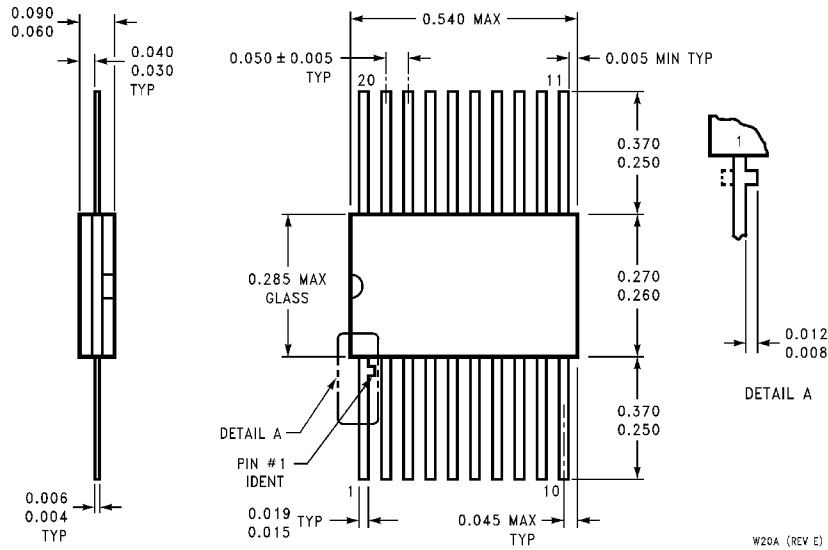


20-Lead Wide Small Outline Molded Package (M)
Order Number DM74LS299WM
Package Number M20B



20-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS299N
Package Number N20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Ceramic Flat Package (W)
Order Number DM54LS299W
Package Number W20A

W20A (REV E)

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