

PSMN9R8-30MLC

N-channel 30 V 9.8 mΩ logic level MOSFET in LFPAK33 using **NextPower Technology**

Rev. 3 — 15 June 2012

Product data sheet

Product profile 1.

1.1 General description

Logic level enhancement mode N-channel MOSFET in LFPAK33 package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- Low parasitic inductance and resistance
- Optimised for 4.5V Gate drive utilising NextPower Superjunction technology

1.3 Applications

- DC-to-DC converters
- Load switching

1.4 Quick reference data

Ultra low QG, QGD, & QOSS	for high
system efficiencies at low and loads	l high

Synchronous buck regulator

Table 1.	Quick reference data					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C	-	-	30	V
I _D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; see <u>Figure 1</u>	-	-	50	А
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>	-	-	45	W
Tj	junction temperature		-55	-	175	°C
Static cha	aracteristics					
R _{DSon}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 15 A; T _j = 25 °C; see <u>Figure 10</u>	-	10.65	12.4	mΩ
		V_{GS} = 10 V; I_D = 15 A; T_j = 25 °C; see <u>Figure 10</u>	-	8.5	9.8	mΩ
Dynamic	characteristics					
Q _{GD}	gate-drain charge	V_{GS} = 4.5 V; I_D = 15 A; V_{DS} = 15 V; see <u>Figure 12</u> ; see <u>Figure 13</u>	-	1.5	-	nC
Q _{G(tot)}	total gate charge	$V_{GS} = 4.5 \text{ V}; I_D = 15 \text{ A}; V_{DS} = 15 \text{ V};$ see Figure 12; see Figure 13	-	5	-	nC



N-channel 30 V 9.8 mΩ logic level MOSFET in LFPAK33 using NextPower Technology

2. Pinning information

Table 2.	Pinning	information		
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		2
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		mbb076 S
			SOT1210 (LFPAK33)	

3. Ordering information

Table 3. Ordering information					
Type number	Package				
	Name	Description	Version		
PSMN9R8-30MLC	LFPAK33	Plastic single ended surface mounted package (LFPAK33); 4 leads	SOT1210		

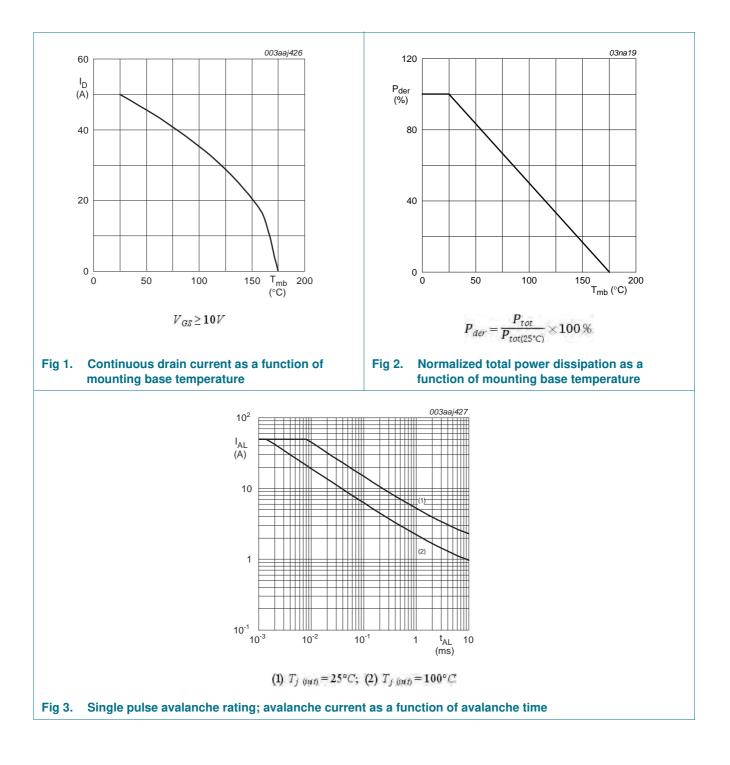
4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

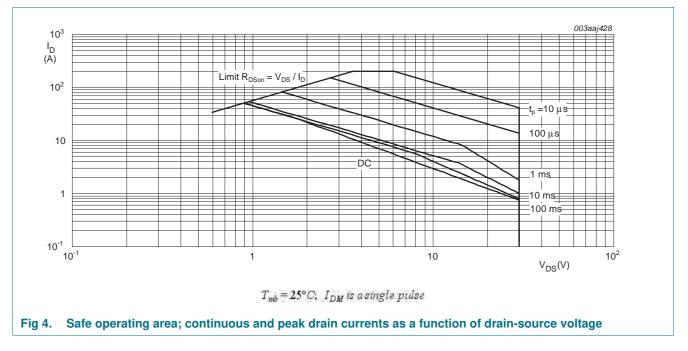
Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	$T_j = 25 \ ^{\circ}C$	-	30	V
V _{GS}	gate-source voltage		-20	20	V
I _D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; see <u>Figure 1</u>	-	50	А
		V_{GS} = 10 V; T_{mb} = 100 °C; see <u>Figure 1</u>	-	36	А
I _{DM}	peak drain current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$; see Figure 4	-	202	А
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>	-	45	W
T _{stg}	storage temperature		-55	175	°C
Tj	junction temperature		-55	175	°C
T _{sld(M)}	peak soldering temperature		-	260	°C
V _{ESD}	electrostatic discharge voltage	MM (JEDEC JESD22-A115)	140	-	V
Source-drain	n diode				
I _S	source current	T _{mb} = 25 °C	-	41	А
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$	-	202	А
Avalanche ru	uggedness				
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	$ \begin{array}{l} V_{GS} = 10 \text{ V}; \text{T}_{j(\text{init})} = 25 \text{ °C}; \text{I}_{\text{D}} = 50 \text{ A}; \\ V_{sup} \leq 30 \text{ V}; \text{R}_{GS} = 50 \Omega; \text{ unclamped}; \\ \text{see } \underline{\text{Figure 3}} \end{array} $	-	8	mJ

PSMN9R8-30MLC



PSMN9R8-30MLC

N-channel 30 V 9.8 mΩ logic level MOSFET in LFPAK33 using NextPower Technology



5. Thermal characteristics

Table 5.Thermal characteristics

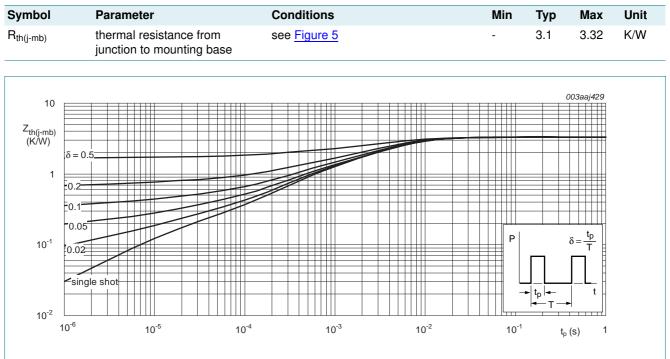


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

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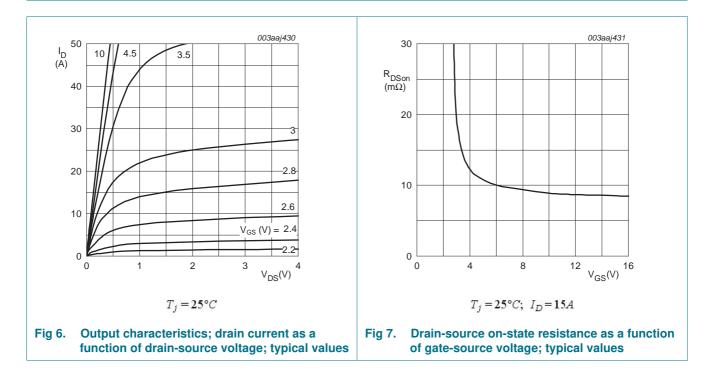
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6. Characteristics

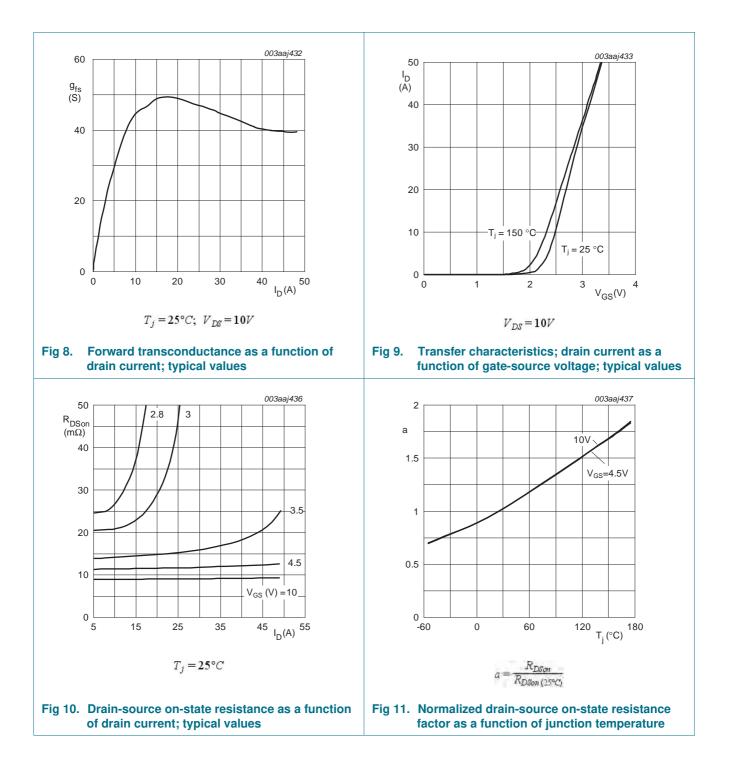
Table 6.	Characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
(01)000	drain-source	$I_D = 250 \ \mu\text{A}; \ V_{GS} = 0 \ V; \ T_j = 25 \ ^\circ\text{C}$	30	-	-	V
	breakdown voltage	$I_D = 250 \ \mu\text{A}; \ V_{GS} = 0 \ V; \ T_j = -55 \ ^\circ\text{C}$	27	-	-	V
V _{GS(th)}	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C}$	1.3	1.64	1.95	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature		-	-4	-	mV/K
I _{DSS}	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	1	μA
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ °C}$	-	-	100	μA
I _{GSS}	gate leakage current	V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 °C	-	-	100	nA
		V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 °C	-	-	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 15 A; T _j = 25 °C; see <u>Figure 10</u>	-	10.65	12.4	mΩ
		V _{GS} = 4.5 V; I _D = 15 A; T _j = 150 °C; see <u>Figure 11</u> ; see <u>Figure 10</u>	-	-	21.1	mΩ
		V _{GS} = 10 V; I _D = 15 A; T _j = 25 °C; see <u>Figure 10</u>	-	8.5	9.8	mΩ
		V _{GS} = 10 V; I _D = 15 A; T _j = 150 °C; see <u>Figure 11;</u> see <u>Figure 10</u>	-	-	16.75	mΩ
R _G	gate resistance	f = 1 MHz	0.9	1.8	3.6	Ω
Dynamic cl	haracteristics					
Q _{G(tot)}	total gate charge	$I_D = 15 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 12; see Figure 13	-	10.9	-	nC
		$I_D = 15 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 4.5 \text{ V};$ see <u>Figure 12</u> ; see <u>Figure 13</u>	-	5	-	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	10	-	nC
Q _{GS}	gate-source charge	$I_D = 15 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 4.5 \text{ V};$	-	2	-	nC
Q _{GS(th)}	pre-threshold gate-source charge	see Figure 12; see Figure 13	-	1.2	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge		-	0.8	-	nC
Q _{GD}	gate-drain charge		-	1.5	-	nC
V _{GS(pl)}	gate-source plateau voltage	$I_D = 15 \text{ A}; V_{DS} = 15 \text{ V};$ see <u>Figure 12</u> ; see <u>Figure 13</u>	-	3.1	-	V
C _{iss}	input capacitance	V _{DS} = 15 V; V _{GS} = 0 V; f = 1 MHz;	-	690	-	pF
C _{oss}	output capacitance	T _j = 25 °C; see Figure 14	-	170	-	pF
C _{rss}	reverse transfer capacitance		-	52	-	pF

PSMN9R8-30MLC

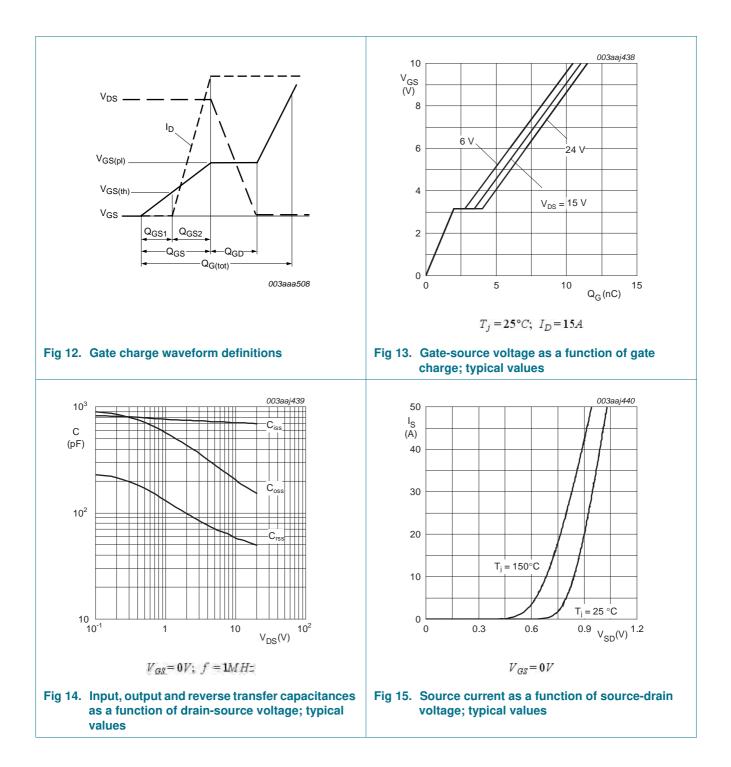
Table 6.	Characteristics continued					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
t _{d(on)}	turn-on delay time	$V_{DS} = 15 \text{ V}; \text{ R}_{L} = 1 \Omega; \text{ V}_{GS} = 4.5 \text{ V};$	-	7.4	-	ns
t _r	rise time	$R_{G(ext)} = 5 \Omega$	-	7.7	-	ns
t _{d(off)}	turn-off delay time		-	11.7	-	ns
t _f	fall time		-	5.3	-	ns
Q _{oss}	output charge	V_{GS} = 0 V; V_{DS} = 15 V; f = 1 MHz; T _j = 25 °C	-	4.9	-	nC
Source-dra	in diode					
V _{SD}	source-drain voltage	I _S = 15 A; V _{GS} = 0 V; T _j = 25 °C; see <u>Figure 15</u>	-	0.84	1.1	V
t _{rr}	reverse recovery time	$I_{S} = 15 \text{ A}; dI_{S}/dt = -100 \text{ A}/\mu s; V_{GS} = 0 \text{ V};$	-	12.9	-	ns
Qr	recovered charge	V _{DS} = 15 V	-	5.3	-	nC
t _a	reverse recovery rise time	V_{GS} = 0 V; I _S = 15 A; dI _S /dt = -100 A/µs; V _{DS} = 15 V; see <u>Figure 16</u>	-	7.9	-	ns
t _b	reverse recovery fall time		-	5	-	ns



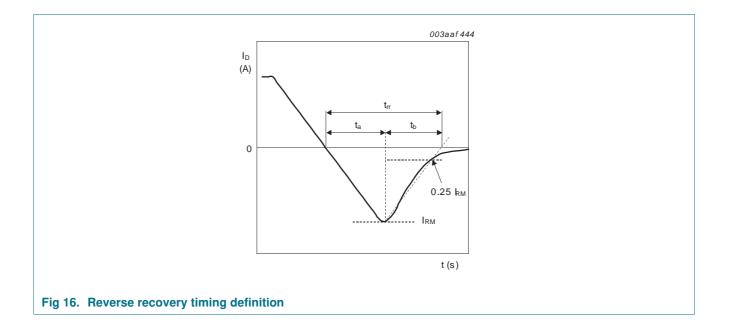
PSMN9R8-30MLC



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N-channel 30 V 9.8 mΩ logic level MOSFET in LFPAK33 using NextPower Technology

7. Package outline

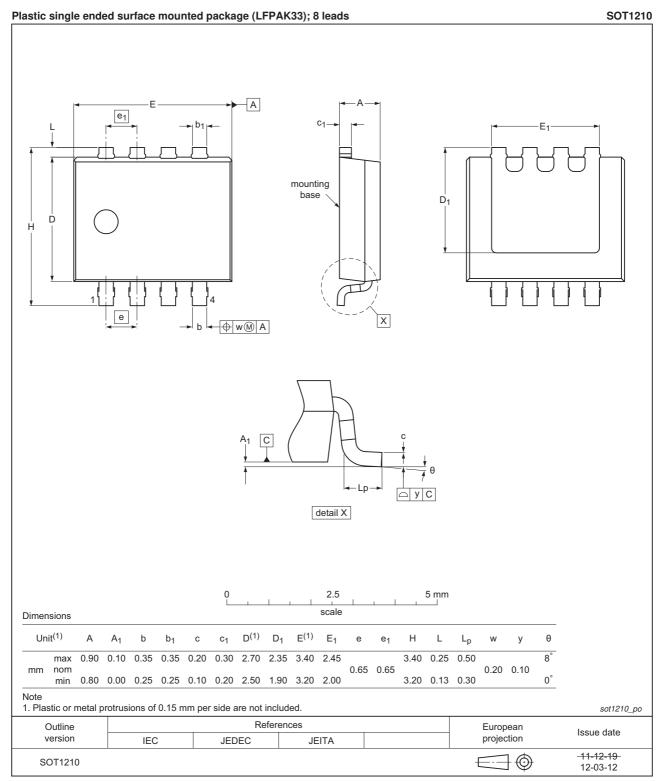


Fig 17. Package outline SOT1210 (LFPAK33)

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PSMN9R8-30MLC

N-channel 30 V 9.8 mΩ logic level MOSFET in LFPAK33 using NextPower Technology

8. Revision history

Table 7.Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN9R8-30MLC v.3	20120615	Product data sheet	-	PSMN9R8-30MLC v.2
Modifications:	Status changed froVarious changes to	om objective to product.		
PSMN9R8-30MLC v.2	20120607	Objective data sheet	-	PSMN9R8-30MLC v.1

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Legal information 9.

9.1 Data sheet status

Document status[1] [2]	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions

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PSMN9R8-30MLC

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PSMN9R8-30MLC

N-channel 30 V 9.8 mΩ logic level MOSFET in LFPAK33 using NextPower Technology

11. Contents

1	Product profile1
1.1	General description1
1.2	Features and benefits1
1.3	Applications1
1.4	Quick reference data1
2	Pinning information2
3	Ordering information2
4	Limiting values2
5	Thermal characteristics4
6	Characteristics5
7	Package outline10
8	Revision history11
9	Legal information12
9.1	Data sheet status12
9.2	Definitions12
9.3	Disclaimers
9.4	Trademarks13
10	Contact information13