EVALSTGAP2SiCS

Data brief

Demonstration board for STGAP2SiCS isolated 4 A single gate driver

Features

- Board
  - High voltage rail up to 1200 V
  - Negative gate driving
  - Onboard isolated DC-DC converters to supply high-side and low-side gate drivers, fed by VAUX = 5 V, with 5.2 kV maximum isolation
  - 3.3 V VDD logic supply generated onboard or 5 V (externally applied)
  - Easy jumper selection of driving voltage configuration: +17/0 V; +17/-3 V; +19/0 V; +19/-3 V
- Device
  - Driver current capability: 4 A source/sink @ 25 °C
  - Separate sink and source for easy gate driving configuration
  - 6000 V Galvanic isolation
  - Short propagation delay: 75 ns
  - UVLO function
  - Gate driving voltage up to 26 V
  - 3.3 V, 5 V TTL/CMOS inputs with hysteresis
  - Temperature shut down protection
  - Stand-by function

Product status link
EVALSTGAP2SiCS

Description

The STGAP2SiCS is an isolated single gate driver.

The gate driver is characterized by 4 A current capability and rail-to-rail outputs, making the device also suitable for high power inverter applications such as motor drivers in industrial applications equipped with SiC power switches.

The separate source and sink outputs allow independent turn-on and turn-off optimization through dedicated gate resistors.

The device integrates protection functions: UVLO and thermal shut down are included to easily design highly reliable systems. Dual input pins allow choosing the control signal polarity and also implementing HW interlocking protection in order to avoid cross-conduction in case of controller malfunction.

The device allows implementing negative gate driving, and the on board isolated DC-DC converters allows working with optimized driving voltage for SiC.

The EVALSTGAP2SiCS board allows evaluation of all the STGAP2SiCS features while driving a half-bridge power stage with voltage rating up to 1200 V in TO-220 or TO-247 packages.

The board components are easy to access and modify in order to make driver performance evaluation easier under different application conditions and fine adjustment of final application components.

1 Schematic diagrams

Figure 1. **EVALSTGAP2SiCS circuit schematic – gate drivers**

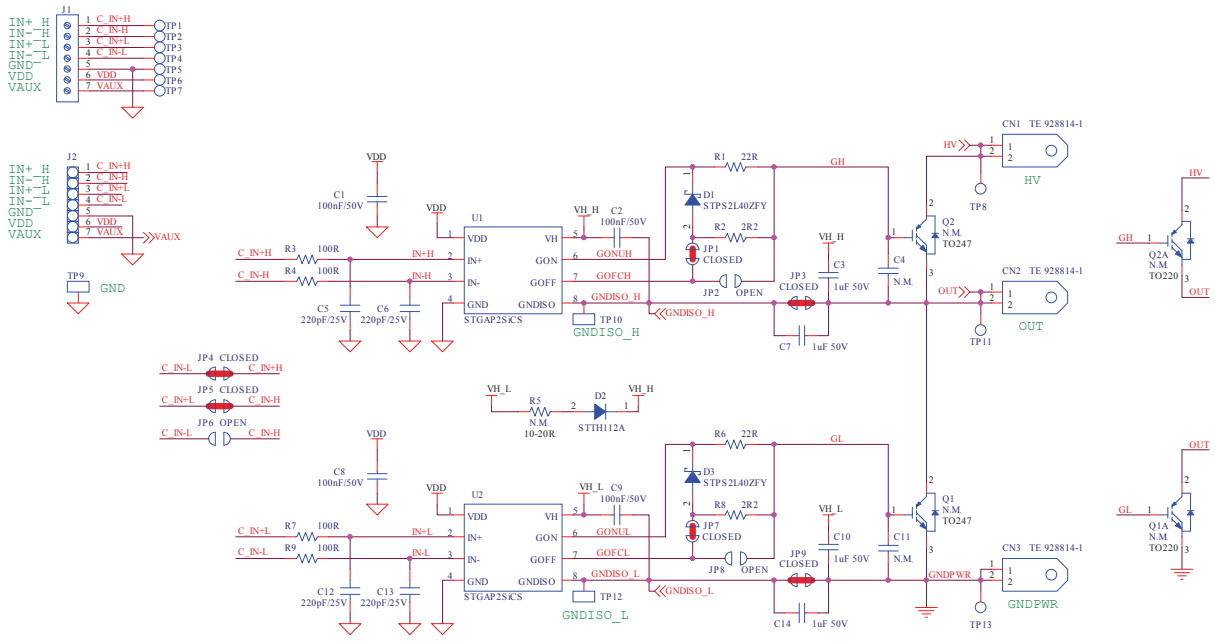
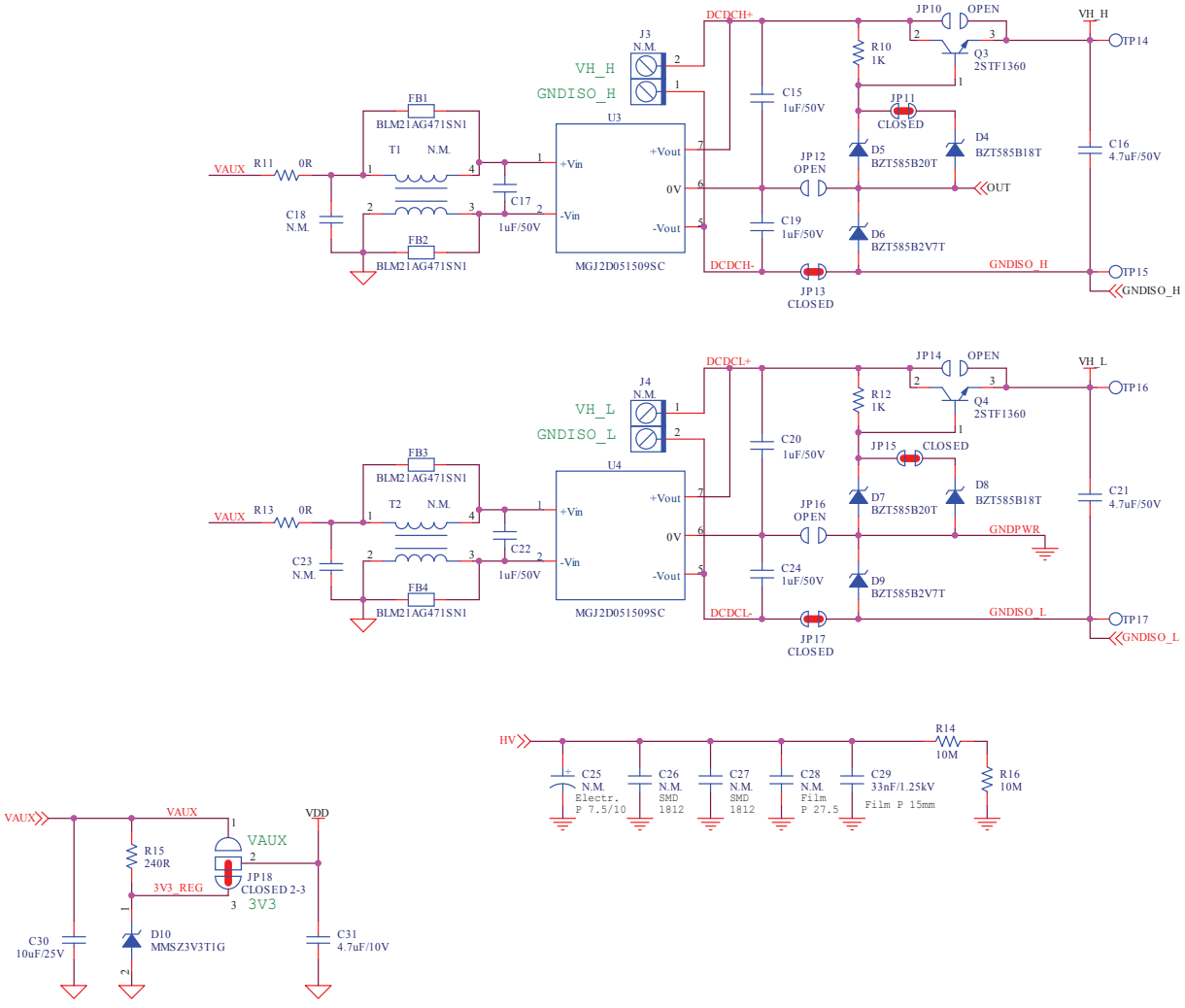


Figure 2. EVALSTGAP2SiCS circuit schematic – supply, connectors and decoupling



2 Bill of material

Table 1. Bill of Material – components common to all device variants

Reference	Description	Value / Generic Part Number
CN1, CN2, CN3	Tab FASTON 250 Horizontal	TE 928814-1
C1, C2, C8, C9	SMT Ceramic capacitor	100nF/50V
C3, C7, C10, C14	SMT Ceramic capacitor	1uF/50V
C4, C11	SMT Ceramic capacitor	N.M.
C5, C6, C12, C13	SMT Ceramic capacitor	220pF/25V
C15, C17, C19, C20, C22, C24	SMT Ceramic capacitor	1uF/50V
C16, C21	SMT Ceramic capacitor	4.7uF/50V
C18, C23	SMT Ceramic capacitor	N.M.
C25	THT Electrolitic capacitor	N.M.
C26, C27	SMT Ceramic capacitor	N.M.
C28	Film capacitor	N.M.
C29	Film capacitor	33nF/1.25kV
C30	SMT Ceramic capacitor	10uF/25V
C31	SMT Ceramic capacitor	4.7uF/10V
D1, D3	Automotive low drop power Schottky rectifier	STPS2L40ZFY
D2	High voltage ultrafast rectifier	STTH112A
D4, D8	SURFACE MOUNT PRECISION ZENER DIODE	BZT585B18T
D5, D7	SURFACE MOUNT PRECISION ZENER DIODE	BZT585B20T
D6, D9	SURFACE MOUNT PRECISION ZENER DIODE	BZT585B2V7T
D10	Zener Voltage Regulator 500mW	MMSZ3V3T1G
FB1, FB2, FB3, FB4	Ferrite Beads	BLM21AG471SN1
JP1, JP3, JP4, JP5, JP7, JP9, JP11, JP13, JP15, JP17	SMT jumper	CLOSED
JP2, JP6, JP8, JP10, JP12, JP14, JP16	SMT jumper	OPEN
JP18	SMT jumper	CLOSED 2-3
J1	Connector terminal block T.H. 7 POS 3.5 mm	MORSV-350-7P_screw
J2	Strip connector 7 pos, 2.54 mm	STRIP 1x7
J3, J4	Connector terminal block T.H. 2 POS 5.08 mm	N.M.
Q1, Q2	N-channel MOSFET up to 1700 V	N.M.
Q1A, Q2A	N-channel MOSFET up to 1700 V	N.M.
Q3, Q4	Low voltage fast-switching NPN power transistors	2STF1360
R1, R6	SMT Resistor	22R
R2, R8	SMT Resistor	2R2
R3, R4, R7, R9	SMT Resistor	100R
R5	SMT Resistor	N.M.
R10, R12	SMT Resistor	1K

Reference	Description	Value / Generic Part Number
R11, R13	SMT Resistor	0R
R14, R16	SMT Resistor	10M
R15	SMT Resistor	240R
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP11, TP13, TP14, TP15, TP16, TP17	Test point - PCB 1.5 mm diameter	T POINT R
TP9, TP10, TP12	THT Ring Test Point	TPTH-ANELLO-1MM
T1, T2	Common mode choke, SMD 4.7x4.5 mm	N.M.
U1, U2	Galvanically isolated 4 A single gate driver for SIC MOSFETs	STGAP2SiCS
U3, U4	5.2KVDC Isolated 2W Gate Drive DC/DC Converters	MGJ2D051509SC
	P.C.B. EVALSTGAP2SiC Rev.1	

3 Layout and component placements

Figure 3. **EVALSTGAP2SiCS – Layout (component placement top view)**

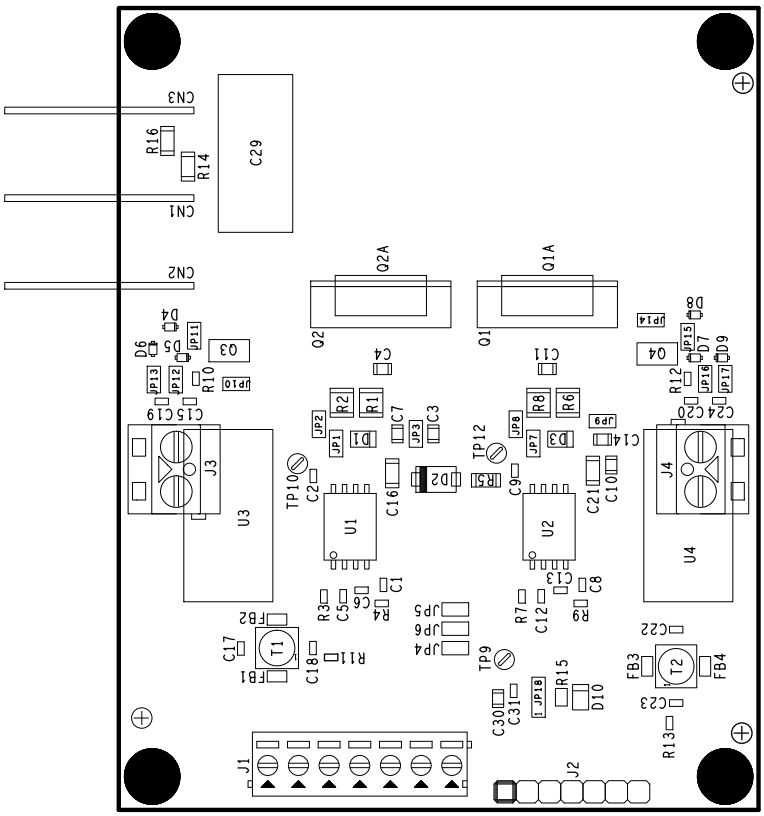


Figure 4. **EVALSTGAP2SiCS – Layout (component placement bottom view)**

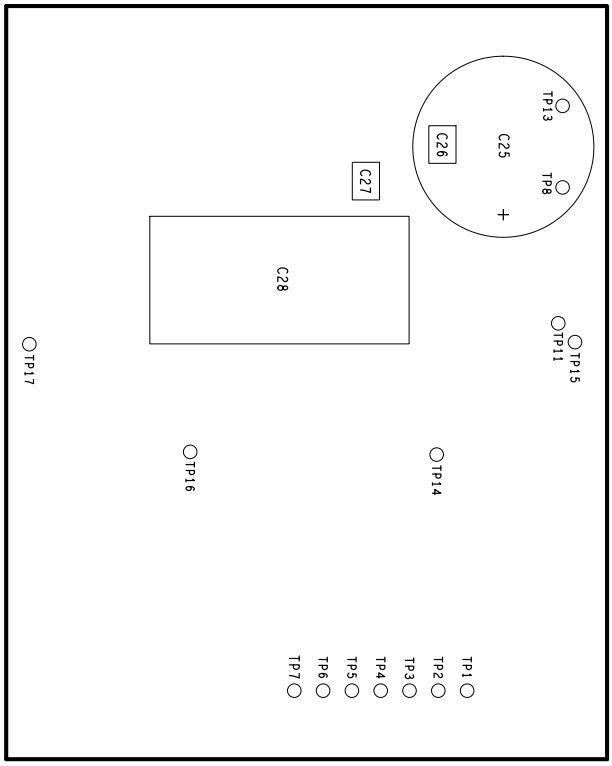


Figure 5. **EVALSTGAP2SiCS – Layout (top layer)**

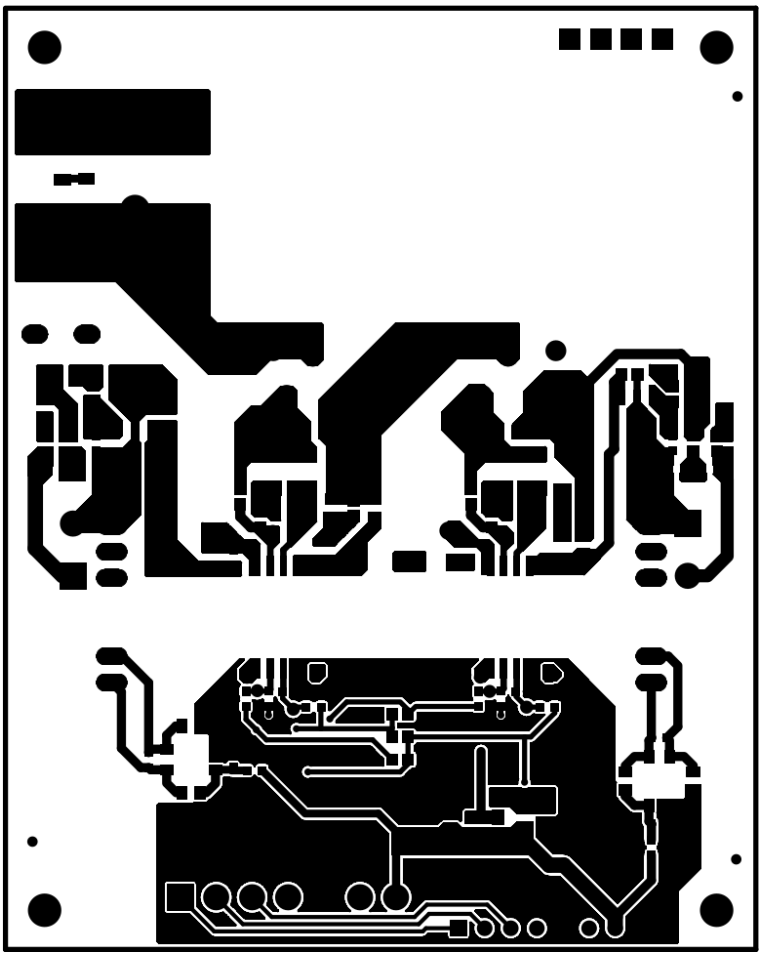
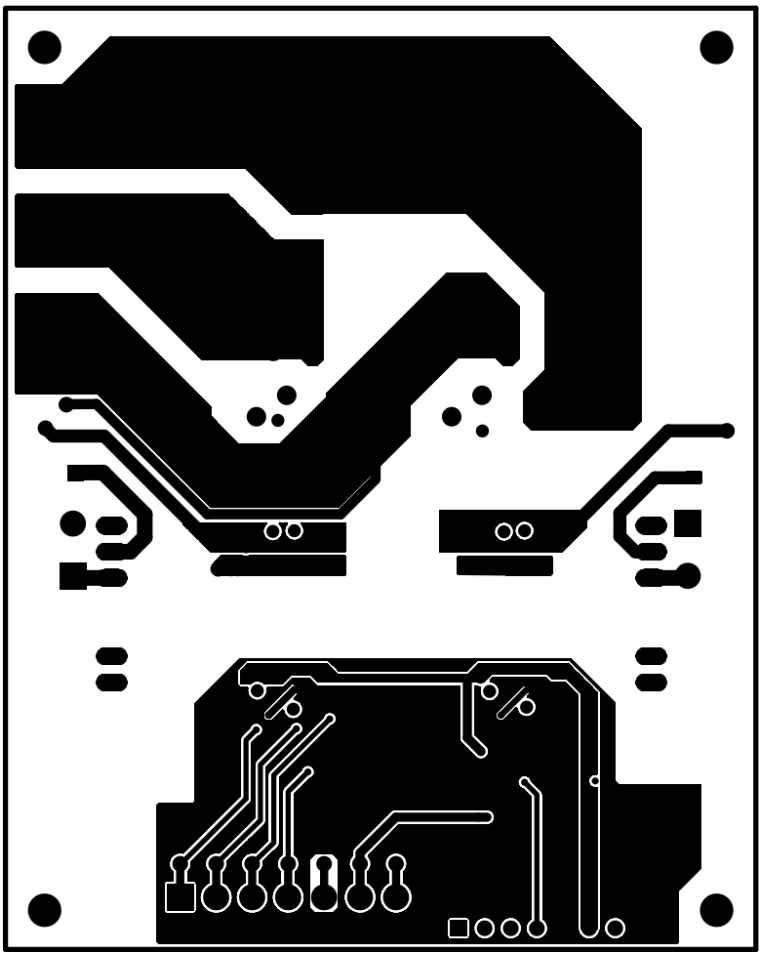


Figure 6. **EVALSTGAP2SiCS – Layout (bottom layer)**



Revision history

Table 2. **Document revision history**

Date	Version	Changes
01-Oct-2020	1	Initial release.

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