Data Sheet | February 5, 2015 | FN4423.3

Transient Voltage Regulator DeCAPitator

The Intersil DeCAPitator helps to stabilize a power system voltage during severe transients. It accomplishes this by supplying current when the voltage is more than 1% low or sinking current when the voltage is higher than 1.5% from the average load voltage. The fast transient response of the DeCAPitator can make up for the slow response time of many switching DC/DC converters.

Although the HIP6200 serves as a simple replacement for large output capacitors for any dynamic load, it is especially useful in stabilizing the CPU core voltage in portable computer applications, where size and efficiency are major concerns. The DeCAPitator enables power supply designs for more powerful microprocessors without increasing converter size or decreasing converter efficiency.

The DeCAPitator acts independently of the PWM control circuitry. This simplifies converter layout because the DeCAPitator and the load may be located separately from the DC/DC converter. The DeCAPitator should be located near the load for optimum performance.

Features

- Saves Power System Size and Cost
  - Replaces Expensive Bulk Capacitors
  - Small 8 Lead SOIC Package
- Linear Regulator Response
  - Greater than 5MHz Bandwidth
- Very Low Static Power Dissipation
  - Shutdown Current. . . . . .<5µA
  - Power Dissipated Only During Load Transients
- Over Temperature Shutdown/Signal
- Simplifies Power Supply Layout
  - Allows for Remotely Located CPU DC/DC Converter

Applications

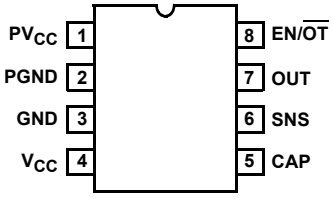
- Notebook Computers
- Pentium™, Pentium Pro, and Pentium II Power Supplies

Ordering Information

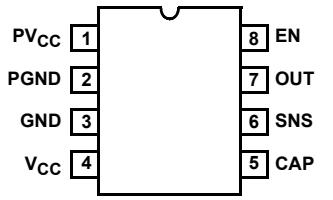
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HIP6200CB	0 to 70	8 Ld SOIC	M8.15
HIP6201CB	0 to 70	8 Ld SOIC	M8.15

Pinouts

HIP6200 (SOIC)
TOP VIEW



HIP6201 (SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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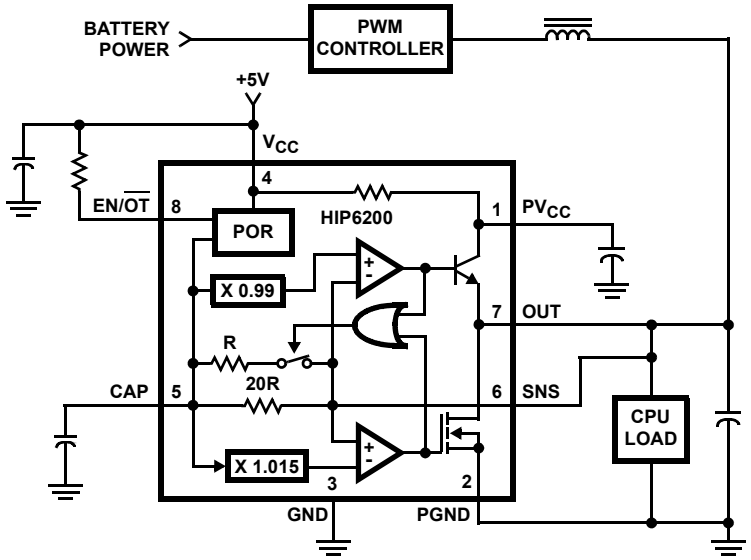
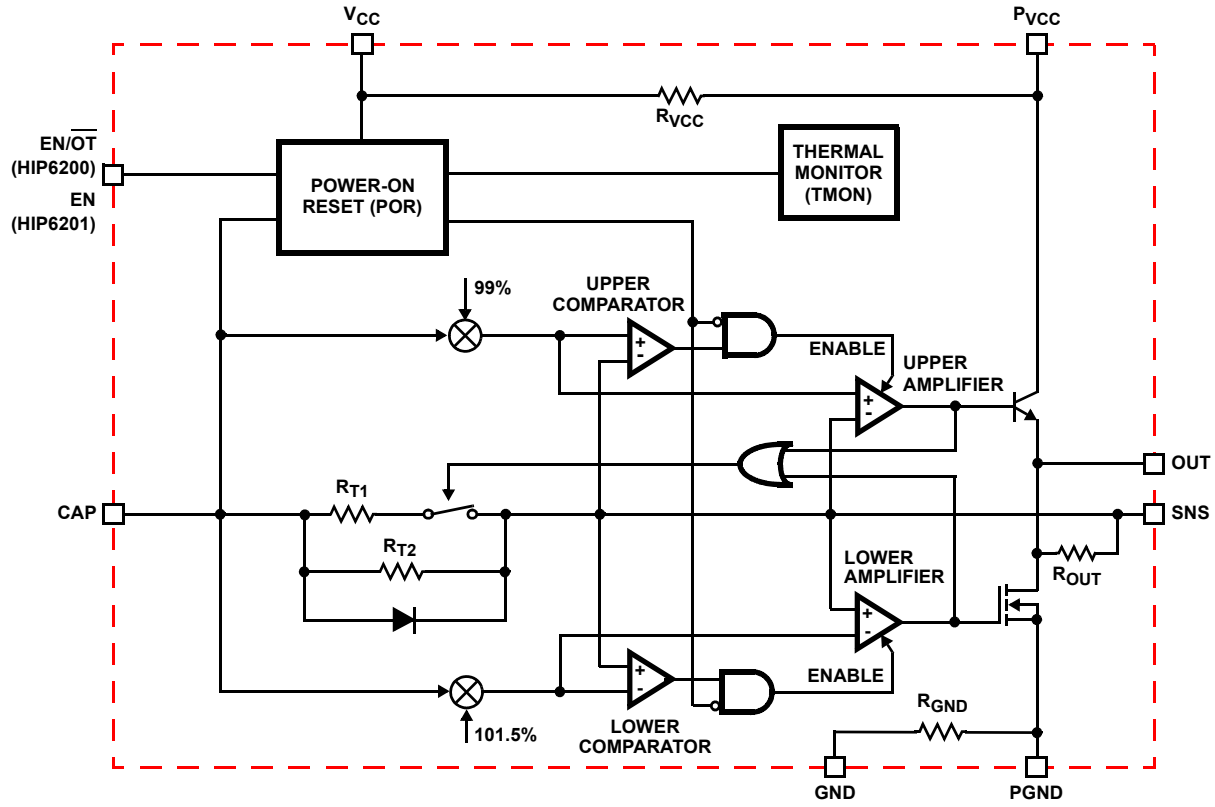
Typical Application - Portable CPU Dynamic Regulator



Block Diagram



Functional Pin Description

P_{VCC} (Pin 1)

P_{VCC} is the power source for the npn transistor output device. P_{VCC} is connected internally to V_{CC} through a resistor. Bulk capacitance should be placed between this pin and PGND to minimize voltage deviations.

PGND (Pin 2)

PGND is power ground for the N-Channel MOSFET output device. Tie this pin to the ground plane of the circuit board.

GND (Pin 3)

GND is signal ground for the IC. Tie this pin to the ground plane of the circuit board.

V_{CC} (Pin 4)

V_{CC} provides bias power to the chip. It should be tied to system 5V. Provide local decoupling to this pin.

CAP (Pin 5)

Connect a capacitor to GND to set the internal amplifiers' on-time response to a rapid voltage change at the SNS pin.

SNS (Pin 6)

SNS is the remote sense of the output voltage to be regulated. If the output voltage increases rapidly by greater than 1.5%, the lower amplifier responds by turning on the N-Channel MOSFET to sink current through the OUT pin to PGND. If the output voltage decreases rapidly by greater than 1%, the upper amplifier responds by turning on the npn transistor to source current from P_{VCC} to OUT.

OUT (Pin 7)

This pin is the output pin of the IC. Tie this pin directly to the voltage to be regulated.

EN/$\overline{OT}$ or EN (Pin 8)

This pin is the only differentiation between the HIP6200 and the HIP6201.

On the HIP6200, this pin is multiplexed. It is chip enable and also an overtemperature indicator. When this pin is low, the chip is disabled. If an overtemperature occurs, this pin will be pulled low internally. Tie EN/$\overline{OT}$ to a pull-up resistor and drive with an open collector signal.

On the HIP6201, this pin is chip enable only. Pulling it low disables the IC. EN should be driven with a logic signal.

Absolute Maximum Ratings

Supply Voltage, V_{CC}, P_{VCC} . . . . . +7.0V
EN, CAP, OUT, SNS . . . . . .GND-0.3V to +7V
GND - PGND . . . . . -0.5V to +0.5V

Operating Conditions

Supply Voltage, V_{CC} . . . . . +5V ±5%
Output Device Supply Voltage, P_{VCC} . . . . . .+4.5V to +5.5V
Output Voltage, OUT = SNS = CAP. . . . . .+1.3V to +2.0V
Load Transient Current . . . . . ±8A
Ambient Operating Temperature Range . . . . . 0°C to 70°C
Junction Temperature Range. . . . . 0°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
SOIC Package . . . . . 145°C/W
Maximum Junction Temperature . . . . . .150°C
Maximum Storage Temperature Range. . . . . .-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . .300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} SUPPLY CURRENT						
Nominal Supply	I_{VCC}		-	300	-	µA
Shutdown Supply	I_{VCC_SD}	EN = GND	-	1	-	µA
PROTECTION CIRCUITRY						
EN Threshold	V_{TH_EN}		0.8	1.5	2.0	V
Overtemperature (OT) Threshold	OT		130	150	170	°C
On-Resistance of OT NMOS	R_{ds_TFN}		-	250	600	Ω
POWER-ON RESET (POR)						
V_{CC} Rising Threshold	V_{THH_VCC}	EN = V_{CC}	-	4.1	4.5	V
V_{CC} Falling Threshold	V_{THL_VCC}	EN = V_{CC}	3.6	4.0	-	V
CAP Rising Threshold	V_{TH_CAP}	EN = V_{CC}	-	1.10	1.20	V
CAP Falling Threshold		EN = V_{CC}	0.95	1.05	-	V
POR Turn-Off Delay to EN Falling			-	2	-	µs
POR Turn-On Delay to EN Rising			-	1	-	ms
POR Turn-Off Delay to V_{CC} UV		EN = V_{CC}, V_{CC} Falling	-	15	-	µs
POR Turn-On Delay after V_{CC} UV		EN = V_{CC}, V_{CC} Rising	-	15	-	µs
POR Turn-Off Delay to CAP UV		EN = V_{CC}, CAP Falling	-	2	-	µs
POR Turn-On Delay after CAP UV		EN = V_{CC}, CAP Rising	-	15	-	µs
REFERENCE VOLTAGE						
V_{SNS} - V_{CAP}	V_{HIGH}	CAP = 2V, SNS Increased Until Amplifier Turns On	-	30	-	mV
V_{CAP} - V_{SNS}	V_{LOW}	CAP = 2V, SNS Decreased Until Amplifier Turns On	-	20	-	mV
AMPLIFIERS						
Transconductance			-	500	-	A/V
Response Time (Rising)		60mV Step on OUT, Time for I_{OUT} < -4A	50	100	175	ns
Response Time (Falling)		-60mV Step on OUT, Time for I_{OUT} > 4A	50	100	175	ns
RESISTOR VALUES						
Small Time Constant Resistor	R_{T1}		120	200	250	Ω
Large Time Constant Resistor	R_{T2}		3000	4000	5500	Ω
V_{CC} to P_{VCC} Resistor	R_{VCC}		6	10	16	Ω
OUT to SNS Resistor	R_{OUT}		1000	1500	2100	Ω
GND to PGND Resistors	R_{GND}		-	140	-	Ω

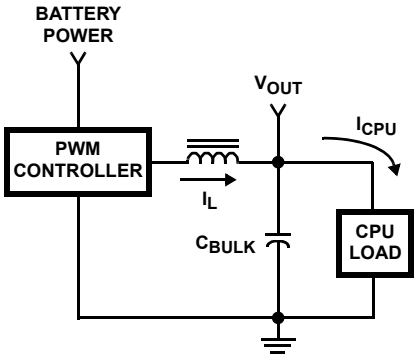
Application Information

Theory of Operation

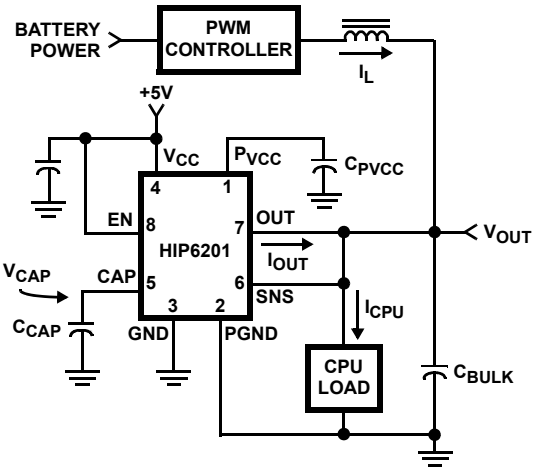
The HIP6200 is used in conjunction with a switching DC/DC converter to provide a regulated DC voltage. The output voltage of a DC/DC converter changes instantly with sudden load changes characteristic of today's microprocessors. This change occurs because the bulk capacitors are imperfect; they have parasitic resistances (ESR) and inductances (ESL) which translate into voltage drops as the load is initially supplied by the bulk capacitance. Also, due to its output inductor, the DC/DC converter takes about 10-20μs (typical) before it provides the load current required by the CPU. The HIP6200 contains two high-speed linear regulators which are inactive except during the converter response time after high di/dt load transients. When active, the linear regulators maintain a small difference between the desired and actual output voltage.

The Typical Application Diagrams below illustrate how the DeCAPitator functions. The left side shows a common DC/DC converter response to a fast 'low-to-high' load transient. The right side shows a similar response with a HIP6200 circuit employed. The HIP6200 allows the use of fewer bulk capacitors to handle the regulation requirements of the high edge-rate load transients. The response time of the HIP6200's linear regulators (100ns typical) are fast enough to help with the leading edge spike. Output voltage deviations during the converter response time are reduced with the HIP6200 since it helps supply the load while the inductor current slews.

Typical Application Diagrams



C_{BULK}: (11) 220μF, 10V, 0.1Ω Tantalums



C_{BULK}: (5) 100μF, 10V, 0.1Ω Tantalums
C_{CAP}: small Ceramic (0805)
C_{VCC}: small Ceramic (0805)
C_{PVCC}: (1) 100μF, 10V, 0.1Ω Tantalum

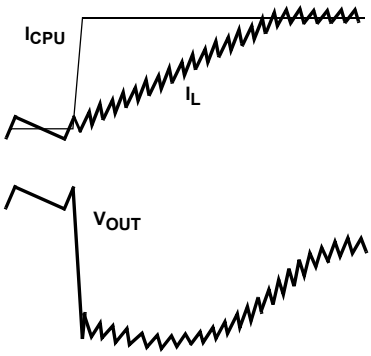


FIGURE 1. PORTABLE CPU WITHOUT HIP6200, HIP6201

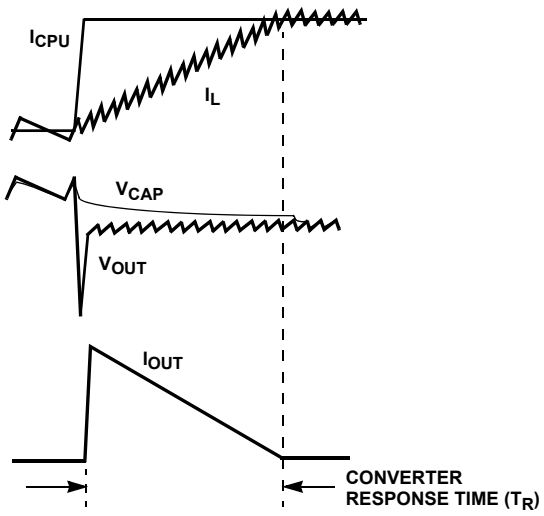


FIGURE 2. PORTABLE CPU WITH HIP6200, HIP6201

Detailed Functional Description

As shown in the Block Diagram, the HIP6200 has two comparators which compare the voltage on the CAP pin to the voltage on the SNS pin. The CAP voltage follows the SNS voltage with an R-C delay which is user programmable and also variable depending upon the state of the amplifiers. Normally, resistor R_{T1} is in parallel with R_{T2} when the amplifiers are not active. R_{T1} is small and the CAP voltage (V_{CAP}) follows the SNS voltage (V_{SNS}) closely. During a transient, when either amplifier is active, the switch in series with R_{T1} opens and R_{T2} alone (with the capacitor on CAP) sets the time constant. Since R_{T2} is 20 times larger than R_{T1}, the DeCAPitator has time to source or sink current as the inductor current slews. The CAP voltage waveform is depicted in the Typical Application Diagrams.

Prior to the load transient, V_{CAP} follows V_{OUT} (and likewise V_{SNS}) closely. This is important in many portable applications because the DC/DC converter will be in an energy-saving skip-cycle mode at light load currents. In this mode, the output voltage ripple may be in excess of ±2% and could trip the HIP6200's comparators if V_{CAP} did not track V_{SNS}. This would turn on the amplifiers and waste power. When a fast load transient occurs, V_{CAP} no longer follows V_{OUT} and the DeCAPitator becomes active when V_{OUT} exceeds +1% or -1.5% of V_{CAP}.

When the DeCAPitator is active, it either supplies current from the P_{VCC} pin or sources current to PGND. Because of this, a high-quality capacitor must be placed locally from P_{VCC} to GND. The system 5V bus typically has a good deal of bulk capacitance as well as high frequency decoupling sprinkled across the application board. P_{VCC} is tied to the system 5V bus through an on-chip 10Ω resistor. This resistor helps isolate the system 5V from the disturbances on P_{VCC}.

The HIP6200 has a power-on reset function which ensures that both V_{CC} and CAP are at some minimum levels before allowing amplifier operation. There is also an EN(ABLE) pin, allowing users to disable the HIP6200 if desired. An overtemperature (OT) shutdown feature ensures that the HIP6200 will not self-destruct from thermal overload. An OT event will shutdown the chip until the junction temperature decreases a few degrees below its trip point.

The DeCAPitator draws very little bias current (300µA typical) when its amplifiers are inactive. When either amplifier is active, the chip draws 15-30mA of bias current. This current is mainly for the active high-speed amplifier and lasts only for the duration of the on-time of the HIP6200.

Component Selection Guidelines

Bulk Output Capacitors

For a given converter design without the HIP6200 in the target application, the number of output capacitors is determined mainly by the output voltage regulation and transient specifications. It is estimated that for a load transient of 0-8A with a di/dt of 20A/µs, eleven 220µF, 0.1Ω low ESR tantalum capacitors are necessary to maintain CPU core voltage regulation specifications. For identical conditions with a HIP6200 employed, only five 100µF, 0.1Ω low ESR tantalums are required. Similar savings in output capacitance can be achieved with other capacitor dielectric-types.

The number of capacitors which can be eliminated on the output is limited by either of the following:

1. Output voltage ripple - this increases proportional to the equivalent ESR of the bulk output capacitance. This may be counteracted by increasing the output inductance. In many cases the inductor can remain the same because the output ripple will still be acceptably small.
2. Leading edge voltage spike - this may increase with reduced number of capacitors. The HIP6200 and its very fast response is very effective in handling this leading edge spike up to a point. Some additional ceramic decoupling on the OUT pin can also help.

P_{VCC} Capacitor

A 100µF, 0.1Ω tantalum is recommended on the P_{VCC} pin for an application which has 8A transients (maximum recommended operation of the HIP6200). R_{VCC} is an internal 10Ω resistor from V_{CC} to P_{VCC} which decouples the P_{VCC} transient from the system 5V (V_{CC}).

CAP Capacitor

The capacitor on the CAP pin sets the amount of time that the HIP6200 has to sink or source current in response to a load transient. The DeCAPitator on-time should be greater than the converter response time. When the HIP6200's amplifiers are not active, the CAP pin follows the output voltage closely to prevent false tripping at light loads due to PWM skip-cycle modes of operation. These two boundaries are addressed with R_{T1} and R_{T2} internal to the HIP6200 but must also be verified on each design.

The converter response time is the time interval required for the inductor current to slew to the output load current. This time is dramatically different for the two edges of the transient event if there is a large differential between input and output voltages of the converter. The converter response times are approximated by v = L*di/dt:

$$T_{R1} = L_{OUT} \bullet \frac{I_{STEP}}{(V_{IN} - V_{OUT})} \quad \text{(EQ. 1)}$$

$$T_{R2} = L_{OUT} \bullet \frac{I_{STEP}}{(V_{OUT})} \quad \text{(EQ. 2)}$$

where

T_{R1} = converter response time to low-to-high load transient

T_{R2} = converter response time to high-to-low load transient

L_{OUT} = output inductor value

I_{STEP} = transient current step amplitude

The value of the capacitor at the CAP pin should be sized so that the HIP6200 can be active in response to a transient for longer than the greater of T_{R1} and T_{R2}. For a 12V to 1.7V DC/DC converter with a 3µH inductor and a 8A maximum transient step size, T_{R1} = 2.3µs and T_{R2} = 14.1µs. Thus, the CAP capacitor should be chosen for the worst-case T_{R2} response. Though the HIP6200 will be active for longer than necessary in response to the low-to-high load transient, the amount of power wasted will be minimal. The upper amplifier will be active, drawing about 15mA, but the power npn darlington will pinch off after the inductor current slews up. The following section details power dissipation further.

Thermal Considerations

HIP6200 Power Dissipation

The power dissipated by the DeCAPitator is a function of many variables. The load transient step size (I_{STEP}), the frequency of the transient events ($1/T_{TRAN}$), and the converter response time (T_{R1}, T_{R2}) have the largest influence. Figure 3 displays these terms.

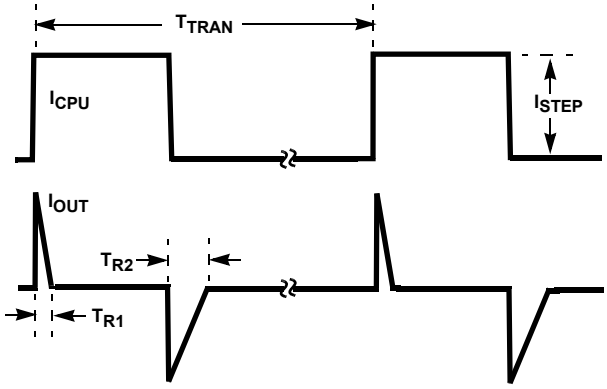


FIGURE 3. IDEALIZED WAVEFORMS OF DeCAPitator OPERATION

Based on some simplifying assumptions, the DeCAPitator power dissipation can be approximated as follows:

$$P_{DISS} = P_{BIAS} + P_{UP} + P_{DWN} \quad \text{(EQ. 3)}$$

where:

$$P_{UP} = (V_{CC} - V_{OUT}) \bullet \left(\frac{I_{STEP}}{2} \bullet \frac{T_{R1}}{T_{TRAN}}\right) \quad \text{(EQ. 4)}$$

$$P_{DWN} = (V_{OUT}) \bullet \left(\frac{I_{STEP}}{2} \bullet \frac{T_{R2}}{T_{TRAN}}\right) \quad \text{(EQ. 5)}$$

$$P_{BIAS} = V_{CC} \bullet (I_{BIAS}) \quad \text{(EQ. 6)}$$

and:

$$I_{BIAS} = I_{IDLE} + \frac{Ibias_{UP} \bullet t_{ACTIVE}}{T_{TRAN}} + \frac{Ibias_{DWN} \bullet t_{ACTIVE}}{T_{TRAN}} \quad \text{(EQ. 7)}$$

I_{IDLE} = nominal supply current when HIP6200 is powered and amplifiers are not active (300µA typical)

$Ibias_{UP}$ = upper amplifier bias current when active (15mA typical)

$Ibias_{DWN}$ = lower amplifier bias current when active (30mA typical)

t_{ACTIVE} = time amplifiers are active. This time is set by CAP capacitor and should be at least as long as T_{R2}.

The bias power is a very small percentage of the total chip power dissipation, but is included for completeness.

Based on these equations, Figures 4 and 5 show how the power dissipation varies with the transient frequency ($1/T_{TRAN}$), step load change (I_{STEP}), and converter response time (T_{R1}, T_{R2}). Both figures assume V_{IN} = 12V and V_{OUT} = 1.7V. Figure 4 assumes a 3µH output inductor and varies the step size (as well as the transient frequency). As mentioned in the previous section, these conditions give T_{R1} = 2.3µs and T_{R2} = 14.1µs for I_{STEP} = 8A. Figure 5 holds I_{STEP} constant at 8A and varies the response time. The converter response time often differs from the ideal (Equations 1 and 2) substantially and therefore should be verified experimentally.

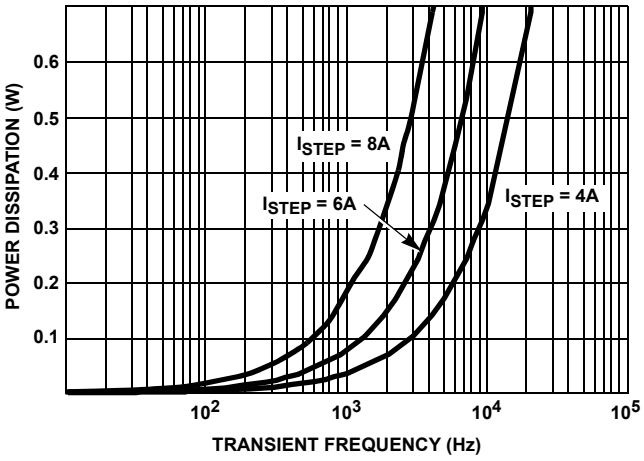


FIGURE 4. ESTIMATED HIP6200, HIP6201 POWER DISSIPATION vs I_{STEP}

Figures 4 and 5 show the relationships between the DeCAPitator power dissipation and the load transient frequency, load transient step size and the converter response time. The power dissipation is linear with the transient frequency but is shown on the log scale to emphasize the fact that the HIP6200/1 power is minimal at frequencies below a few hundred Hertz.

In actual systems, the load transient will most likely be of varying frequency and step size. The power dissipation of the HIP6200/1 becomes even more difficult to estimate analytically.

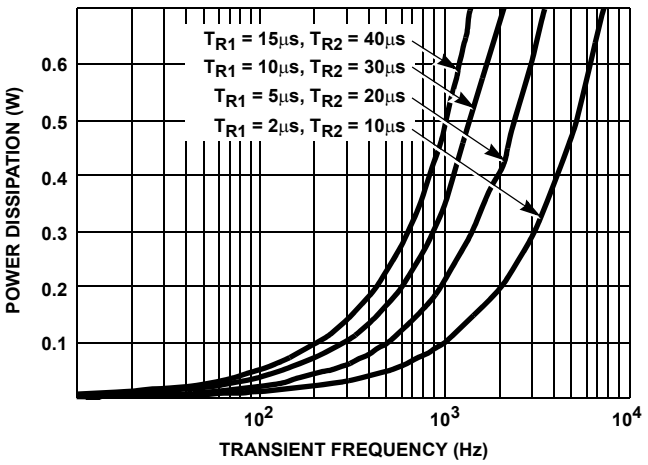


FIGURE 5. ESTIMATED HIP6200, HIP6201 POWER DISSIPATION vs CONVERTER RESPONSE TIME

HIP6200 Temperature Rise

The HIP6200/1 junction temperature can be estimated simply by:

$$T_{HIP6200} = T_{AMBIENT} + (P_{DISS} \bullet \Theta_{JA}) \quad \text{(EQ. 8)}$$

where:

Θ_{JA} is the thermal resistance from junction to ambient.

Example: HIP6200/1 Junction Temperature Calculation

$T_{AMBIENT} = 70^oC$

$P_{DISS} = 0.2W$

$\Theta_{JA} = 100^oC/W$

$T_{HIP6200} = 70^oC + (0.2 \times 100) = 90^oC$

In a similar fashion, one could estimate the maximum allowable power dissipation for given maximum ambient and transient loading and determine the boundary of maximum transient frequency.

Example

Maximum Transient Frequency Calculation

$T_{AMBIENT} = 70^oC$

$T_{HIP6200} = 110^oC$ max

$\Theta_{JA} = 80^oC/W$ (this number is dependent upon airflow and the amount of pc board trace connected to HIP6200

Max $P_{DISS} = (110^oC - 70^oC)/(80^oC/W) = 0.5W$

From Figures 4 and 5, the estimated maximum transient frequency is obtained for any of the seven cases shown. For instance, from Figure 4, the maximum transient frequency is about 4kHz for the 8A transient step and the conditions stipulated.

Layout Considerations

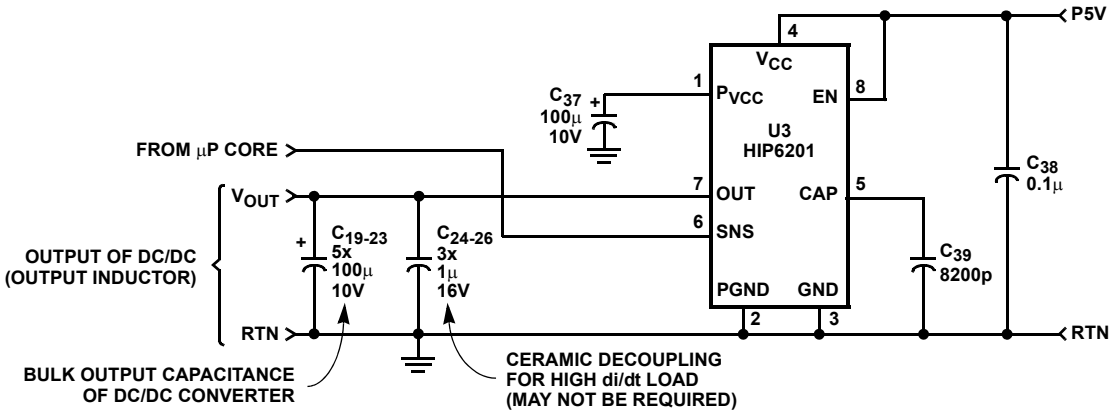
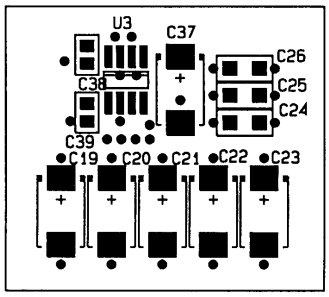


FIGURE 6. TYPICAL SCHEMATIC

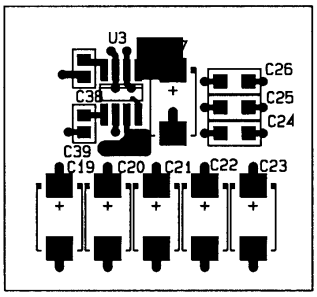
Example Layout

- HIP6200 located near bulk output capacitance (not shown is the microprocessor load itself - for best performance, the HIP6200 and bulk output capacitance should be located close to the µP)
- C_{37} (+5V bulk cap) located near the HIP6200
- Solid ground and V_{OUT} planes with numerous via interconnects

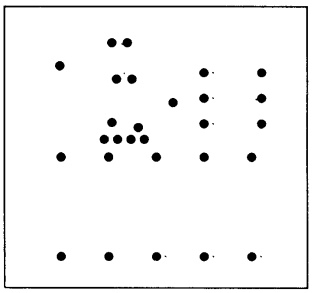
TOP - SILK SCREEN



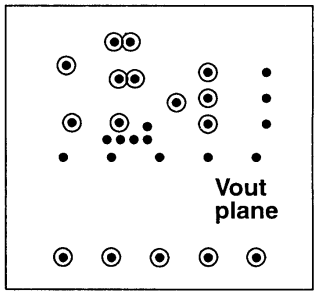
TOP - COMPONENT SIDE



SOLDER SIDE



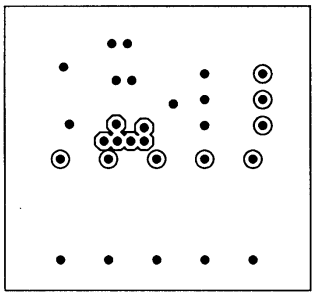
INTERNAL ONE



NOTE: Internal layers are shown as negatives (white is copper):

- via connection to copper plane
- no connection

GND



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