AsahiKASEI MICRODEVICES

AK4432

108dB 192kHz 32bit 2-Channel Audio DAC

1. General Description

The AK4432 is a 32-bit Stereo DAC which corresponds to digital audio systems. An internal circuit includes 32-bit Digital Filter achieving short group delay and high quality sound. The AK4432 has single end SCF outputs, increasing performance for systems with excessive clock jitter. The AK4432 is ideal for a wide range of applications that demands high sound quality including Home Theater and Car audio surround systems. It is housed in a 16-pin TSSOP package, saving more board space.

2. Features

1. 2ch 32bit DAC
- **128 times Oversampling**
- **32-bit High Quality Sound Low Group Delay Digital Filter**
- **Single Ended Output, Smoothing Filter**
- **THD+N: 91dB**
- **DR, S/N: 108dB**
- **Channel Isolation Digital Volume (12dB to -115dB, 0.5dB Step, Mute)**
- **Soft Mute**
- **Audio I/F Format: MSB justified, LSB justified, I^2S, TDM**

2. Sampling Frequency
- **Normal Speed Mode: 8kHz to 48kHz**
- **Double Speed Mode: 48kHz to 96kHz**
- **Quad Speed Mode: 96kHz to 192kHz**

3. Master Clock

256fs, 384fs, 512fs or 768fs	**(Normal Speed Mode: fs=8kHz to 48kHz)**
256fs or 384fs	**(Double Speed Mode: fs=48kHz to 96kHz)**
128fs or 192fs	**(Quad Speed Mode: fs=96kHz to 192kHz)**

4. µP Interface: 3-wire Serial (7MHz max)
I^2C bus (Fast Mode: 400kHz, Fast Mode Plus: 1MHz)

5. Power Supply
- **Analog: AVDD = 3.0 to 3.6V**
- **Input/Output Buffer: LVDD = 3.0 to 3.6V**
- **Integrated LDO for Digital Power Supply**

6. Power Consumption: 7.8mA (fs=48kHz)
7. Operational Temperature: Ta = - 40 to 105°C
8. Package: 16-pin TSSOP (0.65mm pitch)

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4. Block Diagram and Functions

■ Block Diagram

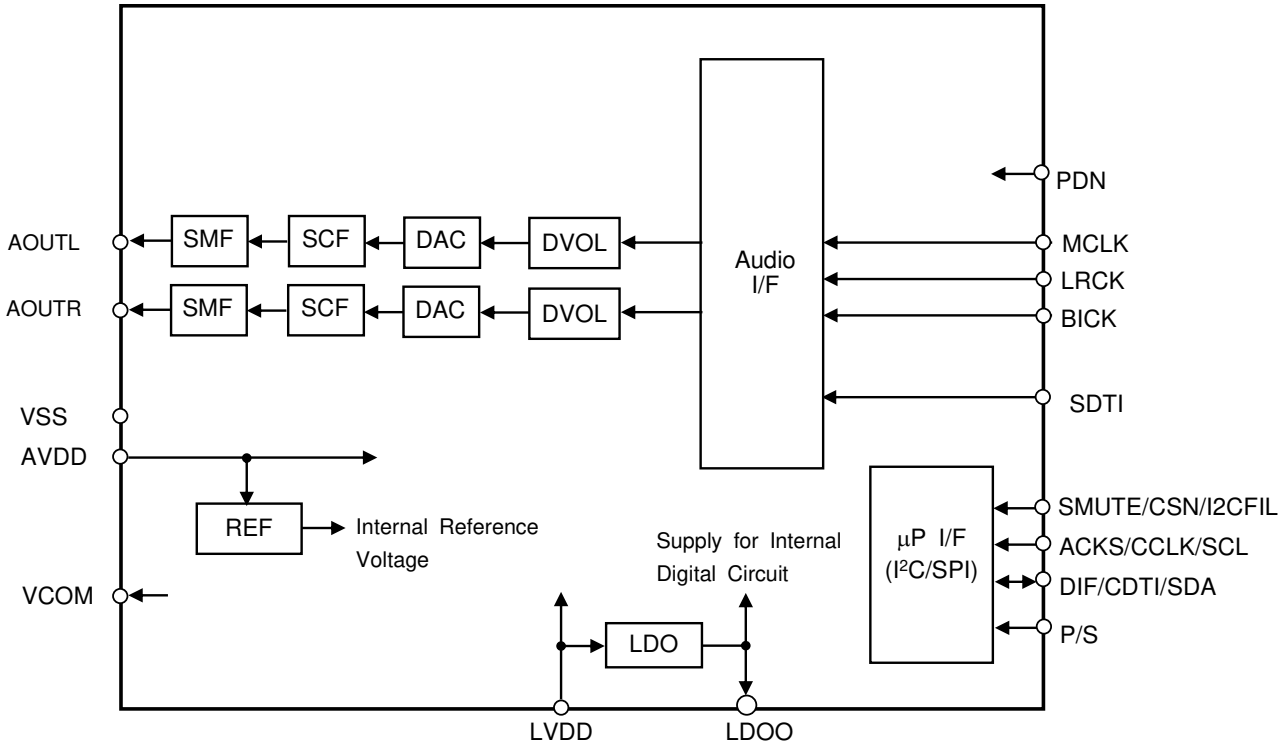


Figure 1. Block Diagram

■ Compatibility with AK4438, AK4452 and AK4458

		AK4432	AK4436 / 38	AK4452 / 54 / 56 / 58
Channel		2ch	6ch / 8ch	2ch / 4ch / 6ch / 8ch
Sampling Frequency fs		8k to 192kHz	8k to 768kHz	8k to 768kHz
S/(N+D)		91dB	91dB	107dB
Dynamic Range		108dB	108dB	115dB
AVDD (Analog Supply)		3.0 to 3.6V	3.0 to 3.6V	3.0 to 5.5V
TVDD or LVDD (Digital Supply)		3.0 to 3.6V	1.7 to 3.6V	1.7 to 3.6V
Digital Filter	Stopband Attenation (Sharp Roll-off)	69.9dB	80dB	80dB
	Group Delay (Sharp Roll-off)	26.4/fs	26.8/fs	26.8/fs
	Group Delay (Short Delay Slow Roll-off)	5.2/fs	4.8/fs	4.8/fs
	Super Slow Roll-off	No	Yes	Yes
OSR Doubler (Over Sampling)		No (128x)	Yes (256x)	Yes (256x)
Zero Detection		No	Yes	Yes
Digital Volume		+12 to -115.0dB	+0 to -127.0dB	+0 to -127.0dB
Attenation Level Transition Time between Max. Gain and Mute (*: default)		4080/fs 1020/fs*	4080/fs* 2040/fs 510/fs 255/fs	4080/fs* 2040/fs 510/fs 255/fs
LR Ch Output Select		No	Yes	Yes
Reset Function (MCLK detect)		No	Yes	Yes
Clock Synchronization		Yes (Note)	Yes	Yes
De-emphasis		No	Yes	Yes
Package		16-pin TSSOP	32-pin QFN	AK4452/54: 32-pin QFN AK4456/58: 48-pin QFN

Note. MSB justified and 32-bit I^2S compatible formats are available for audio interface but LSB justified format is not available.

5. Pin Configurations and Functions

■ Pin Configurations

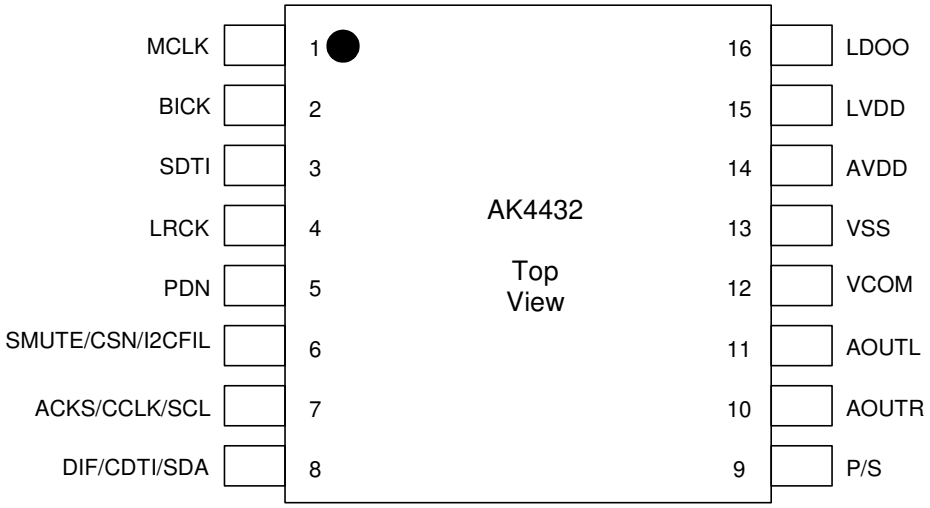


Figure 2. Pin Layout

■ Functions

No.	Pin Name	I/O	State at Power Down	Function
1	MCLK	I	Hi-z	Master Clock Input Pin
2	BICK	I	Hi-z	Audio Serial Data Clock Pin
3	SDTI	I	Hi-z	Audio Serial Data Input Pin
4	LRCK	I	Hi-z	Input Channel Clock Pin
5	PDN	I	Input "L"	Power-Down & Reset Pin When "L", the AK4432 is powered-down and the control registers are reset to default state.
6	SMUTE	I	Hi-z	Soft Mute Pin in Parallel Control mode. When this pin is changed to "H", soft mute cycle is initiated. When returning "L", the output mute releases.
	CSN	I		Chip Select Pin in 3-wire Serial Control mode
	I2CFIL	I		I^2C Interface Mode Select Pin "L": Fast Mode (400kHz), "H": Fast Mode Plus (1MHz). Do not change this pin during PDN pin = "H".
7	ACKS	I	Hi-z	Auto Setting Mode Select Pin in Parallel Control mode "L": Manual Setting mode, "H": Auto Setting mode
	CCLK	I		Control Data Clock Input Pin in 3-wire Serial Control mode
	SCL	I		Control Data Clock Input Pin in I^2C Bus Serial Control mode
8	DIF	I	Hi-z	Audio Data Format Select Pin in Parallel Control mode. "L": 32bit MSB Justified, "H": 32bit I^2S Compatible
	CDTI	I		Control Data Input Pin in 3-wire Serial Control mode
	SDA	I/O		Control Data Input/Output Pin in I^2C Bus Serial Control mode
9	P/S	I	Hi-z	Parallel/Serial Mode Select Pin "L": Serial Mode, "H": Parallel Mode Do not change this pin during PDN pin = "H".
10	AOUTR	O	Hi-z	Rch Analog Output Pin
11	AOUTL	O	Hi-z	Lch Analog Output Pin
12	VCOM	O	500ohm Pull-down	Common Voltage Output Pin, AVDDx1/2 Large external capacitor around 2.2µF is used to reduce power-supply noise.
13	VSS	-	-	Ground Pin
14	AVDD	-	-	Analog Power Supply Pin, 3.0V to 3.6V
15	LVDD	-	-	LDO and Digital I/F Power Supply Pin, 3.0V to 3.6V
16	LDOO	O	580ohm Pull-down	LDO Output Pin This pin should be connected to ground with 1.0µF.

Note 1. All digital input pins must not be allowed to float.

■ Handling of Unused Pin

Handle unused I/O pins as follows.

Classification	Pin Name	Setting
Analog	AOUTL, AOUTR	Open

6. Absolute Maximum Ratings

(VSS =0V; Note 2)

Parameter	Symbol	Min.	Max.	Unit
Power Supply	AVDD	-0.3	4.3	V
Power Supply	LVDD	-0.3	4.3	V
Input Current (any pins except for supplies)	IIN	-	±10	mA
Input Voltage (Note 3)	VIN	-0.3	(LVDD+0.3) or 4.3	V
Ambient Temperature (power applied)	Ta	-40	105	°C
Storage Temperature	Tstg	-65	150	°C

Note 2. All voltages with respect to ground. VSS must be connected to the analog ground plane.
Note 3. The maximum Digital input voltage is smaller value between (LVDD+0.3)V and 4.3V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(VSS=0V; Note 2)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies	Analog	AVDD	3.0	3.3	3.6	V
	LDO, Digital (I/F)	LVDD	3.0	3.3	3.6	V

Note 4. There are no restrictions on the power-up order of AVDD and LVDD. Do not turn off the power supply of the AK4432 with the power supply of the peripheral device turned on. The AK4432's SDA and SCL pins are connected to LVDD with internal protection diodes. When the LVDD pin goes to 0V, the SDA and SCL pins will be shorted to 0V through protection diodes, and as a result other devices on the I^2C bus will not be able to communicate. When using the I^2C interface, pull-up resistors of SDA and SCL pins should be connected to LVDD or less voltage.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

8. Analog Characteristics

(Ta=25°C; AVDD = LVDD=3.3V; VSS =0V; fs=48kHz, 96kHz, 192kHz; BICK=64fs; Signal Frequency=1kHz; 32bit Data; Measurement Frequency=20Hz to 20kHz at fs=48kHz, 20Hz to 40kHz at fs=96kHz, 20Hz to 40kHz at fs=192kHz, unless otherwise specified.)

Parameter		Min.	Typ.	Max.	Unit
DAC Analog Output Characteristics					
Resolution		-	-	32	bit
Output Voltage (Note 5)		2.55	2.83	3.11	Vpp
S/(N+D) (0dBFS)	fs=48kHz	80	91	-	dB
	fs=96kHz	-	89	-	dB
	fs=192kHz	-	89	-	dB
Dynamic Range (-60dBFS)	fs=48kHz (A-weighted)	-	108	-	dB
	fs=96kHz	-	101	-	dB
	fs=192kHz	-	101	-	dB
S/N	fs=48kHz (A-weighted)	-	108	-	dB
	fs=96kHz	-	101	-	dB
	fs=192kHz	-	101	-	dB
Interchannel Isolation		90	110	-	dB
Interchannel Gain Mismatch		-	0	0.7	dB
Load Resistance (Note 6)		10	-	-	kΩ
Load Capacitance		-	-	30	pF

Note 5. Full-scale output voltage. The output voltage is always proportional to AVDD (AVDD x 0.86).
Note 6. AC Load

Parameter		Min.	Typ.	Max.	Unit
Power Supplies Current					
Normal Operation (PDN pin = "H")					
AVDD	fs=48kHz, 96kHz, 192kHz	-	6.5	9.0	mA
LVDD	fs=48kHz	-	1.3	2	mA
	fs=96kHz	-	1.6	2.5	mA
	fs=192kHz	-	2.1	3.0	mA
Power-down mode (PDN pin = "L") (Note 7)		-	10	200	μA

Note 7. Quiescent Current. All digital input pins including clock pins are fixed to VSS.

9. Filter Characteristics

(Ta= -40 to +105°C; AVDD =3.0 to 3.6V, LVDD=3.0 to 3.6V)

■ Sharp Roll-Off Filter (DASD bit = "0", DASL bit = "0")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Passband (Note 8)	-0.08dB to +0.08dB	PB	0	-	22.2	kHz
	-6.0dB	PB	-	23.99	-	kHz
Passband Ripple		PR	-0.08	-	+0.08	dB
Stopband (Note 8)		SB	26.2	-	-	kHz
Stopband Attenuation		SA	69.9	-	-	dB
Group Delay (Note 9)		GD	-	26.4	-	1/fs
Digital Filter + SCF + SMF						
Frequency Response : 0Hz to 20kHz		FR	-0.20	-	0.10	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Passband (Note 8)	-0.08dB to +0.08dB	PB	0	-	44.4	kHz
	-6.0dB	PB	-	48.00	-	kHz
Passband Ripple		PR	-0.08	-	+0.08	dB
Stopband (Note 8)		SB	52.5	-	-	kHz
Stopband Attenuation		SA	69.8	-	-	dB
Group Delay (Note 9)		GD	-	26.4	-	1/fs
Digital Filter + SCF + SMF						
Frequency Response : 0Hz to 40kHz		FR	-0.50	-	0.10	dB

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Passband (Note 8)	-0.08dB to +0.08dB	PB	0	-	88.8	kHz
	-6.0dB	PB	-	96.00	-	kHz
Passband Ripple		PR	-0.08	-	+0.08	dB
Stopband (Note 8)		SB	104.9	-	-	kHz
Stopband Attenuation		SA	69.8	-	-	dB
Group Delay (Note 9)		GD	-	26.4	-	1/fs
Digital Filter + SCF + SMF						
Frequency Response : 0Hz to 80kHz		FR	-2.00	-	0.00	dB

Note 8. The passband and stopband frequencies are proportional to "fs" (sampling rate). Each frequency response refers to that of 1kHz.

Note 9. The calculated delay time caused by digital filtering. The digital filter's delay is calculated as the time from setting 16/24/32bit impulse data into the input register until an analog peak signal is output.

■ **Slow Roll-Off Filter (DASD bit = "0", DASL bit = "1")**

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Passband (Note 8)	-0.07dB to +0.021dB	PB	0	-	9.0	kHz
	-3.0dB	PB	-	19.75	-	kHz
Passband Ripple		PR	-0.07	-	+0.021	dB
Stopband (Note 8)		SB	42.6	-	-	kHz
Stopband Attenuation		SA	72.6	-	-	dB
Group Delay (Note 9)		GD	-	26.4	-	1/fs
Digital Filter + SCF + SMF						
Frequency Response: 0Hz to 20kHz		FR	-3.75	-	-2.75	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Passband (Note 8)	-0.07dB to +0.023dB	PB	0	-	18.1	kHz
	-3.0dB	PB	-	39.6	-	kHz
Passband Ripple		PR	-0.07	-	+0.023	dB
Stopband (Note 8)		SB	85.1	-	-	kHz
Stopband Attenuation		SA	72.6	-	-	dB
Group Delay (Note 9)		GD	-	26.4	-	1/fs
Digital Filter + SCF + SMF						
Frequency Response: 0Hz to 40kHz		FR	-4.25	-	-2.75	dB

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Passband (Note 8)	-0.07dB to +0.023dB	PB	0	-	36.1	kHz
	-3.0dB	PB	-	79.3	-	kHz
Passband Ripple		PR	-0.07	-	+0.023	dB
Stopband (Note 8)		SB	170.3	-	-	kHz
Stopband Attenuation		SA	72.6	-	-	dB
Group Delay (Note 9)		GD	-	26.4	-	1/fs
Digital Filter + SCF + SMF						
Frequency Response: 0Hz to 80kHz		FR	-5.00	-	-3.00	dB

Note 8. The passband and stopband frequencies are proportional to "fs" (sampling rate). Each frequency response refers to that of 1kHz.

Note 9. The calculated delay time caused by digital filtering. The digital filter's delay is calculated as the time from setting 16/24/32bit impulse data into the input register until an analog peak signal is output.

■ **Short Delay Sharp Roll-Off Filter (DASD bit = "1", DASL bit = "0")**

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Passband (Note 8)	-0.07dB to +0.07dB	PB	0	-	22.0	kHz
	-6.0dB	PB	-	24.11	-	kHz
Passband Ripple		PR	-0.07	-	+0.07	dB
Stopband (Note 8)		SB	26.2	-	-	kHz
Stopband Attenuation		SA	56.6	-	-	dB
Group Delay (Note 9)		GD	-	5.9	-	1/fs
Digital Filter + SCF + SMF						
Frequency Response : 0Hz to 20kHz		FR	-0.20	-	0.10	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Passband (Note 8)	-0.08dB to +0.08dB	PB	0	-	44.3	kHz
	-6.0dB	PB	-	48.25	-	kHz
Passband Ripple		PR	-0.08	-	+0.08	dB
Stopband (Note 8)		SB	52.5	-	-	kHz
Stopband Attenuation		SA	56.4	-	-	dB
Group Delay (Note 9)		GD	-	5.9	-	1/fs
Digital Filter + SCF + SMF						
Frequency Response : 0Hz to 40kHz		FR	-0.50	-	0.10	dB

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Passband (Note 8)	-0.08dB to +0.08dB	PB	0	-	88.6	kHz
	-6.0dB	PB	-	96.50	-	kHz
Passband Ripple		PR	-0.08	-	+0.08	dB
Stopband (Note 8)		SB	104.9	-	-	kHz
Stopband Attenuation		SA	56.4	-	-	dB
Group Delay (Note 9)		GD	-	5.9	-	1/fs
Digital Filter + SCF + SMF						
Frequency Response : 0Hz to 80kHz		FR	-2.00	-	0.00	dB

Note 8. The passband and stopband frequencies are proportional to "fs" (sampling rate). Each frequency response refers to that of 1kHz.

Note 9. The calculated delay time caused by digital filtering. The digital filter's delay is calculated as the time from setting 16/24/32bit impulse data into the input register until an analog peak signal is output.

■ **Short Delay Slow Roll-Off Filter (DASD bit = "1", DASL bit = "1")**

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Passband (Note 8)	-0.07dB to +0.05dB	PB	0	-	10.1	kHz
	-3.0dB	PB	-	20.24	-	kHz
Passband Ripple		PR	-0.07	-	+0.05	dB
Stopband (Note 8)		SB	43.0	-	-	kHz
Stopband Attenuation		SA	74.9	-	-	dB
Group Delay (Note 9)		GD	-	5.2	-	1/fs
Digital Filter + SCF + SMF						
Frequency Response : 0Hz to 20kHz		FR	-3.50	-	-2.50	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Passband (Note 8)	-0.07dB to +0.05dB	PB	0	-	20.3	kHz
	-3.0dB	PB	-	40.50	-	kHz
Passband Ripple		PR	-0.07	-	+0.05	dB
Stopband (Note 8)		SB	86.0	-	-	kHz
Stopband Attenuation		SA	74.9	-	-	dB
Group Delay (Note 9)		GD	-	5.2	-	1/fs
Digital Filter + SCF + SMF						
Frequency Response : 0Hz to 40kHz		FR	-4.00	-	-2.50	dB

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
Passband (Note 8)	-0.07dB to +0.05dB	PB	0	-	40.6	kHz
	-3.0dB	PB	-	81.00	-	kHz
Passband Ripple		PR	-0.07	-	+0.05	dB
Stopband (Note 8)		SB	172.0	-	-	kHz
Stopband Attenuation		SA	74.9	-	-	dB
Group Delay (Note 9)		GD	-	5.2	-	1/fs
Digital Filter + SCF + SMF						
Frequency Response : 0Hz to 80kHz		FR	-4.75	-	-2.75	dB

Note 8. The passband and stopband frequencies are proportional to "fs" (sampling rate). Each frequency response refers to that of 1kHz.

Note 9. The calculated delay time caused by digital filtering. The digital filter's delay is calculated as the time from setting 16/24/32bit impulse data into the input register until an analog peak signal is output.

10. DC Characteristics

(Ta= -40 to +105°C; AVDD =3.0 to 3.6V, LVDD =3.0 to 3.6V, VSS=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
All digital input pins except SCL and SDA pins					
High-Level Input Voltage	VIH1	80%LVDD	-	-	V
Low-Level Input Voltage	VIL1	-	-	20%LVDD	V
SCL, SDA Pin					
High-Level Input Voltage	VIH2	70%LVDD	-	-	V
Low-Level Input Voltage	VIL2	-	-	30%LVDD	V
SDA Pin					
Low-Level Output Voltage					
Fast Mode (Iout= 3mA)	VOL1	-	-	0.4	V
Fast Mode Plus (Iout= 20mA)	VOL2	-	-	0.4	V
Input Leakage Current	Iin	-	-	±10	μA

11. Switching Characteristics

■ Clock Timing

(Ta=-40 to 105°C; AVDD=LVDD=3.0 to 3.6V; C_L=20pF, unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Master Clock Timing						
256fsn						
Frequency		fCLK	2.048	-	12.288	MHz
Pulse Width Low		tCLKL	32	-	-	ns
Pulse Width High		tCLKH	32	-	-	ns
384fsn						
Frequency		fCLK	3.072	-	18.432	MHz
Pulse Width Low		tCLKL	22	-	-	ns
Pulse Width High		tCLKH	22	-	-	ns
512fsn, 256fsd, 128fsq						
Frequency		fCLK	4.096	-	24.576	MHz
Pulse Width Low		tCLKL	16	-	-	ns
Pulse Width High		tCLKH	16	-	-	ns
768fsn, 384fsd, 192fsq						
Frequency		fCLK	16.384	-	36.864	MHz
Pulse Width Low		tCLKL	11	-	-	ns
Pulse Width High		tCLKH	11	-	-	ns
LRCK Timing						
Stereo mode (TDM1-0 bits = "00")						
Frequency (fs)	Normal Speed mode	fsn	8	-	48	kHz
	Double Speed mode	fsd	48	-	96	kHz
	Quad Speed mode	fsq	96	-	192	kHz
Duty Cycle		Duty	-	50	-	%
TDM128 mode (TDM1-0 bits = "01")						
Frequency (fs)	Normal Speed mode	fsn	8	-	48	kHz
	Double Speed mode	fsd	48	-	96	kHz
	Quad Speed mode	fsq	96	-	192	kHz
I^2S compatible: Pulse Width Low		tLRL	1/(128fs)	-	127/(128fs)	s
MSB or LSB justified: Pulse Width High		tLRH	1/(128fs)	-	127/(128fs)	s
TDM256 mode (TDM1-0 bits = "10", "11")						
Frequency (fs)	Normal Speed mode	fsn	8	-	48	kHz
	Double Speed mode	fsd	48	-	96	kHz
I^2S compatible: Pulse Width Low		tLRL	1/(256fs)	-	255/(256fs)	s
MSB or LSB justified: Pulse Width High		tLRH	1/(256fs)	-	255/(256fs)	s

■ Audio Interface Timing

(Ta=-40 to 105°C; AVDD=LVDD=3.0 to 3.6V; C_L=20pF, unless otherwise specified)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Audio Interface Timing							
Normal mode (TDM1-0 bits = "00")							
BICK Period	Normal Speed mode		tBCK	1/256fsn	-	-	ns
	Double Speed mode		tBCK	1/256fsd	-	-	ns
	Quad Speed mode		tBCK	1/128fsq	-	-	ns
BICK Pulse Width Low			tBCKL	18	-	-	ns
BICK Pulse Width High			tBCKH	18	-	-	ns
BICK "↑" to LRCK Edge		(Note 10)	tBLR	5	-	-	ns
LRCK Edge to BICK "↑"		(Note 10)	tLRB	5	-	-	ns
SDTI Hold Time			tSDH	5	-	-	ns
SDTI Setup Time			tSDS	5	-	-	ns
TDM128 mode (TDM1-0 bits = "01")							
BICK Period	Normal Speed mode		tBCK	1/128fsn	-	-	ns
	Double Speed mode		tBCK	1/128fsd	-	-	ns
	Quad Speed mode		tBCK	1/128fsq	-	-	ns
BICK Pulse Width Low			tBCKL	18	-	-	ns
BICK Pulse Width High			tBCKH	18	-	-	ns
BICK "↑" to LRCK Edge		(Note 10)	tBLR	5	-	-	ns
LRCK Edge to BICK "↑"		(Note 10)	tLRB	5	-	-	ns
SDTI Hold Time			tSDH	5	-	-	ns
SDTI Setup Time			tSDS	5	-	-	ns
TDM256 mode (TDM1-0 bits = "10", "11")							
BICK Period	Normal Speed mode		tBCK	1/256fsn	-	-	ns
	Double Speed mode		tBCK	1/256fsd	-	-	ns
BICK Pulse Width Low			tBCKL	18	-	-	ns
BICK Pulse Width High			tBCKH	18	-	-	ns
BICK "↑" to LRCK Edge		(Note 10)	tBLR	5	-	-	ns
LRCK Edge to BICK "↑"		(Note 10)	tLRB	5	-	-	ns
SDTI Hold Time			tSDH	5	-	-	ns
SDTI Setup Time			tSDS	5	-	-	ns

Note 10. BICK rising edge must not occur at the same time as LRCK edge.

■ Serial Interface Timing

(Ta=-40 to 105°C; AVDD=LVDD=3.0 to 3.6V; C_L=20pF, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit
3-wire Serial mode					
CCLK frequency	tCCK	-	-	7	MHz
CCLK Pulse Width Low	tCCKL	60	-	-	ns
Pulse Width High	tCCKH	60	-	-	ns
CDTI Setup Time	tCDS	60	-	-	ns
CDTI Hold Time	tCDH	60	-	-	ns
CSN "H" Time	tCSW	150	-	-	ns
CSN "↓" to CCLK "↓"	tCSS	150	-	-	ns
CCLK "↑" to CSN "↑"	tCSH	240	-	-	ns
I²C Fast mode					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling (Note 11)	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-		1.0	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Capacitive load on bus	Cb	-	-	400	pF
I²C Fast mode Plus					
SCL Clock Frequency	fSCL	-	-	1	MHz
Bus Free Time Between Transmissions	tBUF	0.5	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.26	-	-	µs
Clock Low Time	tLOW	0.5	-	-	µs
Clock High Time	tHIGH	0.26	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.26	-	-	µs
SDA Hold Time from SCL Falling (Note 12)	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.05	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.12	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.12	µs
Setup Time for Stop Condition	tSU:STO	0.26	-	-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Capacitive load on bus	Cb	-	-	550	pF
Power-down & Reset Timing					
PDN Pulse Width (Note 13)	tPD	800	-	-	ns

Note 11. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
Note 12. Data must be held for sufficient time to bridge the 120ns transition time of SCL.
Note 13. The AK4432 can be reset by setting the PDN pin to "L" upon power-up. The PDN pin must held "L" for more than 800ns for a certain reset. The AK4432 is not reset by the "L" pulse less than 50ns.
Note 14. I²C is a trademark of NXP B.V.

■ Timing Diagram

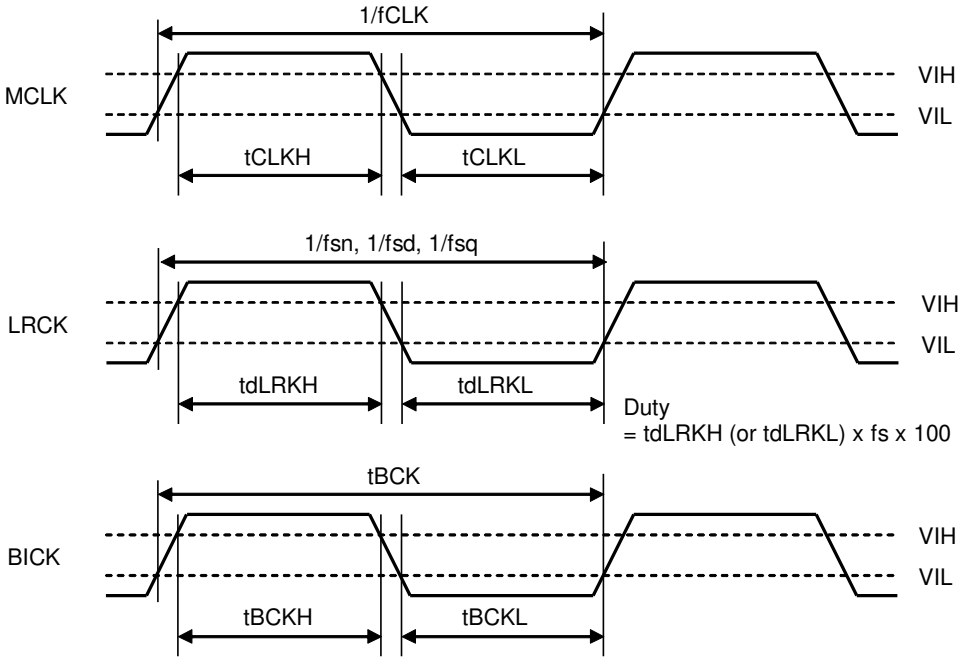


Figure 3. Clock Timing (TDM1-0 bits = “00”)

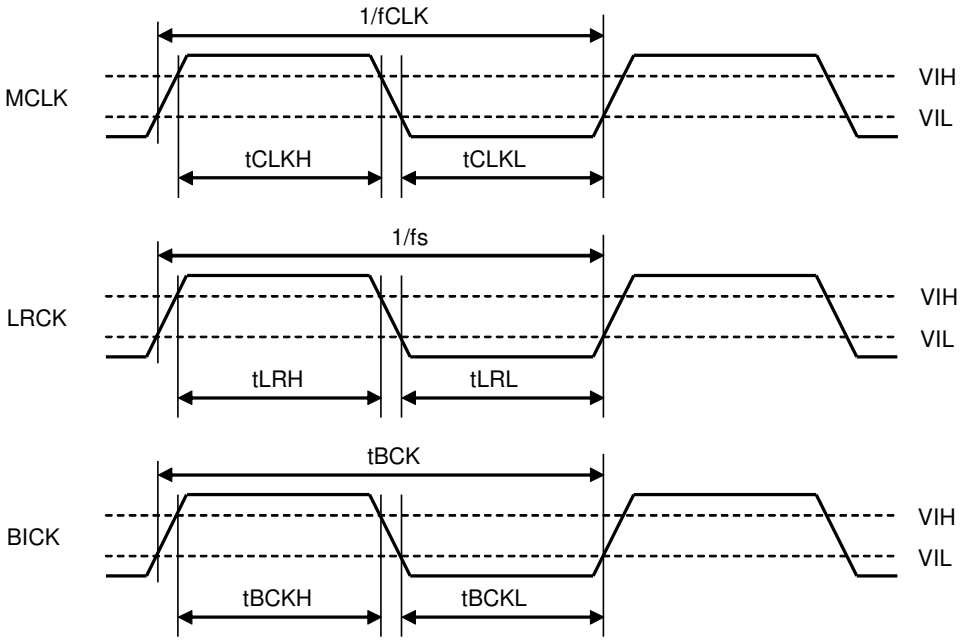


Figure 4. Clock Timing (Except TDM1-0 bits = “00”)

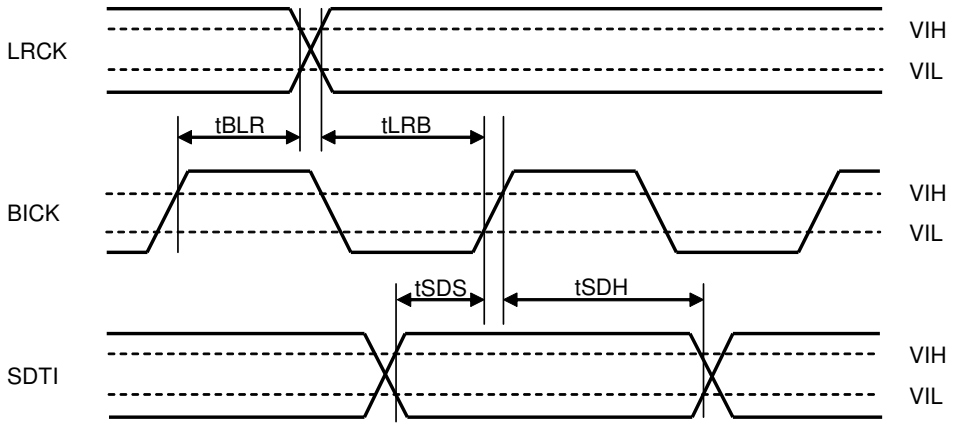


Figure 5. Audio Interface Timing (TDM1-0 bits = “00”)

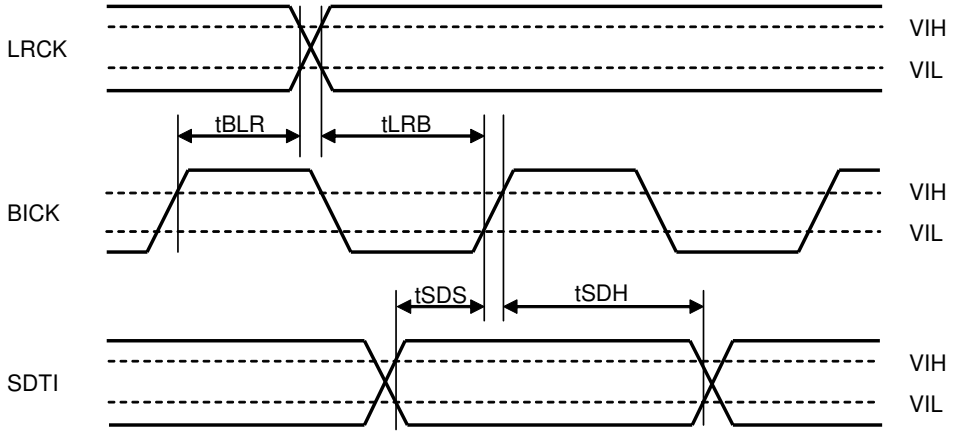


Figure 6. Audio Interface Timing (Except TDM1-0 bits = “00”)

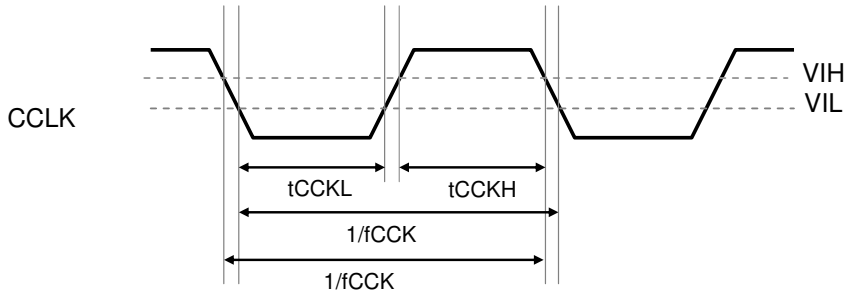


Figure 7. 3-wire Serial Mode Interface Timing

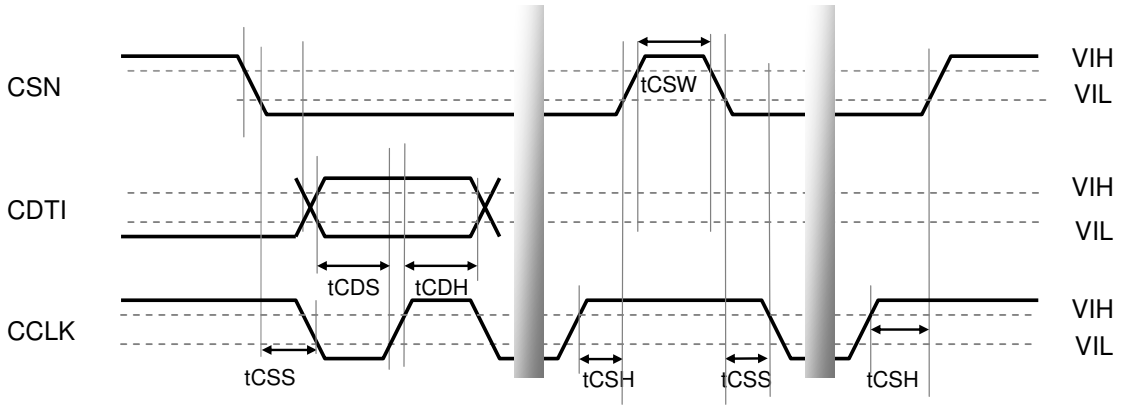


Figure 8. WRITE Data Input Timing (3-wire Serial mode)

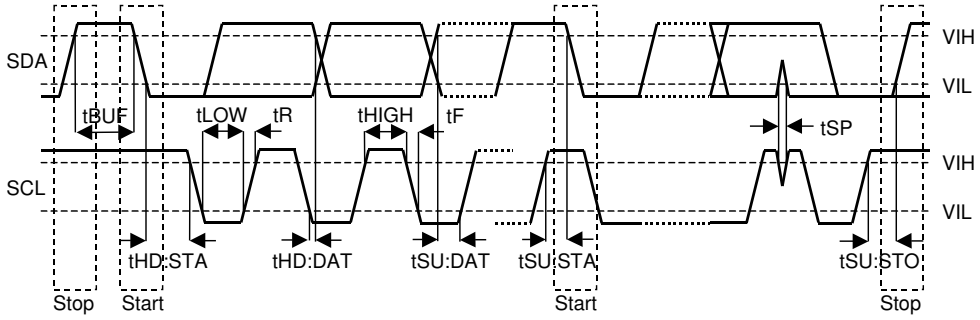


Figure 9. I²C Bus Mode Timing

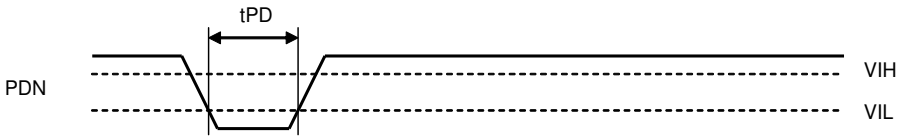


Figure 10. Power-down & Reset Timing

12. Functional Descriptions

■ System Clocks

The external clocks which are required to operate the AK4432 are MCLK, LRCK and BICK. MCLK should be synchronized with LRCK and BICK but the phase is not critical. There are two methods to set sampling frequency. ACKS bit = "0" for manual setting mode and ACKS bit = "1" for auto setting mode. In manual setting mode, the sampling speed mode is set by DFS1-0 bits (Table 1). Table 2, Table 3 and Table 4 show the MCLK frequencies that can be used in each sampling speed mode. In auto setting mode, DFS1-0 bits do not need to be set. Sampling speed mode is automatically detected. The DFS1-0 bits setting is ignored. Table 5 and Table 6 show the MCLK frequencies that can be used in each sampling speed mode.

The internal reset is released by inputting MCLK and LRCK after setting the PDN pin to "H". If the clock is stopped, a click noise occurs when restarting the clock. Mute the digital output externally if the click noise affects system applications.

DFS1 bit	DFS0 bit	Sampling Speed Mode (fs)		
0	0	Normal Speed mode	8kHz to 48kHz	(default)
0	1	Double Speed mode	48kHz to 96kHz	
1	0	Quad Speed mode	96kHz to 192kHz	
1	1	N/A	-	

(N/A: Not available)

Table 1. Sampling Speed Mode (Manual Setting Mode)

LRCK Freq.	MCLK Frequency [MHz]				BICK Freq. [MHz]
fs	256fs	384fs	512fs	768fs	64fs
8.0kHz	2.0480	3.0720	4.0960	6.1440	0.512
44.1kHz	11.2896	16.9344	22.5792	33.8688	2.8224
48.0kHz	12.2880	18.4320	24.5760	36.8640	3.0720

Table 2. System Clock Example (Normal Speed Mode @Manual Setting Mode)

LRCK Freq.	MCLK Frequency [MHz]		BICK Freq. [MHz]
fs	256fs	384fs	64fs
88.2kHz	22.5792	33.8688	5.6448
96.0kHz	24.5760	36.8640	6.1440

Table 3. System Clock Example (Double Speed Mode @Manual Setting Mode)

LRCK Freq.	MCLK Frequency [MHz]		BICK Freq. [MHz]
fs	128fs	192fs	64fs
176.4kHz	22.5792	33.8688	11.2896
192.0kHz	24.5760	36.8640	12.2880

Table 4. System Clock Example (Quad Speed Mode @Manual Setting Mode)

Sampling Speed Mode	MCLK Frequency	
Normal Speed Mode	512fs	768fs
Double Speed Mode	256fs	384fs
Quad Speed Mode	128fs	192fs

Table 5. Sampling Speed Mode and Available MCLK Frequency (Auto Setting Mode)

LRCK	MCLK Frequency [MHz]						Sampling Speed Mode
fs	128fs	192fs	256fs	384fs	512fs	768fs	
8.0kHz	-	-	-	-	4.0960	6.1440	Normal Speed Mode
44.1kHz	-	-	-	-	22.5792	33.8688	
48.0kHz	-	-	-	-	24.5760	36.8640	
88.2kHz	-	-	22.5792	33.8688	-	-	Double Speed Mode
96.0kHz	-	-	24.5760	36.8640	-	-	
176.4kHz	22.5792	33.8688	-	-	-	-	Quad Speed Mode
192.0kHz	24.5760	36.8640	-	-	-	-	

(-: Not available)

Table 6. System Clock Example (Auto Setting Mode)

■ Audio Interface Format

Audio data is shifted in via the SDTI pin using BICK and LRCK inputs. The audio data is latched on the rising edge of BICK. The serial data is MSB first, 2's complement. Data format is selected by the TDM1-0 bits and DIF2-0 bits as shown in Table 7. Input "0" data to unused bits if the data does not use maximum bits when MSB justified, I²S format is selected. (e.g. Mode2 can be used in 16-bit MSB justified by zeroing the unused 8bits LSB). TDM1-0 bits, DIF2-0 bits, SDS2-0 bits and DIF pin settings should not be changed during operation.

Normal Mode (TDM1-0 bit="00")
Two channels audio data is shifted in via the SDTI pin. Eight data formats are supported.

TDM128 Mode (TDM1-0 bit="01")
Four channels audio data is shifted in via the SDTI pin. Two channel data is selected by SDS1-0 bits. BICK is fixed to 128fs. Six data formats are supported.

TDM256 Mode (TDM1-0 bit="1X")
Eight channels audio data is shifted in via the SDTI pin. Two channel data is selected by SDS1-0 bits. BICK is fixed to 256fs. Six data formats are supported.

Mode		TDM1 bit	TDM0 bit	DIF2 bit	DIF1 bit	DIF0 bit	SDTI Input Data Format	LRCK Polarity	BICK Frequency
Normal (Note 15)	0	0	0	0	0	0	16-bit LSB justified	H/L	≥32fs
	1			0	0	1	20-bit LSB justified	H/L	≥40fs
	2			0	1	0	24-bit MSB justified	H/L	≥48fs
	3			0	1	1	16-bit I²S compatible	L/H	32fs
							24-bit I²S compatible	L/H	≥48fs
	4			1	0	0	24-bit LSB justified	H/L	≥48fs
	5			1	0	1	32-bit LSB justified	H/L	≥64fs
	6			1	1	0	32-bit MSB justified	H/L	≥64fs
	7			1	1	1	32-bit I²S compatible	L/H	≥64fs
TDM128	-	0	1	0	0	0	N/A	↑	128fs
	-			0	0	1	N/A	↑	128fs
	8			0	1	0	24-bit MSB justified	↑	128fs
	9			0	1	1	24-bit I²S compatible	↓	128fs
	10			1	0	0	24-bit LSB justified	↑	128fs
	11			1	0	1	32-bit LSB justified	↑	128fs
	12			1	1	0	32-bit MSB justified	↑	128fs
	13			1	1	1	32-bit I²S compatible	↓	128fs
TDM256	-	1	x	0	0	0	N/A	↑	256fs
	-			0	0	1	N/A	↑	256fs
	14			0	1	0	24-bit MSB justified	↑	256fs
	15			0	1	1	24-bit I²S compatible	↓	256fs
	16			1	0	0	24-bit LSB justified	↑	256fs
	17			1	0	1	32-bit LSB justified	↑	256fs
	18			1	1	0	32-bit MSB justified	↑	256fs
	19			1	1	1	32-bit I²S compatible	↓	256fs

(N/A: Not available, x: "0" or "1")

Note 15. BICK that is input to each channel must be longer than the bit length of setting format. For 16-bit I²S compatibility, set BICK to 16 clocks per channel.

Table 7. Audio Data Format

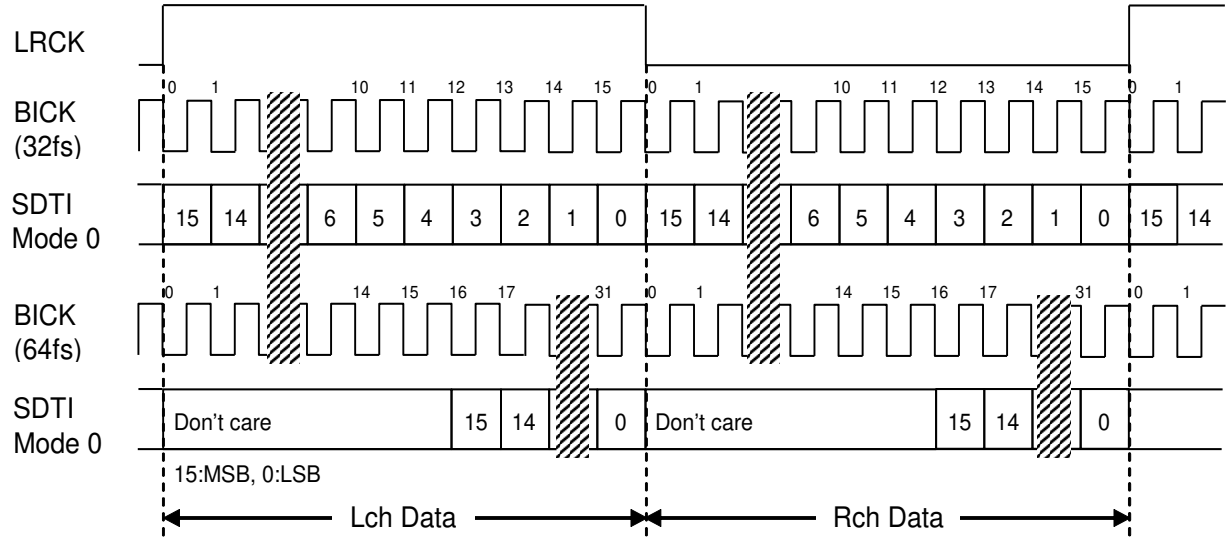


Figure 11. Mode 0 Timing

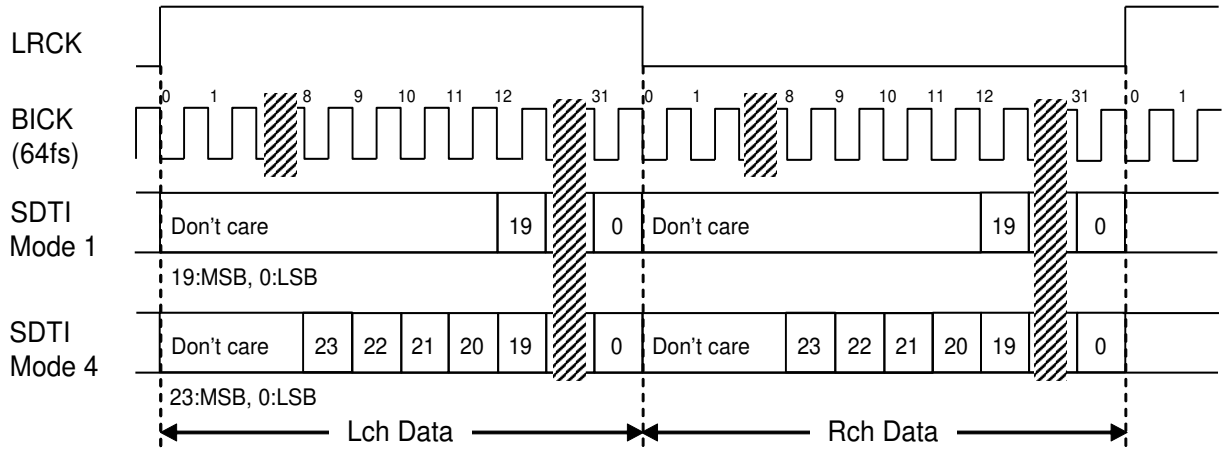


Figure 12. Mode 1/4 Timing

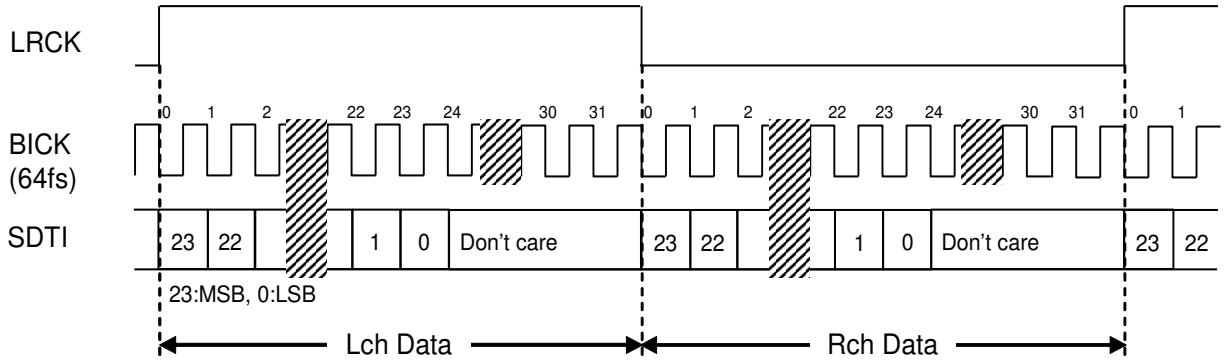


Figure 13. Mode 2 Timing

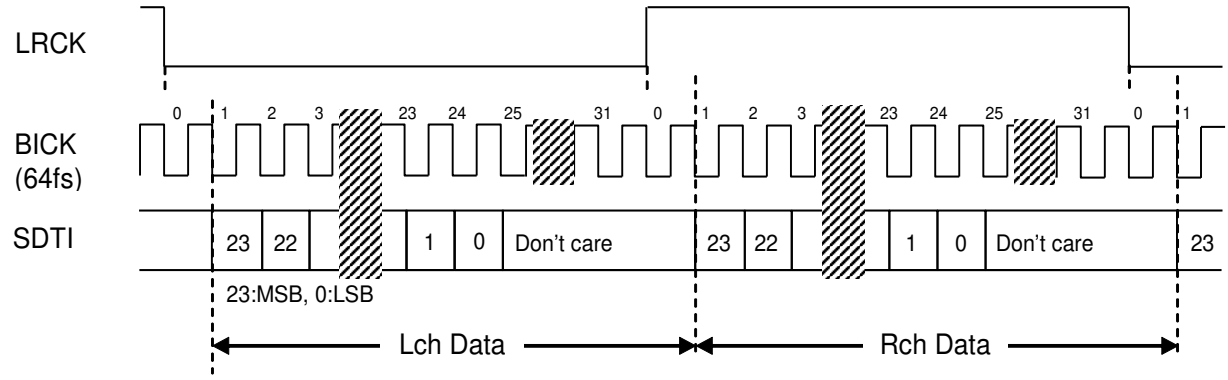


Figure 14. Mode 3 Timing

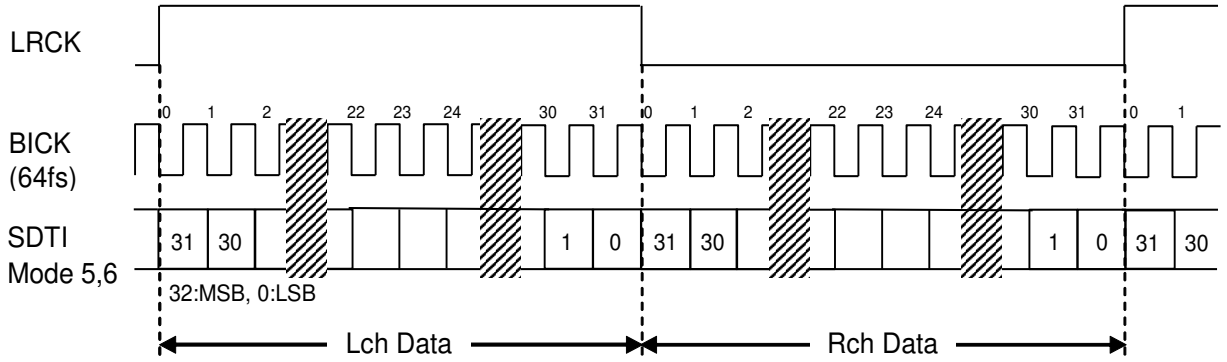


Figure 15. Mode 5/6 Timing

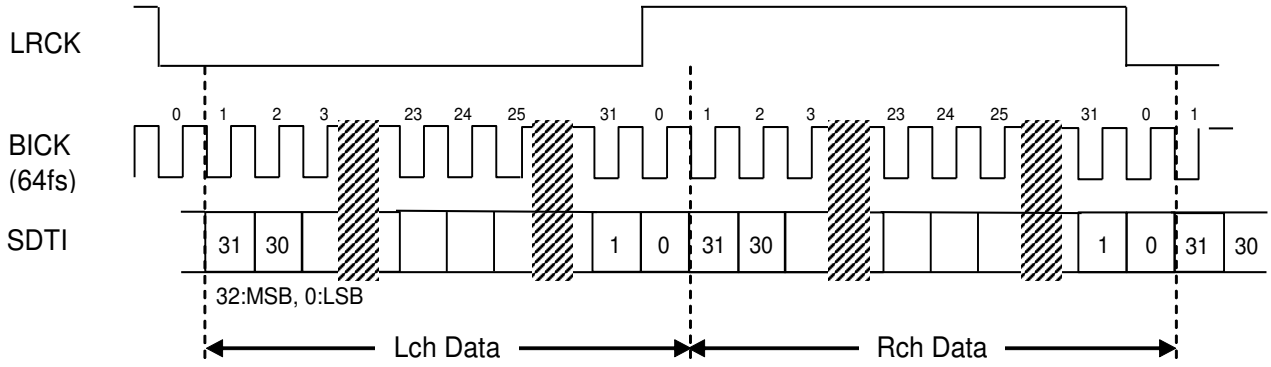


Figure 16. Mode 7 Timing

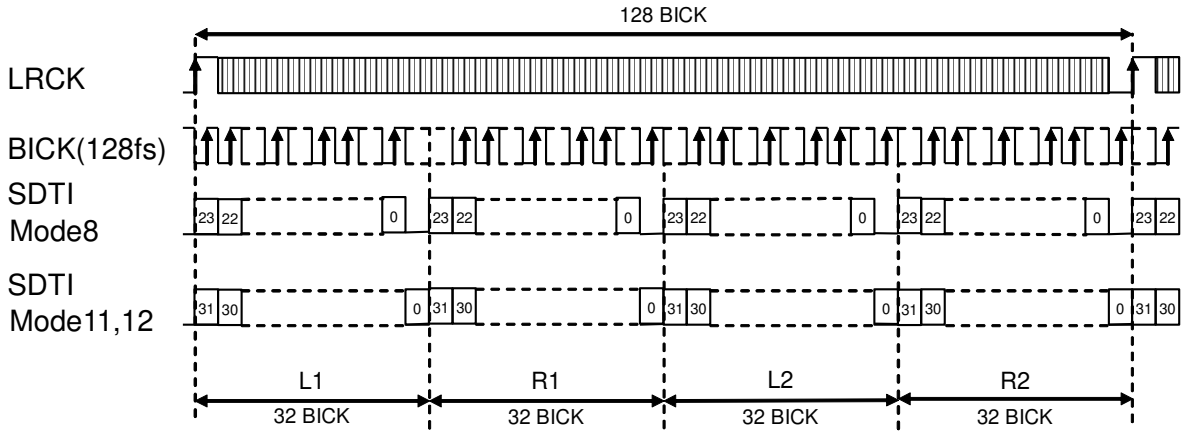


Figure 17. Mode 8/11/12 Timing

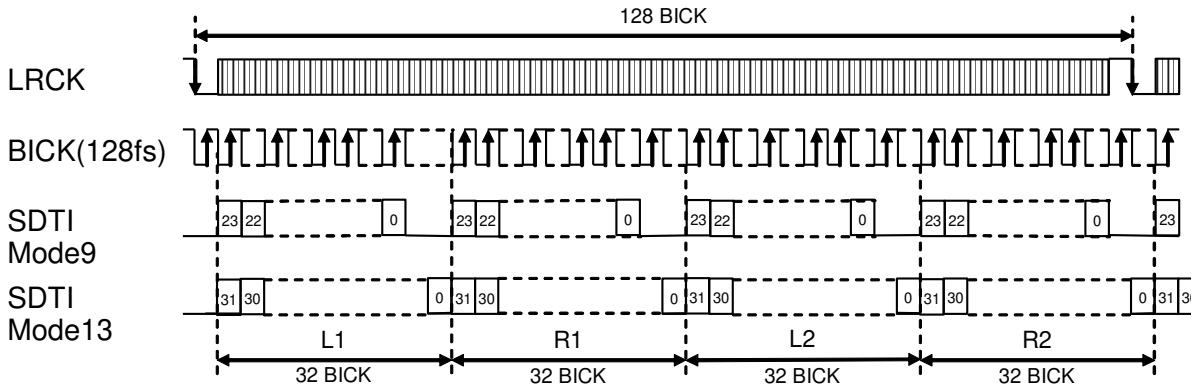


Figure 18. Mode 9/13 Timing

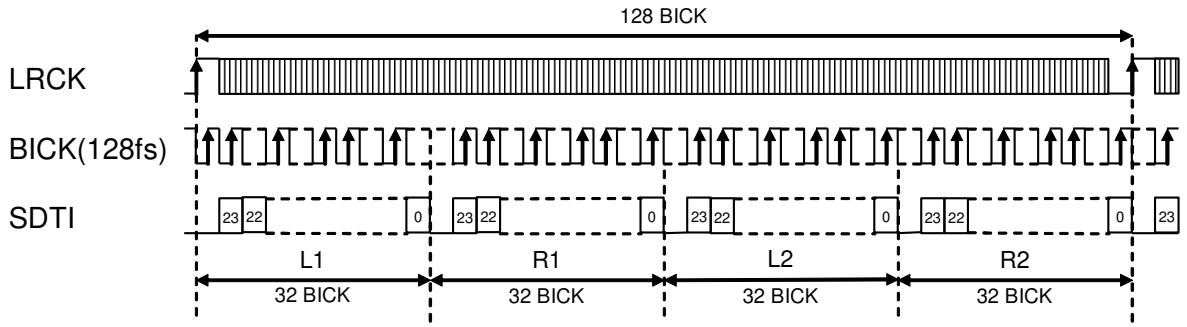


Figure 19. Mode 10 Timing

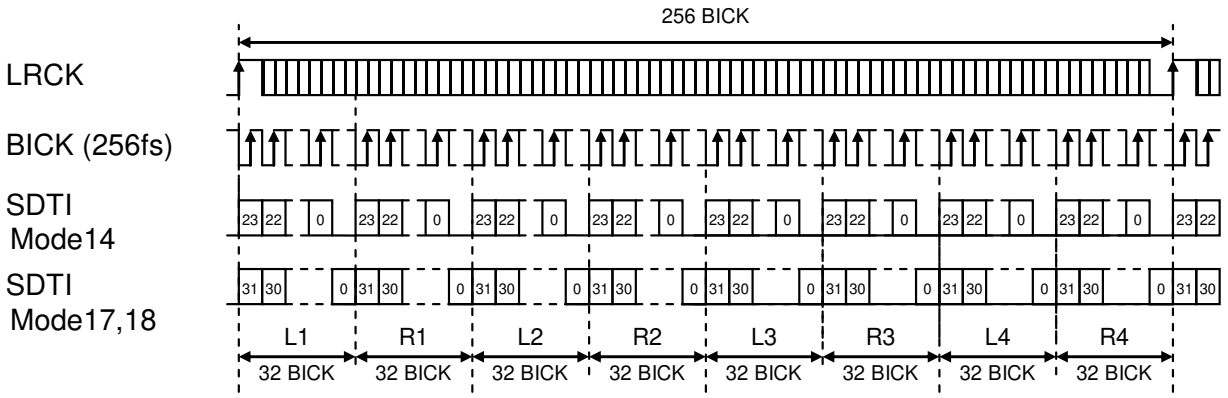


Figure 20. Mode 14/17/18 Timing

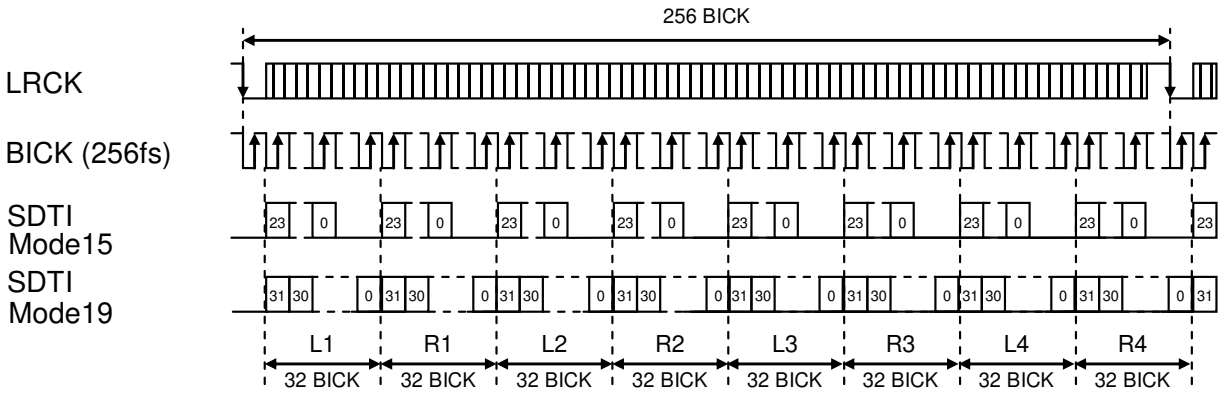


Figure 21. Mode 15/19 Timing

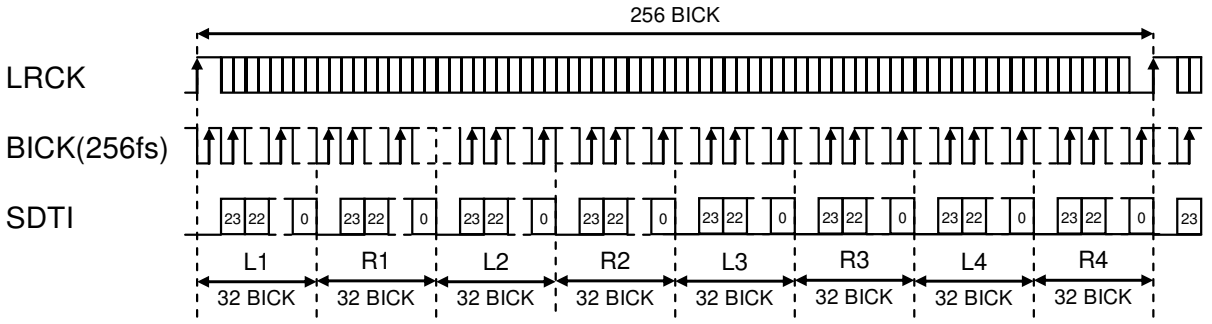


Figure 22. Mode 16 Timing

■ Data Slot and Data Select

Data slots for each input mode are assigned as follows. For TDM128 or TDM256, select the data slot to be played back with SDS1-0 bits.

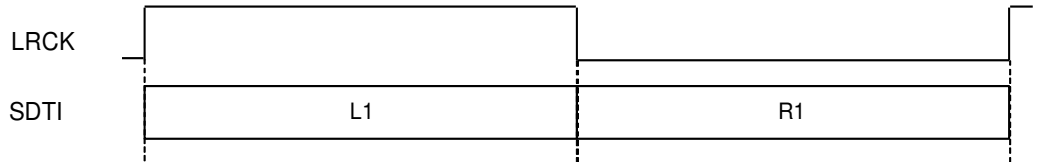


Figure 23. Data Slot in Normal mode

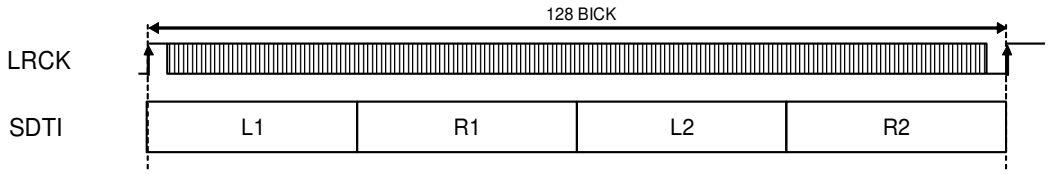


Figure 24. Data Slot in TDM128 mode

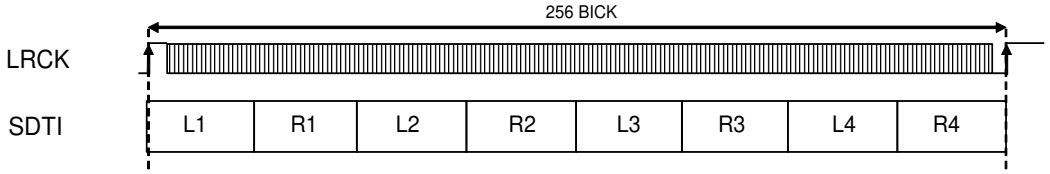


Figure 25. Data Slot in TDM256 mode

Input Mode	SDS1 bit	SDS0 bit	Lch Slot	Rch Slot
Normal	x	x	L1	R1
TDM128	x	0	L1	R1
	x	1	L2	R2
TDM256	0	0	L1	R1
	0	1	L2	R2
	1	0	L3	R3
	1	1	L4	R4

(x: don't care)

Table 8. Data Slot Select

■ Digital Volume Function

The AK4432 has channel-independent digital volume (256 levels, 0.5dB steps). Attenuation level of each channel can be set by ATTL/R7-0 bits, respectively (Table 9).

Lch ATTL7-0 bits	Rch ATTR7-0 bits	Attenuation Level	
00h	00h	+12.0dB	
01h	01h	+11.5dB	
02h	02h	+11.0dB	
:	:	:	
17h	17h	+0.5dB	
18h	18h	0.0dB	(default)
19h	19h	-0.5dB	
:	:	:	
FDh	FDh	-114.5dB	
FEh	FEh	-115.0dB	
FFh	FFh	MUTE (-∞)	

Table 9. Attenuation level of Digital Volume

When ATTL/R7-0 bits are changed, the attenuation level changes by 0.125dB every fixed time and reaches the new attenuation level (soft transition). This suppresses switching noise when changing the attenuation level. The time it takes for the attenuation level to change by 0.125dB can be selected with the ATS bit (Table 10).

Mode	ATS bit	Attenation Transition Speed	Transition Time between 00h and FFh	
0	0	0.125dB per 1/fs	1020/fs	(default)
1	1	0.125dB per 4/fs	4080/fs	

Table 10. Transition time of attenuation level

The transition time from 00h (+12dB) to FFh (MUTE) is 255 × 0.5dB / 0.125dB × 1/fs = 1020/fs in Mode0 and 255 × 0.5dB / 0.125dB × 4/fs = 4080/fs in Mode1.

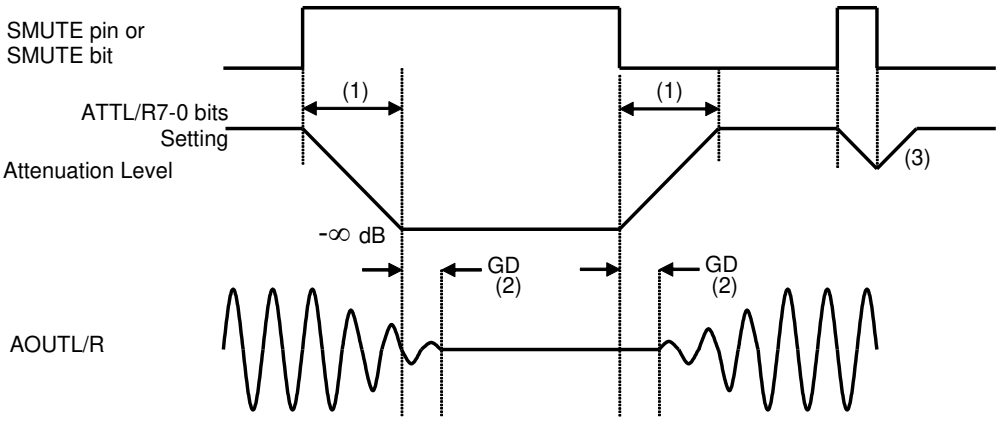
Mode	ATS bit	Transition Time between 00h and FFh				
		1/fs units	fs=48kHz	fs=44.1kHz	fs=8kHz	
0	0	1020/fs	21.3ms	23.1ms	127.5ms	(default)
1	1	4080/fs	85.0ms	92.5ms	510.0ms	

Table 11. Digital Volume Transition Time 00h ⇔ FFh

Just after power up, the digital volume level is at MUTE. The volume changes to the value set by registers in soft transition after releasing the power-down state.

■ Soft Mute Operation

The soft mute operation is performed at digital domain. When the SMUTE pin is set to “H” or the SMUTE bit is set to “1”, the attenuation level softly transitions from the current level to MUTE (-∞ dB). After that, when the SMUTE pin is set to “L” or the SMUTE bit is set to “0”, the attenuation level returns from MUTE to the level set by ATTL/R7-0 bits by soft transition. The transition speed is determined by the ATS bit setting. If the soft mute is cancelled before attenuating to -∞ dB, the attenuation is discontinued and returned to the level set by ATTL/R7-0 bits in the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.



Note:

(1) (255 – ATTL/R7-0 bits setting) × 4 × transition time per 0.125dB.
For example, this time is 1020/fs at ATTL/R7-0 bits = “00h”.

(2) The analog output corresponding to the digital input has group delay (GD).

(3) If the soft mute is cancelled before attenuating –∞ dB, the attenuation is discontinued and returned to the level set by ATTL/R7-0 bits in the same cycle.

Figure 26. Soft Mute Function

■ Error Detection

Three types of error can be detected by the AK4432 (Table 12). The internal LDO will be powered down and register access will be disabled when an error is detected. Once an error is detected, the AK4432 will not return to normal operation automatically even if all error conditions are removed. Reset the AK4432 once by bringing the PDN pin = “L” and start up again. In I^2C mode, errors can be detected by monitoring Acknowledge. If an error occurs, the AK4432 stops sending Acknowledge.

No	Error	Error Condition
1	Internal Reference Voltage Error	Internal reference voltage is not powered up.
2	LDO Over Voltage Detection	LDO voltage > 1.6V (Typ)
3	LDO Over Current Detection	LDO current > 100mA (Typ)

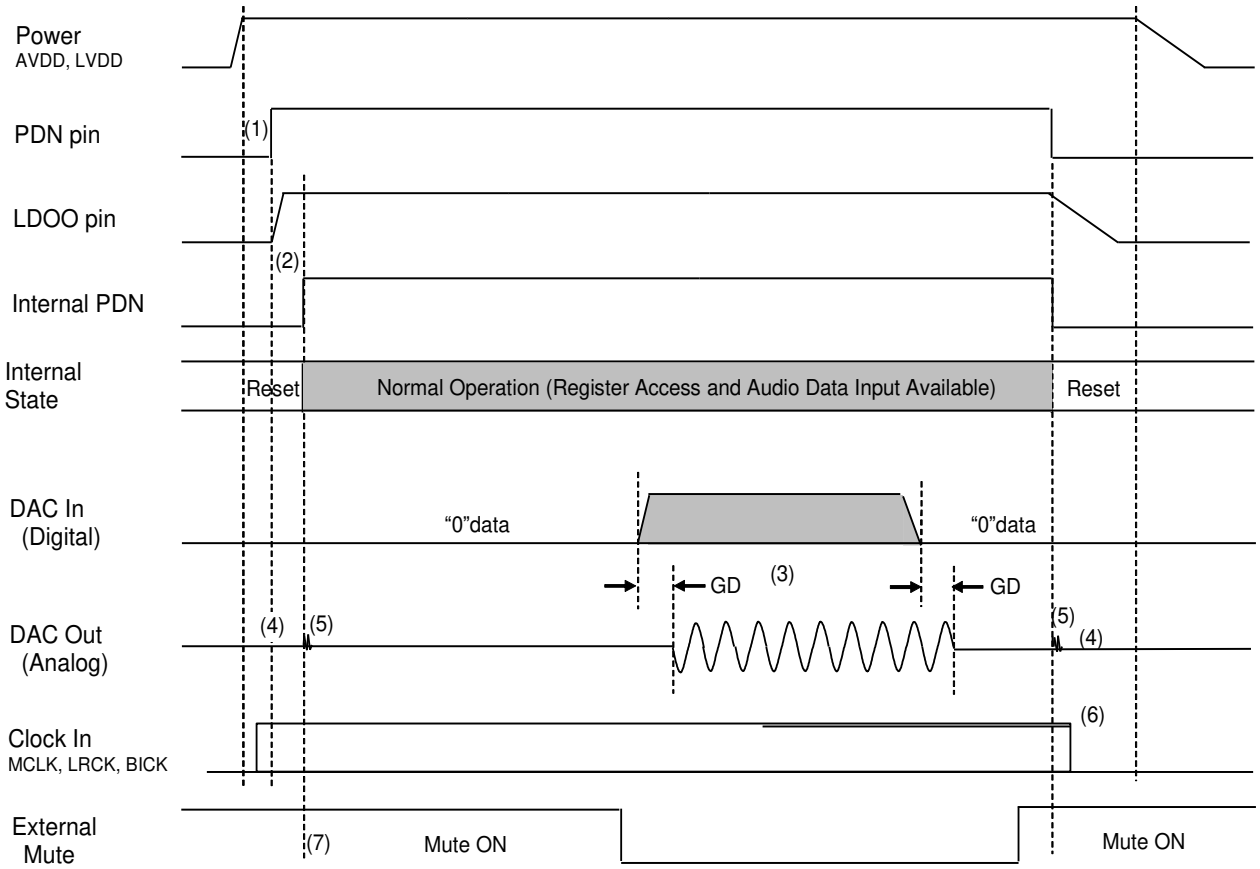
Table 12. ERROR Detection

■ System Reset

The AK4432 should be reset once by bringing the PDN pin = “L” upon power-up. Power-down state of the reference voltage such as LDO and VCOM will be released by the PDN pin = “H”, and then after 1ms register writing becomes available. The internal DAC will be powered up after MCLK and LRCK are input. The AK4432 is in power-down state until MCLK and LRCK are input.

■ Power Down Function

The AK4432 is placed in power-down mode by bringing the PDN pin “L” and the analog outputs become floating (Hi-Z) state. Power-up and power-down timings are shown in Figure 27.



(1) After AVDD and LVDD are powered-up, the PDN pin should be “L” for more than 800ns.
(2) After PDN pin = “H”, the LDO circuit (internal digital block driving power supply) and REF block (analog reference voltage source) are powered up, and control registers are initialized. The Internal PDN (internal power down) is released at maximum 1ms after the PDN pin is set to “H” and normal operation starts. Since the clocks are used to release the internal power down, if the clocks are input after the PDN pin is set to “H”, the internal power down will be released in max.1ms from the start of clock input. Set the control register after releasing the internal power down.
(3) The analog output corresponding to digital input has group delay (GD).
(4) Analog outputs are floating (Hi-Z) in power down mode.
(5) Click noise occurs at an edge of PDN signal. This noise is output even if “0” data is input.
(6) After powering down with the PDN pin = “L”, stop the clock and drop AVDD and LVDD.
(7) Mute the analog output externally if click noise (5) adversely affect system performance. The timing example is shown in this figure.

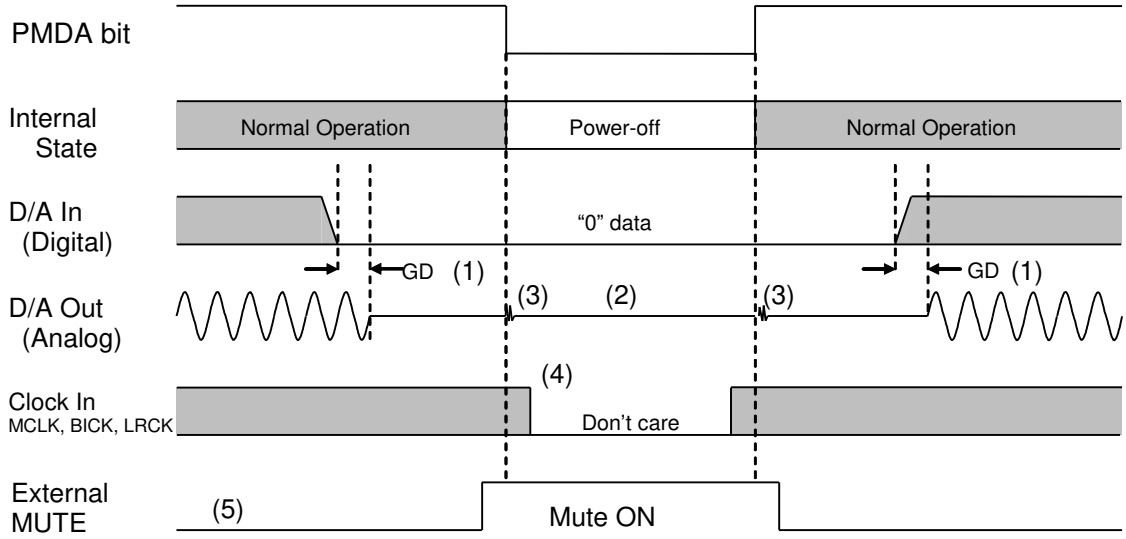
Figure 27. Pin Power Down/Up Sequence Example

■ Power Off Functions

PMDA bit	DAC Block	AOUTL/R pins Output	Digital Circuit	Register Contents	
0	OFF	Hi-Z	OFF	Keep	
1	ON	Normal	ON	Keep	(default)

Table 13. Power OFF Function

When the PMDA bit is set to "0", all internal circuits except registers are powered down immediately. At this time, the analog output becomes floating state (Hi-Z). Figure 28 shows a timing example of power-off and power-on.



Note:

(1) The analog output corresponding to digital input has group delay (GD).
(2) Analog outputs are floating (Hi-Z) in power-off state.
(3) Click noise occurs at the edges ("↑ ↓") of the internal timing of PMDA bit. This noise is output even if "0" data is input.
(4) Each clock input (MCLK, BICK, LRCK) can be stopped in power down mode (PMDA bit = "0").
(5) Mute the analog output externally if the click noise (3) adversely affects system performance.

Figure 28. Power-off/on Sequence Example

■ Clock Synchronization

The AK4432 has a function to adjust the phase difference with the DAC output of the AK7738 within 13/256fs. Clock synchronization function is enabled by SYNCE bit = "1" (default = "1"). SYNCE bit setting must be changed when audio data is all "0" (no audio data input). When SYNCE bit = "1" (default) MSB justified and 32-bit I^{2}S compatible formats are available but LSB justified format is not available.

Synchronization with AK7738

In the use cases shown below (Figure 29), the phase difference of DAC output between the AK7738 and the AK4432 can be kept less than 13/256fs by clock synchronization function. Only BICK=64fs, 32bit MSB justified (DIF2-0 bits = "110b") can be used when synchronizing with the AK7738.

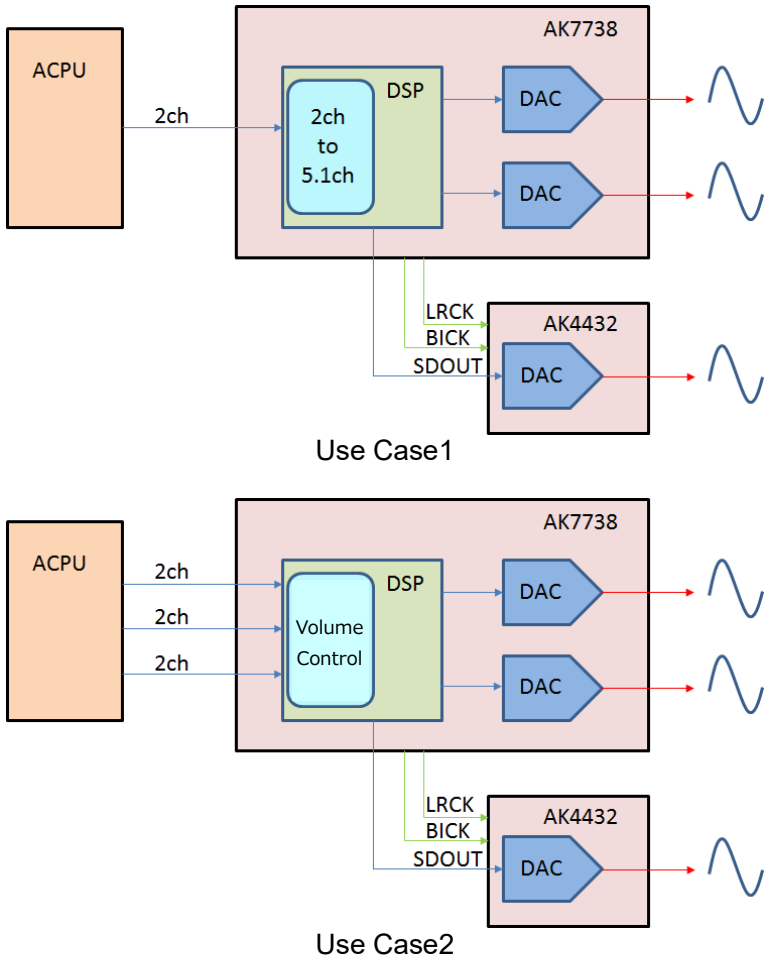


Figure 29. Available Use Cases for Synchronization with the AK7738

Speed Mode	LRCK freq. [kHz]	BICK freq.	MCLK freq.	MCLK freq. [MHz]	Phase Diff. [1/MCLK]	Phase Diff. [μs]	Phase Diff. [deg] (Note 16)
Normal	48	64fs	256fs	12.288	7 ~ 13	0.57 ~ 1.06	4.1 ~ 7.6
Double	96	64fs	256fs	24.576	9 ~ 12	0.37 ~ 0.49	2.6 ~ 3.5
Quad	192	64fs	128fs	24.576	7 ~ 10	0.29 ~ 0.41	2.1 ~ 2.9

Table 14. Phase Difference Relationship between the AK7738 and the AK4432

Note 16. Phase difference to a 20 kHz signal.

■ Parallel Mode

When P/S pin= “H”, AK4432 is in parallel mode. Parallel mode does not require any register settings, and the following three settings can be made with pins. Functions that cannot be set with pins operate with the default setting of the register.

(1) Audio Interface

The DIF pin controls audio interface mode (Table 15). Available modes are 32-bit MSB justified (DIF pin = “L”) and 32-bit I^{2}C compatible (DIF pin = “H”). TDM input mode is not available.

DIF pin	Mode
L	Normal Input, 32-bit Justified (Mode6 in Table 7)
H	Normal Input, 32-bit I^{2}S Compatible (Mode7 in Table 7)

Table 15. Audio Interface Forma (Parallel Mode)

(2) Soft Mute

Soft mute function can be used by the SMUTE pin. (Figure 26)

(3) System Clock

Sampling frequency and MCLK frequency can be selected by ACKS pin. When the ACKS pin is “L”, the sampling frequency is fixed at Normal Speed mode. Double Speed mode and Quad Speed mode can also be used when the ACKS pin is set to “H”. Table 16 shows the MCLK frequencies that can be used for each combination of ACKS pin state and Sampling Speed Mode.

ACKS pin	MCLK	Sampling Speed Mode
L	768fs, 512fs, 384fs, 256fs	Normal Speed Mode
H	512fs, 768fs	Normal Speed Mode
H	256fs, 384fs	Double Speed Mode
H	128fs, 192fs	Quad Speed Mode

Table 16. System Clock (Parallel Mode)

■ Serial Control Interface

The AK4432 corresponds to both 3-wire serial and I²C bus interfaces. After releasing power-down mode, the AK4432 is in I²C interface mode. The 3-wire serial mode will be enabled by writing a dummy command four times continuously following power-up when the CSN pin = “H” (Figure 30) The dummy command is “0xDE, 0xADDA, 0x7A”. The data is MSB first.

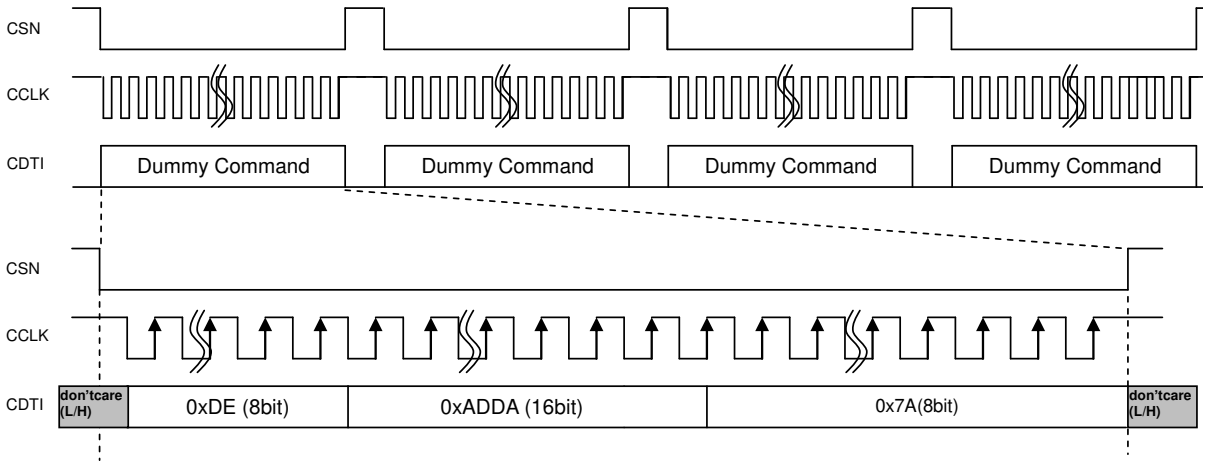


Figure 30. Switch to 3-wire serial mode

(1) 3-wire Serial Control Mode

Write to the register with CSN, CCLK and CDTI pins. CDTI data consists of 8-bit command code, 16-bit register address, and 8-bit control data (Figure 31). Data is MSB first. The most significant bit of the command code is the R/W bit, and only "1" (Write) is valid for the AK4432. The 7 bits following the R/W bit should be "1000000b" (Figure 32). The register address is specified by the lower 3 bits (Figure 33). The AK4432 captures CDTI data at the "↑" of CCLK. Control data is written to the register at the 8th bit CCLK "↑". The frequency of CCLK is up to 7MHz.

Control data can be written continuously (Figure 35). If control data is sent without rising CSN to "H" after sending control data, the register address is automatically incremented and the control data is written to the next address. If control data is sent after writing control data to address 05h, it will be written to address 00h.

The registers are initialized by setting the PDN pin = "L".

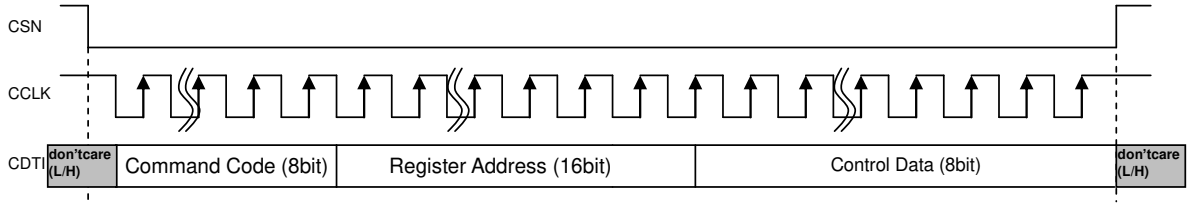


Figure 31. Control I/F Timing

R/W	1	0	0	0	0	0	0

R/W: READ/WRITE (Fixed to "1", Write only)

Figure 32. Command Code

0	0	0	0	0	0	0	0	0	0	0	0	0	A2	A1	A0

Figure 33. Register Address

D7	D6	D5	D4	D3	D2	D1	D0

Figure 34. Control Data

* The AK4432 does not support data read in 3-wire serial mode.
* Control register write is not possible when the PDN pin = "L".
* Cntrol data is not written if CCLK rises 31 times or less during CSN = "L" period.

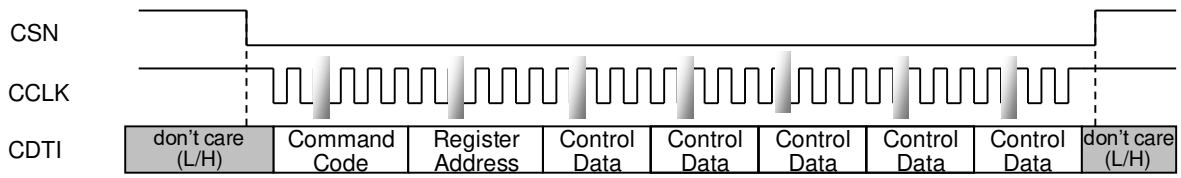


Figure 35. Continuous Write of Control Data

(2) I²C-bus Control Mode

The I²C-bus in the AK4432 can run in fast-mode (max: 400kHz) and fast-mode plus (max: 1MHz) (Table 17). I²C-bus mode should be fixed to either mode during operation. The PDN pin must be “L” when changing the I²C-bus mode.

I2CFIL pin	I²C Bus Mode
L	Fast mode
H	Fast mode Plus

Table 17. I²C-Bus Mode Setting

WRITE Operation

Figure 36 shows the data transfer sequence of the I²C-bus mode. Master begins access to the AK4432 with a START condition. The START condition is to change the SDA line from “H” to “L” while the SCL line is “H” (Figure 44). After the START condition, the master sends the first byte consisting of the 7-bit slave address and data direction bit (R/W) (Figure 37). The slave address of AK4432 is “0011001b”. If the slave addresses match, the AK4432 returns an acknowledge (ACK). The master must send a clock pulse to the SCL line for the AK4432 to return the ACK and release the SDA line (Figure 45). When R/W bit is “0”, data is written to AK4432, and when R/W bit is “1”, data is read from AK4432.

The second byte is an 8-bit command code. The format is MSB first, and it is fixed to “11000000b” (Figure 38).

The third byte and fourth byte consist of the sub address (the control register address of the AK4432). The sub address is 16 bits MSB first, all bits of the third byte are fixed to “0”, and the upper 5 bits of the fourth byte are fixed to “0” (Figure 39, Figure 40). The fifth and subsequent bytes are control data to be written to the register. The control data is 8 bits MSB first (Figure 41). The AK4432 returns an acknowledg every time it completes receiving one byte. Data transfer ends with a stop condition (STOP) generated by the master. The stop condition is to change the SDA line from “L” to “H” while the SCL line is “H” (Figure 44).

The AK4432 can write multiple bytes of control data at once. After sending one byte of control data, if the master sends more control data without sending a stop condition, the data is written to an automatically incremented address. After writing the control data to address “05h”, if further control data is sent, it will be written to address “00h”.

The data on the SDA line must remain stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW (Figure 46) except for the START and STOP conditions.

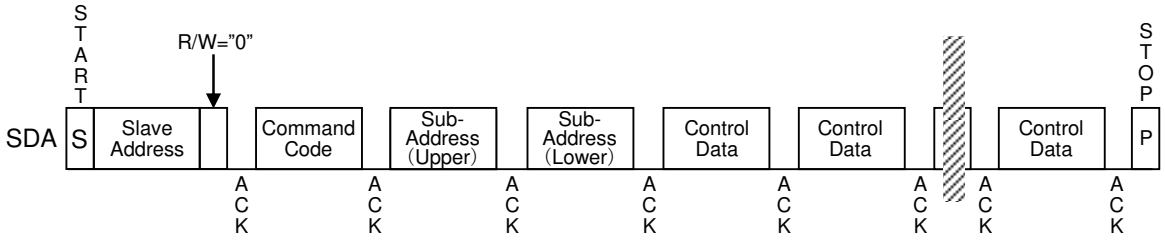


Figure 36. Data Transfer Sequence in I²C-bus Mode

0	0	1	1	0	0	1	R/W

R/W “0”: Write, “1”: Read

Figure 37. The First Byte (Slave Address)

1	1	0	0	0	0	0	0

Figure 38. The Second Byte (Command Code: Write)

0	0	0	0	0	0	0	0

Figure 39. The Third Byte (Sub-Address Upper Byte)

0	0	0	0	0	A2	A1	A0

Figure 40. The Fourth Byte (Sub-Address Lower Byte)

D7	D6	D5	D4	D3	D2	D1	D0

Figure 41. The Fifth and Succeeding Bytes (Control Data)

READ Operation

After the START condition, the master sends the AK4432 slave address and R/W bit = “0” in the first byte, read command code “01000000b” (Figure 43) in the second byte, and register address (sub address) in the third and fourth bytes. Next, when the master sends the AK4432's slave address and R/W bit = “1” after the RESTART condition, the AK4432 outputs the control data of the register specified by the sub address. The AK4432 increments the register address and outputs the control data each time it receives an acknowledg from the master. The read operation ends when the master sends a STOP condition without sending an acknowledg (NACK) after reading the control data. The RESTART condition is the same as the START condition.

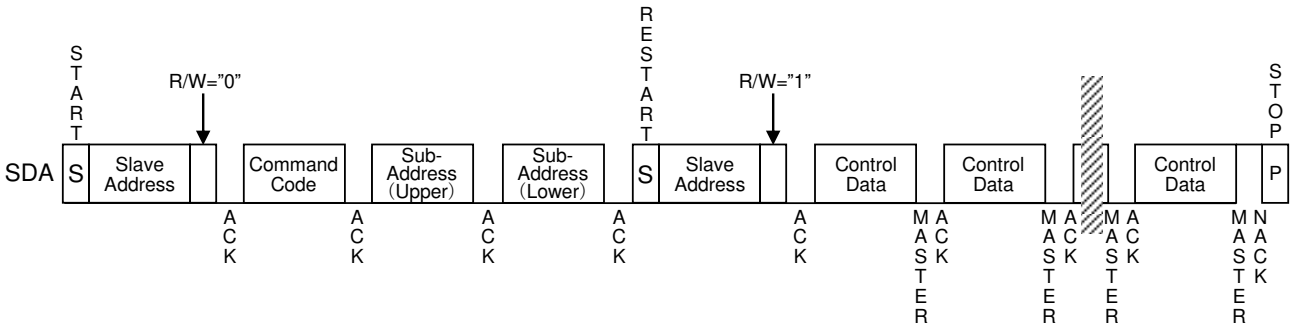


Figure 42. Data read sequence in I²C bus mode

0	1	0	0	0	0	0	0

Figure 43. The Second Byte (Command Code: Read)

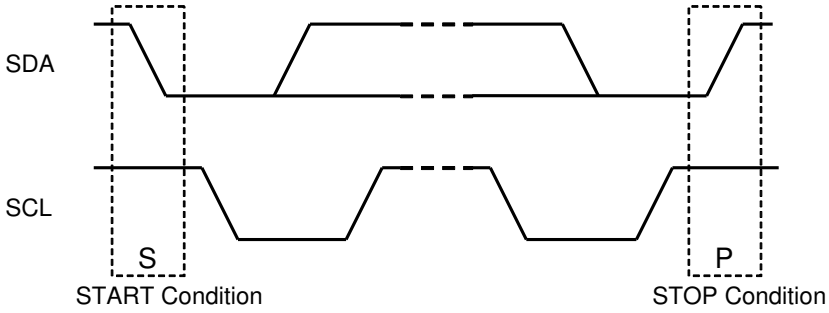


Figure 44. START and STOP Conditions

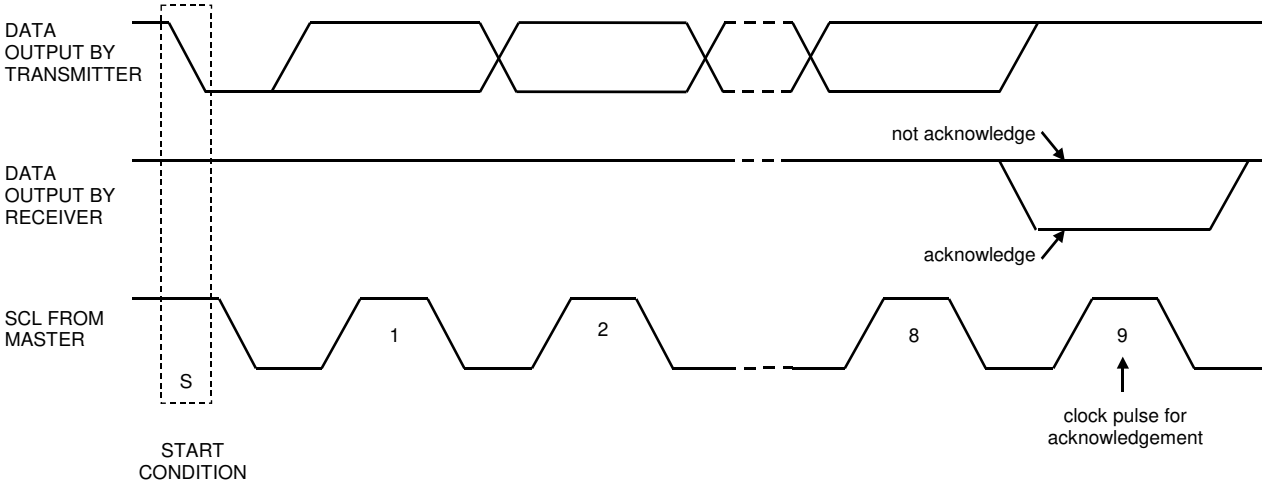


Figure 45. Acknowledge on the I^2C-Bus

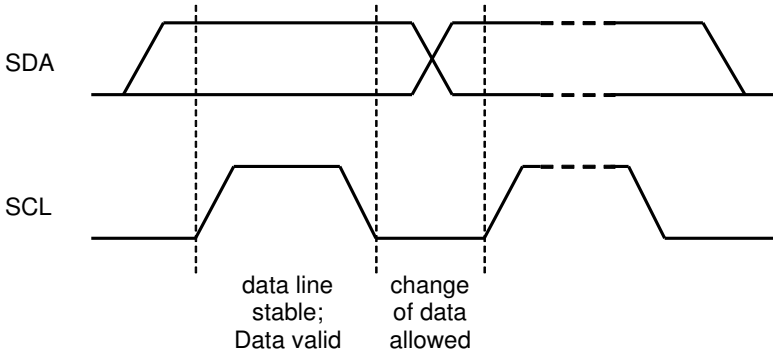


Figure 46. Bit Transfer on the I^2C-Bus

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management	0	0	0	0	0	0	PMDA	0
01H	Control 1	0	0	0	0	0	DFS1	DFS0	ACKS
02H	Data interface	0	SDS1	SDS0	TDM1	TDM0	DIF2	DIF1	DIF0
03H	Control 2	0	0	0	DASL	DASD	ATS	SMUTE	SYNCE
04H	AOUTL Volume Control	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
05H	AOUTR Volume Control	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0

Note 17. Data must not be written into addresses from 06H to FFH.
Note 18. The bit defined as 0 must contain a “0” value.
Note 19. When the PDN pin goes to “L”, the registers are initialized to their default values.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management	0	0	0	0	0	0	PMDA	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	1	0

PMDA DAC Power Management
0: Power Down
1: Normal Operation

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Control 1	0	0	0	0	0	DFS1	DFS0	ACKS
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

ACKS Clock Auto-Recognition Mode Enable
0: Disable (Manual Setting Mode)
1: Enable (Auto Setting Mode)

Sampling speed mode is auto-detected when ACKS = “1”. DFS1-0 bits settings are ignored.
When ACKS = “0”, sampling speed mode is set by DFS1-0 bits.

DFS1-0 Sampling Speed Mode Select (Table 1)

The setting of DFS bits is ignored at ACKS bit =“1”.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Data interface	0	SDS1	SDS0	TDM1	TDM0	DIF2	DIF1	DIF0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	1	1	0

DIF2-0 Audio Interface Mode Select (Table 7)
Default: “110b” (32bit MSB justified)

TDM1-0 TDM Format Select
Default: “00b” (Stereo Mode)

Mode	TDM1	TDM0	Sampling Speed Mode
0	0	0	Stereo mode (Normal, Double, Quad Speed Mode)
1	0	1	TDM128 mode (Normal, Double, Quad Speed Mode)
2	1	0	TDM256 mode (Double, Quad Speed Mode)
3	1	1	TDM256 mode (Double, Quad Speed Mode)

SDS1-0 Data Slot Select in TDM mode (Table 8)
Default: “00b”

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Control 2	0	0	0	DASL	DASD	ATS	SMUTE	SYNCE
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	1

SYNCE Clock Synchronization Enable
0: OFF
1: ON (default)

SMUTE Soft Mute Enable
0: Normal Operation
1: DAC outputs are soft muted

ATS Transition Time Setting of Attenuation Level Select
0: 1/fs (default)
1: 4/fs

DASD Digital Filter Group Delay Select
0: Conventional Delay (default)
1: Short Delay

DASL Digital Filter Roll-Off Select
0: Sharp Roll-Off (default)
1: Slow Roll-Off

DASD bit	DASL bit	Mode	
0	0	Sharp roll-off filter	(default)
0	1	SLow roll-off filter	
1	0	Short Delay Sharp roll-off filter	
1	1	Short Delay Slow roll-off filter	

Table 18 Digital Filter setting for DAC

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	AOUTL Volume Control	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
05H	AOUTR Volume Control	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	1	0	0	0

ATTL7-0: Lch Attenuation Level (Table 9)
Default:18h (0dB)

ATTR7-0: Rch Attenuation Level (Table 9)
Default:18h (0dB)

13. Recommended External Circuits

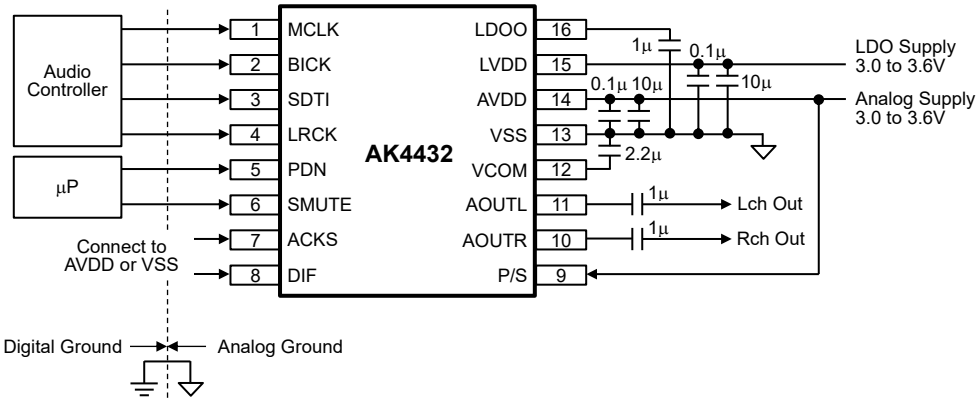


Figure 47. System Connection Diagram (Parallel mode)

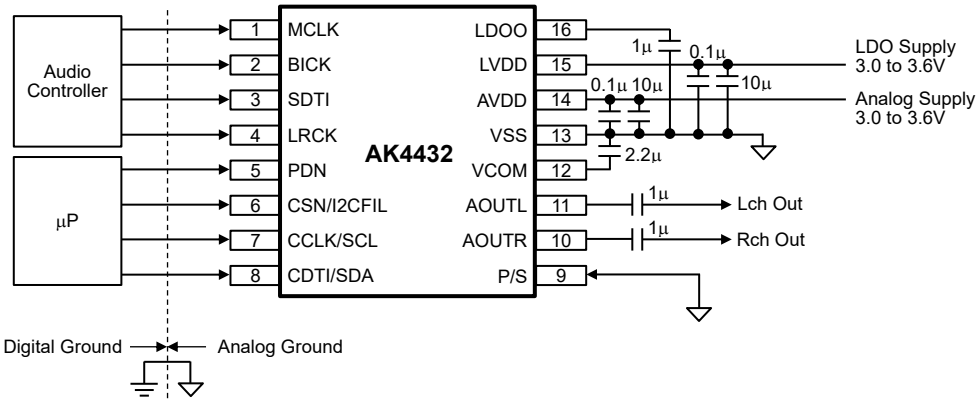


Figure 48. System Connection Diagram (Serial mode)

1. Grounding and Power Supply Decoupling

The AK4432 requires careful attention to power supply and grounding arrangements. **VSS must be connected to the analog ground plane.** Decoupling capacitors should be as near to the AK4432 as possible.

2. Voltage Reference

VCOM is a signal ground of this chip and output the voltage AVDDx1/2. A 2.2μF (±50% includes temperature characteristics) ceramic capacitor attached between the VCOM pin and VSS eliminates the effects of high frequency noise. This capacitor should be as close to the pin as possible. No current can be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK4432.

The LDOO pin is a power supply for internal digital circuit and outputs 1.2V. A 1μF (±50% includes temperature characteristics) ceramic capacitor attached between the LDOO pin and VSS eliminates the effects of high frequency noise. This capacitor should be connected as close as possible to the pin. No current can be drawn from the LDOO pin.

3. Analog Output

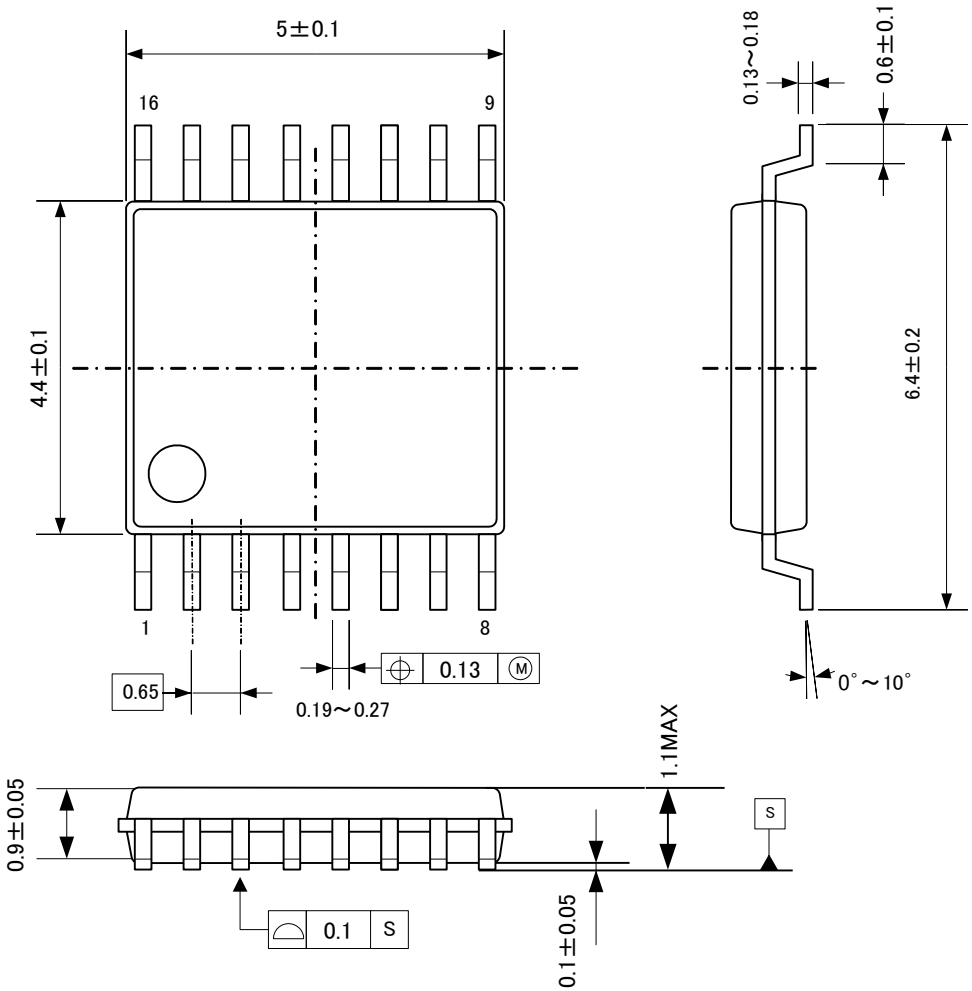
The output signal range is nominally 0.86 x AVDD Vpp (typ.) centered around the VCOM voltage. The DAC input data format is 2's complement. The output voltage is a positive full scale for 7FFFFFFFH(@32bit) and a negative full scale for 80000000H(@32bit). The ideal output is VCOM voltage for 00000000H(@32bit). The internal switched capacitor filter (SCF) and smoothing filter (SMF) remove most of the noise generated by the delta-sigma modulator of DAC beyond the audio passband.

The DAC output has a few mV DC offset with respect to VCOM. The DC offset and VCOM voltage are rejected with an external AC-coupling capacitor.

14. Package

■ Outline Dimensions

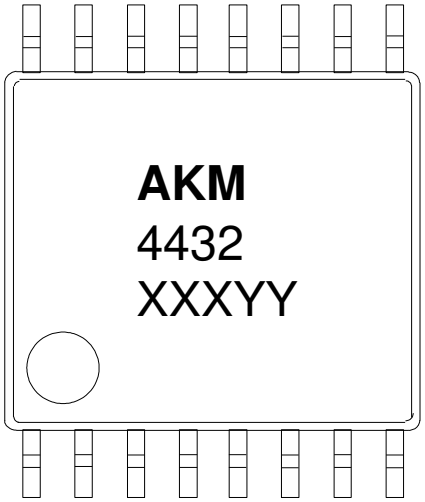
16-pin TSSOP (Unit: mm)



■ Material & Lead Finish

Package molding compound:	Epoxy, Halogen (Br and Cl) free
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

■ **Marking**



1) Pin #1 Index Mark
2) Date Code 5 digits
   XXX: Week Code (Last Digit of the Year 1 digit + Week's Serial# 2 digits)
   YY: Factory Control Code
3) Marking Code: 4432
4) AKM Logo

15. Ordering Guide

AK4432VT	-40 ~ +105°C	16-pin TSSOP (0.65mm pitch)
AKD4432	Evaluation Board for the AK4432	

16. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
15/02/18	00	First Edition	-	-
22/12/20	01	Error Correction	1	Removed from features because it does not have de-emphasis function and zero detection function.
		Description Change	1	2. Sampling Frequency Make the lower frequency the same as the switching specification. Double Speed Mode "64kHz" → "48kHz" Quad Speed Mode "128kHz" → "96kHz"
		Error Correction	6	Pin Funcion of SDA "Caintrol Data Input Pin " → "Control Dara Input/Output Pin"
		Description Change	6	Power down states of digital input pins "-" → "Hi-z" for clarification (Only PDN pin "Input "L"")
		Error Correction	9	Conditions for filter characteristics Removed "DEM=OFF" because it does not have de-emphasis function.
		Error Correction	9	Filter Characteristics Sharp Roll-Off Filter fs=48k, 96kHz Frequency Response max.-0.1dB → max.0.1dB
		Error Correction	11	Filter Characteristics Short Delay Sharp Roll-Off Filter fs=48k, 96kHz Frequency Response max.-0.1dB → max.0.1dB
		Description Change	27	Digital Volume Function Table 10 Simplified to only 0.125dB transition time
		Error Correction	27	Transition time from 00H (+12dB) to FFH (MUTE) Mode0: 255step*4/fs+1/fs=1020/fs → 255 x 0.5 / 0.125 x 1/fs = 1020/fs Mode1: 255step*16/fs+4/fs=4084/fs → 255 x 0.5 / 0.125 x 4/fs = 4080/fs
		Error Correction	27	Digital Volume Function Table 11 Recalculation of transition time based on 1020/fs and 4080/fs
		Description Change	28	Soft Mute Operation Note (1) Write formulas with concrete elements. "ATT_DATA × ATT transition time" →"(255 – ATTL/R7-0 bits setting) × 4 × transition time per 0.125dB"
		Error Correction	28	Soft Mute Operation Note (1) "at ATT_DATA=255 in Normal Speed Mode" → "at ATTL/R7-0 bits = 00h"
		Error Correction	28	Error Detection Table 12 LDO Over Current Detection "< 100mA (Typ)" → "> 100mA (Typ)"
		Description Change	29	Power Down Function Note (1) "the PDN pin should be "L" for 800ns." → "the PDN pin should be "L" for more than 800ns." Clarified that 800ns is a minimum value.
		Error Correction	32	(3) System Clock In the description and the table "MCKI" → "MCLK"

Date (Y/M/D)	Revision	Reason	Page	Contents
22/12/20	01	Error Correction	34	(1) 3-wire Serial Control Mode "if there are 17times or more CCLK rising edges, or 15times or less CCLK rising edges while the CSN pin is "L"." → "if CCLK rises 31 times or less during CSN = "L" period."
		Description Change	39	Register Definitions Address 02H, SDS1-0 bits Only default value and reference table are described according to the description of other registers.
		Description Change	whole	Fixed unclear description
23/3/31	02	Error Correction	43	Marking (In figure) "XXYYY" → "XXXYY" 2) Date Code 4 digits → 5 digits Add characters meaning.
		Description Added	43	Marking Add "4) AKM Logo"

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