

MOSFET

OptiMOS™5 Power-Transistor, 100 V

Features

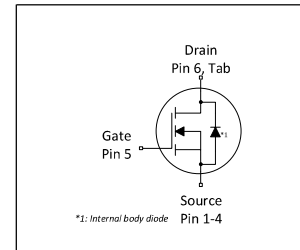
- Optimized for low voltage motor drives application
- Optimized for battery powered applications
- Enables automated optical solder inspection
- 100% avalanche tested
- N-channel
- 175°C rated
- Pb-free lead plating : RoHS compliant

Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on),max}$	2.6	mΩ
I_D	248	A
Q_{oss}	154	nC
$Q_G(0V..10V)$	89	nC



Type / Ordering Code	Package	Marking	Related Links
IST026N10NM5	sTOLL	026N10N5	-

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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	248 175 27	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{THJA}=40\text{ °C/W}^2)$
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	992	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	326	mJ	$I_D=100\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	313 3.8	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{THJA}=40\text{ °C/W}^2)$
Operating and storage temperature	T_j , T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	0.3	0.48	°C/W	-
Device on PCB, 6 cm ² cooling area	R_{thJA}	-	-	40	°C/W	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature at 25°C. For higher case temperature please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.2	-	3.8	V	$V_{DS}=V_{GS}$, $I_D=148\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	5 100	μA	$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	2.1 2.6	2.6 3.5	$\text{m}\Omega$	$V_{GS}=10\text{ V}$, $I_D=100\text{ A}$ $V_{GS}=6\text{ V}$, $I_D=50\text{ A}$
Gate resistance ¹⁾	R_G	-	0.8	-	Ω	-
Transconductance	g_{fs}	140	210	-	S	$ V_{DS} \geq 2 I_D /R_{DS(on)max}$, $I_D=100\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	6300	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}	-	980	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance	C_{rss}	-	43	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	24	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	29	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	43	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Fall time	t_f	-	10	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$

Table 6 Gate charge characteristics²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	30	-	nC	$V_{DD}=50\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	19	-	nC	$V_{DD}=50\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	Q_{gd}	-	18	-	nC	$V_{DD}=50\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	Q_{sw}	-	29	-	nC	$V_{DD}=50\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total ¹⁾	Q_g	-	89	125	nC	$V_{DD}=50\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	4.7	-	V	$V_{DD}=50\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	78	-	nC	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge	Q_{oss}	-	154	-	nC	$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$

¹⁾ Defined by design. Not subject to production test.

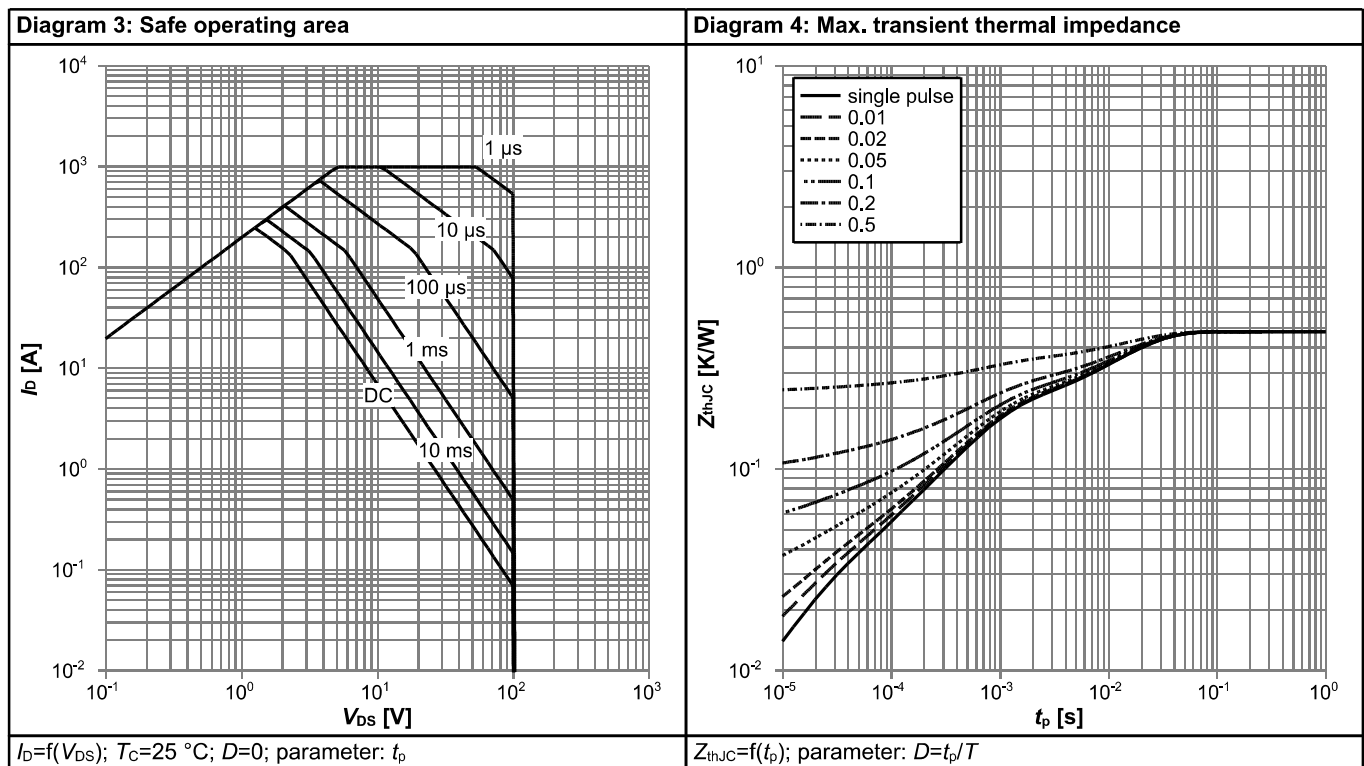
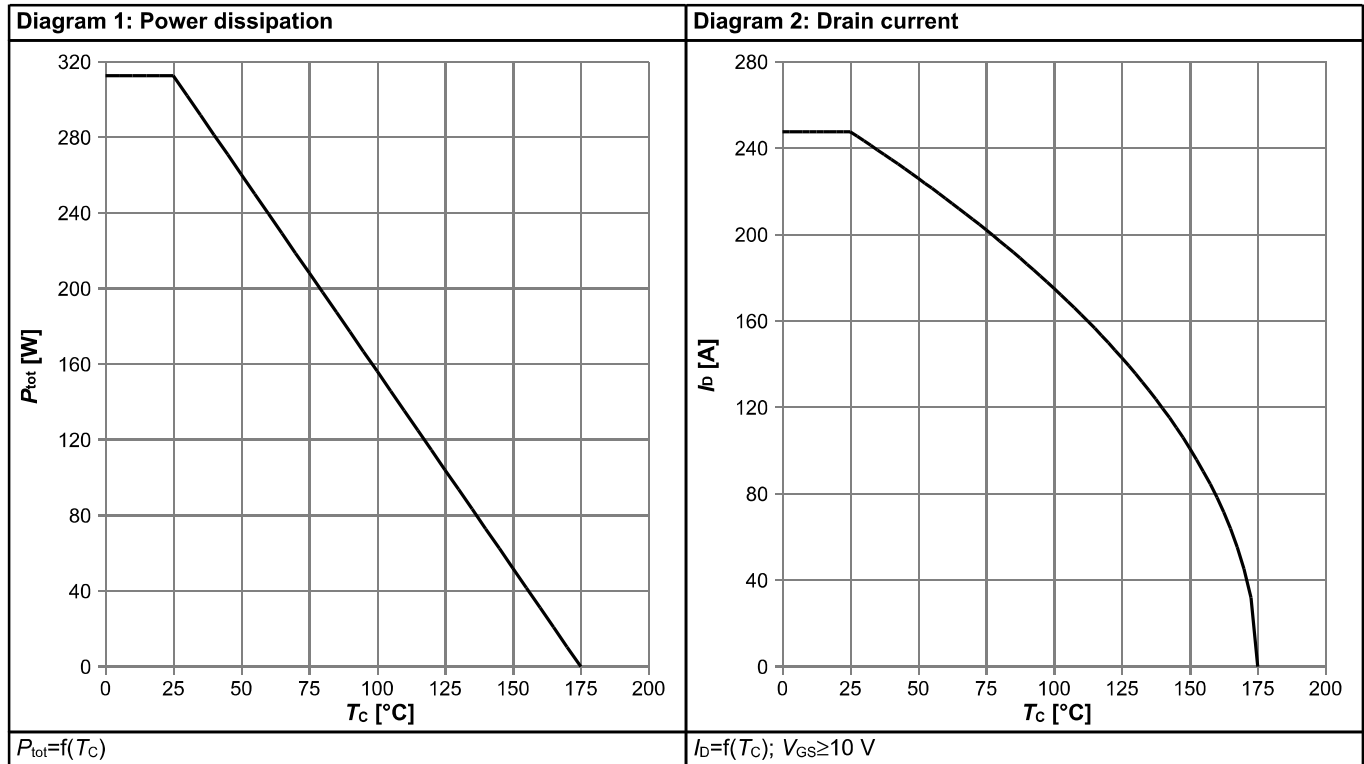
²⁾ See "Gate charge waveforms" for parameter definition

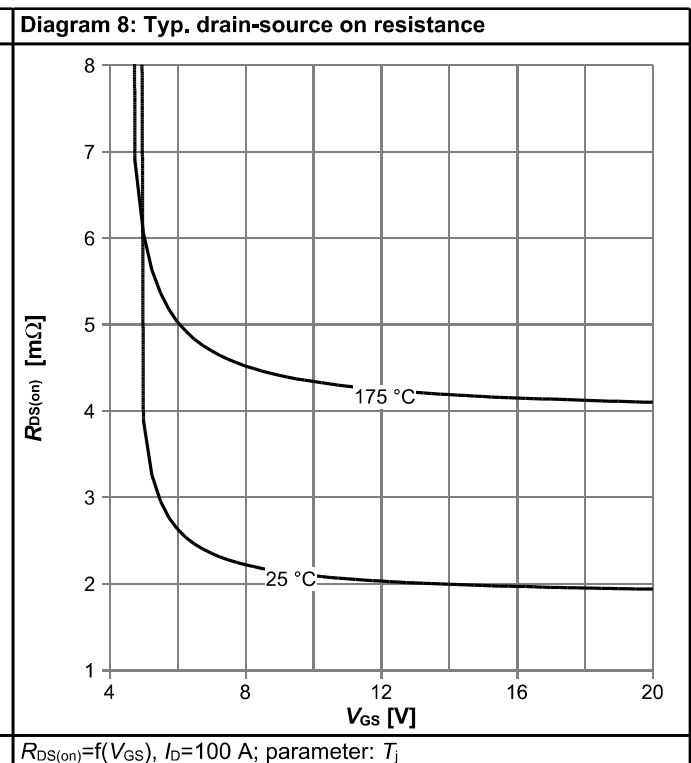
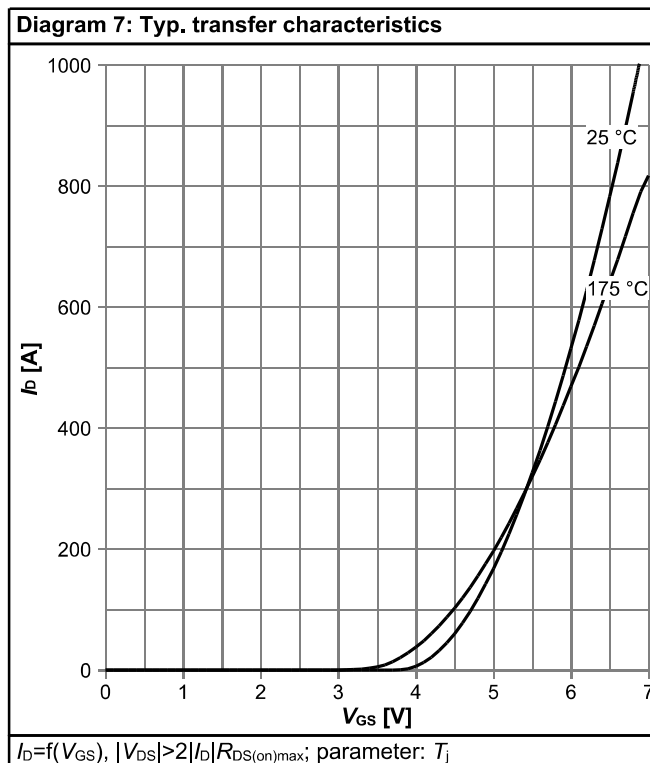
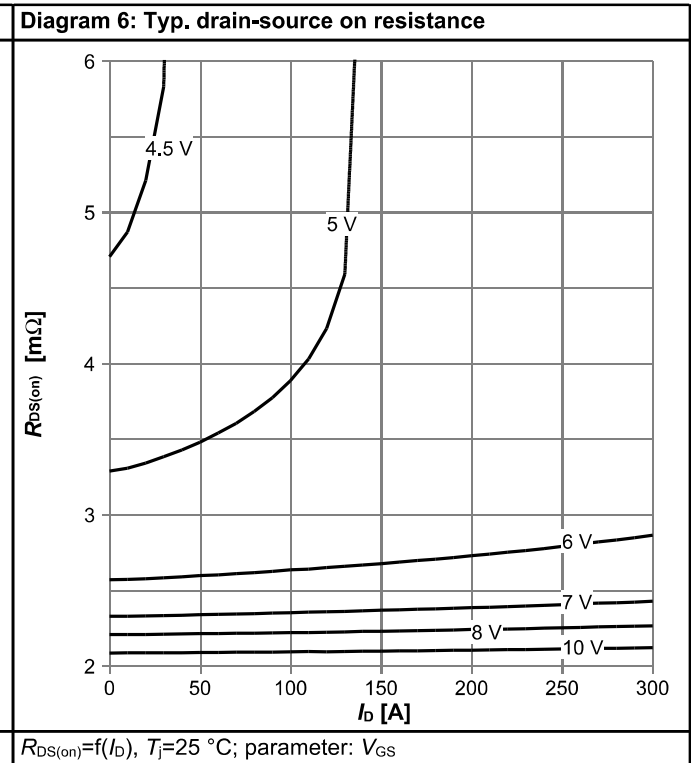
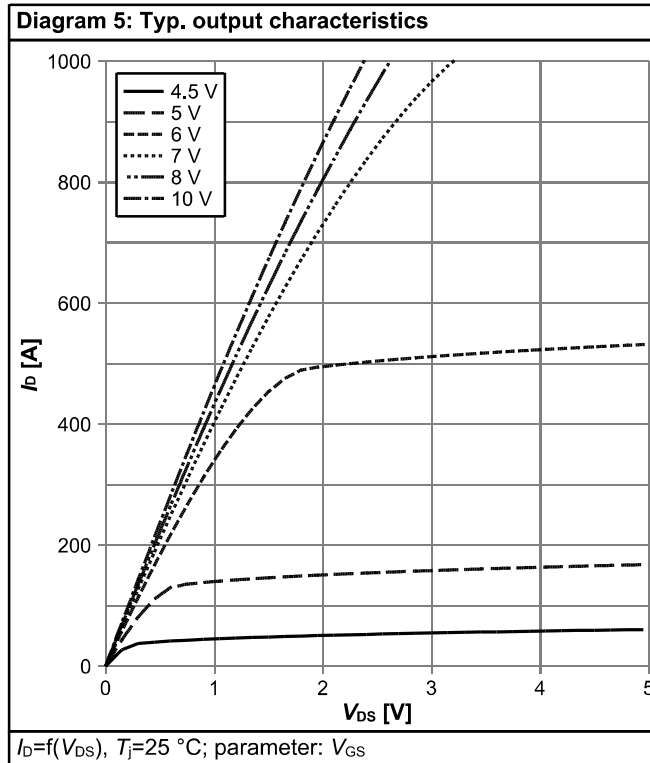
Table 7 Reverse diode

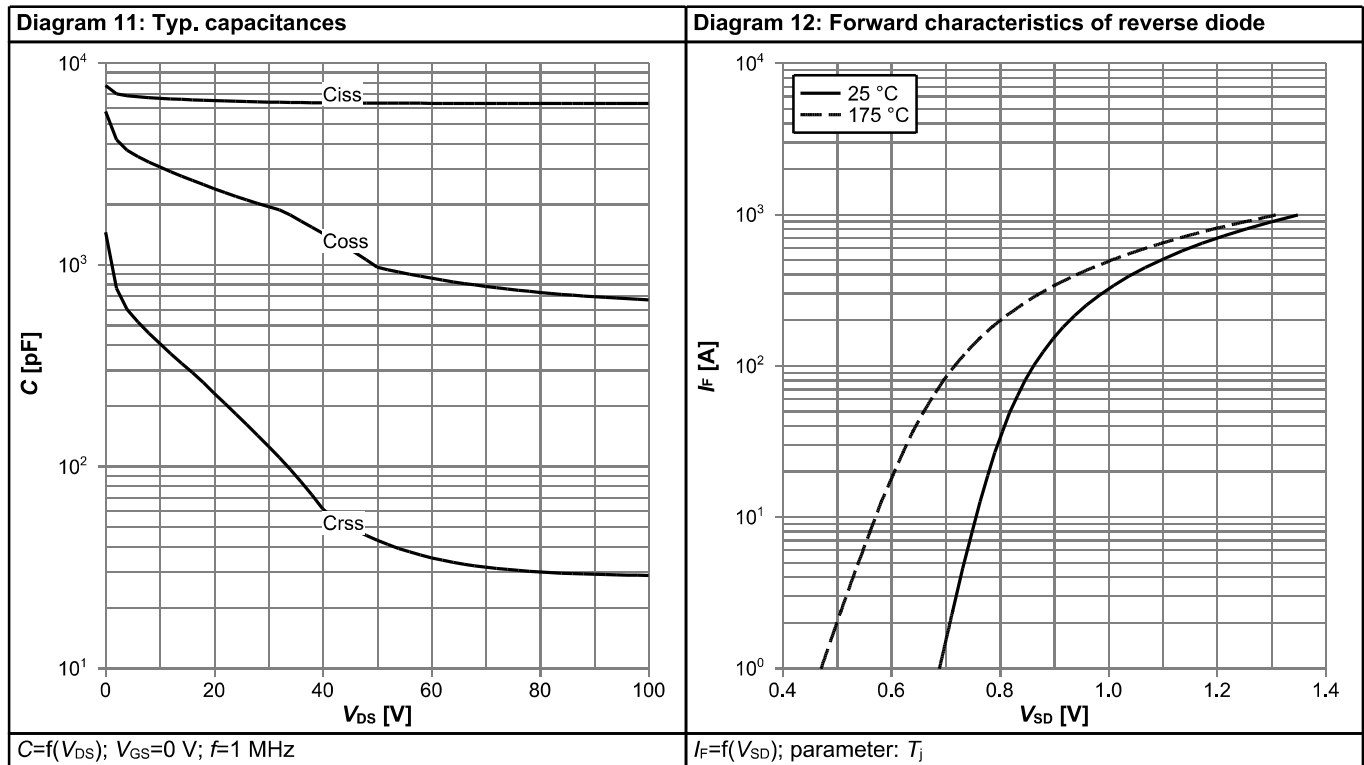
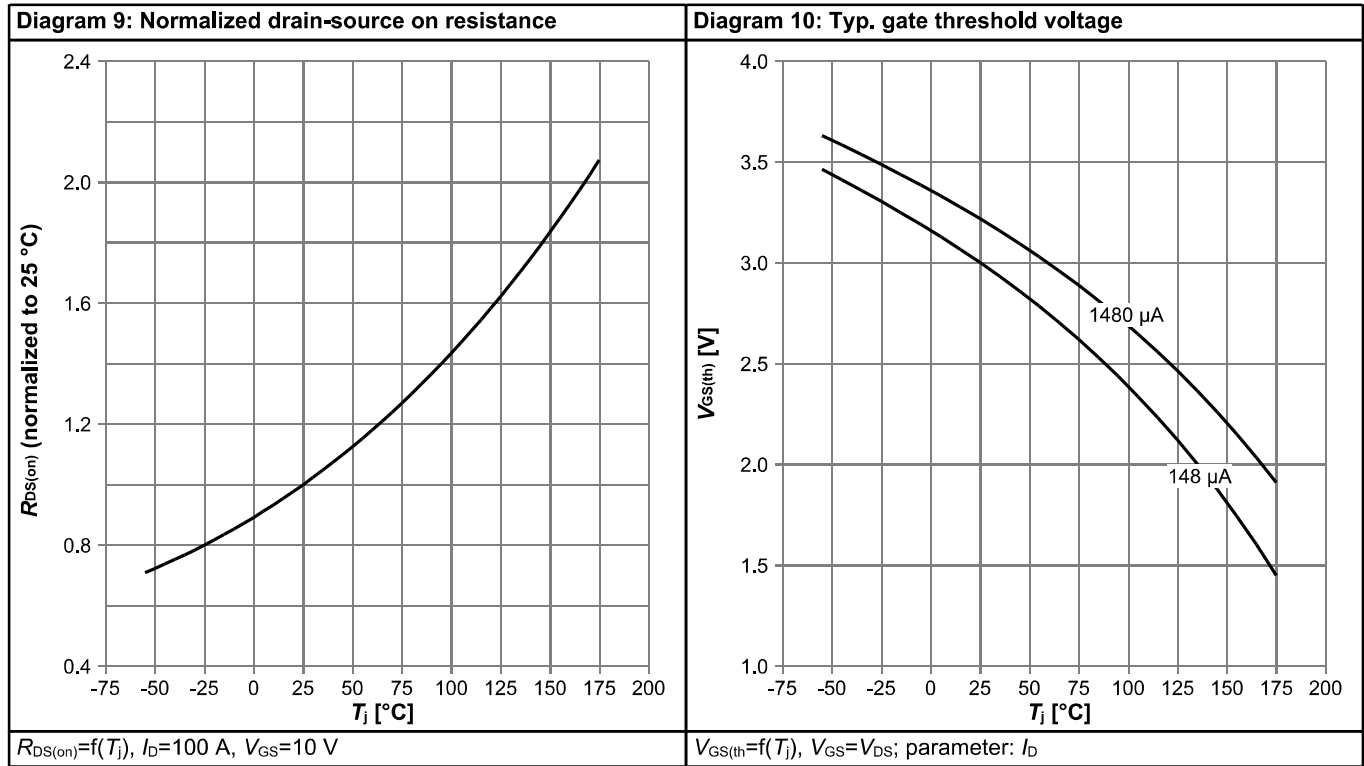
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	245	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	992	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.9	1.1	V	$V_{GS}=0\text{ V}, I_F=100\text{ A}, T_j=25\text{ °C}$
Reverse recovery time ¹⁾	t_{rr}	-	51	-	ns	$V_R=50\text{ V}, I_F=100\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁾	Q_{rr}	-	75	-	nC	$V_R=50\text{ V}, I_F=100\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$

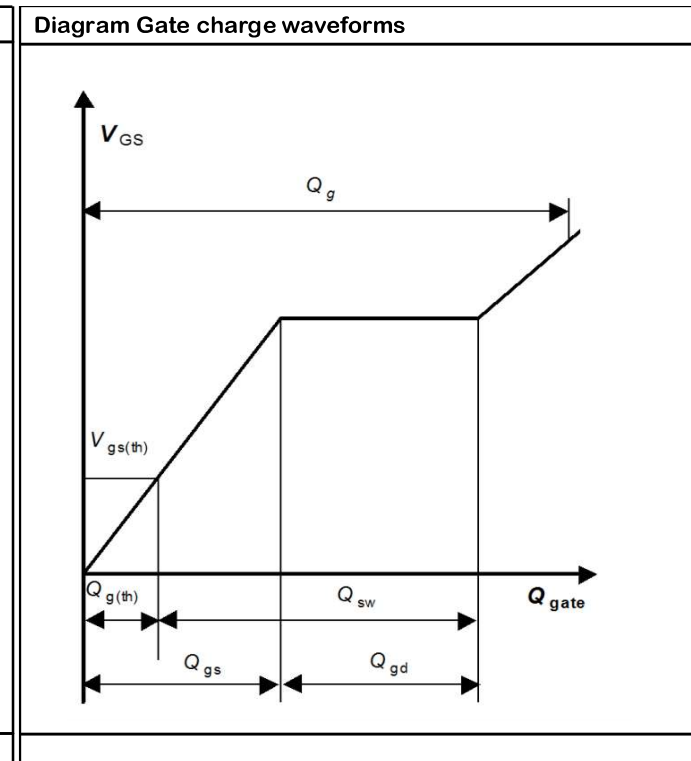
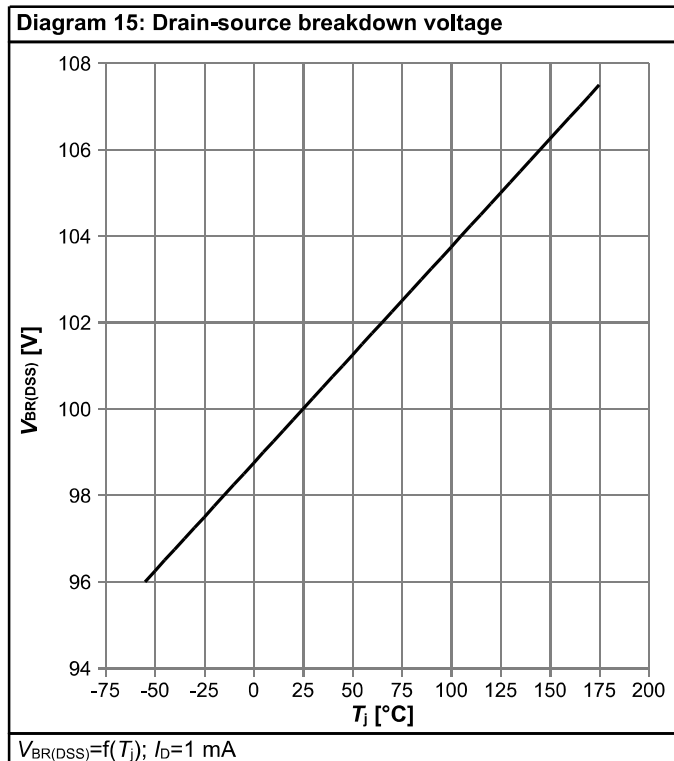
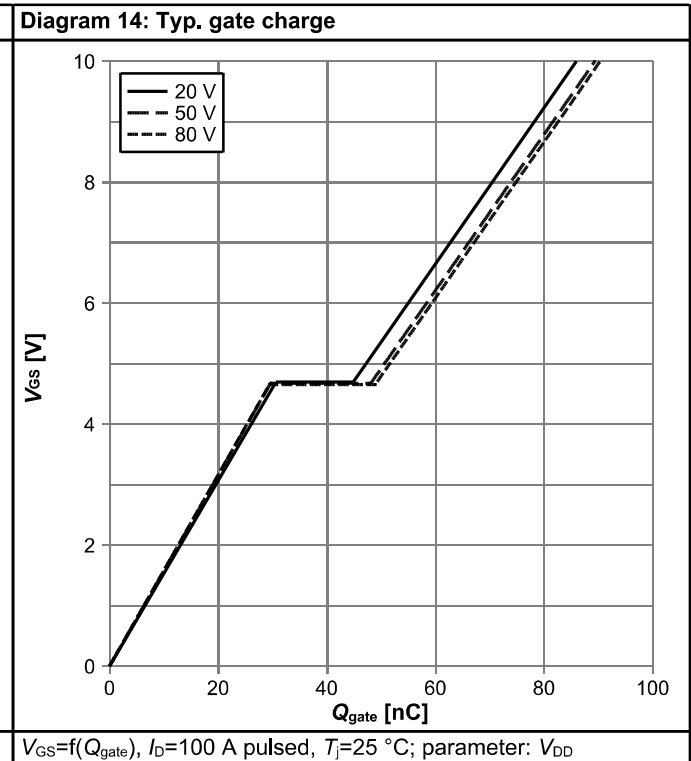
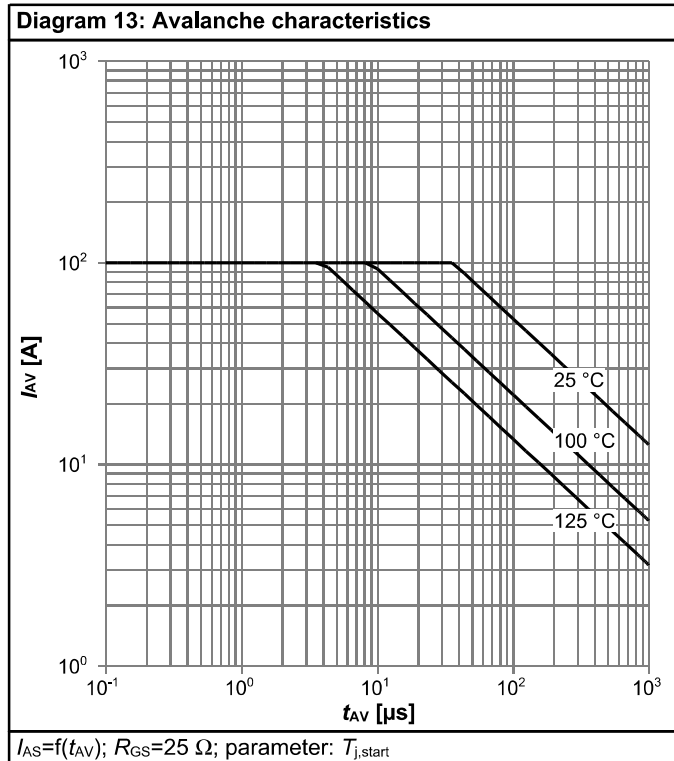
¹⁾ Defined by design. Not subject to production test.

4 Electrical characteristics diagrams

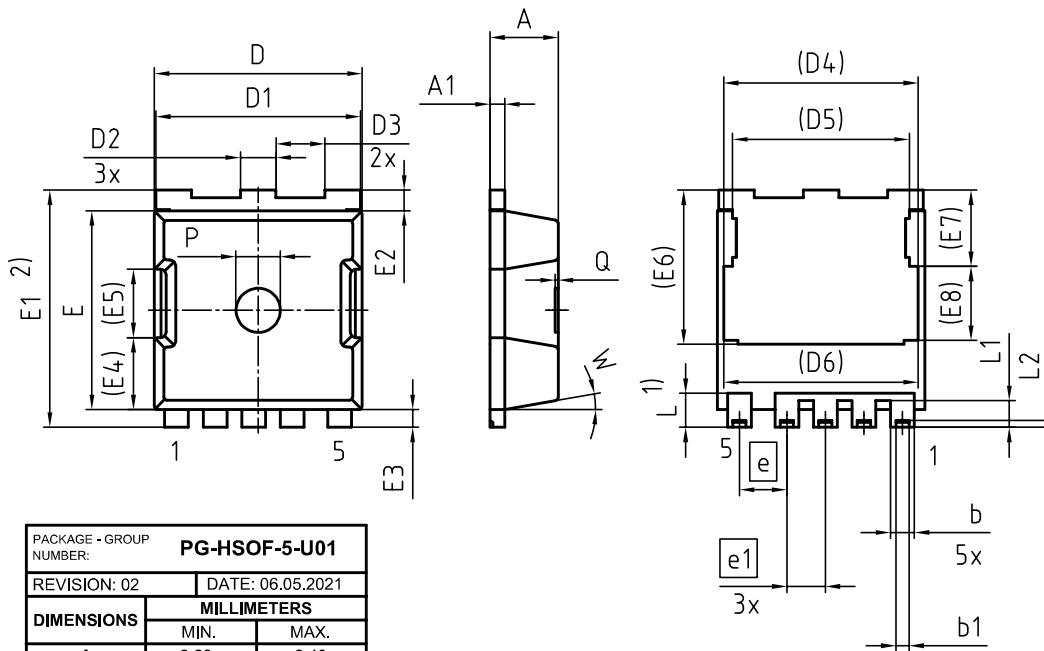








5 Package Outlines



PACKAGE - GROUP NUMBER: PG-HSOF-5-U01		
REVISION: 02		DATE: 06.05.2021
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	2.20	2.40
A1	0.40	0.60
b	0.70	0.90
b1	0.42	0.50
D	6.80	7.20
D1	6.80	7.00
D2	1.10	1.30
D3	1.55	1.75
D4	6.56	
D5	5.96	
D6	5.60	
E	6.50	6.90
E1	7.80	8.20
E2	0.60	0.80
E3	0.50	0.70
E4	2.43	
E5	2.30	
E6	5.20	
E7	2.57	
E8	2.50	
e	1.60	
e1	1.30	
L	1.05	1.25
L1	0.80	1.00
L2	0.13	0.33
P	1.40	1.60
Q	0.00	0.10
W	8.50°	11.50°

- 1) LEAD LENGTH UP TO ANTI FLASH PROFILE, MOLD FLASHES EXCLUDED.
2) EXCLUDING BURR

Figure 1 Outline sTOLL, dimensions in mm

Revision History

IST026N10NM5

Revision: 2022-01-24, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2020-11-20	Release of final version
2.1	2022-01-24	Update Part Marking

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