Integer-N/Fractional-N PLL Synthesizer

Data Sheet

ADF4155

FEATURES

- Input frequency range: 500 MHz to 8000 MHz
- Fractional-N synthesizer and integer-N synthesizer
- Phase frequency detector (PFD) up to 125 MHz
- High resolution 38-bit modulus
- Separate charge pump supply (V_P) allows extended tuning voltage in 5 V systems
- Programmable divide by 1, 2, 4, 8, 16, 32, or 64 output
- Differential and single-ended reference inputs
- Power supply: 3.3 V ± 5%
- Logic compatibility: 1.8 V
- Programmable dual-modulus prescaler (P) of 4/5 or 8/9
- Programmable output power level
- 3-wire serial interface
- Analog and digital lock detect

APPLICATIONS

- Wireless infrastructure (W-CDMA, TD-SCDMA, WiMAX, GSM, PCS, DCS, DECT)
- Point to point/point to multipoint microwave links
- Test equipment
- Wireless LANs, CATV equipment
- Clock generation

GENERAL DESCRIPTION

The ADF4155 allows implementation of fractional-N or integer-N phase-locked loop (PLL) frequency synthesizers when used with an external loop filter, external voltage controlled oscillator (VCO), and external reference frequency.

The ADF4155 is for use with external VCO parts up to an 8 GHz operating frequency. The high resolution programmable modulus allows synthesis of exact frequencies with 0 Hz error.

The VCO frequency can be divided by 1, 2, 4, 8, 16, 32, or 64 to allow the user to generate RF output frequencies as low as 7.8125 MHz.

Control of all on-chip registers is through a simple 3-wire interface. The device operates with a nominal power supply of 3.3 V ± 5% and can be powered down when not in use.

The ADF4155 is available in a 24-lead, 4 mm × 4 mm LFCSP package.

FUNCTIONAL BLOCK DIAGRAM

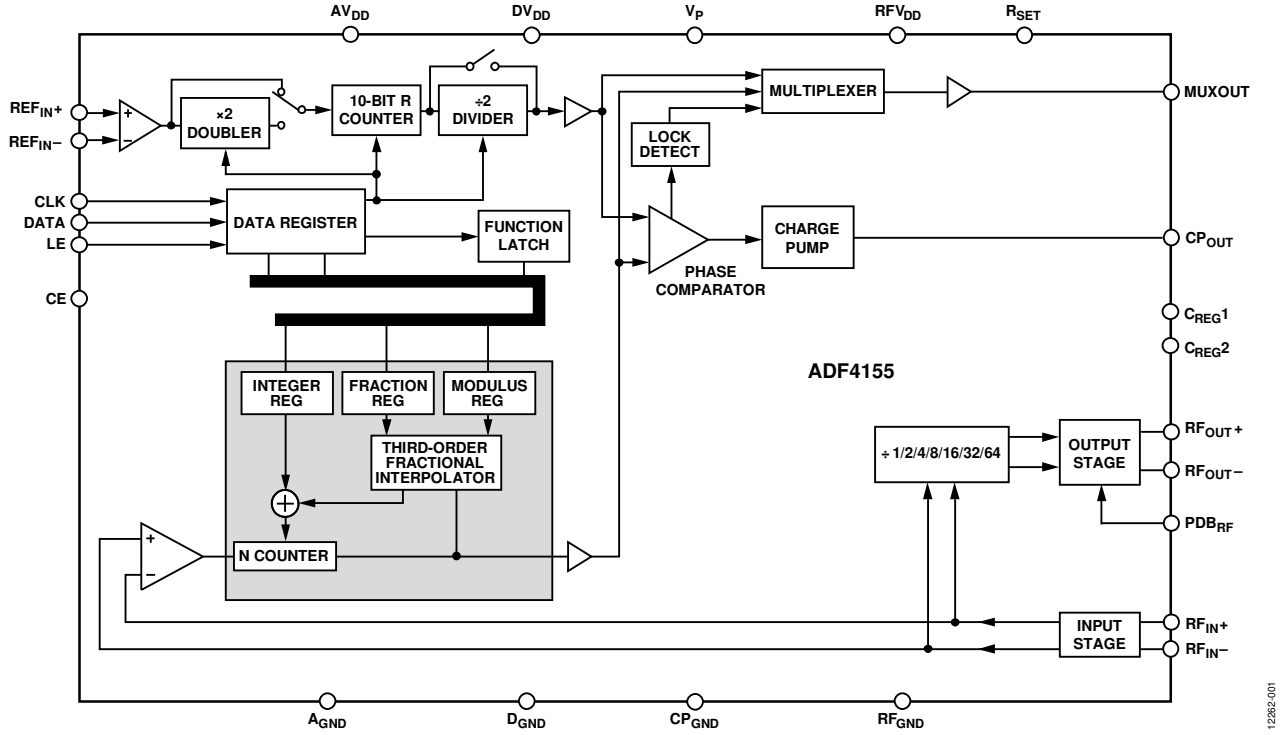

Figure 1.

Rev. 0 Document Feedback

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REVISION HISTORY

4/14—Revision 0: Initial Version

SPECIFICATIONS

AV_{DD} = DV_{DD} = RFV_{DD} = 3.3 V ± 5%, $AV_{DD} \le V_P \le 5.5$ V, A_{GND} = D_{GND} = RF_{GND} = CP_{GND} = 0 V, and T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Operating temperature range is −40°C to +85°C.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REF_{IN}+\REF_{IN}− CHARACTERISTICS					
Input Frequency					For f < 10 MHz, ensure slew rate > 21 V/µs
Single-Ended Mode	10		250	MHz	
Differential Mode	10		600	MHz	
Input Sensitivity					
Single-Ended Mode	0.7		AV_{DD}	V p-p	REF_{IN}+ biased at AV_{DD}/2; ac coupling ensures AV_{DD}/2 bias
Differential Mode	0.4		1.8	V p-p	LVDS and LVPECL compatible, REF_{IN}+\REF_{IN}− biased at 2.1 V; ac coupling ensures 2.1 V bias
Input Capacitance					
Single-Ended Mode		6.9		pF	
Differential Mode		1.4		pF	
Input Current			±60	µA	
PHASE DETECTOR					
Phase Detector Frequency			125	MHz	Negative bleed on
			100	MHz	Pulsed bleed on
			125	MHz	Negative bleed off and pulsed bleed off
			75	MHz	CSR enabled
RF_{IN}+\RF_{IN}− CHARACTERISTICS					For lower frequencies, ensure that the slew rate > 400 V/µs
RF Input Frequency	0.5		6.0	GHz	−10 dBm minimum/0 dBm maximum
			8.0	GHz	−5 dBm minimum/0 dBm maximum
Prescaler Output Frequency			1.5	GHz	
CHARGE PUMP (CP)					
I_{CP} Sink/Source					R_{SET} = 4.7 kΩ
High Value		5		mA	
Low Value		0.31		mA	
R_{SET} Range	2.7	4.7	10	kΩ	
Sink and Source Current Matching		3		%	0.5 V ≤ V_{CP} ≤ V_P − 0.5 V
I_{CP} vs. V_{CP}		3		%	0.5 V ≤ V_{CP} ≤ V_P − 0.5 V
I_{CP} vs. Temperature		1.5		%	V_{CP} = 2.5 V
LOGIC INPUTS					
Input High Voltage, V_{INH}	1.5			V	Compatible with 1.8 V and 3 V logic
Input Low Voltage, V_{INL}			0.6	V	
Input Current, I_{INH}/I_{INL}			±1	µA	
Input Capacitance, C_{IN}		3.0		pF	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	DV_{DD} − 0.4			V	CMOS output selected
Output High Current, I_{OH}			500	µA	
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 500 µA
POWER SUPPLIES					
AV_{DD}	3.135		3.465	V	
DV_{DD}		AV_{DD}		V	Voltage must equal AV_{DD}
RFV_{DD}		AV_{DD}		V	Voltage must equal AV_{DD}
V_P	AV_{DD}		5.5	V	
I_P		4.1		mA	
Output Dividers		6 to 36		mA	Each output divide by 2 consumes 6 mA; see Table 6 for details on the current consumption as a function of the output power and divider

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Total I_{DD} (DI_{DD} + AI_{DD} + RFI_{DD})		38	47	mA	RF output (Bit DB6, Register 6) disabled, 3.6 GHz at VCO output
		105	131	mA	RF_{OUT}+/RF_{OUT}− = 1800 MHz, divide by 2 enabled, 5 dBm
Low Power Sleep Mode		10	22	µA	Hardware powered down using CE
		500	530	µA	Software powered down, serial peripheral interface (SPI) powered up in low power sleep mode
RF_{OUT}+/RF_{OUT}− CHARACTERISTICS					
Maximum Output Frequency			4000	MHz	
Minimum Output Frequency Using Dividers	7.8125			MHz	500 MHz fundamental output and divide by 64 selected
Harmonic Content (Second)		−16		dBc	RF_{OUT}+/RF_{OUT}− = 2.9 GHz, fundamental mode
		−26		dBc	RF_{OUT}+/RF_{OUT}− = 2.9 GHz, divide by 2 enabled
Harmonic Content (Third)		−22		dBc	RF_{OUT}+/RF_{OUT}− = 2.9 GHz, fundamental mode
		−7		dBc	RF_{OUT}+/RF_{OUT}− = 2.9 GHz, divide by 2 enabled
Minimum RF Output Power[1]		−4		dBm	Programmable in 3 dB steps
Maximum RF Output Power[1]		5		dBm	
NOISE CHARACTERISTICS					Negative bleed enabled
Normalized Phase Noise Floor, PN_{SYNTH}[2]					PLL bandwidth = 500 kHz
Integer-N Mode		−223		dBc/Hz	FRAC = 0
Fractional-N-Mode		−218		dBc/Hz	
Normalized 1/f Noise, PN_{1_f}[3]		−116		dBc/Hz	10 kHz offset; normalized to 1 GHz
In-Band Phase Noise[4]		−98		dBc/Hz	10 kHz offset from 5.8 GHz carrier
Spurious Signals due to PFD		−110		dBc/Hz	At 5.8 GHz VCO output, f_{PFD} = 61.44 MHz
Frequency		−112		dBc/Hz	At 5.8 GHz VCO output, f_{PFD} = 30.72 MHz
Level of Signal with RF Mute Enabled		−40		dBm	

[1] Using an external 18 nH pull-up inductor to RFV_{DD} into a 50 Ω load.
[2] The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20 logN (where N is the N counter value) and 10 logf_{PFD}. PN_{SYNTH} = PN_{TOT} − 10 log f_{PFD} − 20 logN.
[3] The PLL phase noise is composed of 1/f (flicker) noise plus the normalized PLL noise floor. The formula for calculating the 1/f noise contribution at an RF frequency (f_{RF}) and at a frequency offset (f) is given by PN = P_{1_f} + 10log(10kHz/f) + 20log(f_{RF}/1 GHz). Both the normalized phase noise floor and flicker noise are modeled in the ADIsimPLL design tool.
[4] f_{REFIN} = 122.88 MHz, f_{PFD} = 61.44 MHz, frequency offset = 10 kHz, VCO frequency = 5.8 GHz, RF_{OUT} = 5.8 GHz, N = 94.40104167, loop bandwidth = 60 kHz, I_{CP} =0. 938 mA, and I_{BLEED} = 60 µA.

TIMING CHARACTERISTICS

AV_{DD} = DV_{DD} = RFV_{DD} = 3.3 V ± 5%, AV_{DD} ≤ V_P ≤ 5.5V, A_{GND} = D_{GND} = RF_{GND} = CP_{GND} = 0 V, 1.8 V and 3 V logic levels used, and T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Limit	Unit	Description
t_1	20	ns min	LE setup time
t_2	10	ns min	DATA to CLK setup time
t_3	10	ns min	DATA to CLK hold time
t_4	25	ns min	CLK high duration
t_5	25	ns min	CLK low duration
t_6	10	ns min	CLK to LE setup time
t_7	20	ns min	LE pulse width

Timing Diagram

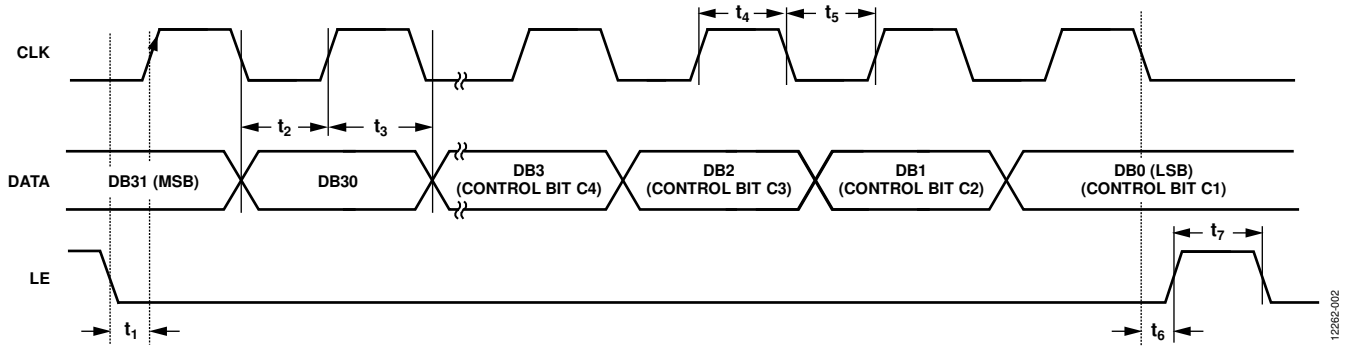


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AV_{DD} to GND[1]	−0.3 V to +3.6 V
AV_{DD} to DV_{DD}	−0.3 V to +0.3 V
RFV_{DD} to AV_{DD}	−0.3 V to +0.3 V
RFV_{DD} to DV_{DD}	−0.3 V to +0.3 V
V_P to GND[1]	−0.3 V to +5.8 V
V_P to AV_{DD}	−0.3 V to +2.5 V
Digital I/O Voltage to GND[1]	−0.3 V to DV_{DD} + 0.3 V
Analog I/O Voltage to GND[1]	−0.3 V to AV_{DD} + 0.3 V
REF_{IN}+, REF_{IN}− to GND[1]	−0.3 V to V_{DD} + 0.3 V
REF_{IN}+ to REF_{IN}−	±2.1 V
RF_{IN}+ to RF_{IN}−	±700 mV
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
LFCSP θ_{JA}, Thermal Impedance (Pad Soldered to GND)	47.3°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec
ESD	
Charged Device Model	1250 V
Human Body Model	4000 V

[1] GND = A_{GND} = D_{GND} = RF_{GND} = CP_{GND} = 0 V.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

TRANSISTOR COUNT

The transistor count for the ADF4155 is 31,190 (CMOS) and 1652 (bipolar).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

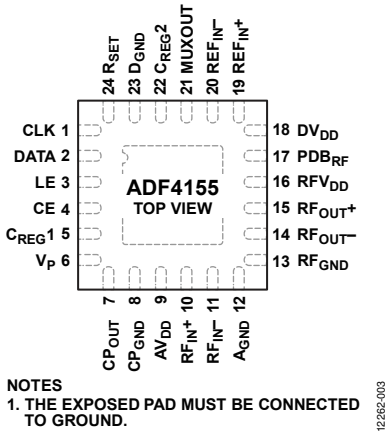


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CLK	Serial Clock Input. Data is clocked into the 32-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
2	DATA	Serial Data Input. The serial data is loaded MSB first with the four LSBs as the control bits. This input is a high impedance CMOS input.
3	LE	Load Enable Input. When LE goes high, the data stored in the shift register is loaded into the register that is selected by the four LSBs. This input is a high impedance CMOS input.
4	CE	Chip Enable. A logic low on this pin powers down the device and puts the charge pump into three-state mode. A logic high on this pin powers up the device, depending on the status of the power-down bits.
5	$C_{REG}1$	Output of Internal Low Dropout (LDO) Regulator. Supply voltage to digital circuits. Nominal voltage of 1.8 V. 100 nF decoupling capacitors to ground required.
6	V_P	Charge Pump Power Supply. V_P must have the same or greater value than AV_{DD} up to 5.5 V. Connect decoupling capacitors, as close to this pin as possible, to the analog ground plane.
7	CP_{OUT}	Charge Pump Output. When enabled, this output provides $\pm I_{CP}$ to the external loop filter. The output of the loop filter is connected to the V_{TUNE} pin of the external VCO.
8	CP_{GND}	Charge Pump Ground. This output is the ground return pin for the CP_{OUT} pin.
9	AV_{DD}	Analog Power Supply. This pin ranges from 3.135 V to 3.465 V. Connect decoupling capacitors, as close to this pin as possible, to the analog ground plane. AV_{DD} must have the same value as DV_{DD} and RFV_{DD}.
10	$RF_{IN}+$	RF Input. This small signal input must be ac-coupled to the external VCO.
11	$RF_{IN}-$	Complementary RF Input. Decouple this pin to the ground plane with a small bypass capacitor, typically 100 pF. If driven differentially, connect this input similar to $RF_{IN}+$.
12	A_{GND}	Analog Ground. Ground return pins for the analog circuitry.
13	RF_{GND}	RF Ground. This output is the ground return pin for the RFV_{DD} pin.
14	$RF_{OUT}-$	Complementary RF Output. The output level is programmable. The VCO fundamental output or a divided-down version is available.
15	$RF_{OUT}+$	RF Output. The output level is programmable. The VCO fundamental output or a divided-down version is available.
16	RFV_{DD}	Analog Power Supply for RF Outputs. This pin ranges from 3.135 V to 3.465 V. Connect decoupling capacitors, as close to this pin as possible, to the analog ground plane. RFV_{DD} must have the same value as AV_{DD} and DV_{DD}.
17	PDB_{RF}	RF Power-Down. A logic low on this pin mutes the RF outputs. This function is also software controllable.
18	DV_{DD}	Digital Power Supply. This pin must be at the same voltage as AV_{DD} and RFV_{DD}. Connect decoupling capacitors, as close to this pin as possible, to the ground plane.
19	$REF_{IN}+$	Reference Input.
20	$REF_{IN}-$	Complementary Reference Input.
21	MUXOUT	Multiplexer Output. The multiplexer output allows the lock detect, the scaled RF, or the scaled reference frequency to be externally accessed.

Pin No.	Mnemonic	Description
22	$C_{REG}2$	Output of Internal LDO. Supply voltage to digital circuits. Nominal voltage of 1.8 V. 100 nF decoupling capacitors to ground required.
23	D_{GND}	Digital Ground. Ground return pins for the digital circuitry.
24	R_{SET}	Connect a resistor between this pin and ground to set the charge pump output current. The nominal voltage bias at the R_{SET} pin is 0.55 V. The relationship between I_{CP_MAX} and R_{SET} is as follows: $I_{CP\_MAX} = 23.5/R_{SET}$ where: R_{SET} = 4.7 kΩ. I_{CP} = 5 mA.
	EPAD	Exposed Pad. The exposed pad must be connected to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

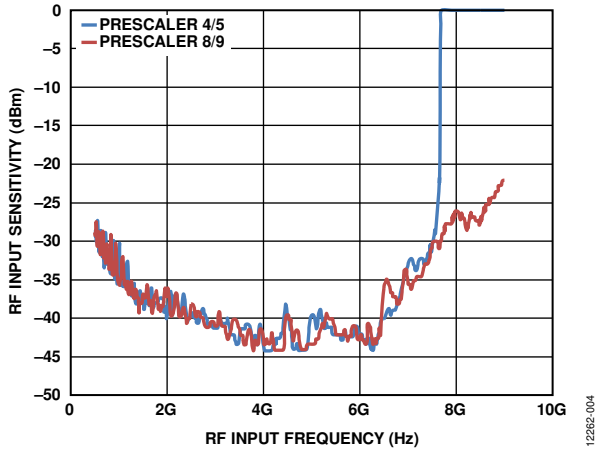


Figure 4. RF Input Sensitivity vs. RF Input Frequency, RF Output Disabled

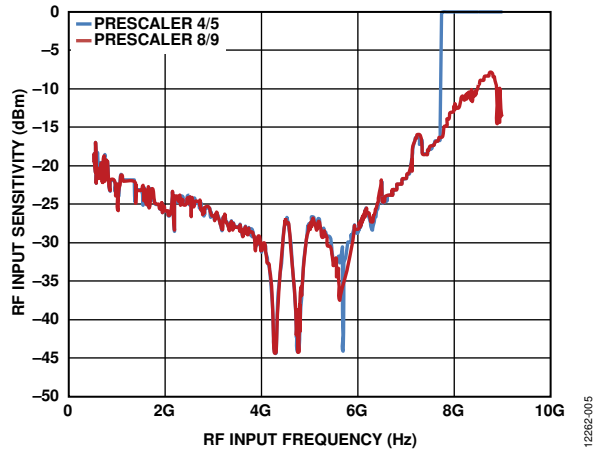


Figure 5. RF Input Sensitivity vs. RF Input Frequency, RF Output Enabled, RF Divide-by-2 Selected

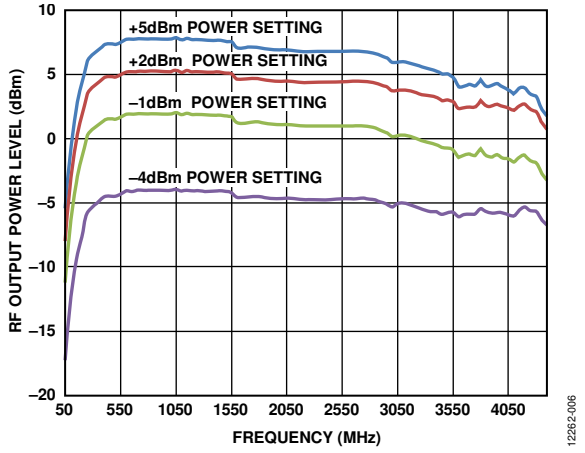


Figure .6. Single-Ended RF Output Power Level vs. Frequency and Power Setting, RF Output Pins Pulled Up to 3.3 V via 18 nH Inductors

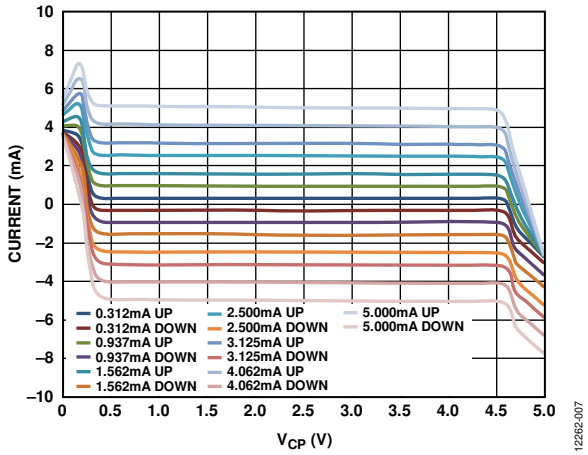


Figure 7. Charge Pump Output Characteristics, V_P = 5 V, Selected I_{CP} Values Between 0.312 mA (Minimum) and 5.000 mA (Maximum), R_{SET} = 4.7 kΩ

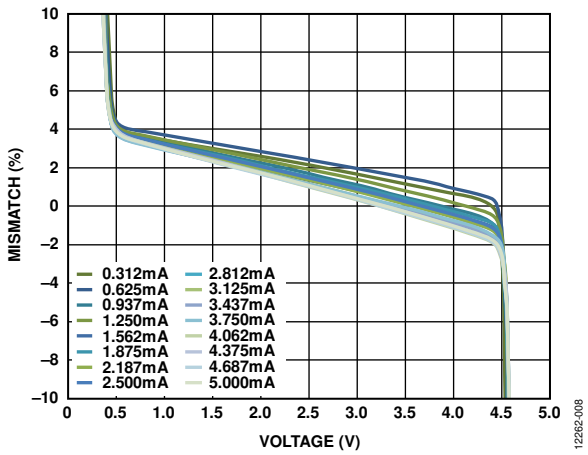


Figure 8. Charge Pump Output Mismatch vs. V_{CP}, Selected I_{CP} Values Between 0.312 mA (Minimum) and 5.000 mA (Maximum), R_{SET} = 4.7 kΩ

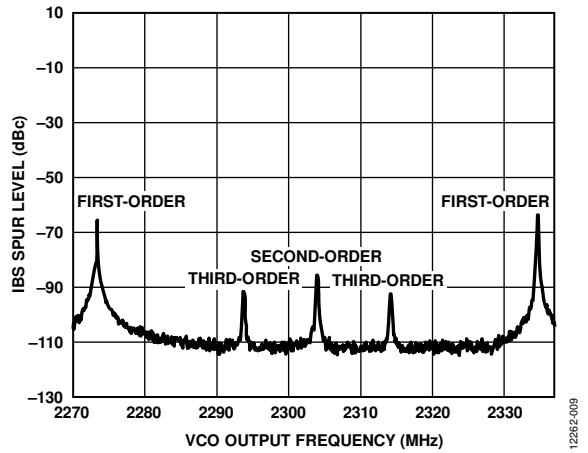


Figure 9. Integer Boundary Spurs (IBS) Spur Level vs. VCO Output Frequency, f_{PFD} = 61.44 MHz, Sweep Resolution = 80 kHz

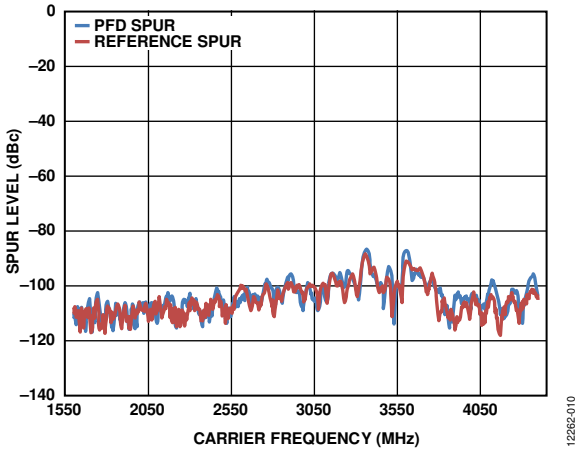


Figure 10. PFD and Reference Spur Level vs. Carrier Frequency Measured at VCO Output, f_{PFD} = 61.44 MHz, REF_{IN}+/REF_{IN}− = 122.88 MHz

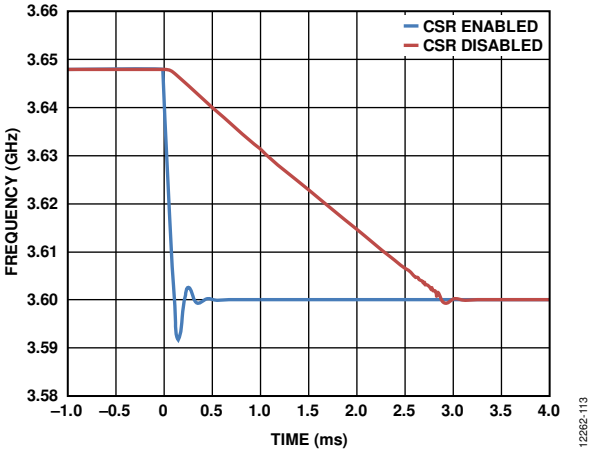


Figure 13. PLL Lock Time with Cycle Sleep Reduction (CSR) On/Off, Locking over 50 MHz Range (Jump from 3.648 GHz to 3.6 GHz), f_{PFD} = 61.44 MHz, Loop Bandwidth = 15 kHz, I_{CP} = 0.31 mA

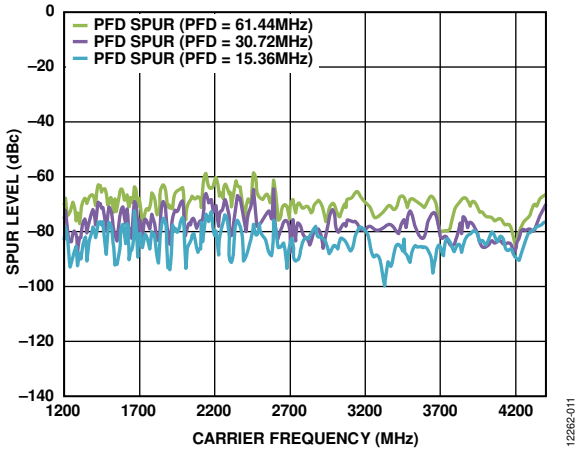


Figure 11. PFD Spur Level vs. Carrier Frequency Measured at RF Output, REF_{IN}+/REF_{IN}− = 122.88 MHz (Note the improvement in the PFD spurs when the PFD frequency is lower.)

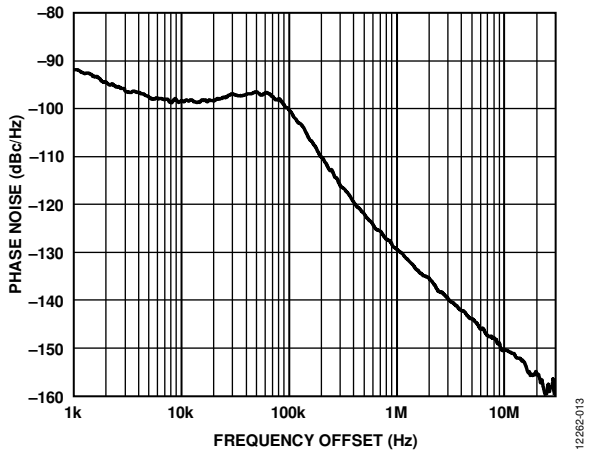


Figure 14. Integer-N Phase Noise and Spur Performance; VCO_{OUT} = 5775.36 MHz, REF_{IN}+/REF_{IN}− = 122.88 MHz, f_{PFD} = 61.44 MHz, Loop Filter Bandwidth= 60 kHz

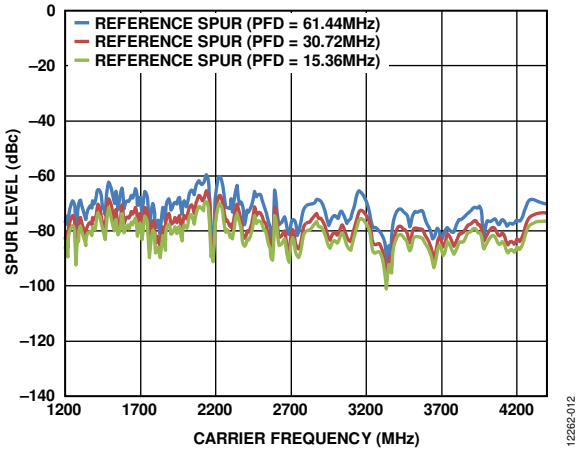


Figure 12. Reference Spur Level vs. Carrier Frequency Measured at RF Output, REF_{IN}+/REF_{IN}− = 122.88 MHz (Note the improvement in the PFD spurs when the PFD frequency is lowered.)

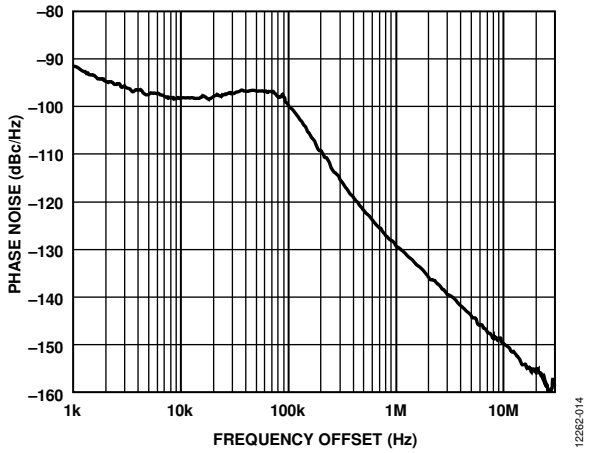


Figure 15. Fractional-N Phase Noise and Spur Performance, VCO_{OUT} = 5800 MHz, REF_{IN}+/REF_{IN}− = 122.88 MHz, f_{PFD} = 61.44 MHz, Loop Filter Bandwidth = 60 kHz

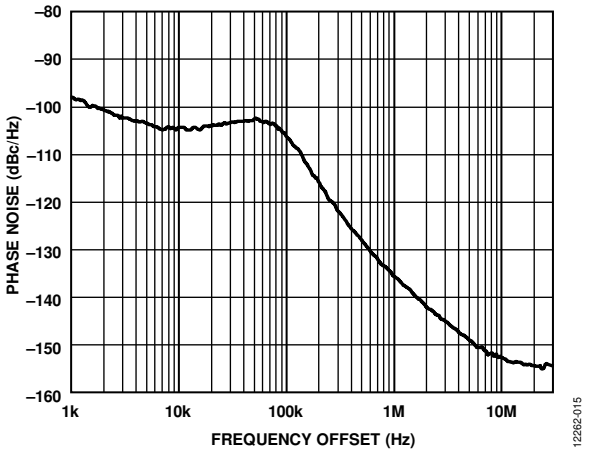


Figure 16. RF Output Phase Noise, RF Divider = 2 Enabled, Fractional-N, RF_{OUT}+ = 2900 MHz, REF_{IN}+/REF_{IN}− = 122.88 MHz, f_{PFD} = 61.44 MHz, Loop Filter Bandwidth = 60 kHz

CIRCUIT DESCRIPTION

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 17. The reference input can accept both single-ended and differential signals, and the choice is controlled by the reference input mode bit (Bit DB30, Register 6). To use a differential signal for the reference input, this bit must be programmed high. In this case, the SW1 and SW2 switches are opened, the SW3 and SW4 switches are closed, and the current source driving the differential pair of the transistors is switched on. The differential signal is buffered, before it is fed to the emitter-coupled logic (ECL) to a CMOS converter. When a single-ended signal is used as the reference, Bit DB30 in Register 6 must be programmed to 0. In this case, the SW1 and SW2 switches are closed, the SW3 and SW4 switches are opened, and the current source driving the differential pair of transistors is switched off.

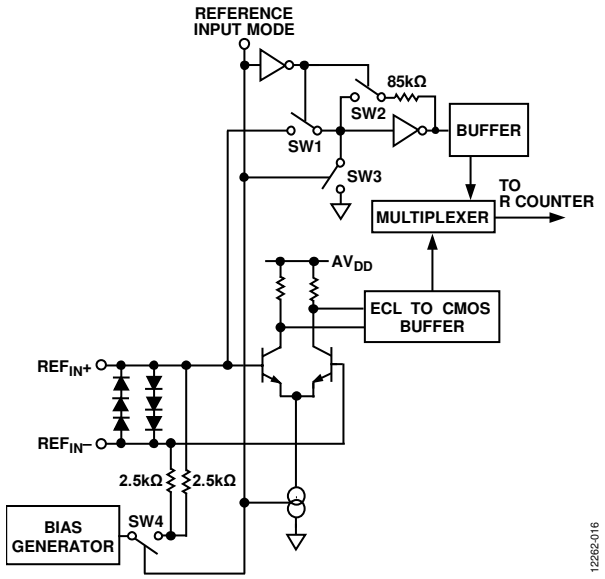


Figure 17. Reference Input Stage

RF N COUNTER

The RF N counter allows a division ratio in the PLL feedback path. The division ratio is determined by the INT, FRAC1, MOD1, FRAC2, and MOD2 values, which build up this divider (see Figure 18). Note that MOD1 is a fixed nonprogrammable value equal to 2^{24}.

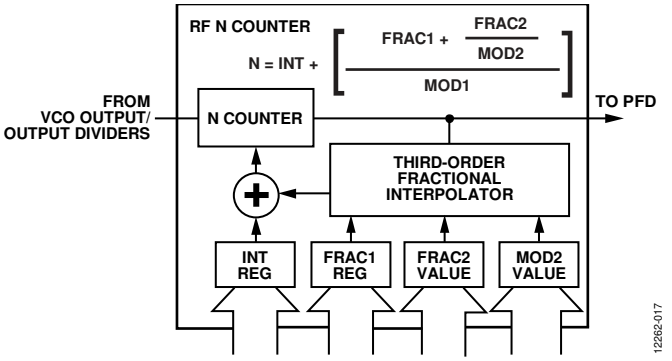


Figure 18. RF N Counter

INT, FRAC, MOD, and R Counter Relationship

The INT, FRAC1, FRAC2, MOD1, and MOD2 values, in conjunction with the R counter, make it possible to generate output frequencies that are spaced by fractions of the PFD frequency (f_{PFD}). For more information, see the RF Synthesizer—A Worked Example section.

Calculate the RF VCO frequency (RF_{OUT}) by the following:

$$RF_{OUT} = f_{PFD} \times N \quad (1)$$

where:
RF_{OUT} is the output frequency of the external VCO voltage controlled oscillator (without using the output divider).
f_{PFD} is a frequency of phase frequency detector.
N is the desired value of the feedback counter N.

Calculate the f_{PFD} by the following equation:

$$f_{PFD} = REF_{IN} \times [(1 + D)/(R \times (1 + T))] \quad (2)$$

where:
REF_{IN} is the reference input frequency.
D is the REF_{IN} doubler bit.
R is the preset divide ratio of the binary 10-bit programmable reference counter (1 to 1023).
T is the REF_{IN} divide by 2 bit (0 or 1)

N comprises

$$N = INT + \frac{FRAC1 + \frac{FRAC2}{MOD2}}{MOD1} \quad (3)$$

where:
INT is the 16-bit integer value (23 to 32,767 for 4/5 prescaler, 75 to 65,535 for 8/9 prescaler).
FRAC1 is the numerator of the primary modulus (1 – 16,777,215).
FRAC2 is the numerator of the 14-bit auxiliary modulus (1 – 16,383).
MOD2 is the programmable, 14-bit auxiliary fractional modulus (2 – 16,383).
MOD1 is a 24-bit primary modulus with a fixed value of 2^{24} (16,777,216).

This results in a very fine frequency resolution with no residual frequency error. To apply this formula, take the following steps:

1. Calculate N by dividing RF_{OUT}/f_{PFD}.
2. The integer value of this number forms INT.
3. Subtract this value from the full N value.
4. Multiply the remainder by 2^{24}.
5. The integer value of this number forms FRAC1.
6. Calculate the MOD2 basis on the channel spacing (f_{CHSP}) by
   $$MOD2 = f_{PFD}/GCD(f_{PFD}, f_{CHSP}) \quad (4)$$
   where:
   f_{CHSP} is the desired channel spacing frequency.
   $GCD(f_{PFD}, f_{CHSP})$ is a greatest common divider of the PFD frequency and the channel spacing frequency.
7. Calculate FRAC2 by the following equation:
   $$FRAC2 = [(N - INT) \times 2^{24} - FRAC1)] \times MOD2 \quad (5)$$

INT N Mode

If FRAC1 and FRAC2 = 0, the synthesizer operates in integer-N mode.

R Counter

The 10-bit R counter allows the input reference frequency, REF_{IN}, to be divided down to produce the reference clock to the PFD. Division ratios from 1 to 1023 are allowed.

PHASE FREQUENCY DETECTOR AND CHARGE PUMP

The phase frequency detector takes inputs from the R counter and N counter and produces an output proportional to the phase and frequency difference between them. Figure 19 is a simplified schematic of the phase frequency detector. The PFD includes a fixed delay element that sets the width of the antibacklash pulse (ABP), which is typically 2.6 ns. This pulse ensures that there is no dead zone in the PFD transfer function and provides a consistent reference spur level.

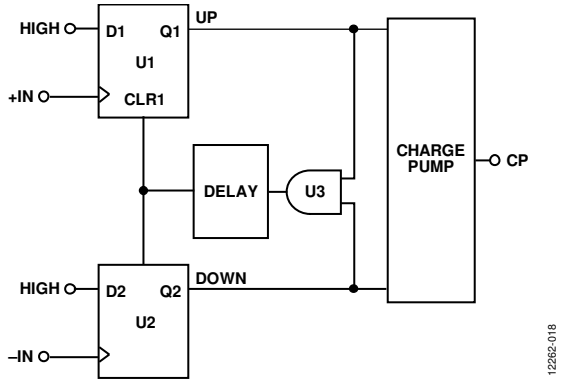


Figure 19. PFD Simplified Schematic

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4155 allows the user to access various internal points on the chip. The state of MUXOUT is controlled by the M3, M2, and M1 bits in Register 4 (for further details, see Figure 28). Figure 20 shows the MUXOUT section in block diagram form.

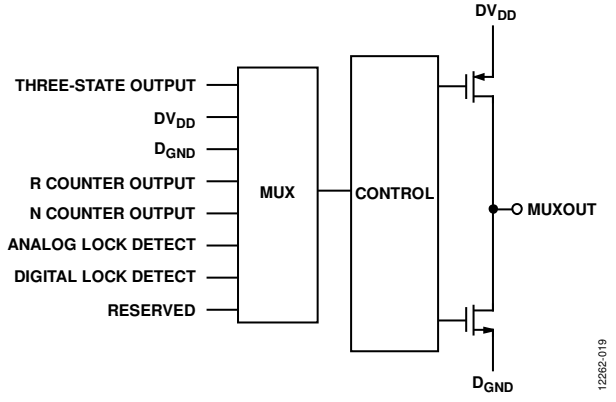


Figure 20. MUXOUT Schematic

INPUT SHIFT REGISTERS

Data is clocked into the 32-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of the nine latches on the rising edge of LE.

The destination latch is determined by the state of the four control bits (C4, C3, C2, and C1) in the shift register. These are the four LSBs: DB3, DB2, DB1, and DB0, as shown in Figure 2. The truth table for these bits is shown in Table 5. Figure 22 and Figure 23 summarize how the latches are programmed.

Table 5. Truth Table for the C4, C3, C2, and C1 Control Bits

Control Bits				
C4	C3	C2	C1	Register
0	0	0	0	Register 0 (R0)
0	0	0	1	Register 1 (R1)
0	0	1	0	Register 2 (R2)
0	0	1	1	Register 3 (R3)
0	1	0	0	Register 4 (R4)
0	1	0	1	Register 5 (R5)
0	1	1	0	Register 6 (R6)
0	1	1	1	Register 7 (R7)
1	0	0	0	Register 8 (R8)

PROGRAM MODES

Table 5 and Figure 24 through Figure 32 show how the program modes must be set up in the ADF4155.

The following ADF4155 settings are double buffered: the fractional value (FRAC1/FRAC2), the modulus value (MOD2), the reference doubler, the reference divide by 2 (RDIV2), the R counter value, the charge pump current setting, and the R divider select. This means that two events must occur before the device can use a new value for any of the double buffered settings. First, the new value must be latched into the device by writing to the appropriate register. Second, a new write must be performed on Register R0.

For example, any time that the modulus value is updated, Register 0 (R0) must be written to, to ensure that the modulus value is loaded correctly.

OUTPUT STAGE

For best spur performance, it is recommended to use the VCO output and disable the RF output (Bit DB6, Register 6) stage.

The RF output stage is used where lower frequency operation is required by enabling one of the output dividers.

The RF_{OUT}+ and RF_{OUT}− pins of the ADF4155 are connected to the collectors of an NPN differential pair driven by a signal from the RF divider block, as shown in Figure 21.

To optimize the output power requirements, the tail current of the differential pair is programmable using Bits[DB5:DB4] in Register 6 (R6). Four current levels can be set. These levels give output power levels of −4 dBm, −1 dBm, +2 dBm, and +5 dBm.

The current consumption as a function of the output power and the RF divider is shown in Table 6.

The output stage uses an internal 50 Ω resistor to RFV_{DD}. An external pull-up inductor to RFV_{DD} is necessary prior to ac coupling into a 50 Ω load. Alternatively, the output can be combined in a 1 + 1:1 transformer or a 180° microstrip coupler. If the outputs are used individually, the unused complimentary output must be terminated with a similar circuit to the used output.

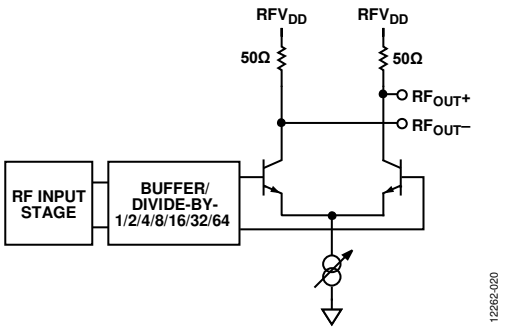


Figure 21. Output Stage

Another feature of the ADF4155 is that the supply current to the RF output stage can be shut down until the device achieves lock as measured by the digital lock detect circuitry. This shutdown is enabled by using the mute till lock detect (MTLD) bit (DB11) in Register 6 (R6).

Table 6. Total I_{DD} (DI_{DD} + AI_{DD} + RFI_{DD})

Divide By	RF_{OUT} Off	RF_{OUT} = −4 dBm	RF_{OUT} = −1 dBm	RF_{OUT} = +2 dBm	RF_{OUT} = +5 dBm
1	37.4	55.3	67.5	83.9	96.0
2	46.5	64.4	76.6	93.0	105.1
4	53.1	70.9	83.2	99.6	111.7
8	61.3	79.1	91.4	107.8	119.8
16	66.3	84.2	96.4	112.8	124.9
32	70.4	88.2	100.5	116.9	129.0
64	72.9	90.8	103.0	119.4	131.5

REGISTER MAPS

REGISTER 0

RESERVED											PRESCALER	16-BIT INTEGER VALUE (INT)														CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	PR1	N16	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	C4(0)	C3(0)	C2(0)	C1(0)

REGISTER 1

RESERVED				24-BIT MAIN FRACTIONAL VALUE (FRAC1) DBR[1]																						CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	F24	F23	F22	F21	F20	F19	F18	F17	F16	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C4(0)	C3(0)	C2(0)	C1(1)

REGISTER 2

RESERVED														14-BIT AUXILIARY MODULUS VALUE (MOD2) DBR[1]												CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	M14	M13	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	C4(0)	C3(0)	C2(1)	C1(0)

REGISTER 3

RESERVED														14-BIT AUXILIARY FRACTIONAL WORD (FRAC2) DBR[1]												CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	C4(0)	C3(0)	C2(1)	C1(1)

REGISTER 4

RESERVED	DITHER 2	MUXOUT			REFERENCE DOUBLER DBR[1]	DBR[1] RDIV2	10-BIT R COUNTER DBR$_1$										DOUBLE BUFFER	CHARGE PUMP CURRENT SETTING DBR$_1$				RESERVED	MUXOUT LEVEL SELECT	PHASE DETECTOR POLARITY	PD	CHARGE PUMP THREE-STATE	COUNTER RESET	CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	L2	M3	M2	M1	RD2	RD1	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	D1	CP4	CP3	CP2	CP1	0	LVS	U4	U3	U2	U1	C4(0)	C3(1)	C2(0)	C1(0)

REGISTER 5

RESERVED				PULSE BLEED DELAY		PB	RESERVED	ABP SELECT	RESERVED			CSR	RESERVED														CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	PB2	PB1	PB	0	ABP	0	0	0	CSR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C4(0)	C3(1)	C2(0)	C1(1)

[1] DBR = DOUBLE BUFFERED REGISTER—BUFFERED BY THE WRITE TO REGISTER 0.

12262-021

Figure 22. Register Summary (Register 0 to Register 5)

REGISTER 6

RESERVED	REF_{IN} MODE	RESERVED	DBB[1] RF DIVIDER SELECT	BLEED CURRENT SETTINGS	NEG BLEED	MTLD	RESERVED	RF OUTPUT ENABLE	OUTPUT POWER	CONTROL BITS
DB31	DB30	DB29 DB28 DB27 DB26 DB25 DB24	DB23 DB22 DB21	DB20 DB19 DB18 DB17 DB16 DB15 DB14 DB13	DB12	DB11	DB10 DB9 DB8 DB7	DB6	DB5 DB4	DB3 DB2 DB1 DB0
1	RM1	1 0 0 1 1 1	D12 D11 D10	BL8 BL7 BL6 BL5 BL4 BL3 BL2 BL1	BLE	D8	0 0 0 0	D3	D2 D1	C4(0) C3(1) C2(1) C1(0)

REGISTER 7

RESERVED	LOCK DETECT CYCLE COUNT	LOL MODE	RESERVED	LD MODE	CONTROL BITS
DB31 DB30 DB29 DB28 DB27 DB26 DB25 DB24 DB23 DB22 DB21 DB20 DB19 DB18 DB17 DB16 DB15 DB14 DB13 DB12 DB11 DB10	DB9 DB8	DB7	DB6 DB5	DB4	DB3 DB2 DB1 DB0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	LD5 LD4	LOL	1 1	LD1	C4(0) C3(1) C2(1) C1(1)

REGISTER 8

RESERVED	DITHER 1	PHASE WORD	CONTROL BITS
DB31 DB30 DB29	DB28	DB27 DB26 DB25 DB24 DB23 DB22 DB21 DB20 DB19 DB18 DB17 DB16 DB15 DB14 DB13 DB12 DB11 DB10 DB9 DB8 DB7 DB6 DB5 DB4	DB3 DB2 DB1 DB0
0 0 0	L1	1 1 1 0 1 0 1 0 0 1 0 1 1 1 1 1 1 1 1 0 0 0 0 1	C4(1) C3(0) C2(0) C1(0)

12262-022

[1] DBB = DOUBLE BUFFERED BITS—BUFFERED BY THE WRITE TO REGISTER 0 IF, AND ONLY IF, DB14 OF REGISTER 4 IS HIGH.

Figure 23. Register Summary (Register 6 to Register 8)

REGISTER 0

Register 0 Control Bits

With Bits[C4:C1] set to 0000, Register 0 is programmed. Figure 24 shows the input data format for programming this register.

16-Bit Integer Value (INT)

The 16 bits [DB19:DB4] set the INT value, which determines the integer part of the feedback division factor. The INT value is used in Equation 3 (see the INT, FRAC, MOD, and R Counter Relationship section). All integer values from 23 to 32,767 are allowed for 4/5 prescaler. For prescaler 8/9, the minimum integer value is 75, and the maximum integer value value is 65,535.

Prescaler (P) Value

The dual-modulus prescaler (P/P + 1), along with the INT, FRAC1, MOD1, FRAC2, and MOD2 counters, determines the overall division ratio from the VCO output to the PFD input.

Operating at CML levels, the prescaler takes the clock from the VCO output and divides it down for the counters. It is based on a synchronous 4/5 core. When the prescaler is set to 4/5, the maximum RF frequency allowed is 6 GHz. Therefore, when operating the ADF4155 above 6 GHz, set the prescaler to 8/9. The prescaler limits the INT value to the following:

- P = 4/5, INT_{MIN} = 23, INT_{MAX} = 32,767
- P = 8/9, INT_{MIN} = 75, INT_{MAX} = 65,535

In the ADF4155, the PR1 bit (DB20) in Register 0 sets the prescaler value.

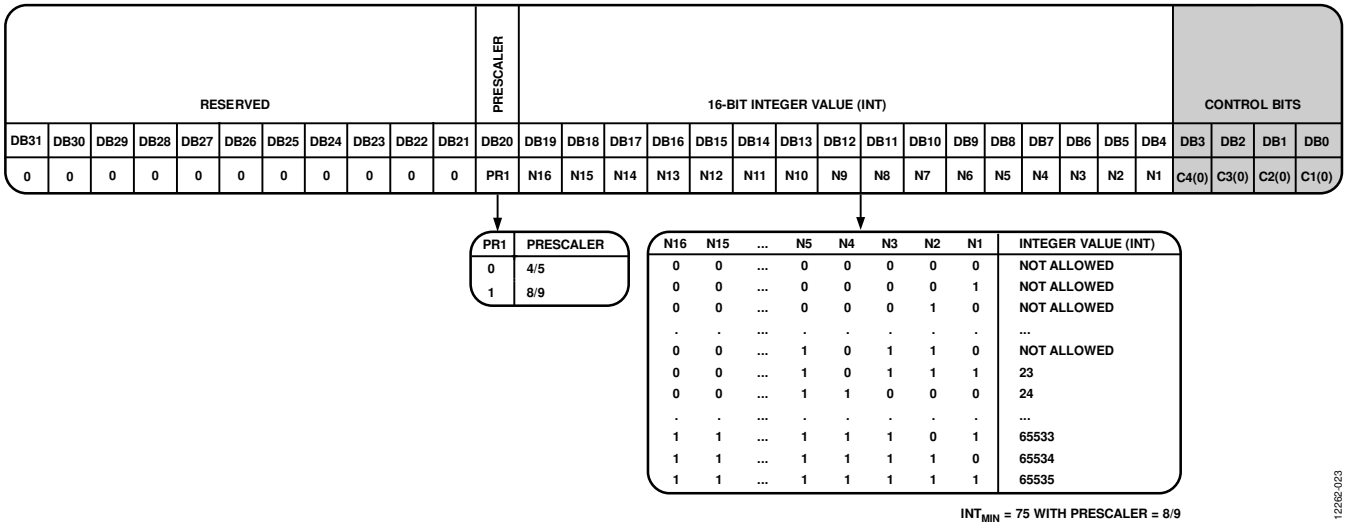


Figure 24. Register 0 (R0)

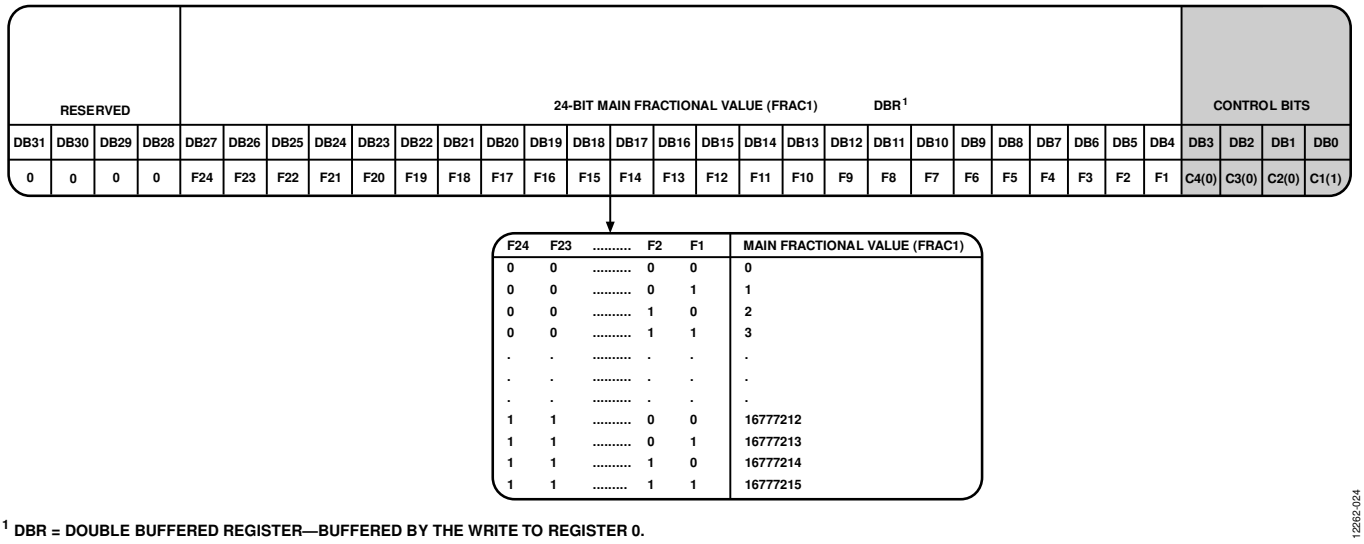
REGISTER 1

Register 1 Control Bits

With Bits[C4:C1] set to 0001, Register 1 is programmed. Figure 25 shows the input data format for programming this register.

24-Bit Main Fractional Value (FRAC1)

The 24 FRAC1 bits [DB27:DB4] together with FRAC2 and MOD2 set the numerator of the fraction that is input to the Σ-Δ modulator. This fraction, along with the INT value, specifies the new frequency channel that the synthesizer locks to, as shown in the RF Synthesizer—A Worked Example section. FRAC1 values from 0 to (2^{24} – 1) cover channels over a frequency range equal to the PFD reference frequency.



[1] DBR = DOUBLE BUFFERED REGISTER—BUFFERED BY THE WRITE TO REGISTER 0.

Figure 25. Register 1 (R1)

REGISTER 2

Register 2 Control Bits

With Bits[C4:C1] set to 0010, Register 2 is programmed. Figure 26 shows the input data format for programming this register.

14-Bit Auxiliary Modulus Value (MOD2)

The 14 MOD2 bits [DB17:DB4] set the auxiliary fractional modulus. The auxiliary fractional modulus is used to correct any residual error due to the main fractional modulus. For more information, see the RF Synthesizer—A Worked Example section.

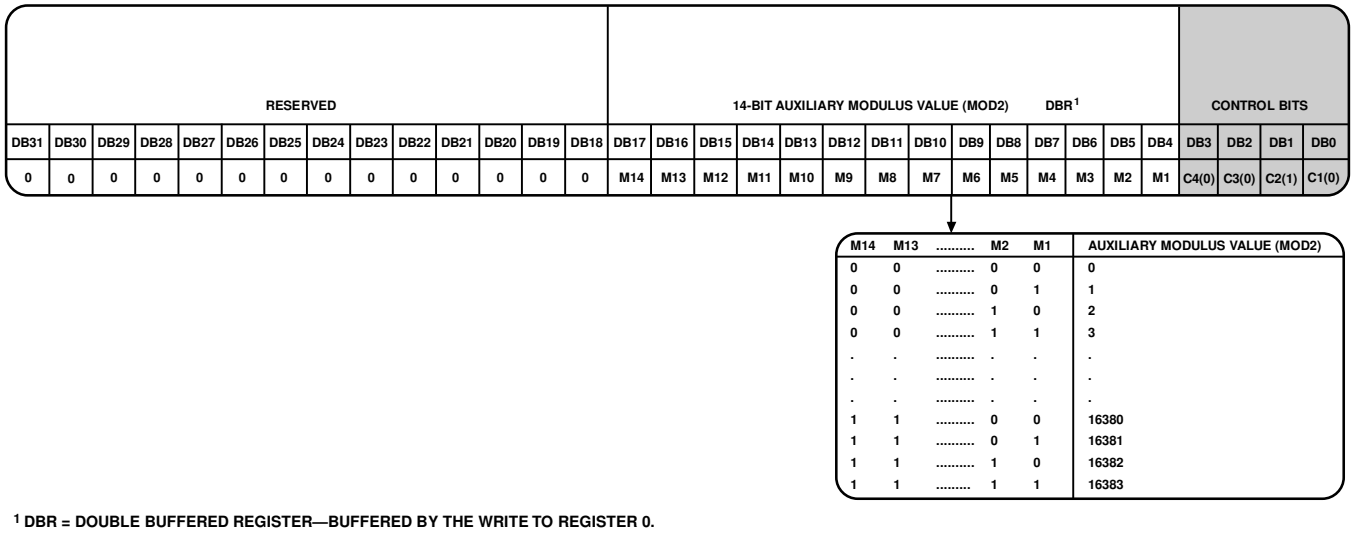
REGISTER 3

Register 3 Control Bits

With Bits[C4:C1] set to 0011, Register 3 is programmed. Figure 27 shows the input data format for programming this register.

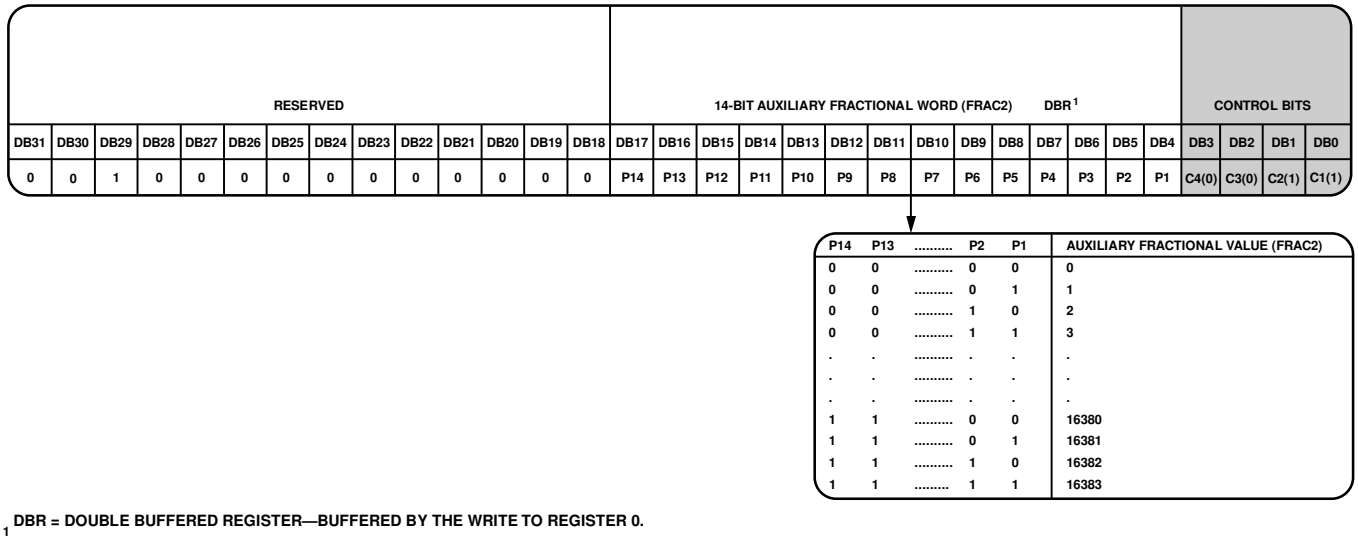
14-Bit Auxiliary Fractional Value (FRAC2)

The auxiliary fractional value bits [DB17:DB4] control the auxiliary fractional word. The word must be less than the MOD2 value programmed in Register 2.



[1] DBR = DOUBLE BUFFERED REGISTER—BUFFERED BY THE WRITE TO REGISTER 0.

Figure 26. Register 2 (R2)



[1] DBR = DOUBLE BUFFERED REGISTER—BUFFERED BY THE WRITE TO REGISTER 0.

Figure 27. Register 3 (R3)

REGISTER 4

Register 4 Control Bits

With Bits[C4:C1] set to 0100, Register 4 is programmed. Figure 28 shows the input data format for programming this register.

Dither 2

Dither to the second stage of the main Σ-Δ modulator can be activated on the ADF4155 by setting Bit DB30 in Register 4 (see Figure 28) to 1. This feature allows the user to optimize a design for improved spurious performance.

Dither randomizes the fractional quantization noise so that it resembles white noise rather than spurious noise. As a result, the device is optimized for improved spurious performance. This operation is normally used for fast locking applications when the PLL closed-loop bandwidth is wide.

MUXOUT

The on-chip multiplexer is controlled by Bits[DB29:DB27] (see Figure 28).

Reference Doubler

Setting DB26 to 0 feeds the reference frequency input (REF_{IN}) directly to the 10-bit R counter, disabling the doubler. Setting this bit to 1 multiplies the REF_{IN} by a factor of 2 before feeding it into the 10-bit R counter. When the doubler is disabled, the REF_{IN} falling edge is the active edge at the PFD input to the fractional synthesizer. When the doubler is enabled, both the rising and falling edges of REF_{IN} become active edges at the PFD input.

When the doubler is enabled and the dither is enabled, the in-band phase noise performance is sensitive to the REF_{IN} duty cycle. The phase noise degradation can be as much as 5 dB for REF_{IN} duty cycles outside a 45% to 55% range. The phase noise is insensitive to the REF_{IN} duty cycle when the dither is switched off and when the doubler is disabled.

The maximum allowable REF_{IN} frequency when the reference doubler is enabled is 80 MHz.

RDIV2

Setting the DB25 bit to 1 inserts a divide by 2 toggle flip-flop between the R counter and PFD, which extends the maximum REF_{IN} input rate. This function allows a 50% duty cycle signal to appear at the PFD input, which is necessary for cycle slip reduction.

10-Bit R Counter

The 10-bit R counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the PFD. Division ratios from 1 to 1023 are allowed.

Double Buffer

The DB14 bit enables or disables double buffering of Bits[DB23:DB21] in Register 6. The Program Modes section explains how double buffering works.

Charge Pump Current Setting

Bits[DB13:DB10] set the charge pump current. Set this value to the charge pump current that the loop filter is designed with (see Figure 28).

MUXOUT Level Select

The DB8 bit sets the voltage level used on the MUXOUT output. If the bit is programmed to 0, the MUXOUT uses a value of 1.8 V as the high level. When this bit is set to 1, the high level on the MUXOUT output is equal to DV_{DD} (3.3 V ± 5%).

Phase Detector Polarity

The DB7 bit sets the phase detector polarity. When a passive loop filter or a noninverting active loop filter is used, set this bit to 1. If an active filter with an inverting characteristic is used, set this bit to 0.

Power-Down (PD) Mode

DB6 provides the programmable power-down mode. Setting this bit to 1 performs a power-down. Setting this bit to 0 returns the synthesizer to normal operation. In software power-down mode, the device retains all information in its registers. The register contents are only lost if the supply voltages are removed.

Note that the software power-down issue requires a software workaround by using the following write sequence until fixed.

To perform a power-down, take the following steps:

1. Write INT = 65535 (0xFFFF) and prescaler = 1 in Register 0 (R0).
2. Write DB6 = 1 in Register 4 (R4).

To exit from a power-down, take the following steps:

1. Write the correct INT value and prescaler value in Register 0 (R0).
2. Write DB6 = 0 in Register 4 (R4).

When power-down is activated, the following events occur:

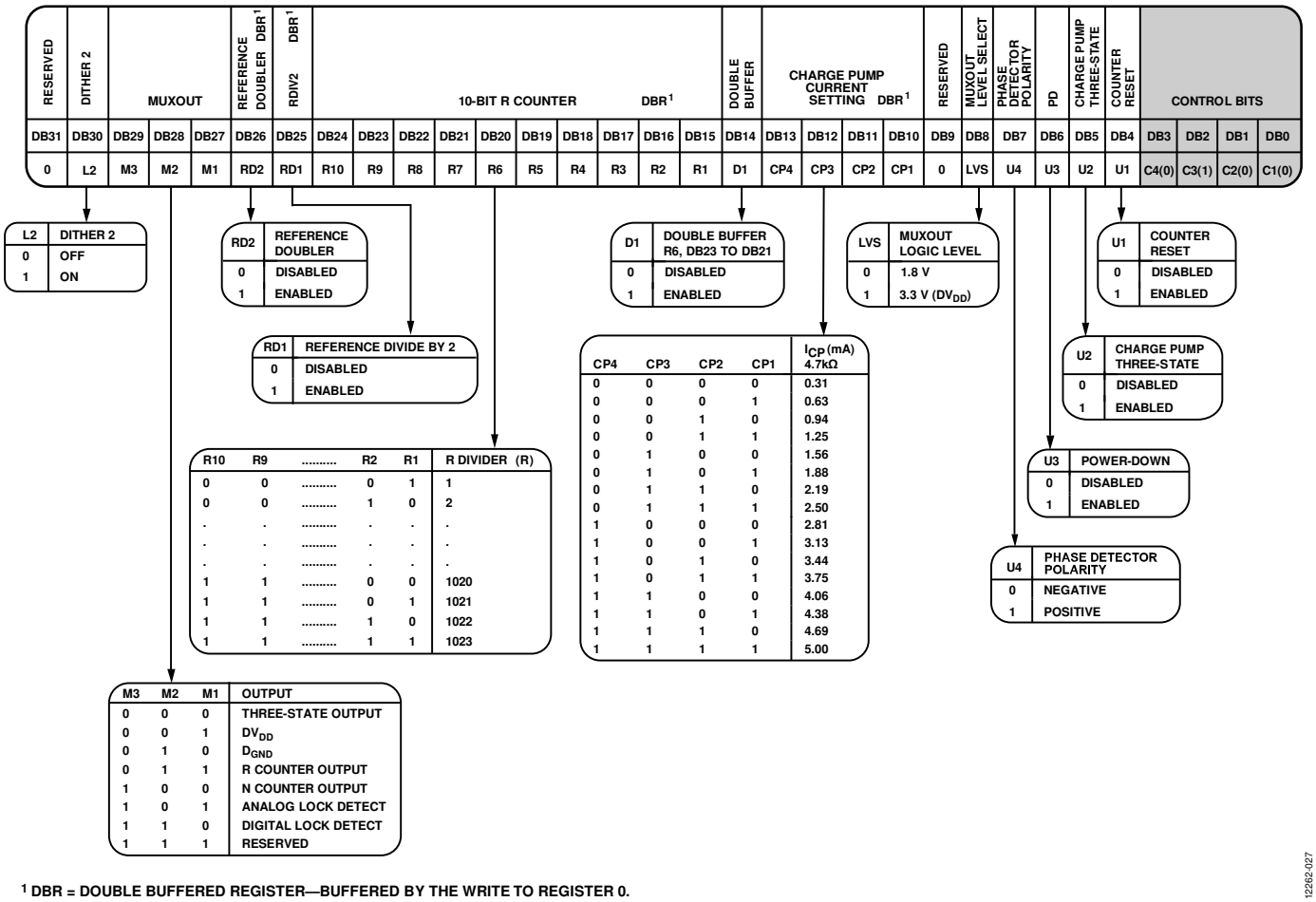
- Synthesizer counters are forced to their load state conditions.
- Charge pump is forced into three-state mode.
- Digital lock detect circuitry is reset.
- RF output buffers are disabled.
- Input registers remain active and capable of loading and latching data.

Charge Pump (CP) Three-State

Setting the DB5 bit to 1 puts the charge pump into three-state mode. Set this bit to 0 for normal operation.

Counter Reset

The DB4 bit is the reset bit for the R counter and the N counter of the ADF4155. When this bit is set to 1, the RF synthesizer N counter and R counter are held in reset. For normal operation, set this bit to 0.



[1] DBR = DOUBLE BUFFERED REGISTER—BUFFERED BY THE WRITE TO REGISTER 0.

Figure 28. Register 4 (R4)

REGISTER 5

Register 5 Control Bits

With Bits[C4:C1] set to 0101, Register 5 is programmed. Figure 29 shows the input data format for programming this register.

Pulse Bleed Delay

In some cases, pulsed bleed (DB25) can improve spurious performance compared to constant negative bleed. If enabling pulsed bleed, disable the constant negative bleed bit (Register 6, Bit DB12). Pulsed bleed works by adding a programmable delay to the charge pump down pulse, thereby introducing a phase offset in the loop and improving the linearity of the charge pump. The advantage over the constant negative bleed is that the programmable delay is only on for a short time within one PFD period compared to the constant negative bleed which is constantly on. This pulsed bleed can improve the spurious performance. The downside of a pulsed bleed is that there is less resolution to program the amount of bleed compared to the constant negative bleed.

The pulsed bleed delay is programmed using Bits[DB27:DB26].

Selecting the pulsed bleed delay so that the phase offset is <90 degrees is recommended.

$$PHASE\_OFFSET_{DEGREES} = (PULSED\_BLEED\_DELAY \times f_{PFD}) \times 360$$

Pulse bleed on the ADF4155 can be activated by setting Bit DB25 to 1 (see Figure 29).

Antibacklash Pulse (ABP) Select

Set DB23 to 0 to select the pulsed bleed delay, Bits[DB27:DB26] as the antibacklash pulse width. The recommended default setting is pulse bleed delay (2.6 ns). The pulse bleed delay bits (DB27:DB26) function as the antibacklash pulse width irrespective of whether the pulse bleed is enabled or disabled.

Set DB23 to 1 to use a narrow antibacklash pulse width of 1.6 ns. For PFD frequencies greater than 80 MHz, it is recommended to use the 1.6 ns pulse width.

Cycle Slip Reduction (CSR)

Setting DB19 to 1 enables cycle slip reduction. When using cycle slip reduction, the signal at the PFD must have a 50% duty cycle for the cycle slip reduction to work. The charge pump current setting must also be set to a minimum. Refer to the Cycle Slip Reduction for Faster Lock Times section for more information.

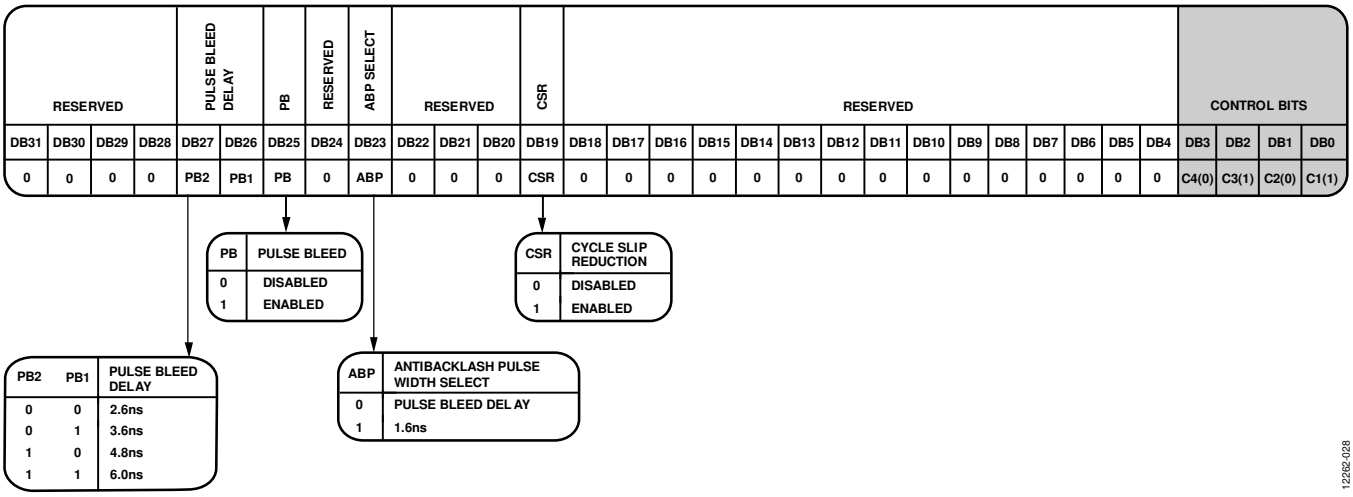


Figure 29. Register 5 (R5)

REGISTER 6

Register 6 Control Bits

With Bits[C4:C1] set to 0110, Register 6 is programmed. Figure 30 shows the input data format for programming this register.

Reference Input (REF_{IN}) Mode

When DB30 is set to 1, differential mode is used on the reference input. When this bit is set to 0, single-ended mode is used on the reference input.

RF Divider Select

Bits[DB23:DB21] select the value of the RF output divider (see Figure 30).

Bleed Current Settings

Enabling the constant negative bleed (DB12) is the recommended default mode to optimize the PLL in-band phase noise and spur performance. Constant negative bleed works by adding a constant offset to the charge pump and, therefore, improves its linearity.

Bits[DB20:DB13] and DB12 are used to control the amount of constant negative bleed current.

Bits[DB20:DB13] set the value of this bleed current with a resolution of 3.75 μA. The correct value of bleed current (I_{BLEED}) depends on the programmed charge pump current (I_{CP}) and the N counter value and must be calculated with following formula:

$$I_{BLEED} = 6 \times I_{CP}/N$$

The closest higher value must be chosen with the bleed current setting bits.

Constant Negative Bleed Current

When set to 1, Bit DB12 enables the constant negative bleed current. When set to 0, it disables the constant negative bleed current.

Mute Till Lock Detect (MTLD)

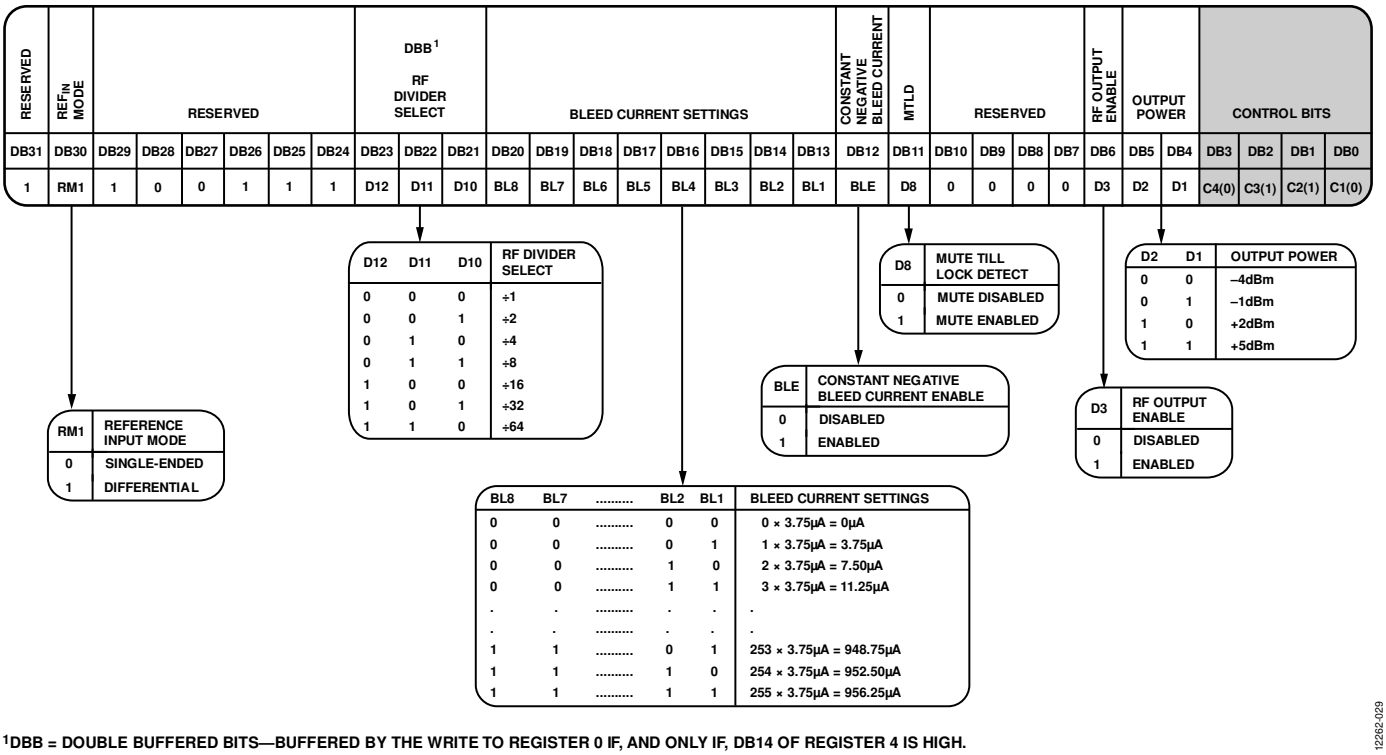
When DB11 is set to 1, the supply current to the RF output stage is shut down until the device achieves lock, as measured by the digital lock detect circuitry.

RF Output Enable

The DB6 bit enables or disables the RF output. If DB5 is set to 0, the RF output is disabled. If DB5 is set to 1, the RF output is enabled.

Output Power

Bits[DB5:DB4] set the value of the RF output power level (see Figure 30).



[1]DBB = DOUBLE BUFFERED BITS—BUFFERED BY THE WRITE TO REGISTER 0 IF, AND ONLY IF, DB14 OF REGISTER 4 IS HIGH.

Figure 30. Register 6 (R6)

REGISTER 7

Register 7 Control Bits

With Bits[C4:C1] set to 0111, Register 7 is programmed. Figure 31 shows the input data format for programming this register.

Lock Detect Cycle Count

Bits[DB9:DB8] set the number of consecutive cycles counted by the lock detect circuitry before asserting the lock detect high. See Figure 31 for more details.

Loss of Lock (LOL) Mode

Use this function if the application is a fixed frequency application in which the reference ($REF_{IN}+/REF_{IN}-$) is likely to be removed, such as a clocking application. The standard lock detect circuit assumes that the reference is always present. This functionality is enabled by setting DB7 to 1.

Lock Detect (LD) Mode

If DB4 is set to 0, each reference cycle is 5 ns long, which is appropriate for fractional-N mode. If DB4 is set to 1, each reference cycle is 2.4 ns long, which is more appropriate for integer-N mode. The lock detect signal goes high after the proper number of reference cycles, programmed by bits of the lock detect count field (Bits[DB9:DB8]), occurs.

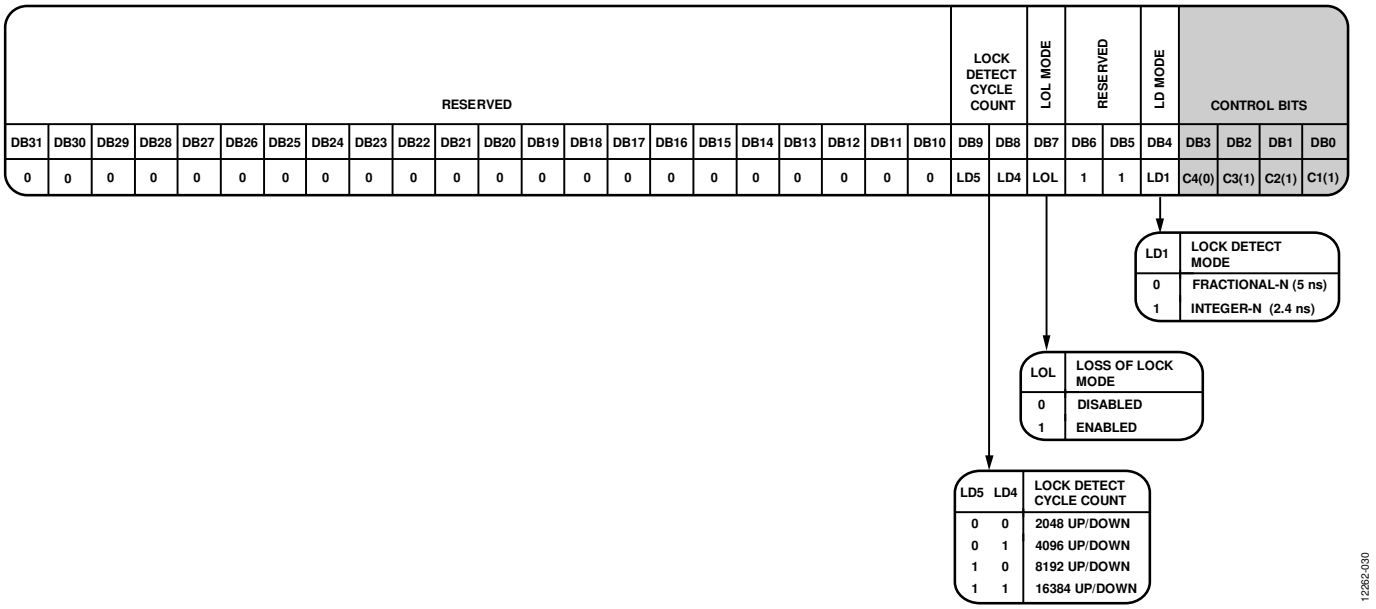


Figure 31. Register 7 (R7)

REGISTER 8

Register 8 Control Bits

With Bits[C4:C1] set to 1000, Register 8 is programmed. Figure 32 shows the input data format for programming this register.

Dither 1

Dither to the fixed accumulator (FRAC1/MOD1) can be activated on the ADF4155 by setting DB28 in Register 8. This is the default setting to optimize the spurious performance.

Phase Word

Bits[DB27:DB4] set the phase word that is also the seed word for the Σ-Δ modulator. For best spur performance, setting this value to a nonzero prime number is recommended. A register setting of 0x01EA5FE18 is the recommended default value.

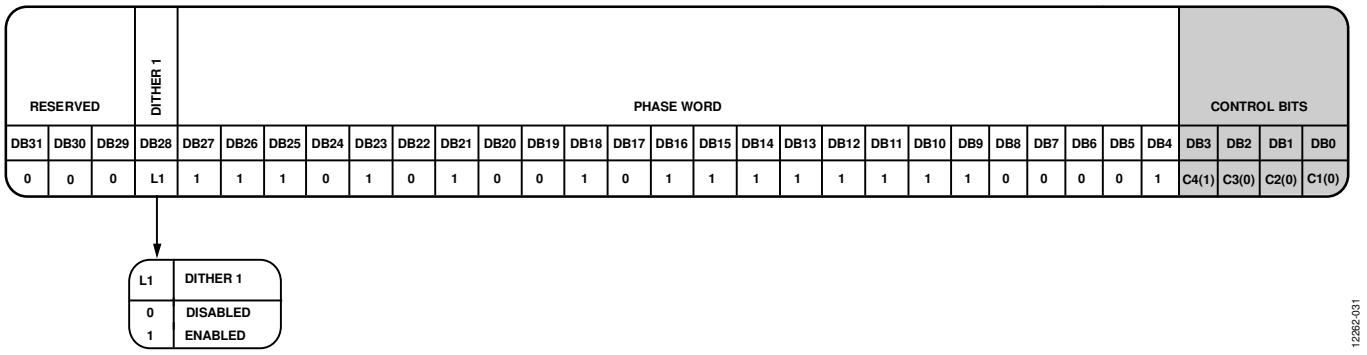


Figure 32. Register 8 (R8)

REGISTER INITIALIZATION SEQUENCE

At initial power-up, after the correct application of voltages to the supply pins, start the ADF4155 registers in the following sequence:

1. Register 8
2. Register 7
3. Register 6
4. Register 5
5. Register 4
6. Register 3
7. Register 2
8. Register 1
9. Register 0

RF SYNTHESIZER—A WORKED EXAMPLE

The following equations are used to program the ADF4155 synthesizer:

$$RF_{OUT} = \left(INT + \frac{FRAC1 + \frac{FRAC2}{MOD2}}{MOD1} \right) \times \frac{f_{PFD}}{RF\ Divider} \quad (6)$$

where:
RF_{OUT} is the RF frequency output.
INT is the integer division factor.
FRAC1 is the 24-bit main fractional value.
FRAC2 is the 14-bit auxiliary fractional value.
MOD2 is the 14-bit auxiliary modulus value.
MOD1 is the 24-bit fixed modulus value.
RF Divider is the output divider that divides down the VCO frequency.

$$f_{PFD} = REF_{IN} \times [(1 + D)/(R \times (1 + T))] \quad (7)$$

where:
REF_{IN} is the reference frequency input.
D is the reference doubler bit.
R is the reference division factor.
T is the reference divide by 2 bit (0 or 1).

For example, in a UMTS system where a 2114.6 MHz RF frequency output (RF_{OUT}) is required, a 122.88 MHz reference frequency input (REF_{IN}) is available. Therefore, the RF divider of 2 can be used to improve the phase noise at the RF outputs (VCO frequency = 4229.2 MHz, RF_{OUT} = VCO frequency/RF divider = 4229.2 MHz/2 = 2114.6 MHz).

The ADF4155 allows closing the loop only before the output divider (see Figure 33).

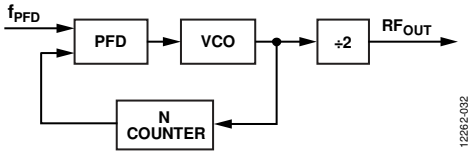


Figure 33. Loop Closed Before Output Divider

With REF_{IN} = 122.88 MHz, a f_{PFD} = 61.44 MHz is selected.

Use the following values with Equation 6:

- N counter = VCO Frequency/f_{PFD}
- INT = integer(VCO Frequency/f_{PFD}); INT = 68
- FRAC = remainder(VCO Frequency/f_{PFD}) = 0.834635
- MOD1 = 2^{24} = 16,777,216
- FRAC1 = integer(MOD1 × FRAC) = 14,002,858
- Remainder = 0.6672 = FRAC2/MOD2

With a channel spacing of 200 kHz, MOD2 and FRAC2 equal the following:

- MOD2 = 61440 kHz/GCD(61440 kHz, 200 kHz). GCD(f_{PFD}, f_{CHSP}) is a greatest common divider of the PFD frequency and the channel spacing frequency. Therefore, MOD2 = 1536.
- FRAC2 = integer(MOD2 × 0.6672) =1024

From Equation 7, the following is true:

$$f_{PFD} = [122.88\ MHz \times (1 + 0)/2] = 61.44\ MHz$$

$$2112.6\ MHz = [61.44\ MHz \times [(INT + (FRAC1 + FRAC2/MOD2)/2^{24}])/2$$

where:
INT = 68.
FRAC1 = 14,002,858.
FRAC2 = 1024.
MOD2 = 1536.
RF Divider = 2.

REFERENCE DOUBLER AND REFERENCE DIVIDER

The on-chip reference doubler allows the input reference signal to be doubled. This feature is useful for increasing the PFD comparison frequency. Making the PFD frequency higher improves the noise performance of the system. Doubling the PFD frequency usually improves noise performance by 3 dB. Note that the PFD frequency cannot operate above 125 MHz due to a limitation in the speed of the Σ-Δ circuit of the N counter.

The reference divide by 2 divides the reference signal by 2, resulting in a 50% duty cycle PFD frequency.

CYCLE SLIP REDUCTION FOR FASTER LOCK TIMES

To achieve good attenuation of the unwanted spurs, narrow loop bandwidth is recommended. However, in fast locking applications, the loop bandwidth generally needs to be wide, and, therefore, the filter does not provide much attenuation of the spurs. If the cycle slip reduction feature is enabled, the narrow loop bandwidth is maintained for spur attenuation but faster lock times are still possible.

Cycle Slips

Cycle slips occur in integer-N/fractional-N synthesizers when the loop bandwidth is narrow compared to the PFD frequency. The phase error at the PFD inputs accumulates too fast for the PLL to correct, and the charge pump temporarily pumps in the wrong direction, slowing down the lock time dramatically. The ADF4155 contains a cycle slip reduction feature that extends the linear range of the PFD, allowing faster lock times without modifications to the loop filter circuitry.

When the circuitry detects that a cycle slip is about to occur, it turns on an extra charge pump current cell. This outputs a constant current to the loop filter or removes a constant current from the loop filter (depending on whether the VCO tuning voltage needs to increase or decrease to acquire the new frequency). The effect is that the linear range of the PFD is increased. Loop stability is maintained because the current is constant and is not a pulsed current.

If the phase error increases again to a point where another cycle slip is likely, the ADF4155 turns on another charge pump cell. This cycle slip and addition of a charge pump cell continues until the ADF4155 detects that the VCO frequency has gone past the desired frequency. The extra charge pump cells are turned off one by one until all the extra charge pump cells have been disabled, and the frequency is settled with the original loop filter bandwidth.

Up to seven extra charge pump cells can be turned on. In most applications, it is enough to eliminate cycle slips altogether, giving much faster lock times.

Setting Bit DB19 in Register 5 to 1 enables cycle slip reduction. Note that the PFD requires a 45% to 55% duty cycle for CSR to operate correctly.

SPURIOUS OPTIMIZATION

Narrow loop bandwidths can filter unwanted spurious signals; however, these bandwidths usually have a long lock time. A wider loop bandwidth achieves faster lock times but can lead to increased spurious signals inside the loop bandwidth.

SPUR MECHANISMS

This section describes the different spur mechanisms that arise with a fractional-N synthesizer, and how to minimize them in the ADF4155.

Integer Boundary Spurs

One of the mechanisms for fractional spur creation is the interactions between the RF VCO frequency and the reference frequency. When these frequencies are not integer related (the purpose of a fractional-N synthesizer), spur sidebands appear on the VCO output spectrum at an offset frequency that corresponds to the beat note or the difference frequency between an integer multiple of the reference and the VCO frequency. These spurs are attenuated by the loop filter and are more noticeable on channels close to integer multiples of the reference where the difference frequency can be inside the loop bandwidth (thus the name integer boundary spurs).

Reference Spurs

Reference spurs are generally not a problem in fractional-N synthesizers because the reference offset is far outside the loop bandwidth. However, any reference feedthrough mechanism that bypasses the loop can cause a problem. Feedthrough of low levels of on-chip reference switching noise, through the $RF_{IN}+/RF_{IN}-$ pins back to the VCO, can result in reference spur levels as high as −90 dBc. The printed circuit board (PCB) layout must ensure adequate isolation between VCO traces and the input reference to avoid a possible feedthrough path on the board.

Fractional Spurs

The combination of the high fixed modulus MOD1 and the programmable modulus MOD2 gives a very high effective 38-bit resolution and spreads the Σ-Δ quantization energy into small subhertz discrete bins that then appear as broadband noise rather than discrete spurs. The use of negative bleed at the recommended setting (see Register 6 and Figure 30), and the wider ABP of 2.6 ns, linearizes the transfer function from the Σ-Δ output to the VCO output and minimizes the spur regrowth. For some combinations of FRAC2 and MOD2, discrete spurs can reappear. In these cases, changing FRAC2 or MOD2 by 1 LSB often removes these spurs.

For best spur performance, take the PLL output from the external VCO rather than the internal RF buffer.

APPLICATIONS INFORMATION

LOCAL OSCILLATOR WITH RF BUFFER

Figure 34 shows the ADF4155 used with a VCO and an RF buffer to produce a local oscillator (LO) at 5.8 GHz.

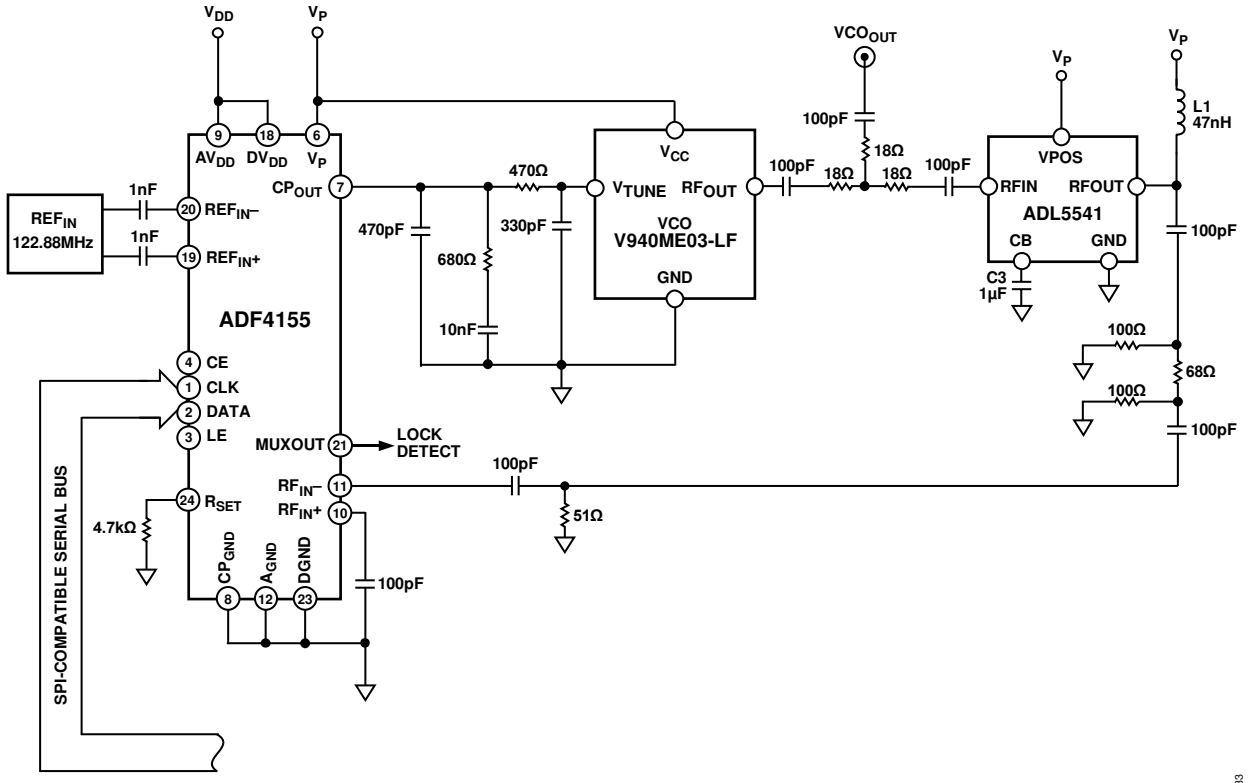
The differential reference input signal is applied to the circuit at $REF_{IN}+$ and $REF_{IN}-$. A 122.88 MHz reference is used, which is divided by 2 to serve as the 61.44 MHz PFD frequency.

The charge pump output (I_{CP} = 0.938 mA) of the ADF4155 drives the loop filter. The ADIsimPLL design tool is used to calculate the loop filter components. It is designed for a loop bandwidth of 80 kHz and a phase margin of 45°.

The loop filter output drives the VCO, whose output is fed back to the RF input of the PLL synthesizer via an RF buffer. It also drives the RF output terminal (VCO_{OUT}). A T-circuit configuration provides 50 Ω matching between the VCO_{OUT}, the RFOUT, and the RFIN pins of the ADL5541 RF buffer.

The RF buffer is an optional buffer inserted in the feedback between the VCO and the $RF_{IN}+/RF_{IN}-$ pins of the PLL, where an improvement in spur performance is required. The pie attenuator is required to reduce the RF buffer output to within the required range of the PLL $RF_{IN}+/RF_{IN}-$ pins.

In a PLL system, it is important to know when the loop is in lock. The locking is achieved by using the MUXOUT signal from the synthesizer. The MUXOUT pin can be programmed to monitor various internal signals in the synthesizer. One of these is the lock detect signal.



NOTES
THIS IS A SIMPLIFIED SCHEMATIC, DECOUPLING CAPACITORS AND SPI CONNECTION DETAILS HAVE BEEN OMITTED FOR CLARITY.

Figure 34. Typical Application Diagram

OUTLINE DIMENSIONS

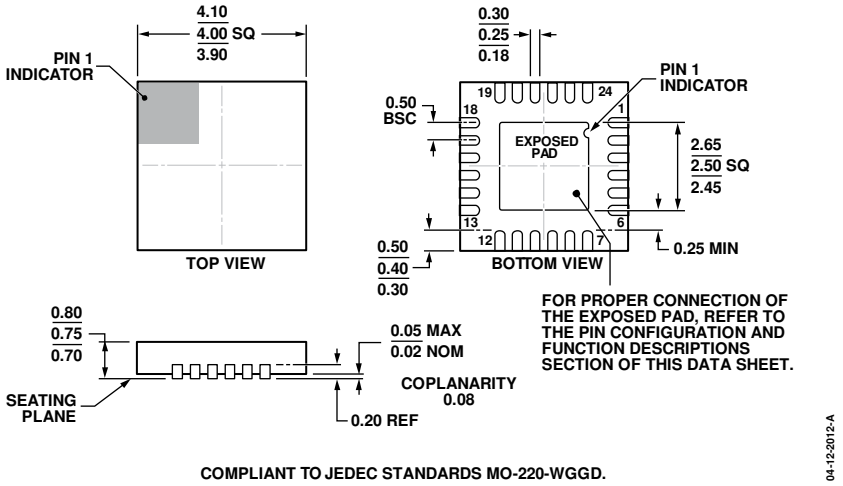


Figure 35. 24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-24-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADF4155BCPZ	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-24-7
ADF4155BCPZ-RL7	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-24-7
EV-ADF4155EB1Z		Evaluation Board	

[1] Z = RoHS Compliant Part.

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