

FEATURES

- 0.58 Ω typical on resistance**
- 0.82 Ω maximum on resistance at 85°C**
- 1.8 V to 5.5 V single supply**
- High current carrying capability: 250 mA continuous**
- Rail-to-rail switching operation**
- Fast-switching times: <20 ns**
- Typical power consumption: <0.1 μ W**
- 2.1 mm \times 2.1 mm mini LFCSP**

APPLICATIONS

- Cellular phones
- PDA's
- MP3 players
- Power routing
- Battery-powered systems
- PCMCIA cards
- Modems
- Audio and video signal routing
- Communication systems

GENERAL DESCRIPTION

The **ADG858** is a low voltage CMOS device containing four single-pole, double-throw (SPDT) switches. This device offers ultralow on resistance of less than 0.82 Ω over the full temperature range. The **ADG858** is fully specified for 4.2 V to 5.5 V and 2.7 V to 3.6 V supply operation.

Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. The **ADG858** exhibits break-before-make switching action.

The **ADG858** is available in a 2.1 mm \times 2.1 mm, 16-lead mini LFCSP. This tiny package makes the device ideal for space-constrained applications, such as handsets, PDA's, and MP3's.

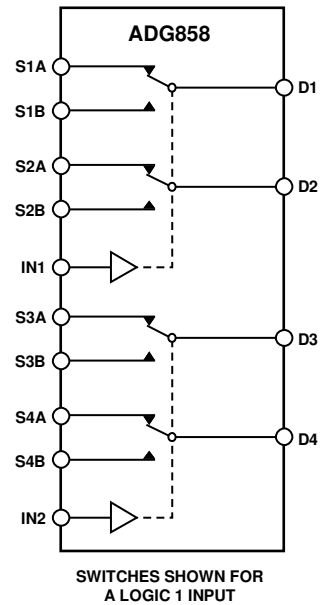
FUNCTIONAL BLOCK DIAGRAM


Figure 1.

070940-001

PRODUCT HIGHLIGHTS

1. <0.82 Ω over the full temperature range of -40°C to $+85^{\circ}\text{C}$.
2. Single 1.8 V to 5.5 V operation.
3. Compatible with 1.8 V CMOS logic.
4. High current handling capability (250 mA continuous current per channel).
5. Low THD + N: 0.06% typical.
6. 2.1 mm \times 2.1 mm, 16-lead mini LFCSP.

Rev. B

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REVISION HISTORY

4/16—Rev. A to Rev. B

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Updated Outline Dimensions	13
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8/08—Rev. 0 to Rev. A

Changes to Features Section.....	1
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8/08—Revision 0: Initial Version

SPECIFICATIONS

$V_{DD} = 4.2\text{ V}$ to 5.5 V , $GND = 0\text{ V}$, unless otherwise noted.

Table 1.

Parameter	+25°C	-40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 to V_{DD}	V	
On Resistance, R_{ON}	0.58		Ω typ	$V_{DD} = 4.2\text{ V}$, $V_S = 0\text{ V}$ to V_{DD} , $I_S = 100\text{ mA}$, see Figure 16
	0.72	0.82	Ω max	
On-Resistance Match Between Channels, ΔR_{ON}	0.04		Ω typ	$V_{DD} = 4.2\text{ V}$, $V_S = 2\text{ V}$, $I_S = 100\text{ mA}$
		0.14	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	0.12		Ω typ	$V_{DD} = 4.2\text{ V}$, $V_S = 0\text{ V}$ to V_{DD}
		0.26	Ω max	$I_S = 100\text{ mA}$
LEAKAGE CURRENTS				
Source Off Leakage, I_S (Off)	± 10		pA typ	$V_{DD} = 5.5\text{ V}$ $V_S = 0.6\text{ V}/4.2\text{ V}$, $V_D = 4.2\text{ V}/0.6\text{ V}$, see Figure 17
Channel On Leakage, I_D , I_S (On)	± 10		pA typ	$V_S = V_D = 0.6\text{ V}$ or 4.2 V , see Figure 18
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.004		μA typ	$V_{IN} = V_{GND}$ or V_{DD}
		0.05	μA max	
Digital Input Capacitance, C_{IN}	2		pF typ	
DYNAMIC CHARACTERISTICS¹				
t_{ON}	20		ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$
	27	36	ns max	$V_S = 3\text{ V}/0\text{ V}$, see Figure 19
t_{OFF}	8		ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$
	12	13	ns max	$V_S = 3\text{ V}$, see Figure 19
Break-Before-Make Time Delay, t_{BBM}	14		ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$
		9	ns min	$V_{S1} = V_{S2} = 1.5\text{ V}$, see Figure 20
Charge Injection	45		pC typ	$V_S = 1.5\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$, see Figure 21
Off Isolation	-67		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$, see Figure 22
Channel-to-Channel Crosstalk	-85		dB typ	S1A to S2A/S1B to S2B/S3A to S4A/S3B to S4B, $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$, see Figure 25
	-67		dB typ	S1A to S1B/S2A to S2B/S3A to S3B/S4A to S4B, $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$, see Figure 24
Total Harmonic Distortion, THD + N	0.06		%	$R_L = 32\ \Omega$, $f = 20\text{ Hz}$ to 20 kHz , $V_S = 2\text{ V p-p}$
Insertion Loss	-0.05		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, see Figure 23
-3 dB Bandwidth	70		MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, see Figure 23
C_S (Off)	25		pF typ	
C_D , C_S (On)	75		pF typ	
POWER REQUIREMENTS				
I_{DD}	0.003		μA typ	$V_{DD} = 5.5\text{ V}$ Digital inputs = 0 V or 5.5 V
		1	μA max	

¹ Guaranteed by design, not subject to production test.

$V_{DD} = 2.7\text{ V}$ to 3.6 V , $GND = 0\text{ V}$, unless otherwise noted.

Table 2.

Parameter	+25°C	-40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 to V_{DD}	V	
On Resistance, R_{ON}	1		Ω typ	$V_{DD} = 2.7\text{ V}$, $V_S = 0\text{ V}$ to V_{DD} , $I_S = 100\text{ mA}$, see Figure 16
	1.35	1.5	Ω max	
On-Resistance Match Between Channels, ΔR_{ON}	0.05		Ω typ	$V_{DD} = 2.7\text{ V}$, $V_S = 0.7\text{ V}$, $I_S = 100\text{ mA}$
		0.15	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	0.35		Ω typ	$V_{DD} = 2.7\text{ V}$, $V_S = 0\text{ V}$ to V_{DD} , $I_S = 100\text{ mA}$
		0.79	Ω max	
LEAKAGE CURRENTS				
Source Off Leakage I_S (Off)	± 10		μA typ	$V_{DD} = 3.6\text{ V}$ $V_S = 0.6\text{ V}/3.3\text{ V}$, $V_D = 3.3\text{ V}/0.6\text{ V}$, see Figure 17
Channel On Leakage I_D , I_S (On)	± 10		μA typ	$V_S = V_D = 0.6\text{ V}$ or 3.3 V , see Figure 18
DIGITAL INPUTS				
Input High Voltage, V_{INH}		1.35	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.004		μA typ	$V_{IN} = V_{GND}$ or V_{DD}
		0.05	μA max	
Digital Input Capacitance, C_{IN}	2		pF typ	
DYNAMIC CHARACTERISTICS¹				
t_{ON}	30		ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$
	50	59	ns max	$V_S = 1.5\text{ V}/0\text{ V}$, see Figure 19
t_{OFF}	9		ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$
	14	15	ns max	$V_S = 1.5\text{ V}$, see Figure 19
Break-Before-Make Time Delay, t_{BBM}	25		ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$
		11	ns min	$V_{S1} = V_{S2} = 1.5\text{ V}$, see Figure 20
Charge Injection	35		pC typ	$V_S = 1.5\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$, see Figure 21
Off Isolation	-67		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$, see Figure 22
Channel-to-Channel Crosstalk	-85		dB typ	S1A to S2A/S1B to S2B/S3A to S4A/S3B to S4B, $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$, see Figure 25
			dB typ	S1A to S1B/S2A to S2B/S3A to S3B/S4A to S4B, $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$, see Figure 24
Total Harmonic Distortion, THD + N	0.1		%	$R_L = 32\ \Omega$, $f = 20\text{ Hz}$ to 20 kHz , $V_S = 1.5\text{ V}$ p-p
Insertion Loss	-0.06		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, see Figure 23
-3 dB Bandwidth	70		MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, see Figure 23
C_S (Off)	25		pF typ	
C_D , C_S (On)	75		pF typ	
POWER REQUIREMENTS				
I_{DD}	0.003		μA typ	$V_{DD} = 3.6\text{ V}$ Digital inputs = 0 V or 3.6 V
		1	μA max	

¹ Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	-0.3 V to +6 V
Analog Inputs ¹	-0.3 V to $V_{DD} + 0.3$ V
Digital Inputs ¹	-0.3 V to V_{DD} or 10 mA, whichever occurs first
Peak Current, S or D	500 mA (pulsed at 1 ms, 10% duty cycle max)
Continuous Current, S or D	250 mA
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
16-Lead Mini LFCSP	
θ_{JA} Thermal Impedance, 3-Layer Board	84.9°C/W
Reflow Soldering, Pb-Free	
Peak Temperature	260(+0/-5)°C
Time at Peak Temperature	10 sec to 40 sec

¹ Overvoltages at IN, S, or D are clamped by internal diodes. Current must be limited to the maximum ratings given.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

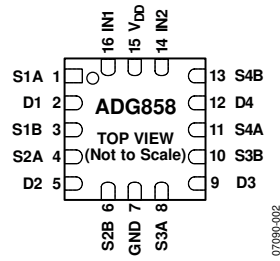


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 4, 6, 8, 10, 11, 13	S1A, S1B, S2A, S2B, S3A, S3B, S4A, S4B	Source Terminal. Can be an input or output.
2, 5, 9, 12	D1, D2, D3, D4	Drain Terminal. Can be an input or output.
7	GND	Ground (0 V) Reference.
14, 16	IN2, IN1	Logic Control Input.
15	V _{DD}	Most Positive Power Supply Potential.

Table 5. ADG858 Truth Table

Logic (IN1/IN2)	Switch A (S1A/S2A/S3A/S4A)	Switch B (S1B/S2B/S3B/S4B)
0	Off	On
1	On	Off

TYPICAL PERFORMANCE CHARACTERISTICS

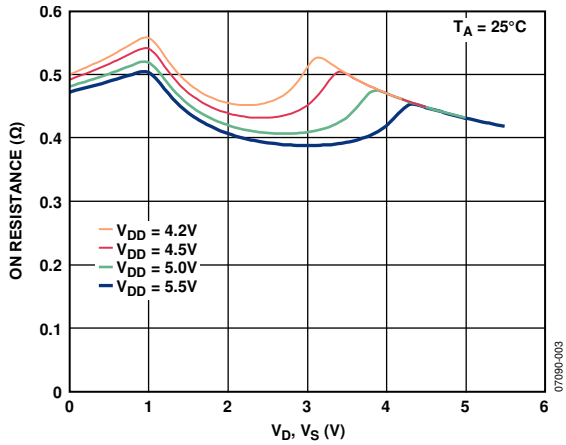


Figure 3. On Resistance vs. V_D (V_S), $V_{DD} = 4.2$ V to 5.5 V

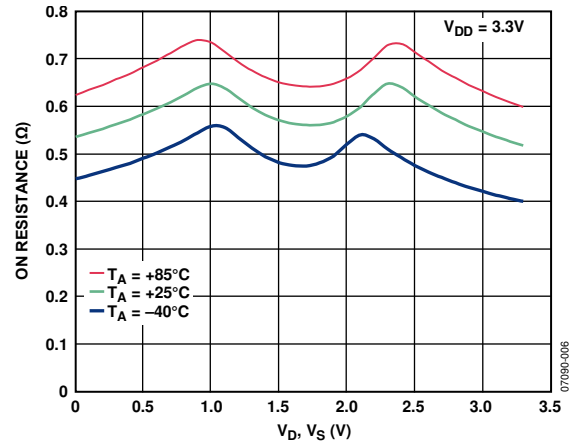


Figure 6. On Resistance vs. V_D (V_S) for Different Temperatures, $V_{DD} = 3.3$ V

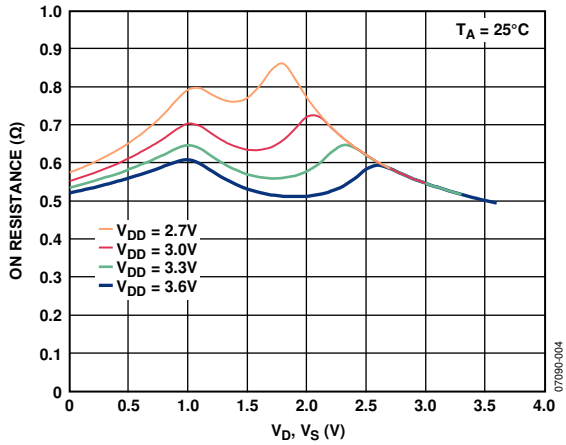


Figure 4. On Resistance vs. V_D (V_S), $V_{DD} = 2.7$ V to 3.6 V

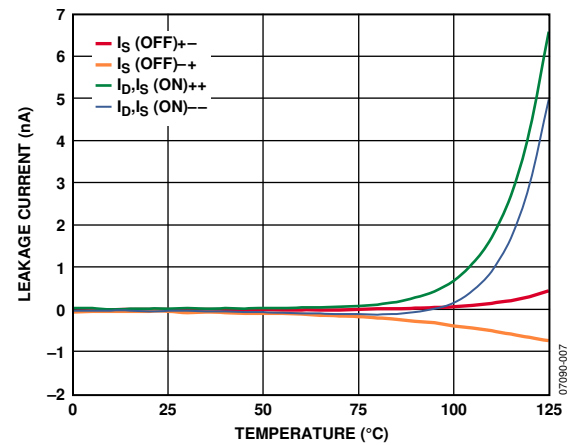


Figure 7. Leakage Current vs. Temperature, $V_{DD} = 5$ V

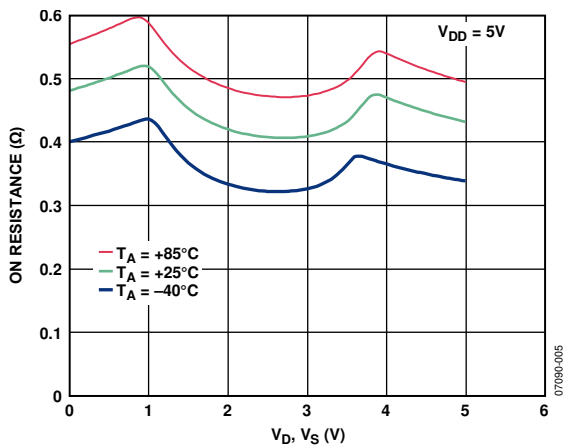


Figure 5. On Resistance vs. V_D (V_S) for Different Temperatures, $V_{DD} = 5$ V

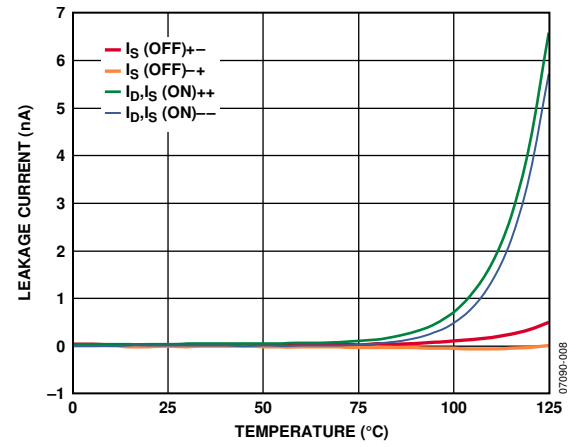


Figure 8. Leakage Current vs. Temperature, $V_{DD} = 3.3$ V

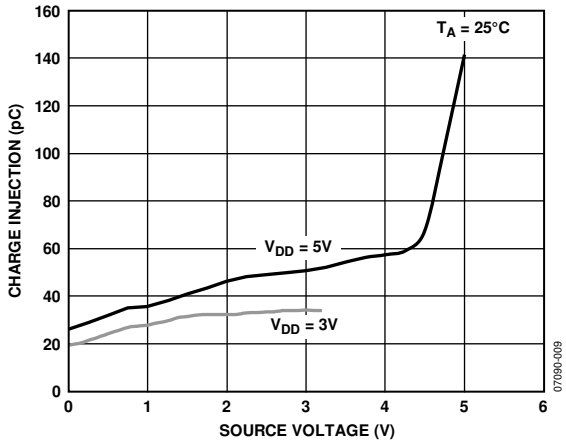


Figure 9. Charge Injection vs. Source Voltage

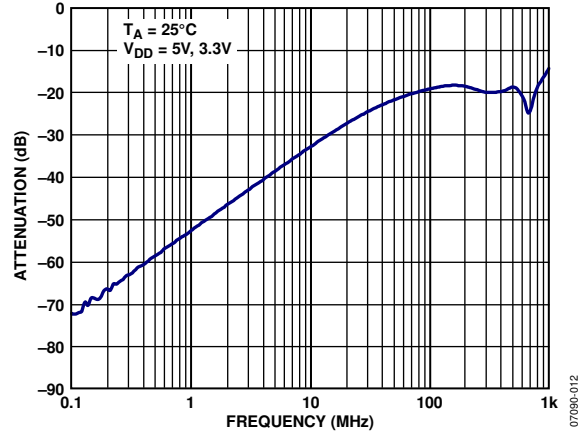


Figure 12. Off Isolation vs. Frequency

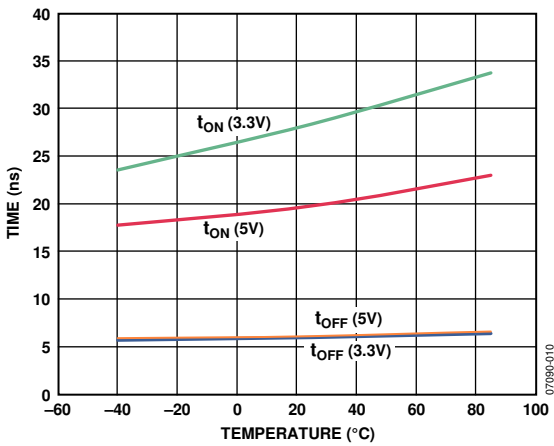


Figure 10. t_{ON}/t_{OFF} Times vs. Temperature

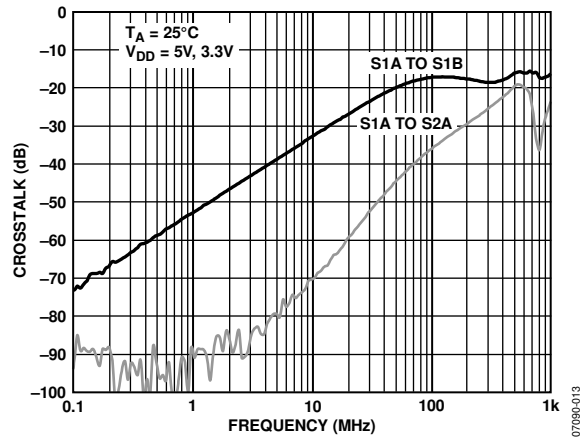


Figure 13. Crosstalk vs. Frequency

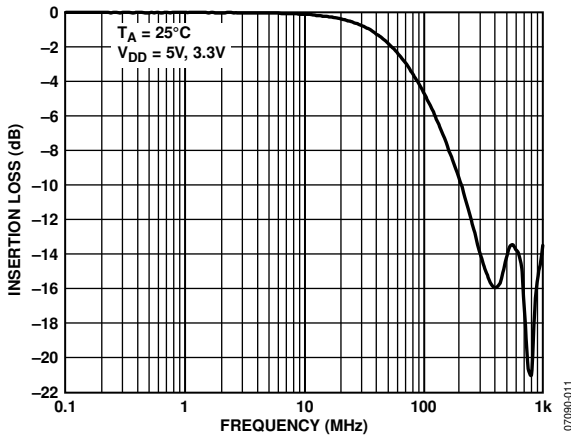


Figure 11. Bandwidth

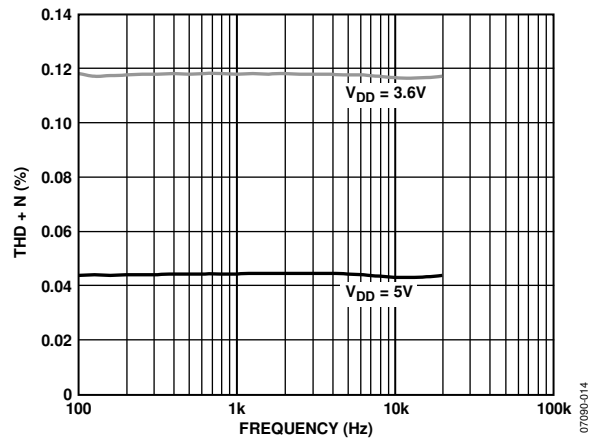


Figure 14. Total Harmonic Distortion + Noise (THD + N) vs. Frequency

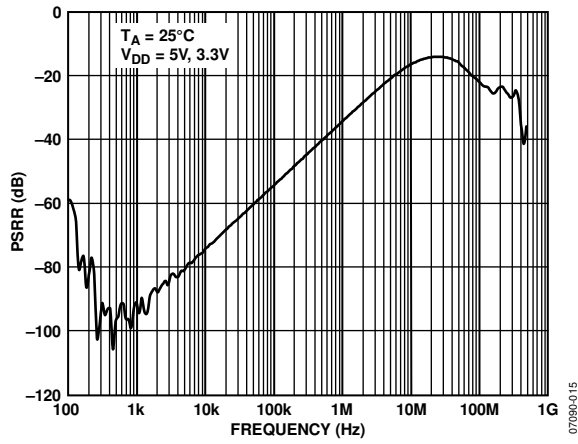


Figure 15. PSRR vs. Frequency

TEST CIRCUITS

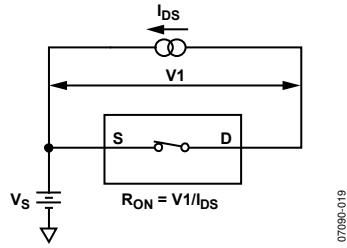


Figure 16. On Resistance

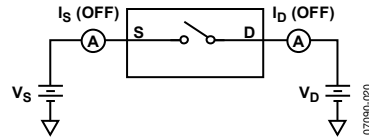


Figure 17. Off Leakage

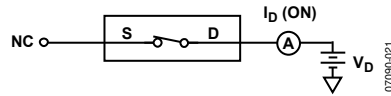


Figure 18. On Leakage

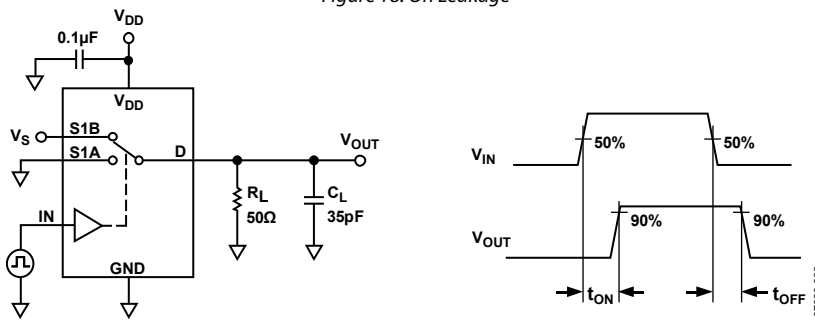


Figure 19. Switching Times, t_{ON} , t_{OFF}

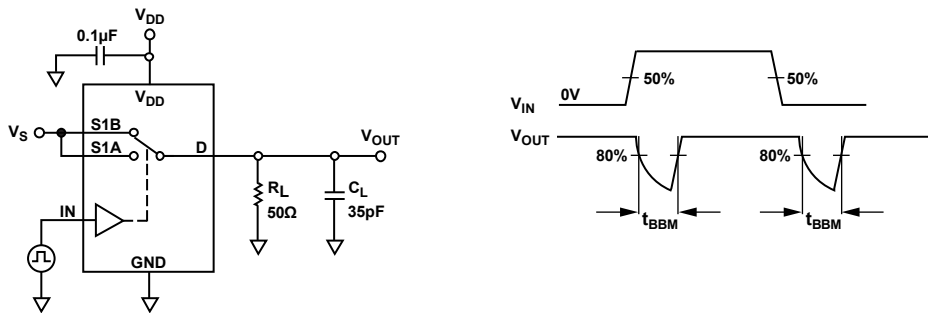


Figure 20. Break-Before-Make Time Delay, t_{BBM}

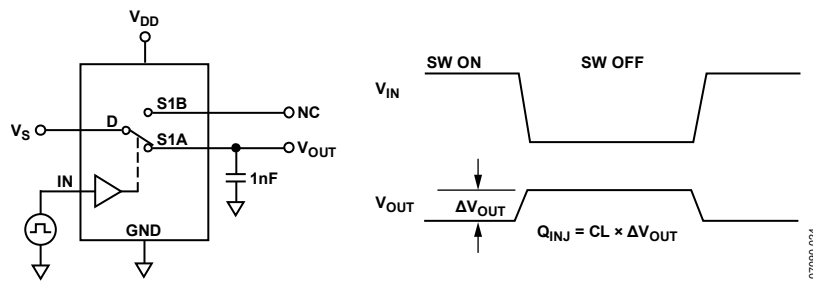
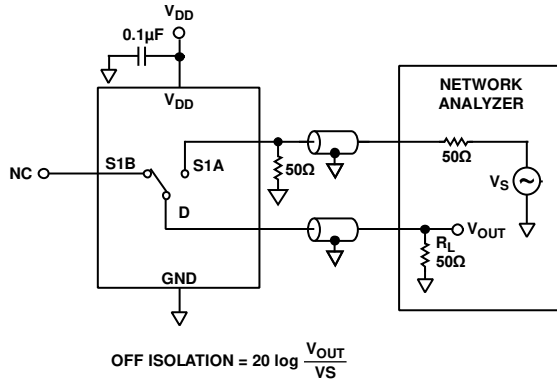
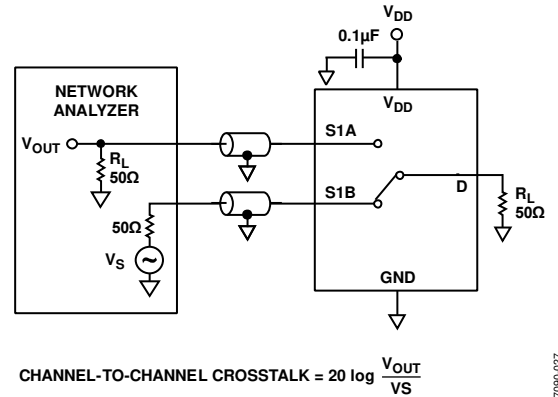


Figure 21. Charge Injection



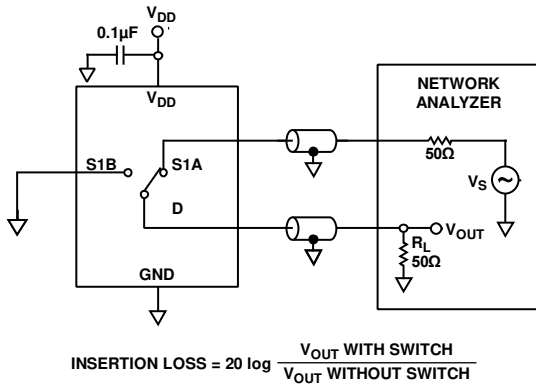
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Figure 22. Off Isolation



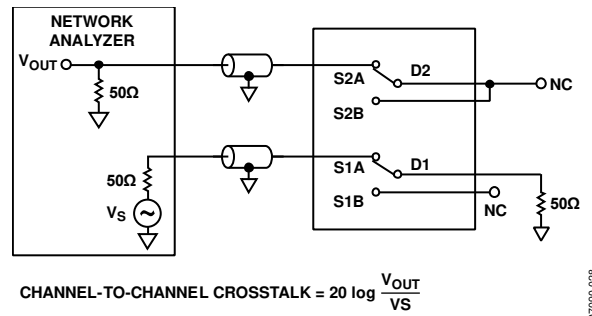
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Figure 24. Channel-to-Channel Crosstalk (S1A to S1B)



07090-026

Figure 23. Bandwidth



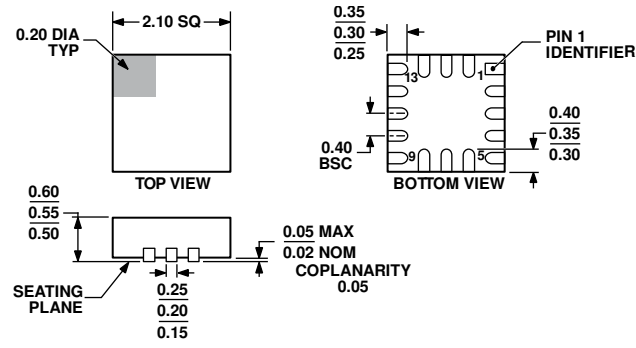
07090-028

Figure 25. Channel-to-Channel Crosstalk (S1A to S2A)

TERMINOLOGY

I_{DD} Positive supply current.	C_D, C_S (On) On switch capacitance. Measured with reference to ground.
V_D (V_S) Analog voltage on Terminal D and Terminal S.	C_{IN} Digital input capacitance.
R_{ON} Ohmic resistance between Terminal D and Terminal S.	t_{ON} Delay time between the 50% and 90% points of the digital input and switch on condition.
R_{FLAT (ON)} The difference between the maximum and minimum values of on resistance as measured on the switch.	t_{OFF} Delay time between the 50% and 90% points of the digital input and switch off condition.
ΔR_{ON} On resistance match between any two channels.	t_{BEM} On or off time measured between the 80% points of both switches when switching from one to another.
I_S (Off) Source leakage current with the switch off.	Charge Injection Measure of the glitch impulse transferred from the digital input to the analog output during on/off switching.
I_D (Off) Drain leakage current with the switch off.	Off Isolation Measure of unwanted signal coupling through an off switch.
I_D, I_S (On) Channel leakage current with the switch on.	Crosstalk Measure of unwanted signal that is coupled from one channel to another because of parasitic capacitance.
V_{INL} Maximum input voltage for Logic 0.	–3 dB Bandwidth Frequency at which the output is attenuated by 3 dB.
V_{INH} Minimum input voltage for Logic 1.	On Response Frequency response of the on switch.
I_{INL} (I_{INH}) Input current of the digital input.	Insertion Loss The loss due to the on resistance of the switch.
C_S (Off) Off switch source capacitance. Measured with reference to ground.	THD + N Ratio of the harmonics amplitude plus noise of a signal to the fundamental.
C_D (Off) Off switch drain capacitance. Measured with reference to ground.	

OUTLINE DIMENSIONS



061308-0

Figure 26. 16-Lead Lead Frame Chip Scale Package [LFCSP_UQ]
 2.10 mm × 2.10 mm Body, Ultra Thin Quad
 (CP-16-15)
 Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADG858BCPZ-REEL7 ¹	-40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_UQ]	CP-16-15	11

¹ Z = RoHS Compliant Part.

NOTES

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