

N-channel 600 V, 4 Ω typ., 0.6 A MDmesh™ K3 Power MOSFET in a TO-92 package

Datasheet - production data

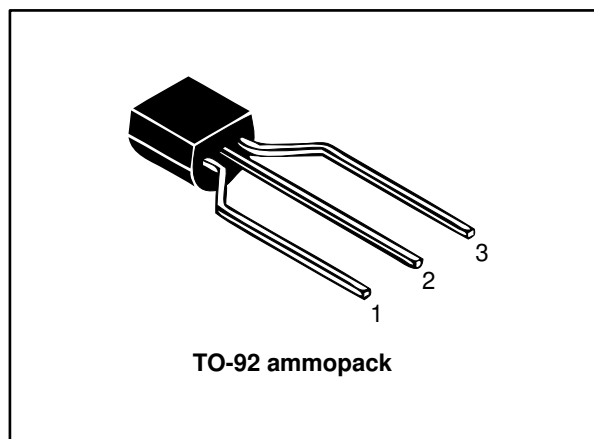
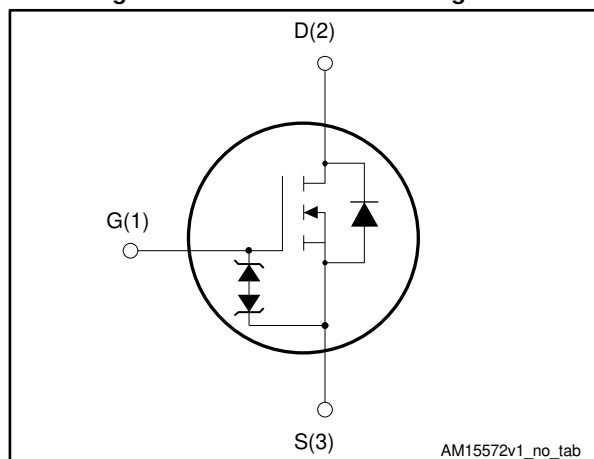


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	I _D	P _{TOT}
STQ2LN60K3-AP	600 V	4.5 Ω	0.6 A	2.5 W

- 100% avalanche tested
- Extremely high dv/dt capability
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

Applications

- Switching applications

Description

This MDmesh™ K3 Power MOSFET is the result of improvements applied to STMicroelectronics' MDmesh™ technology, combined with a new optimized vertical structure. This device boasts an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering it suitable for the most demanding applications.

Table 1: Device summary

Order code	Marking	Package	Packaging
STQ2LN60K3-AP	2LN60K3	TO-92	Ampmpack

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	0.6	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	0.38	A
$I_{DM}^{(1)}$	Drain current (pulsed)	2.4	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	2.5	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	12	V/ns
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_j	Operating junction temperature range		

Notes:

⁽¹⁾Pulse width limited by safe operating area.

⁽²⁾ $I_{SD} \leq 2\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS(\text{peak})} < V_{(BR)DSS}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-case}}$	Thermal resistance junction-case	50	$^\circ\text{C}/\text{W}$
$R_{thj\text{-amb}}$	Thermal resistance junction-ambient	120	$^\circ\text{C}/\text{W}$

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AS}	Single pulse avalanche current (pulse width limited by $T_{j\text{max}}$)	2	A
E_{AS}	Single pulse avalanche energy (starting $T_J=25\text{ }^\circ\text{C}$, $I_D=I_{AR}$, $V_{DD}=50\text{ V}$)	80	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0 V	600			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 600 V			1	μA
		V _{GS} = 0 V, V _{DS} = 600 V, T _C = 125 °C ⁽¹⁾			50	
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = ±20 V			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 50 μA	3	3.75	4.5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 1 A		4	4.5	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 50 V, f = 1 MHz, V _{GS} = 0 V	-	235	-	pF
C _{oss}	Output capacitance		-	22	-	pF
C _{rss}	Reverse transfer capacitance		-	3.5	-	pF
C _{o(tr)} ⁽¹⁾	Eq. capacitance time related	V _{GS} = 0 V, V _{DS} = 0 to 480 V	-	14	-	pF
C _{o(er)} ⁽²⁾	Eq. capacitance energy related		-	10	-	pF
Q _g	Total gate charge	V _{DD} = 480 V, I _D = 1 A, V _{GS} = 0 to 10 V (see Figure 16: "Test circuit for gate charge behavior")	-	12	-	nC
Q _{gs}	Gate-source charge		-	1.8	-	nC
Q _{gd}	Gate-drain charge		-	7.7	-	nC
R _G	Gate input resistance	f=1 MHz, I _D =0 A	-	7	-	Ω

Notes:

⁽¹⁾C_{oss eq.} time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

⁽²⁾C_{oss eq.} energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 1\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 15: "Test circuit for resistive load switching times" and Figure 20: "Switching time waveform")	-	10	-	ns
t_r	Rise time		-	8.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	23.5	-	ns
t_f	Fall time		-	21	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		0.6	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		2.4	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 2\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 2\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 17: "Test circuit for inductive load switching and diode recovery times")	-	200		ns
Q_{rr}	Reverse recovery charge		-	800		nC
I_{RRM}	Reverse recovery current		-	8		A
t_{rr}	Reverse recovery time	$I_{SD} = 2\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 17: "Test circuit for inductive load switching and diode recovery times")	-	230		ns
Q_{rr}	Reverse recovery charge		-	950		nC
I_{RRM}	Reverse recovery current		-	8.5		A

Notes:

(1)Pulse width limited by safe operating area.

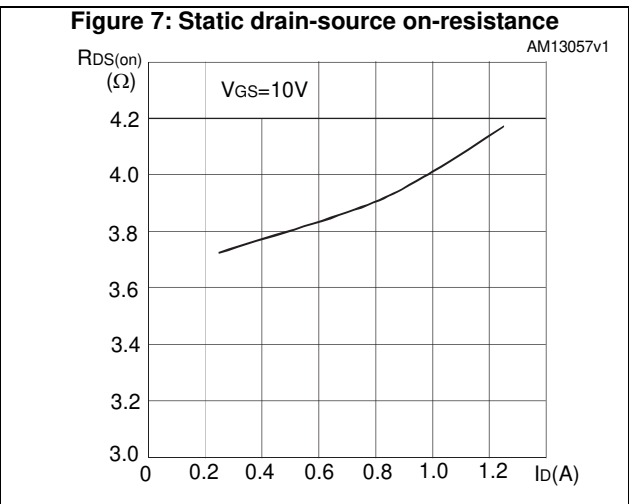
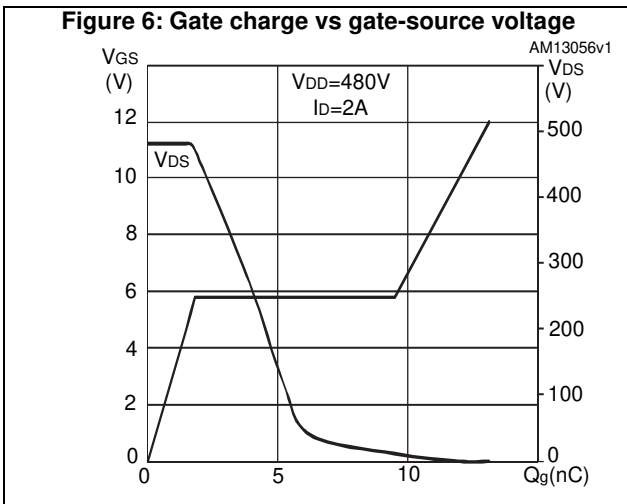
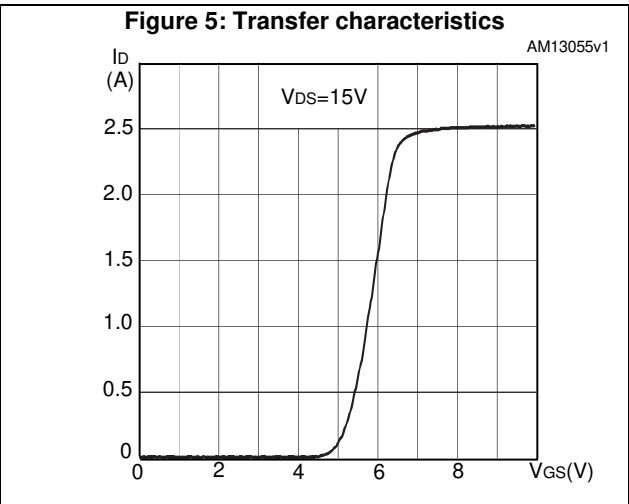
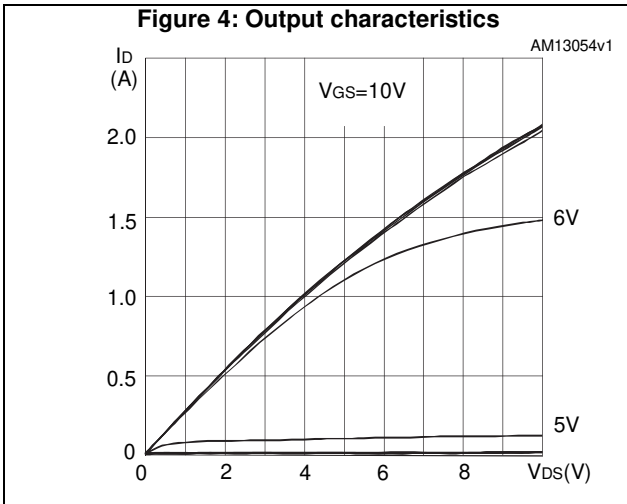
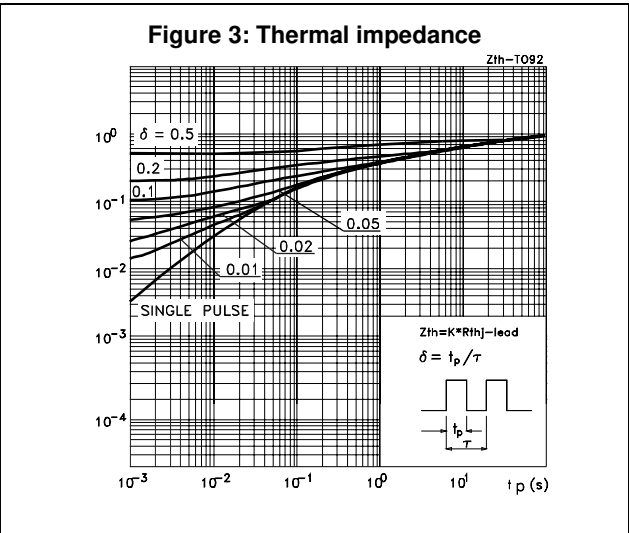
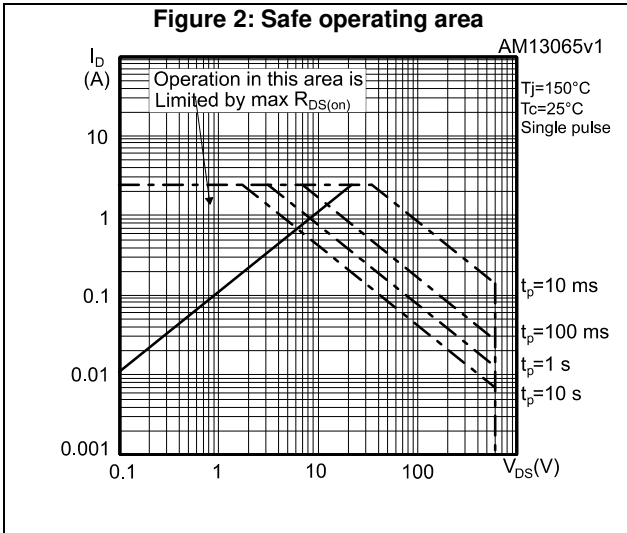
(2)Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$, $I_D = 0\text{ A}$	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)



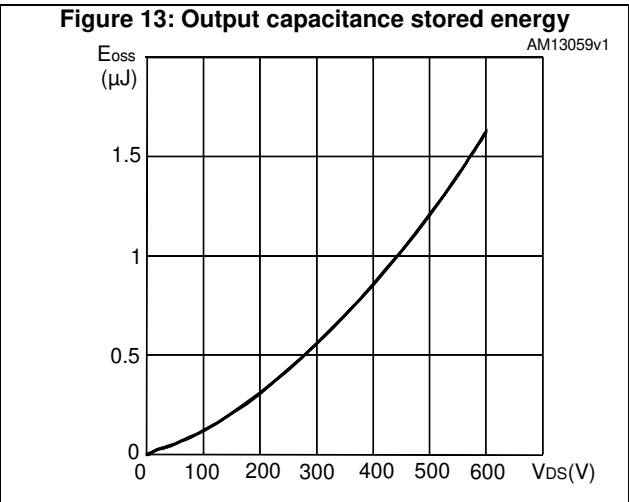
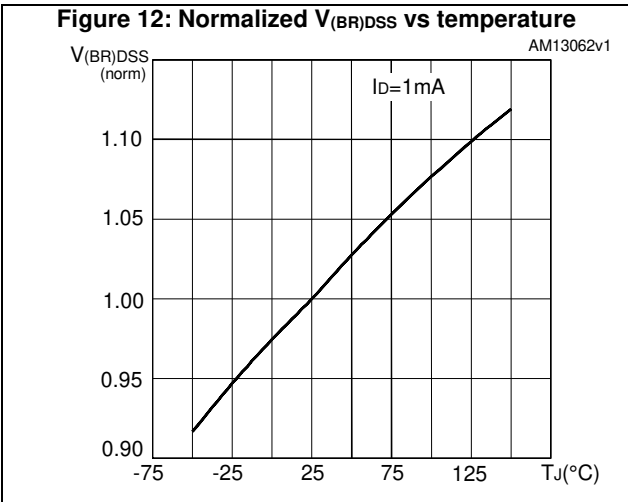
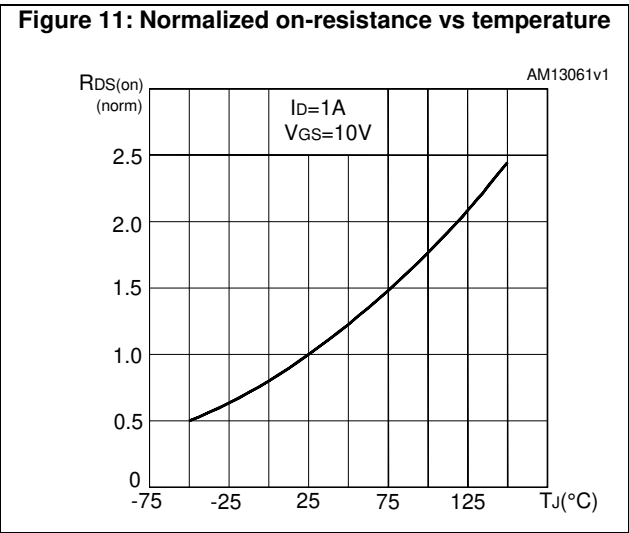
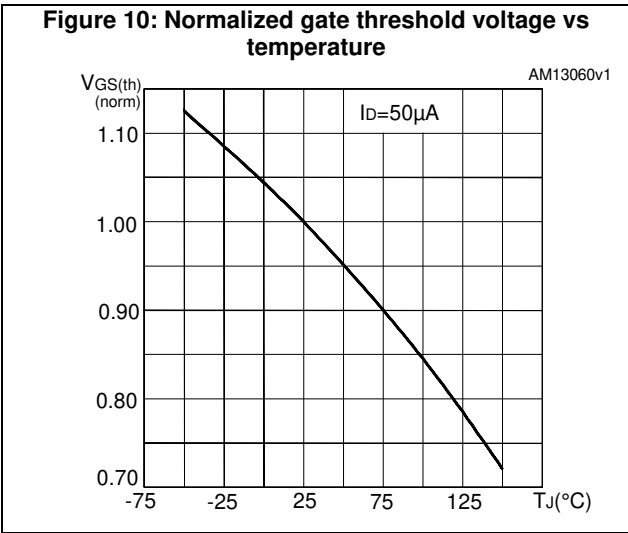
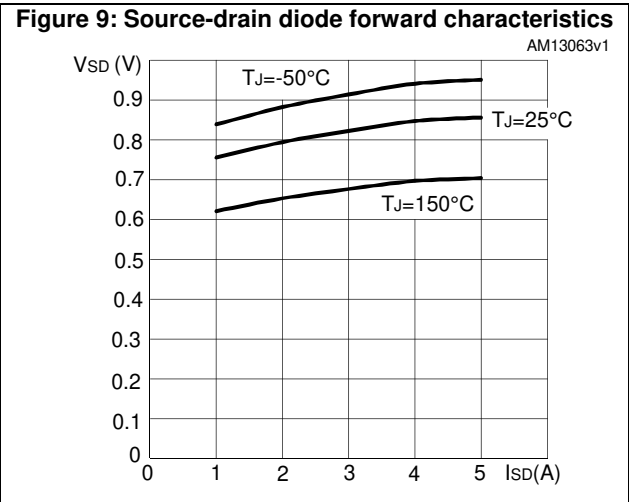
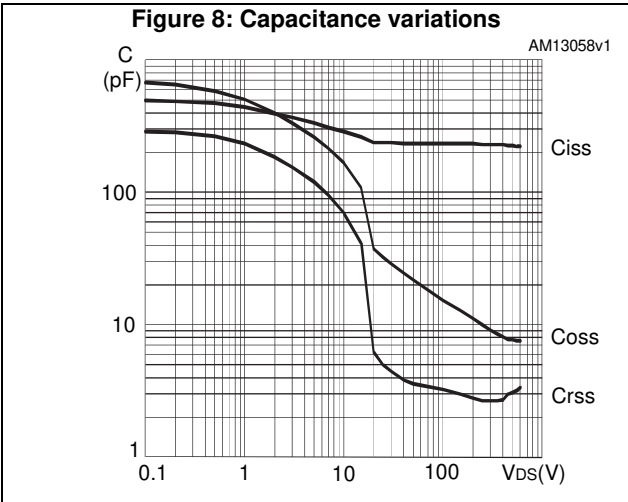
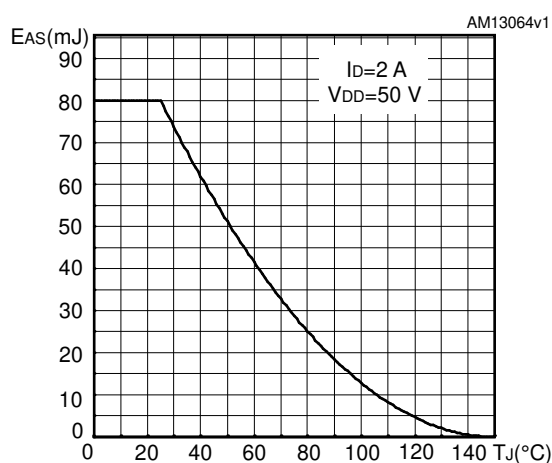
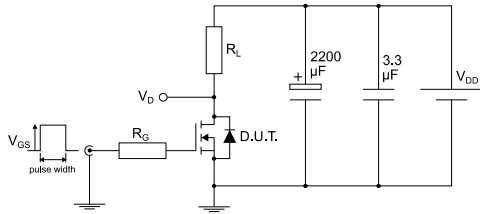


Figure 14: Maximum avalanche energy vs temperature



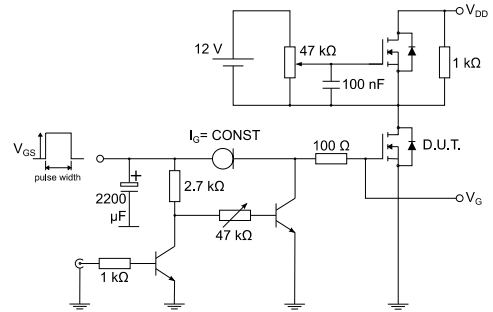
3 Test circuits

Figure 15: Test circuit for resistive load switching times



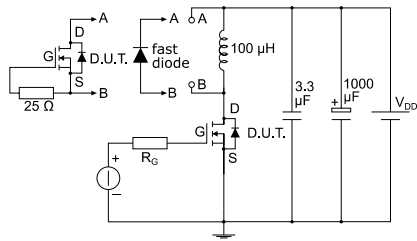
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Figure 16: Test circuit for gate charge behavior



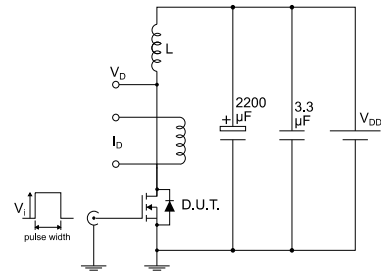
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Figure 17: Test circuit for inductive load switching and diode recovery times



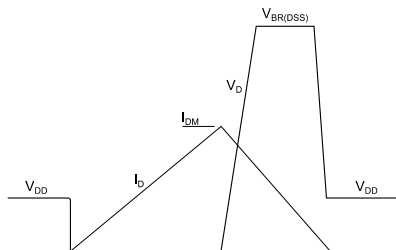
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Figure 18: Unclamped inductive load test circuit



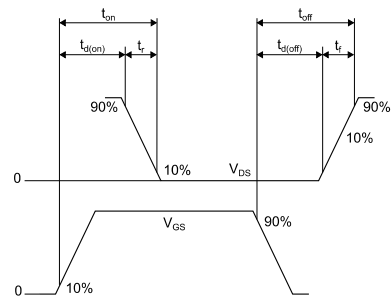
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Figure 19: Unclamped inductive waveform



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Figure 20: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-92 ammpack package information

Figure 21: TO-92 ammpack package outline

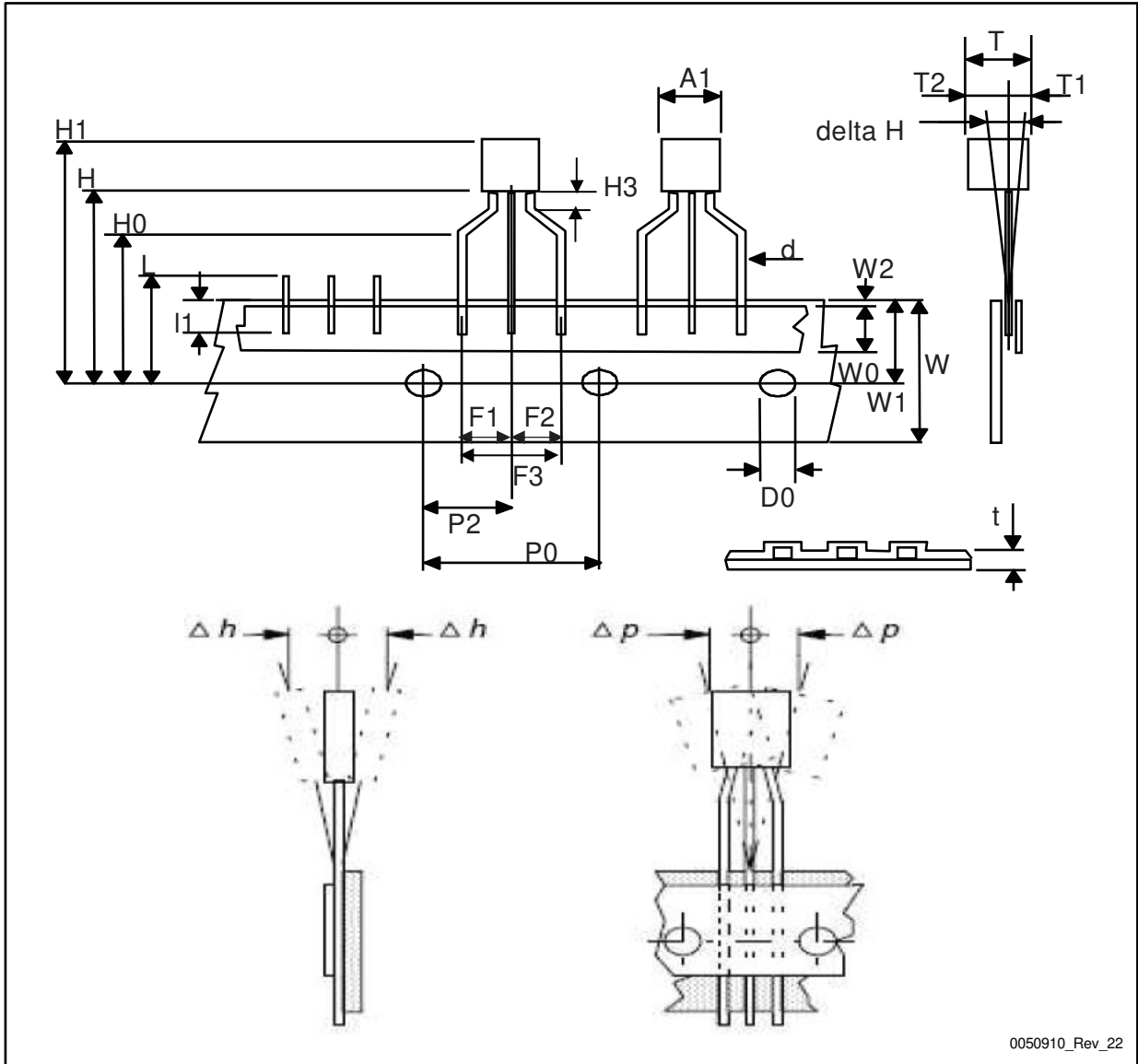


Table 10: TO-92 ammpak mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A1			4.80
T			3.80
T1			1.60
T2			2.30
d	0.45	0.47	0.48
P0	12.50	12.70	12.90
P2	5.65	6.35	7.05
F1, F2	2.40	2.50	2.94
F3	4.98	5.08	5.48
delta H	-2.00		2.00
W	17.50	18.00	19.00
W0	5.50	6.00	6.50
W1	8.50	9.00	9.25
W2			0.50
H		18.50	21.00
H0	15.50	16.00	18.20
H1		25.00	27.00
H3	0.50	1.00	2.00
D0	3.80	4.00	4.20
t			0.90
L			11.00
l1	3.00		
delta P	-1.00		1.00

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
19-Jul-2012	1	First release.
24-Jan-2017	2	Modified title, features and description on cover page Modified <i>Table 2: "Absolute maximum ratings"</i> , <i>Table 5: "On/off states"</i> and <i>Table 9: "Gate-source Zener diode"</i> Modified: <i>Figure 11: "Normalized on-resistance vs temperature"</i> Updated <i>Section 4.1: "TO-92 ammpack package information"</i> Minor text changes
01-Feb-2017	3	Modified <i>Figure 2: "Safe operating area"</i> . Minor text changes.

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