74CB3Q3257-Q100

4-bit 1-of-2 FET multiplexer/demultiplexer with charge pump

Rev. 1 — 20 February 2019 Product data sheet

1. General description

The 74CB3Q3257-Q100 is a quad high-bandwidth single-pole, double-throw FET bus switch. The device features one select input (S) and one output enable input ($\overline{OE}$). The switch is disabled when the $\overline{OE}$ input is HIGH. An internal charge-pump increases the gate voltage of the NMOS pass transistor. The result is improved R_{ON} and $R_{ON(flat)}$ performance and the ability to switch 5 V signals when V_{CC} = 3.3 V.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 3) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 3)
  - Specified from -40 °C to +85 °C
- Wide supply voltage range from 2.3 V to 3.6 V
- Overvoltage switching on switch ports:
  - 0 V to 5 V switching with V_{CC} = 2.5 V
  - 0 V to 5 V switching with V_{CC} = 3.3 V
- 4 Ω (typical) ON resistance
- 3.5 pF (typical) OFF-state capacitance
- High bandwidth 0.5 GHz (maximum)
- Low input/output capacitance minimizes loading and signal distortion
- Fast switching frequency f_{max} = 20 MHz (maximum)
- Low power consumption I_{CC} = 0.4 mA (typical)
- Control inputs can be driven by TTL or 5 V/3.3 V CMOS outputs
- I_{OFF} supports partial power-down mode operation
- Latch-up performance exceeds 100 mA per JESD 78E Class II Level A
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 2000 V
  - HBM ANSI/ESDA/Jedec JS-001 Class 2 exceeds 2 kV

3. Applications

- Communication infrastructure
- Bus isolation
- Memory interleaving
- Sensor multiplexing

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74CB3Q3257PW-Q100	-40 °C to +85 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

5. Functional diagram

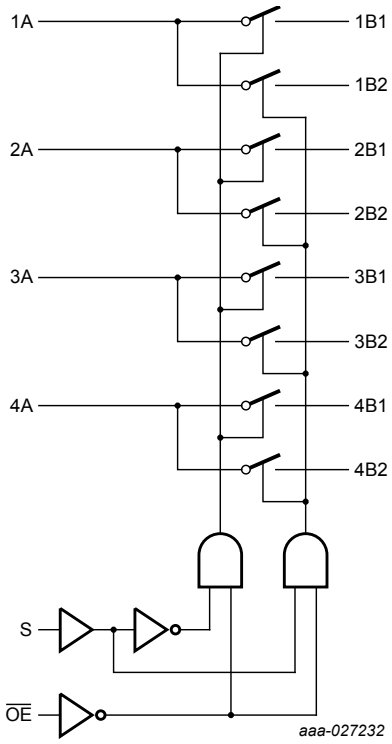


Fig. 1. Logic symbol

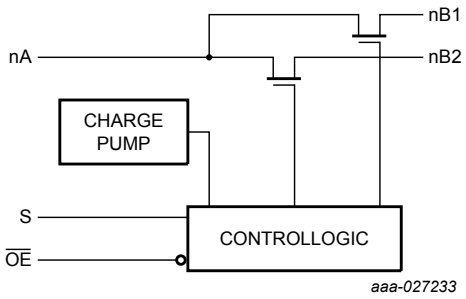


Fig. 2. Logic diagram (one switch)

6. Pinning information

6.1. Pinning

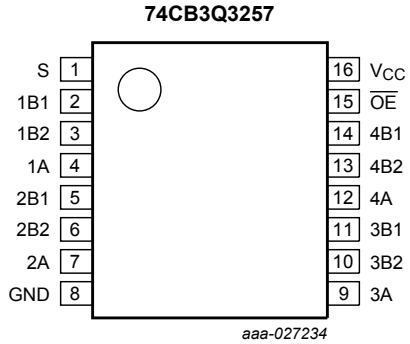


Fig. 3. Pin configuration TSSOP16 (SOT403-1)

6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
S	1	select input
1B1	2	independent input or output
1B2	3	independent input or output
1A	4	common output or input
2B1	5	independent input or output
2B2	6	independent input or output
2A	7	common output or input
GND	8	ground (0 V)
3A	9	common output or input
3B2	10	independent input or output
3B1	11	independent input or output
4A	12	common output or input
4B2	13	independent input or output
4B1	14	independent input or output
$\overline{OE}$	15	output enable input (active-LOW)
V_{CC}	16	supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Input		Channel on
S	**$\overline{OE}$**	
L	L	nA = nB1
H	L	nA = nB2
X	H	Z (switch off)

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+4.6	V
V_I	input voltage	S, $\overline{OE}$ input	[1]	-0.5	+7.0	V
V_{SW}	switch voltage		[2]	-0.5	+7.0	V
I_{IK}	input clamping current	V_I < -0.5 V		-50	-	mA
I_{SK}	switch clamping current	V_I < -0.5 V		-50	-	mA
I_{SW}	switch current			-	±120	mA
I_{CC}	supply current			-	+100	mA
I_{GND}	ground current			-100	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +85 °C	[3]	-	500	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.
[2] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed.
[3] For TSSOP16 package: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		2.3	3.6	V
V_I	input voltage	S, $\overline{OE}$ input	0	5.5	V
V_{SW}	switch voltage		0	5.5	V
T_{amb}	ambient temperature		-40	+85	°C
Δt/ΔV	input transition rise and fall rate	S, $\overline{OE}$ input			
		V_{CC} = 2.3 V to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	10	ns/V

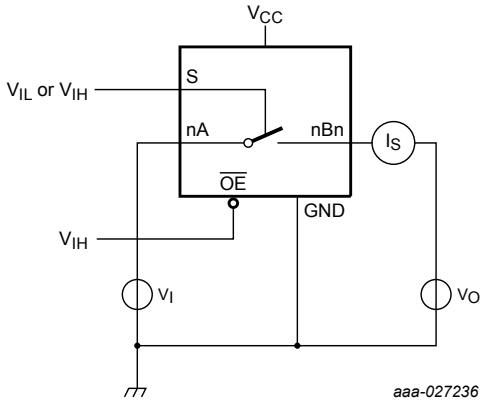
10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground 0 V).

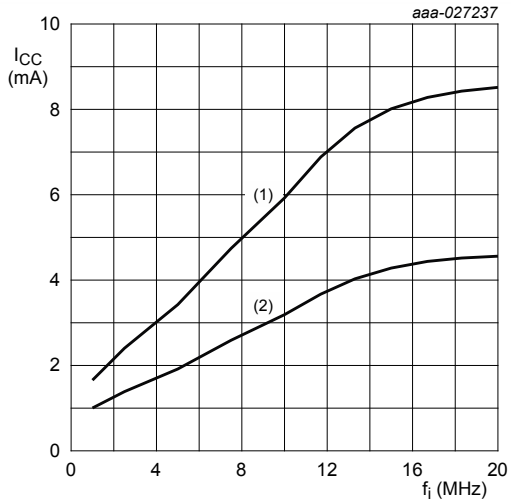
Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} =-40 °C to +85°C		Unit
			Min	Typ	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 2.3 V to 2.7 V	-	-	-	1.7	-	V
		V_{CC} = 2.7 V to 3.6 V	-	-	-	2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.3 V to 2.7 V	-	-	-	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	-	-	0.8	V
V_{IK}	input clamping voltage	nA, nBn; V_{CC} = 3.6 V; I_I = -18 mA	-	-	-	-	-1.8	V
I_I	input leakage current	S, $\overline{OE}$; V_{CC} = 3.6 V; V_I = GND to 5.5 V	-	-	-	-	±1	µA
I_{OFF}	power-off leakage current	per pin; V_{CC} = 0 V; V_{SW} or V_I = 0 V to 5.5 V	-	-	-	-	±1	µA
$I_{S(OFF)}$	OFF-state leakage current	nA, nBn; V_{CC} = 3.6 V; see Fig. 4	-	-	-	-	±1	µA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{SW} = GND or V_{CC}; V_{CC} = 3.6 V	-	0.4	-	-	0.6	mA
ΔI_{CC}	additional supply current	S, $\overline{OE}$; V_{CC} = 3.6 V; one input at 3 V, other inputs at GND or V_{CC}	-	-	-	-	30	µA
C_I	input capacitance	V_{CC} = 3.3 V; V_{SW} = GND or V_{CC}; V_I = 0 V, 3.3 V, 5.5 V						
		S, $\overline{OE}$	-	2.5	-	-	3.5	pF
$C_{S(OFF)}$	OFF-state capacitance	V_{CC} = 3.3 V; V_{SW} = 0 V, 3.3 V, 5.5 V						
		nA	-	5.5	-	-	7	pF
		nBn	-	3.5	-	-	5	pF
$C_{S(ON)}$	ON-state capacitance	V_{CC} = 3.3 V; V_{SW} = 0 V, 3.3 V, 5.5 V						
		nA, nBn	-	10.5	-	-	13	pF

10.1. Test circuit and graph



V_I = 5.5 V or GND and V_O = GND or 5.5 V

Fig. 4. Test circuit for measuring OFF-state leakage current (one channel)



T_{amb} = 25 °C; V_{CC} = 3.3 V; nA and nBn not connected.

(1) S input switching (50% duty cycle)

(2) $\overline{OE}$ input switching (50% duty cycle)

Fig. 5. Typical supply current as function of (S, $\overline{OE}$) input frequency

10.2. ON resistance

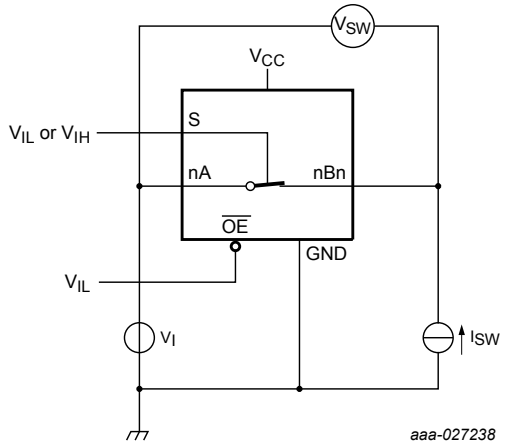
Table 7. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6.

Symbol	Parameter	Conditions		T_{amb} = 25 °C			T_{amb} = -40 °C to +85 °C		Unit
				Min	Typ	Max	Min	Max	
R_{ON}	ON resistance	V_{CC} = 2.3 V; see Fig. 7							
		V_I = 0 V; I_{SW} = 30 mA	[1]	-	4	-	-	8	Ω
		V_I = 1.7 V; I_{SW} = -15 mA	[1]	-	4.4	-	-	9	Ω
		V_{CC} = 3.0 V; see Fig. 7							
		V_I = 0 V; I_{SW} = 30 mA	[2]	-	4	-	-	6	Ω
		V_I = 2.4 V; I_{SW} = -15 mA	[2]	-	4.7	-	-	8	Ω

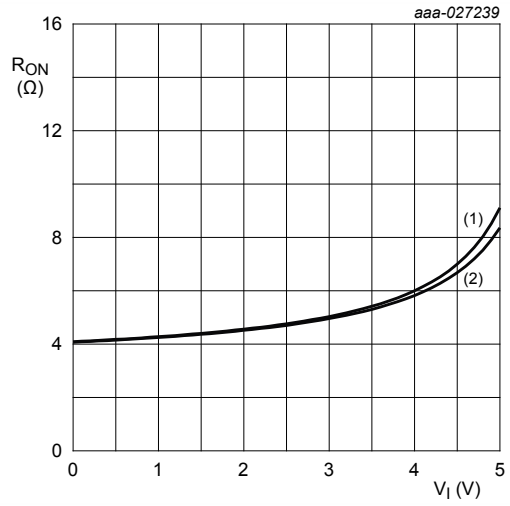
[1] Typical values are measured at V_{CC} = 2.5 V.
[2] Typical values are measured at V_{CC} = 3.3 V.

10.3. ON resistance test circuit and graph



$R_{ON} = V_{SW} / I_{SW}$

Fig. 6. Test circuit for measuring ON resistance (one channel)



T_{amb} = 25 °C
(1) V_{CC} = 2.5 V
(2) V_{CC} = 3.3 V

Fig. 7. Typical ON resistance as a function of input voltage

11. Dynamic characteristics

Table 8. Dynamic characteristics

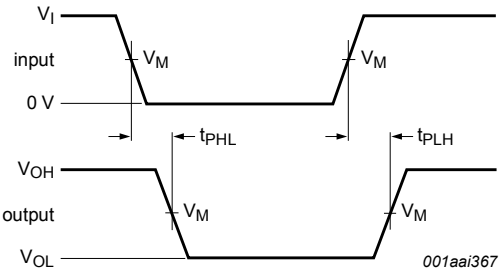
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit, see Fig. 10.

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +85 °C		Unit
			Min	Max	
t_{pd}	propagation delay	nA to nBn or nBn to nA; see Fig. 8 [1] [2]			
		V_{CC} = 2.3 V to 2.7 V	-	0.12	ns
		V_{CC} = 3.0 V to 3.6 V	-	0.20	ns
		S to nA; see Fig. 8 [1]			
		V_{CC} = 2.3 V to 2.7 V	1.5	6.5	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	5.5	ns
t_{en}	enable time	$\overline{OE}$ to nA, nBn; see Fig. 9 [3]			
		V_{CC} = 2.3 V to 2.7 V	1.5	6.5	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	5.5	ns
		S to nBn; see Fig. 9 [3]			
		V_{CC} = 2.3 V to 2.7 V	1.5	6.5	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	5.5	ns

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +85 °C		Unit
			Min	Max	
t_{dis}	disable time	$\overline{OE}$ to nA, nBn; see Fig. 9 [4]			
		V_{CC} = 2.3 V to 2.7 V	1.0	6.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	6.0	ns
		S to nBn; see Fig. 9 [4]			
		V_{CC} = 2.3 V to 2.7 V	1.0	6.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	6.0	ns
f_{max}	maximum frequency	S, $\overline{OE}$; $V_O > V_{CC}$; V_I = 5 V; $R_L \geq 1$ MΩ; C_L = 0 pF			
		V_{CC} = 2.3 V to 2.7 V	-	10	MHz
		V_{CC} = 3.0 V to 3.6 V	-	20	MHz

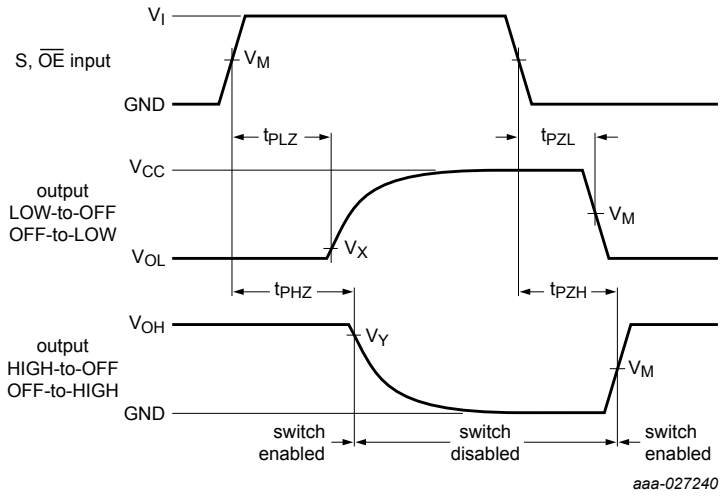
[1] t_{pd} is the same as t_{PLH} and t_{PHL}.
[2] The propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
[3] t_{en} is the same as t_{PZL} and t_{PZH}.
[4] t_{dis} is the same as t_{PLZ} and t_{PHZ}.

11.1. Waveforms and test circuit



Measurement points are given in Table 9.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 8. The data input (nA or nBn) to output (nBn or nA) propagation delays

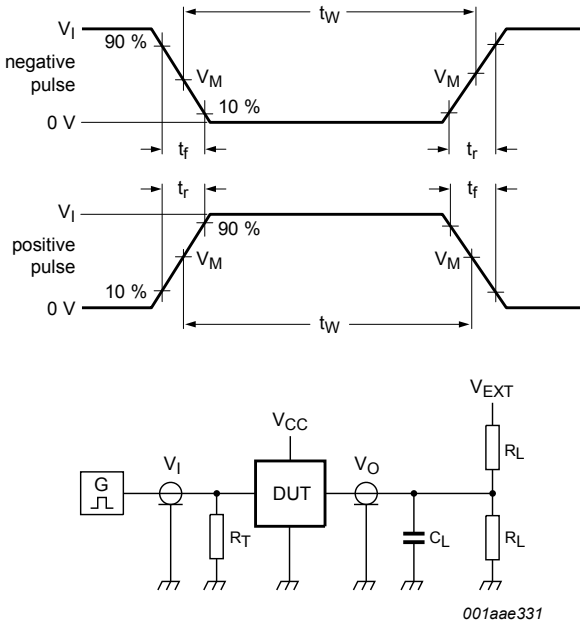


Measurement points are given in Table 9.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 9. Enable and disable times

Table 9. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
2.3 V to 2.7 V	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.15 V	V_{OH} - 0.15 V
3.0 V to 3.6 V	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 10.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

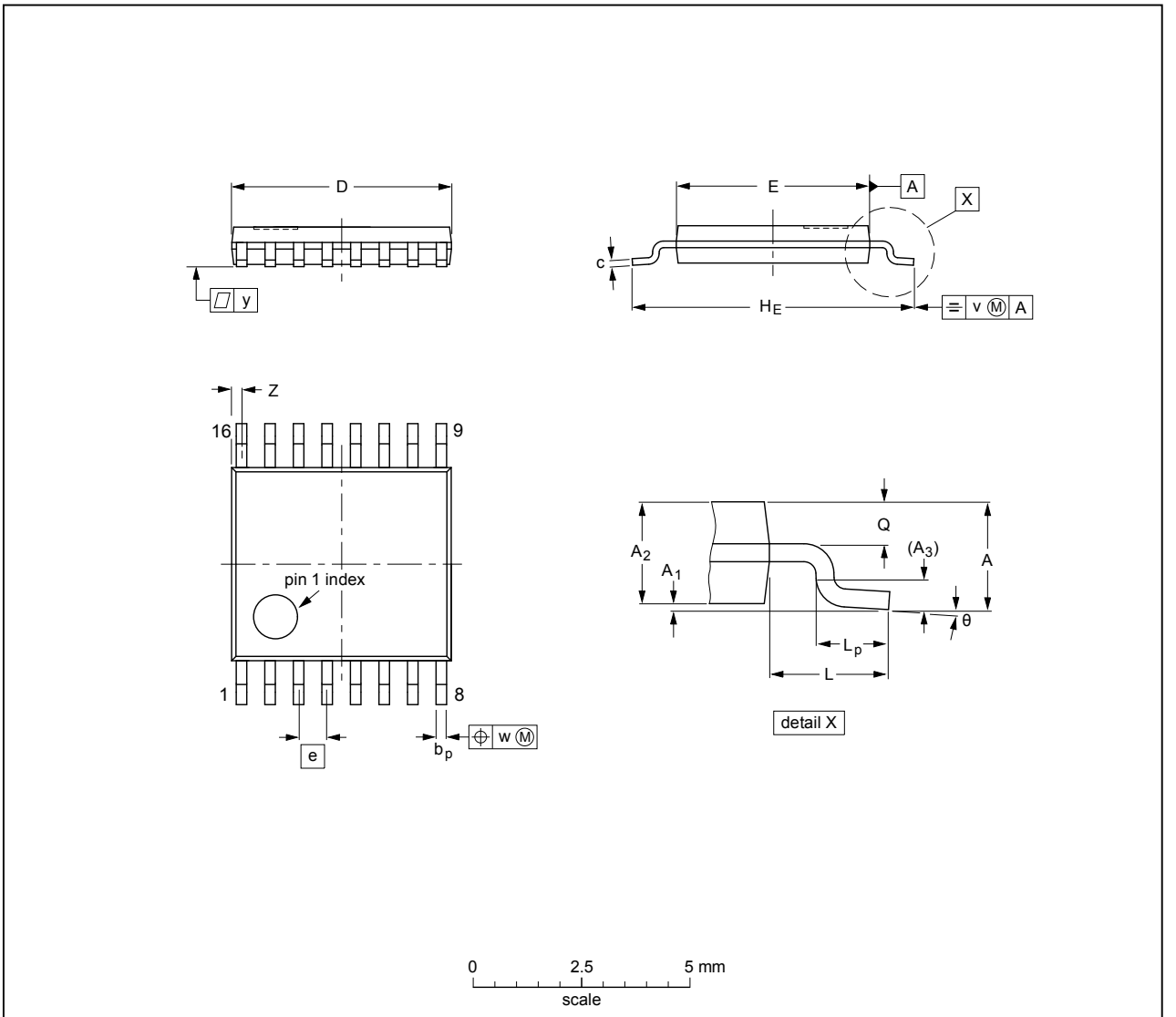
Fig. 10. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PZH}, t_{PHZ}
2.3 V to 2.7 V	V_{CC}	≤ 2.5 ns	30 pF	500 Ω	open	2 × V_{CC}	GND
3.0 V to 3.6 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open	2 × V_{CC}	GND

12. Package outline

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig. 11. Package outline SOT403-1 (TSSOP16)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74CB3Q3257_Q100 v.1	20190220	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Date of release: 20 February 2019