GaAs, pHEMT, Low Noise Amplifier, 18 GHz to 54 GHz

FEATURES

- Integrated power supply capacitors and bias inductors
- Integrated ac-coupling capacitors
- Gain: 21.5 dB typical at 30 GHz to 44 GHz
- Input return loss: 12.5 dB typical at 30 GHz to 44 GHz
- Output return loss: 19 dB typical at 30 GHz to 44 GHz
- OP1dB: 14.5 dB typical at 30 GHz to 44 GHz
- P_{SAT}: 19 dBm typical at 30 GHz to 44 GHz
- OIP3: 21.5 dBm typical at 30 GHz to 44 GHz
- Noise figure: 3.5 dB typical at 30 GHz to 44 GHz
- 3 V typical supply voltage at 120 mA
- 50 Ω matched input and output
- 24-terminal, 5.00 mm × 5.00 mm, chip array small outline no lead cavity [LGA_CAV]

APPLICATIONS

- Test instrumentation
- Military and space

GENERAL DESCRIPTION

The ADL8106 is a gallium arsenide (GaAs), pseudomorphic high electron mobility transfer (pHEMT), monolithic microwave integrated circuit (MMIC), wideband low noise amplifier that operates from 18 GHz to 54 GHz. All the typically required external passive components for operation (ac coupling capacitors and power supply decoupling capacitors) are integrated, which facilitates a small and compact printed circuit board (PCB) footprint.

The ADL8106 provides a gain of 21.5 dB, an output power for 1 dB compression (OP1dB) of 14.5 dBm, and a typical output third-order intercept (OIP3) of 21.5 dBm at 30 GHz to 44 GHz. The ADL8106 requires 120 mA from a 3 V supply voltage (V_{DDx}). The ADL8106 is housed in a 5.00 mm × 5.00 mm, 24-terminal chip array small outline no lead cavity (LGA_CAV) package.

FUNCTIONAL BLOCK DIAGRAM

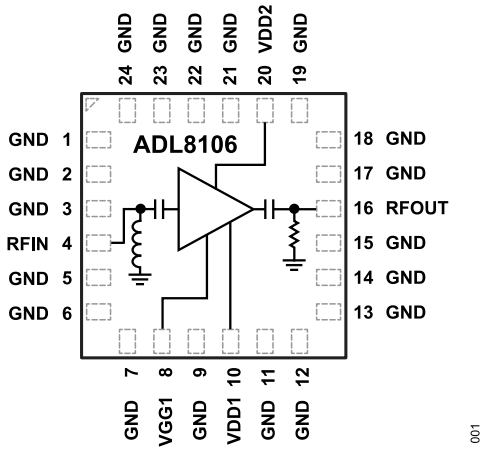

Figure 1. Functional Block Diagram

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8/2022—Revision 0: Initial Version

ELECTRICAL SPECIFICATIONS

18 GHZ TO 20 GHZ FREQUENCY RANGE

T_{CASE} = 25°C, VDD1 drain bias voltage (V_{DD1}) = VDD2 drain bias voltage (V_{DD2}) = 3 V, and quiescent drain current (I_{DQ}) = 120 mA, unless otherwise stated. Adjust the negative gate bias voltage (V_{GG1}) between −2 V to 0 V to achieve an I_{DQ} = 120 mA typical.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	18		20	GHz	
GAIN		18.5		dB	
Gain Variation over Temperature		0.028		dB/°C	
RETURN LOSS					
Input		16		dB	
Output		16.5		dB	
OUTPUT					
OP1dB		11.5		dBm	
Saturated Power (P_{SAT})		14.5		dBm	
OIP3		17.5		dBm	Output power (P_{OUT}) per tone = 0 dBm with 1 MHz tone spacing
Second-Order Intercept (OIP2)		15		dBm	P_{OUT} per tone = 0 dBm with 1 MHz tone spacing
NOISE FIGURE		4		dB	
SUPPLY					
I_{DQ}		120		mA	Adjust V_{GG1} to achieve I_{DQ} = 120 mA typical
V_{DD}	2	3	3.5	V	

20 GHZ TO 30 GHZ FREQUENCY RANGE

T_{CASE} = 25°C, V_{DD1} = V_{DD2} = 3 V, and I_{DQ} = 120 mA, unless otherwise stated. Adjust the V_{GG1} between −2 V to 0 V to achieve an I_{DQ} = 120 mA typical.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	20		30	GHz	
GAIN	17.5	20		dB	
Gain Variation over Temperature		0.028		dB/°C	
RETURN LOSS					
Input		13		dB	
Output		15.5		dB	
OUTPUT					
OP1dB	12	14		dBm	
P_{SAT}		17		dBm	
OIP3		21		dBm	P_{OUT} per tone = 0 dBm with 1 MHz tone spacing
OIP2		24		dBm	P_{OUT} per tone = 0 dBm with 1 MHz tone spacing
NOISE FIGURE		3.0		dB	
SUPPLY					
I_{DQ}		120		mA	Adjust V_{GG1} to achieve I_{DQ} = 120 mA typical
V_{DD}	2	3	3.5	V	

ELECTRICAL SPECIFICATIONS

30 GHZ TO 44 GHZ FREQUENCY RANGE

T_{CASE} = 25°C, V_{DD1} = V_{DD2} = 3 V, and I_{DQ} = 120 mA, unless otherwise stated. Adjust V_{GG1} between −2 V to 0 V to achieve an I_{DQ} = 120 mA typical.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	30		44	GHz	
GAIN	19	21.5		dB	
Gain Variation over Temperature		0.028		dB/°C	
RETURN LOSS					
Input		12.5		dB	
Output		19		dB	
OUTPUT					
OP1dB	12	14.5		dBm	
P_{SAT}		19		dBm	
OIP3		21.5		dBm	P_{OUT} per tone = 0 dBm with 1 MHz tone spacing
NOISE FIGURE		3.5		dB	
SUPPLY					
I_{DQ}		120		mA	Adjust V_{GG1} to achieve I_{DQ} = 120 mA typical
V_{DD}	2	3	3.5	V	

44 GHZ TO 50 GHZ FREQUENCY RANGE

T_{CASE} = 25°C, V_{DD1} = V_{DD2} = 3 V, and I_{DQ} = 120 mA, unless otherwise stated. Adjust V_{GG1} between −2 V to 0 V to achieve an I_{DQ} = 120 mA typical.

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	44		50	GHz	
GAIN		22		dB	
Gain Variation over Temperature		0.031		dB/°C	
RETURN LOSS					
Input		15		dB	
Output		18		dB	
OUTPUT					
OP1dB		16.5		dBm	
P_{SAT}		20.5		dBm	
OIP3		22		dBm	P_{OUT} per tone = 0 dBm with 1 MHz tone spacing
NOISE FIGURE		4		dB	
SUPPLY					
I_{DQ}		120		mA	Adjust V_{GG1} to achieve I_{DQ} = 120 mA typical
V_{DD}	2	3	3.5	V	

ELECTRICAL SPECIFICATIONS

50 GHZ TO 54 GHZ FREQUENCY RANGE

T_{CASE} = 25°C, V_{DD1} = V_{DD2} = 3 V, and I_{DQ} = 120 mA, unless otherwise stated. Adjust V_{GG1} between −2 V to 0 V to achieve an I_{DQ} = 120 mA typical.

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	50		54	GHz	
GAIN		20.5		dB	
Gain Variation over Temperature		0.031		dB/°C	
RETURN LOSS					
Input		15		dB	
Output		14.5		dB	
OUTPUT					
OP1dB		19		dBm	
P_{SAT}		20		dBm	
OIP3		23		dBm	P_{OUT} per tone = 0 dBm with 1 MHz tone spacing
NOISE FIGURE		4		dB	
SUPPLY					
I_{DQ}		120		mA	Adjust V_{GG1} to achieve I_{DQ} = 120 mA typical
V_{DD}	2	3	3.5	V	

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Drain Bias Voltage (V_{DD1} and V_{DD2})	4 V
Negative Gate Bias Voltage (V_{GG1})	−2.1 V to 0 V
RF Input Power (RFIN)	17 dBm
Continuous Power Dissipation (P_{DISS}), T_{CASE} = 85°C (Derate 16.6 mW/°C Above 85°C)	1.49 W
Temperature	
Storage Range	−55°C to +150°C
Operating Range	−40°C to +85°C
Quiescent Channel (T_{CASE} = 85°C, V_{DDx} = 3 V, I_{DQ} = 120 mA, Input Power (P_{IN}) = Off)	106.7°C
Maximum Channel	175°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to system design and operating environment. Careful attention to the PCB thermal design is required.

θ_{JC} is the channel-to-case thermal resistance (channel to exposed metal ground pad on the underside of the device).

Table 7. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
CE-24-2	60.3	°C/W

[1] Thermal resistance (θ_{JC}) was determined by simulation under the following conditions: the heat transfer is due solely to thermal conduction from the channel through the ground paddle to the PCB, and the ground paddle is held constant at the operating temperature of 85°C.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of EDS-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADL8106

Table 8. ADL8106, 24-Terminal LGA_CAV

ESD Model	Withstand Threshold (V)	Class
HBM	±300	1A

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

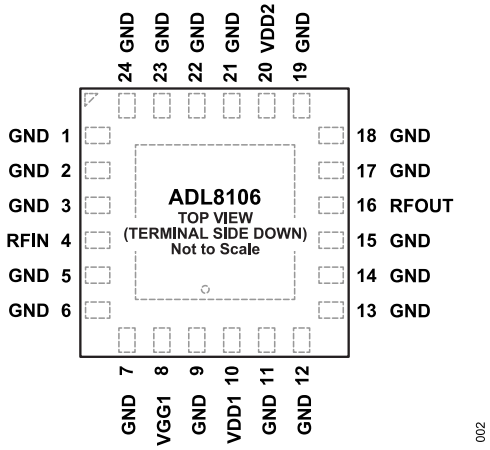

Figure 2. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 3, 5, 6, 7, 9, 11, 12, 13, 14, 15, 17, 18, 19, 21, 22, 23, 24	GND	Ground. Connect to a ground plane that has low electrical and thermal impedance. See Figure 3 for the interface schematic.
4	RFIN	RF Input. The RFIN pin has a dc path to ground followed by an ac coupling capacitor in the RF signal path. If the dc bias level of the input signal is not equal to 0 V, externally ac-couple the RFIN pin. See Figure 4 for the interface schematic.
8	VGG1	Negative Gate Bias Control. The gate voltage can be applied to VGG1. Adjust the negative voltage on the VGG1 pin to set the I_{DQ} to the desired level. See Figure 5 for the interface schematic.
10, 20	VDD1, VDD2	Drain Bias Pads with Integrated RF Chokes. Connect a common dc bias to the VDDx pads to provide drain current. See Figure 6 for the interface schematic.
16	RFOUT	RF Output. The RFOUT pin has a resistive path to ground and an ac coupling capacitor in the RF signal path. If the dc bias level of the next stage is not equal to 0 V, externally ac-couple the RFOUT pin. See Figure 6 for the interface schematic.

INTERFACE SCHEMATICS

Figure 3. GND Interface Schematic

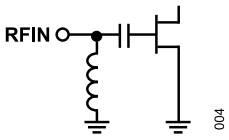

Figure 4. RFIN Interface Schematic

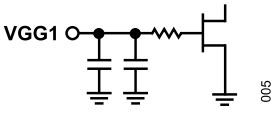

Figure 5. VGG1 Interface Schematic

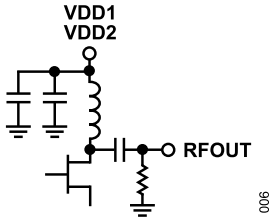

Figure 6. VDD1, VDD2, and RFOUT Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

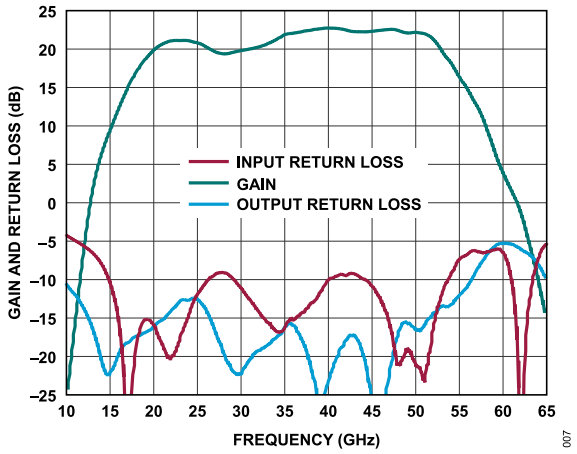

Figure 7. Gain and Return Loss vs. Frequency, V_{DD} = 3 V, I_{DQ} = 120 mA

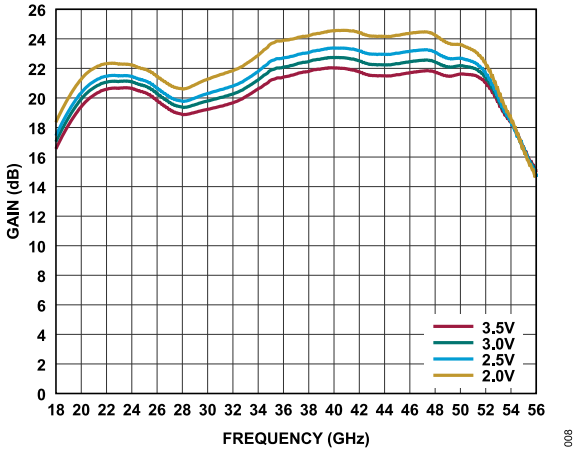

Figure 8. Gain vs. Frequency for Various V_{DD} Values, I_{DQ} = 120 mA

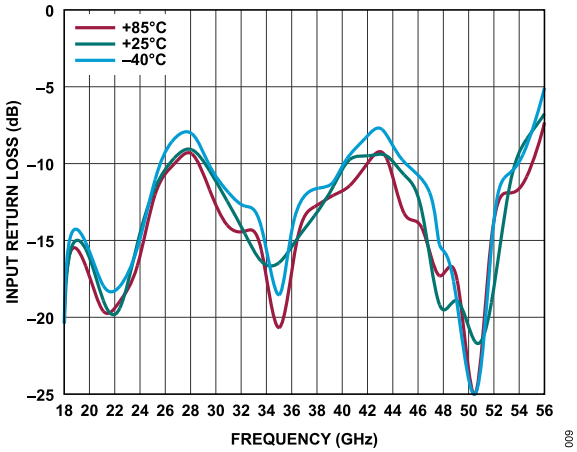

Figure 9. Input Return Loss vs. Frequency for Various Temperatures, V_{DD} = 3 V, I_{DQ} = 120 mA

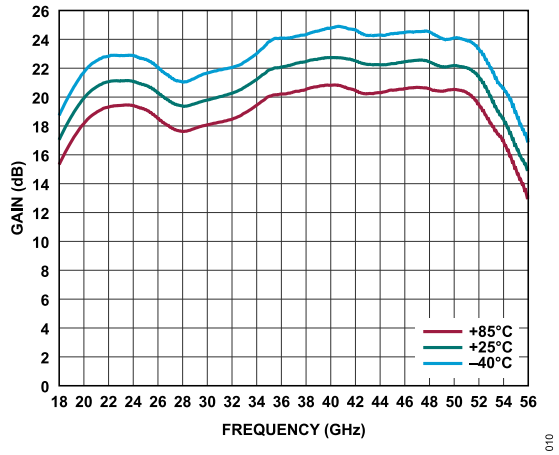

Figure 10. Gain vs. Frequency for Various Temperatures, V_{DD} = 3 V, I_{DQ} = 120 mA

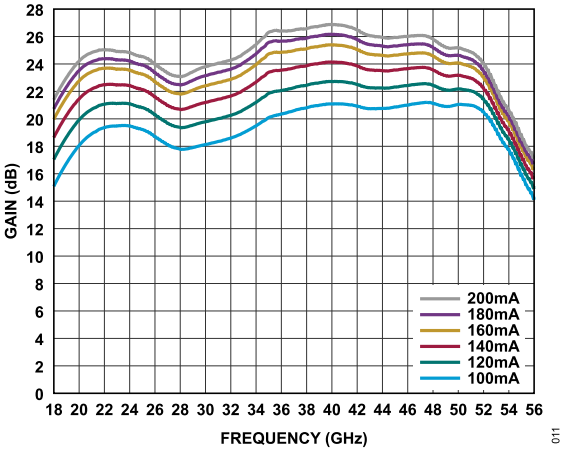

Figure 11. Gain vs. Frequency for Various I_{DQ} Values, V_{DD} = 3 V

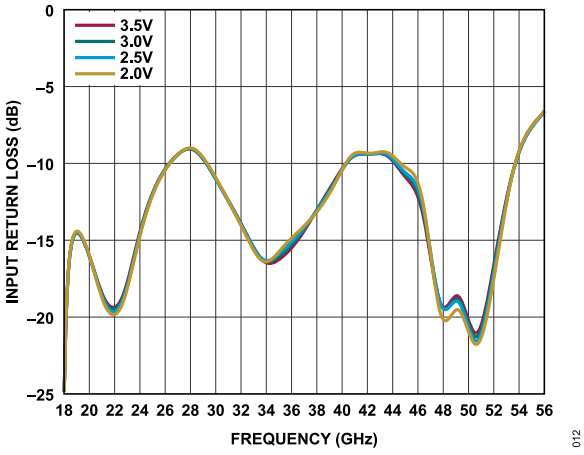

Figure 12. Input Return Loss vs. Frequency for Various V_{DD} Values, I_{DQ} = 120 mA

TYPICAL PERFORMANCE CHARACTERISTICS

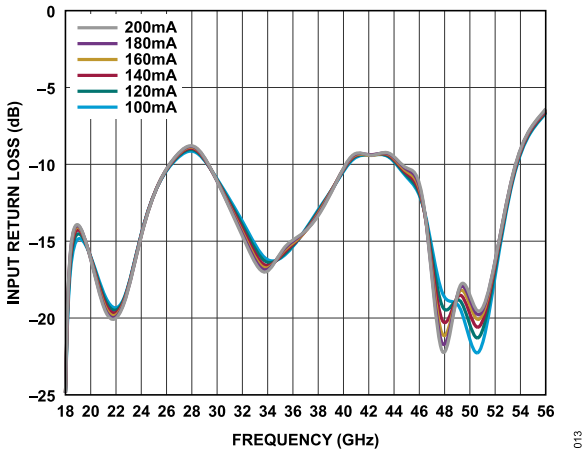

Figure 13. Input Return Loss vs. Frequency for Various I_{DQ} Values, V_{DD} = 3 V

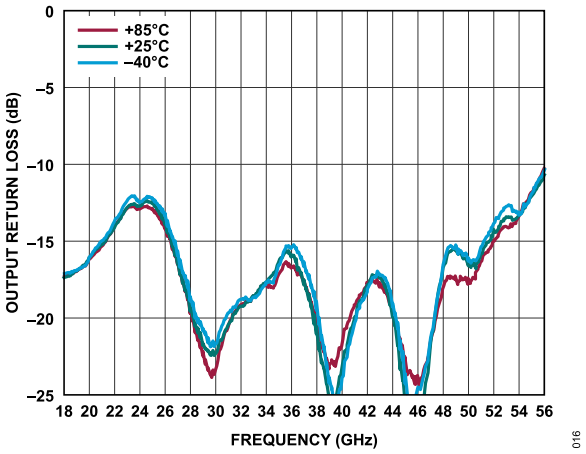

Figure 16. Output Return Loss vs. Frequency for Various Temperatures, V_{DD} = 3 V, I_{DQ} = 120 mA

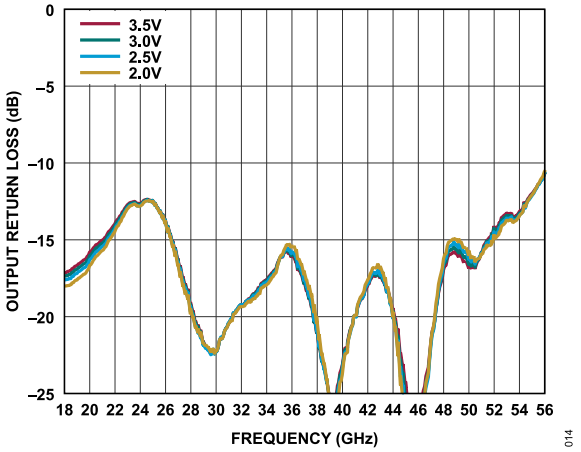

Figure 14. Output Return Loss vs. Frequency for Various V_{DD} Values, I_{DQ} = 120 mA

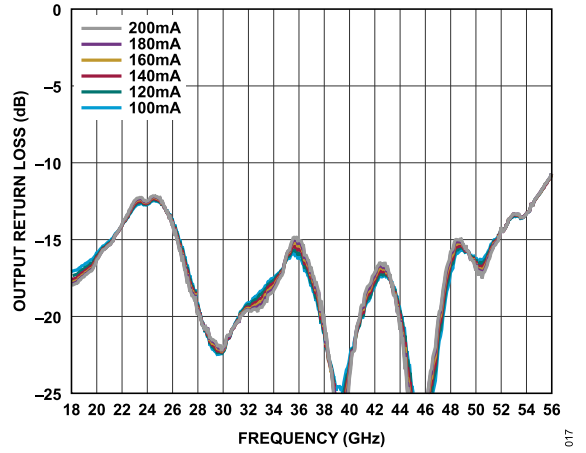

Figure 17. Output Return Loss vs. Frequency for Various I_{DQ} Values, V_{DD} = 3 V

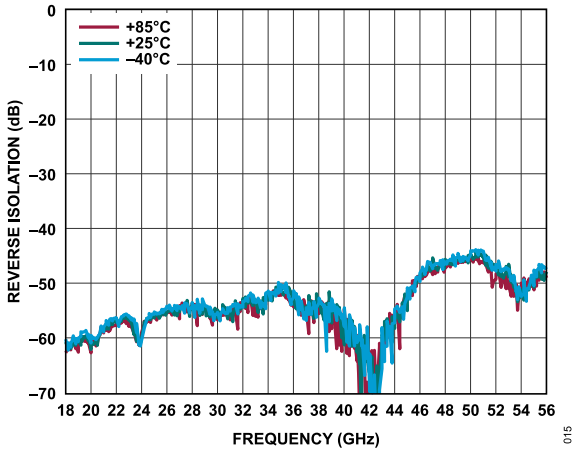

Figure 15. Reverse Isolation vs. Frequency for Various Temperatures, V_{DD} = 3 V, I_{DQ} = 120 mA

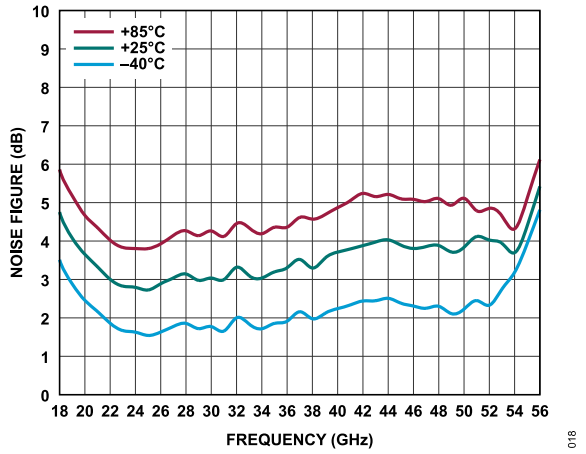

Figure 18. Noise Figure vs. Frequency for Various Temperatures, V_{DD} = 3 V, I_{DQ} = 120 mA

TYPICAL PERFORMANCE CHARACTERISTICS

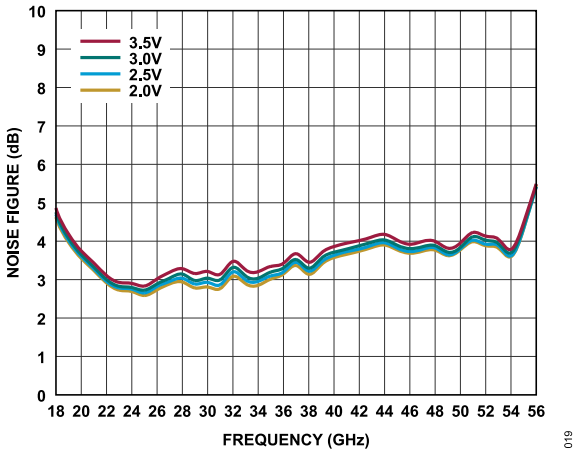

Figure 19. Noise Figure vs. Frequency for Various V_{DD} Values, I_{DQ} = 120 mA

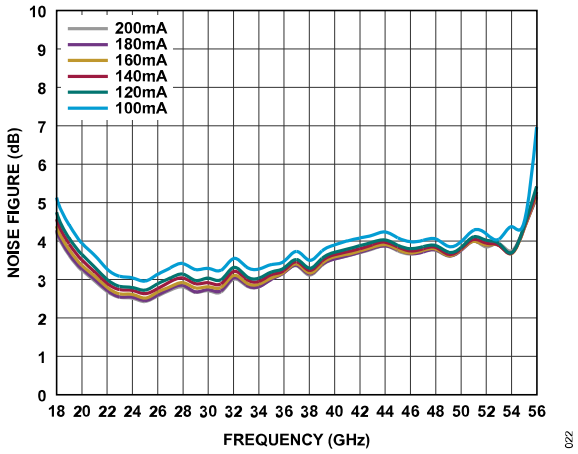

Figure 22. Noise Figure vs. Frequency for Various I_{DQ} Values, V_{DD} = 3 V

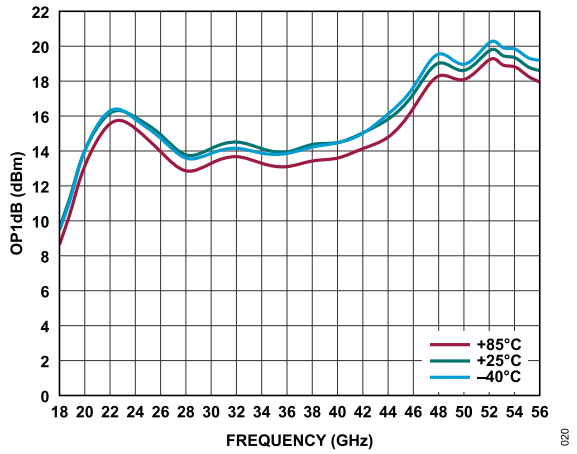

Figure 20. OP1dB vs. Frequency for Various Temperatures, V_{DD} = 3 V, I_{DQ} = 120 mA

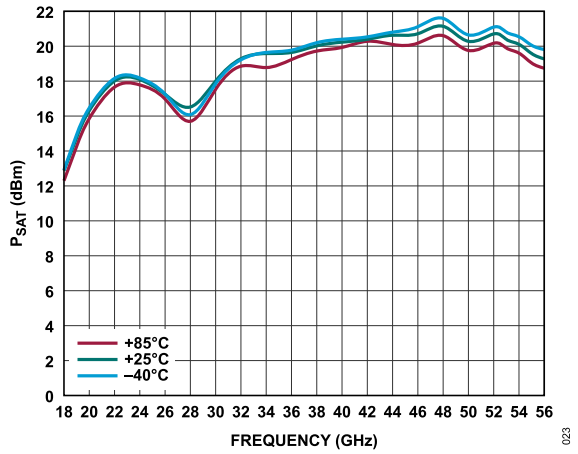

Figure 23. P_{SAT} vs. Frequency for Various Temperatures, V_{DD} = 3 V, I_{DQ} = 120 mA

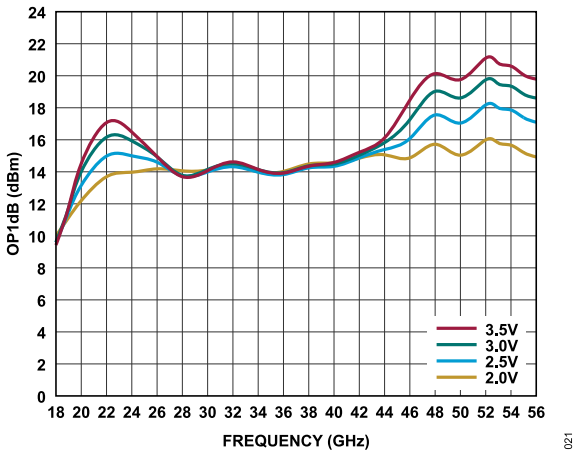

Figure 21. OP1dB vs. Frequency for Various V_{DD} Values, I_{DQ} = 120 mA

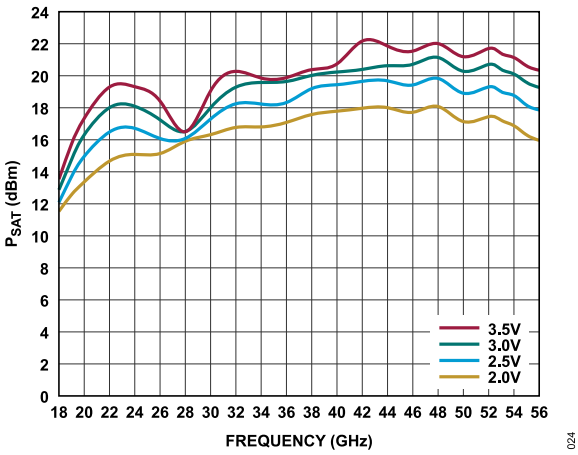

Figure 24. P_{SAT} vs. Frequency for Various V_{DD} Values, I_{DQ} = 120 mA

TYPICAL PERFORMANCE CHARACTERISTICS

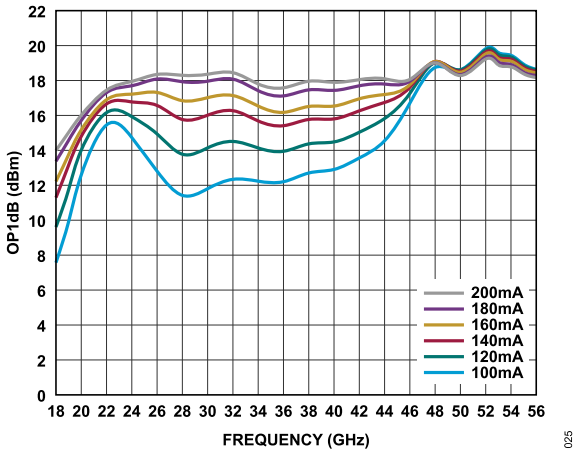

Figure 25. OP1dB vs. Frequency for Various I_{DQ} Values, V_{DD} = 3 V

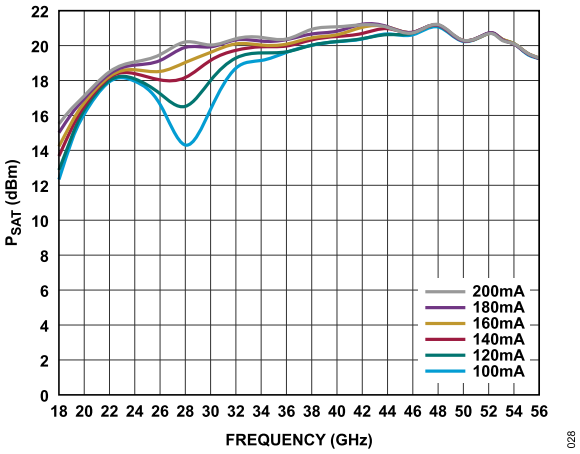

Figure 28. P_{SAT} vs. Frequency for Various I_{DQ} Values, V_{DD} = 3 V

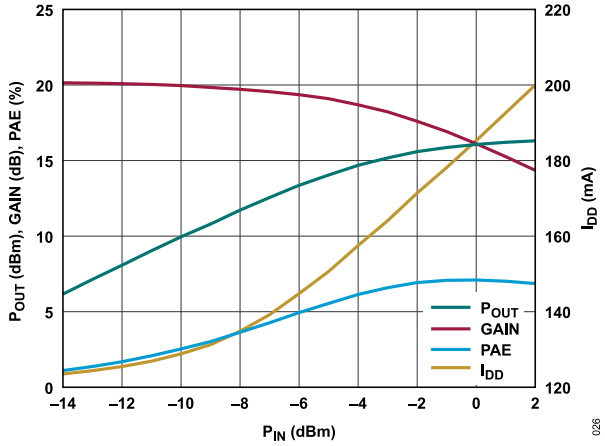

Figure 26. P_{OUT}, Gain, Power Added Efficiency (PAE), and Drain Current (I_{DD}) vs. P_{IN}, 20 GHz, V_{DD} = 3 V, I_{DQ} = 120 mA

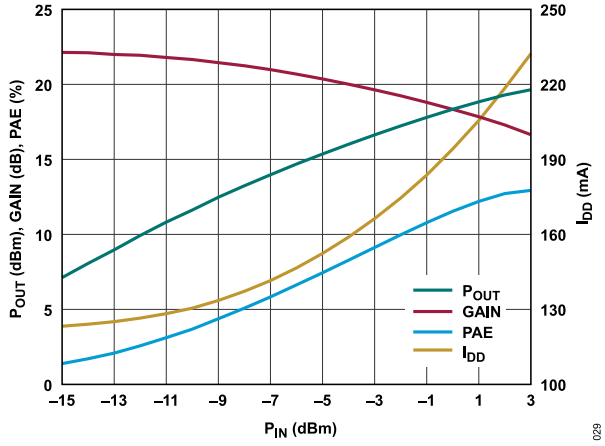

Figure 29. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, 36 GHz, V_{DD} = 3 V, I_{DQ} = 120 mA

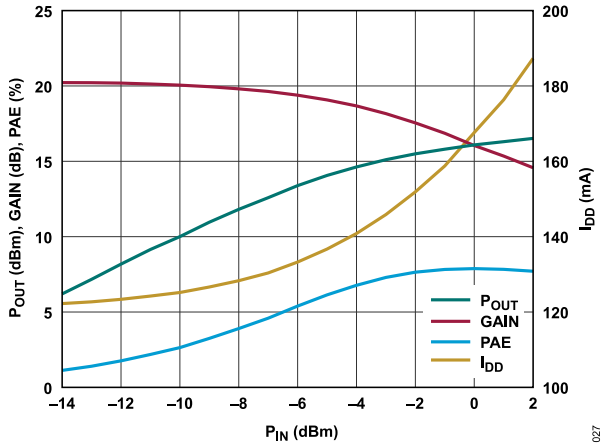

Figure 27. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, 28 GHz, V_{DD} = 3 V, I_{DQ} = 120 mA

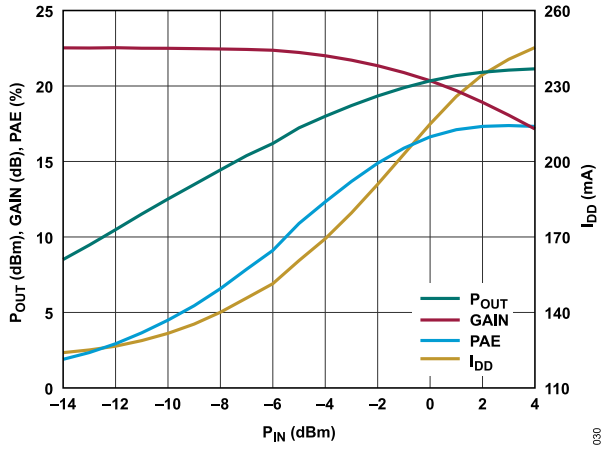

Figure 30. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, 48 GHz, V_{DD} = 3 V, I_{DQ} = 120 mA

TYPICAL PERFORMANCE CHARACTERISTICS

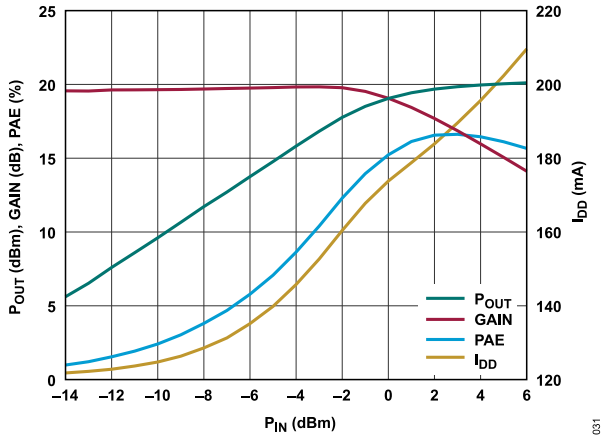

Figure 31. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, 54 GHz, V_{DD} = 3 V, I_{DQ} = 120 mA

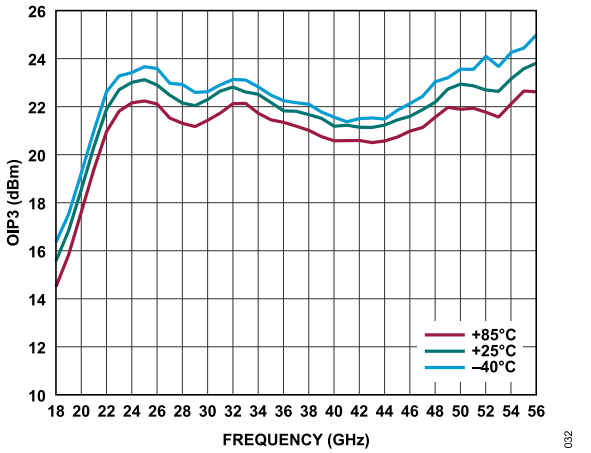

Figure 32. OIP3 vs. Frequency for Various Temperatures, P_{OUT} per Tone = 0 dBm, V_{DD} = 3 V, I_{DQ} = 120 mA

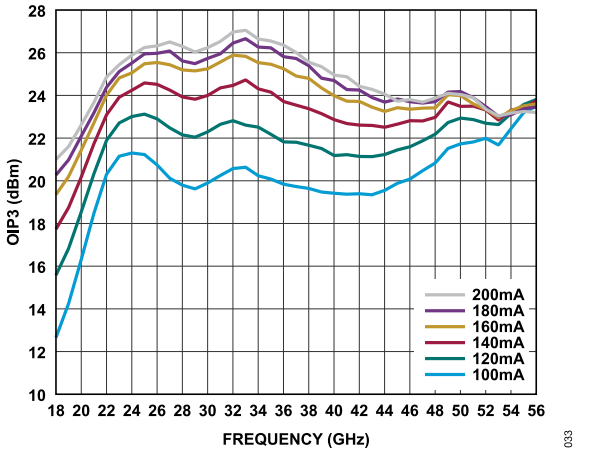

Figure 33. OIP3 vs. Frequency for Various I_{DQ} Values, P_{OUT} per Tone = 0 dBm, V_{DD} = 3 V

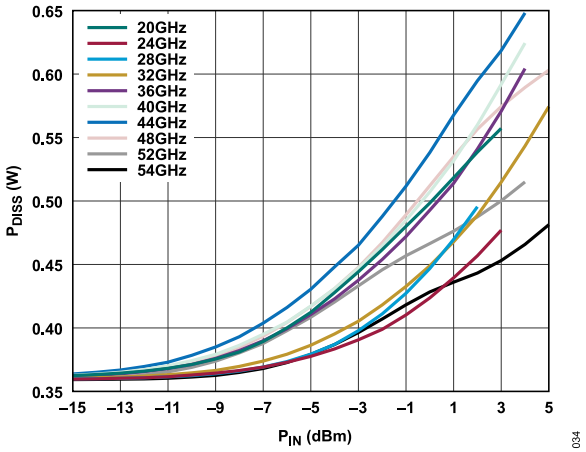

Figure 34. P_{DISS} vs. P_{IN} for Various Frequencies at T_{CASE} = 85°C, V_{DD} = 3 V, I_{DQ} = 120 mA

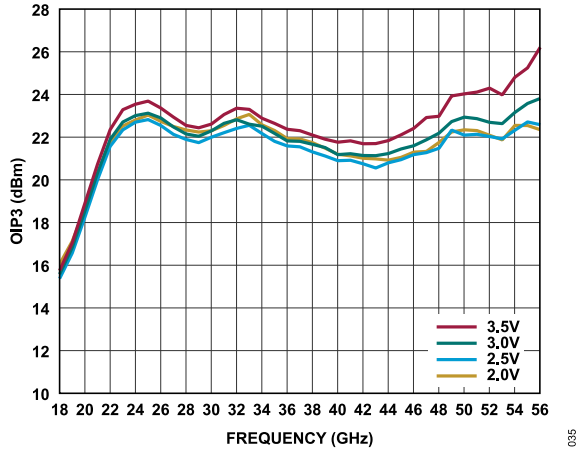

Figure 35. OIP3 vs. Frequency for V_{DD} Values, P_{OUT} per Tone = 0 dBm, I_{DQ} = 120 mA

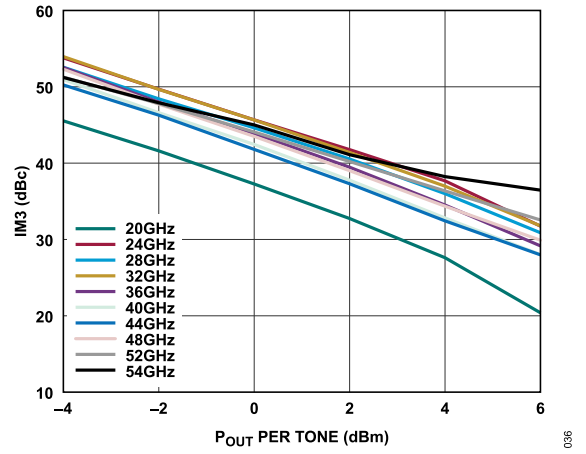

Figure 36. Third-Order Intermodulation Distortion (IM3) vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 2 V, I_{DQ} = 120 mA

TYPICAL PERFORMANCE CHARACTERISTICS

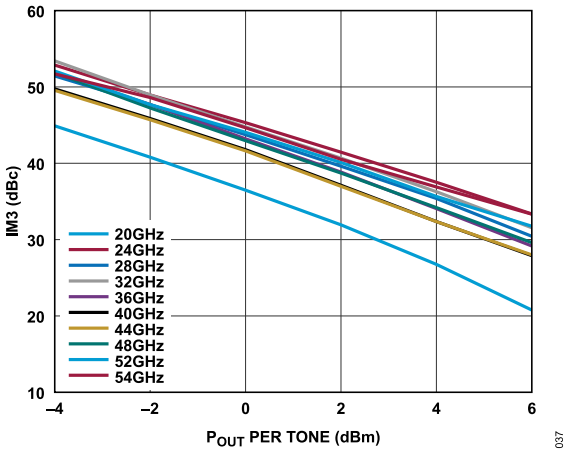

Figure 37. IM3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 2.5 V, I_{DQ} = 120 mA

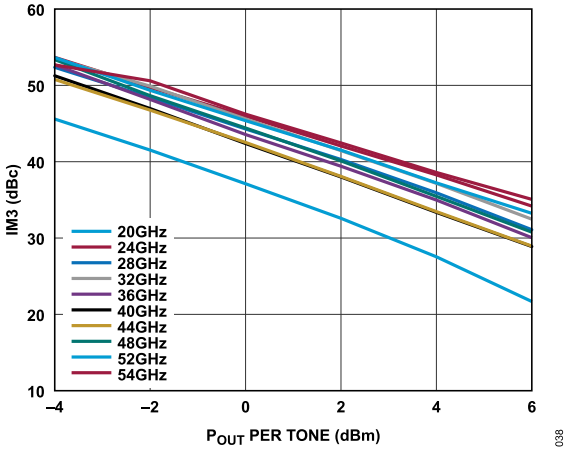

Figure 38. IM3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 3 V, I_{DQ} = 120 mA

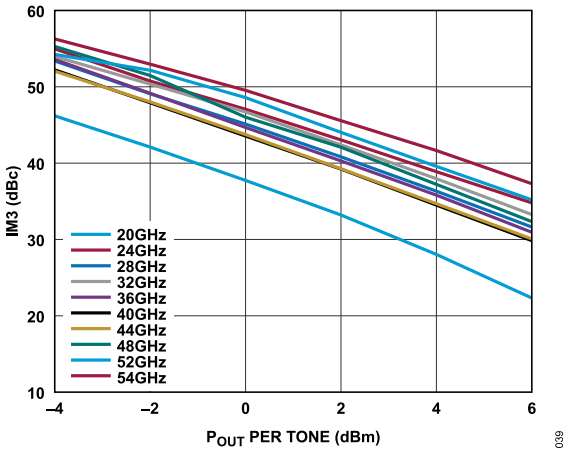

Figure 39. IM3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 3.5 V, I_{DQ} = 120 mA

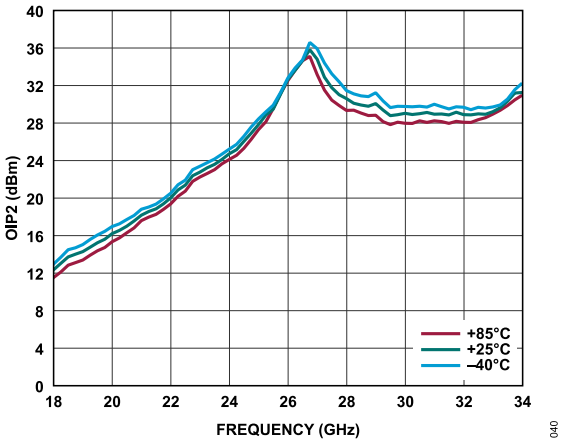

Figure 40. OIP2 vs. Frequency for Various Temperature, P_{OUT} per Tone = 0 dBm, V_{DD} = 3 V, I_{DQ} = 120 mA

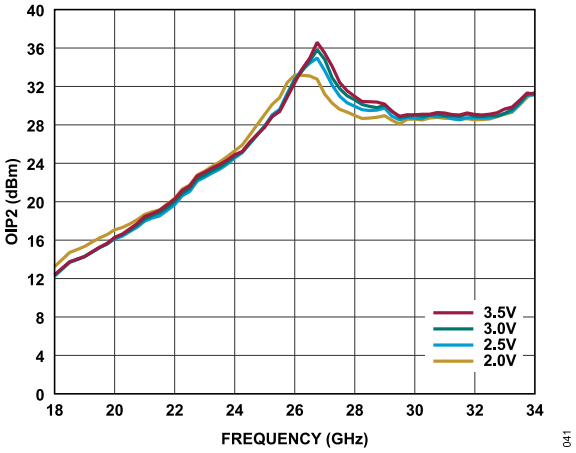

Figure 41. OIP2 vs. Frequency for Various V_{DD} Values, P_{OUT} per Tone = 0 dBm, I_{DQ} = 120 mA

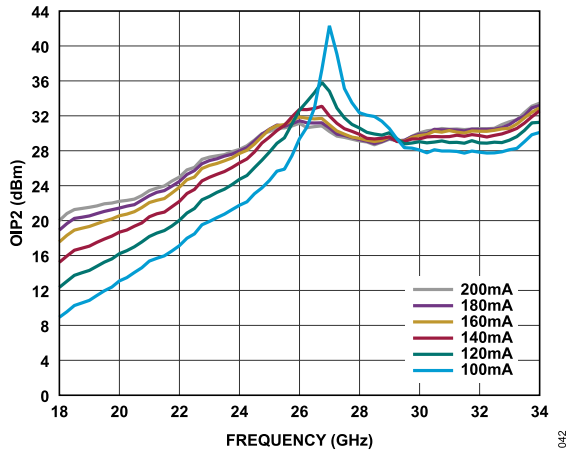

Figure 42. OIP2 vs. Frequency for Various I_{DQ} Values, P_{OUT} per Tone = 0 dBm, V_{DD} = 3 V

TYPICAL PERFORMANCE CHARACTERISTICS

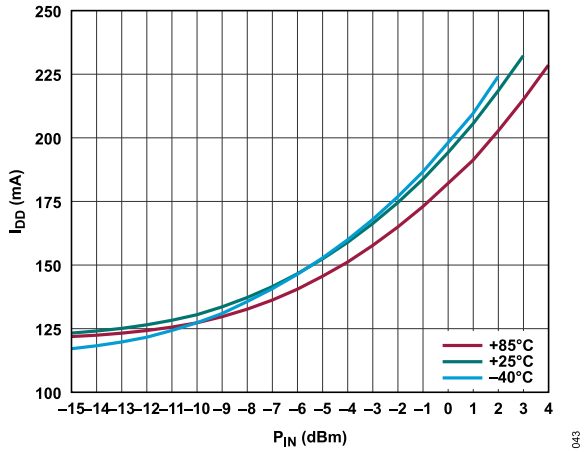

Figure 43. I_{DD} vs. P_{IN} at Various Temperatures, 36 GHz, V_{DD} = 3 V, I_{DQ} = 120 mA

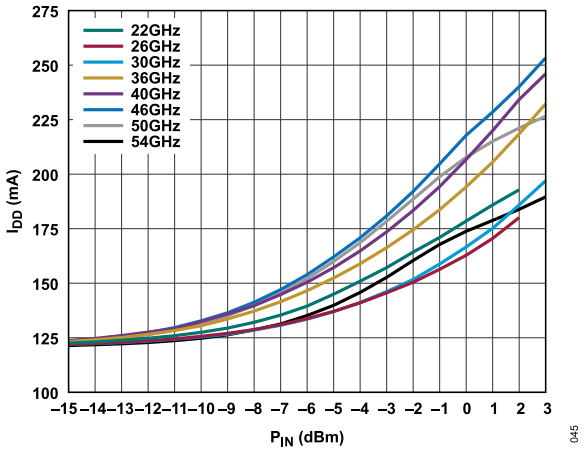

Figure 46. I_{DD} vs. P_{IN} at Various Frequencies, V_{DD} = 3 V, I_{DQ} = 120 mA

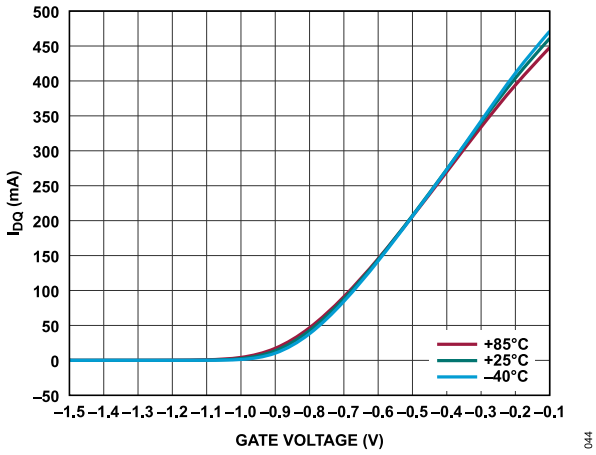

Figure 44. I_{DQ} vs. Gate Voltage for Various Temperature, V_{DD} = 3 V

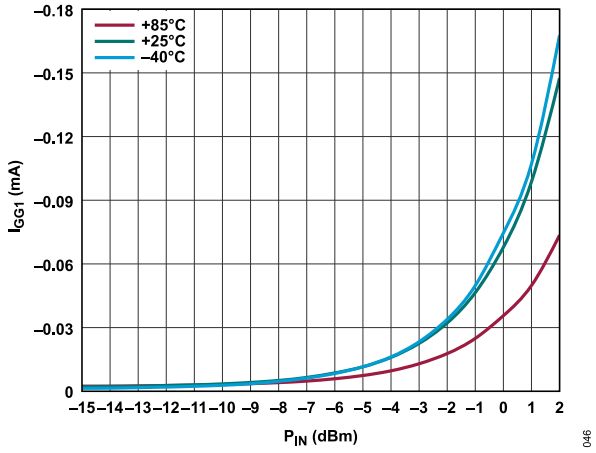

Figure 45. VGG1 Current (I_{GG1}) vs. P_{IN} at Various Temperatures, 36 GHz, V_{DD} = 3 V, I_{DQ} = 120 mA

TYPICAL PERFORMANCE CHARACTERISTICS

LOWER VOLTAGE HIGHER CURRENT OPERATION

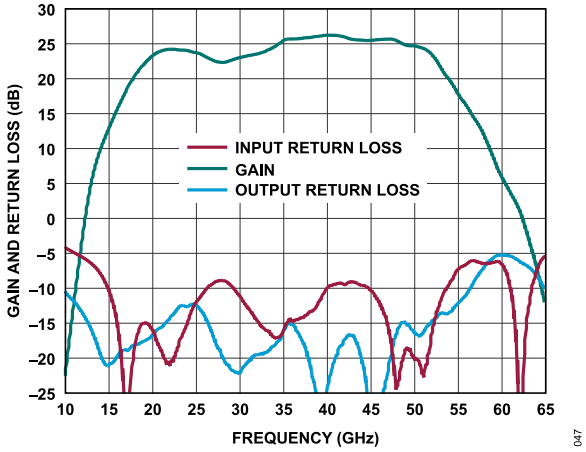

Figure 47. Gain and Return Loss vs. Frequency, V_{DD} = 2.5 V, I_{DQ} = 160 mA

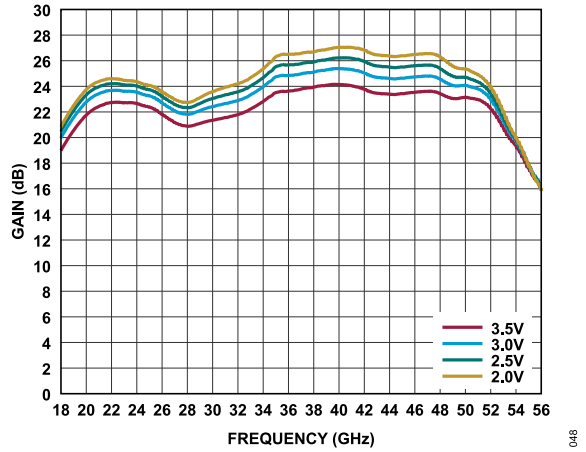

Figure 48. Gain vs. Frequency for Various V_{DD} Values, I_{DQ} = 160 mA

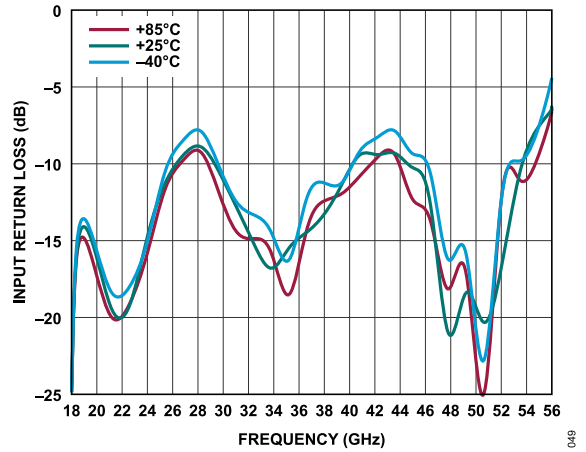

Figure 49. Input Return Loss vs. Frequency for Various Temperatures, V_{DD} = 2.5 V, I_{DQ} = 160 mA

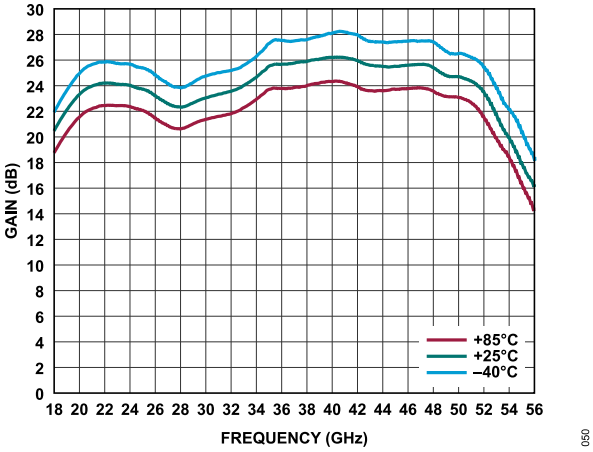

Figure 50. Gain vs. Frequency for Various Temperatures, V_{DD} = 2.5 V, I_{DQ} = 160 mA

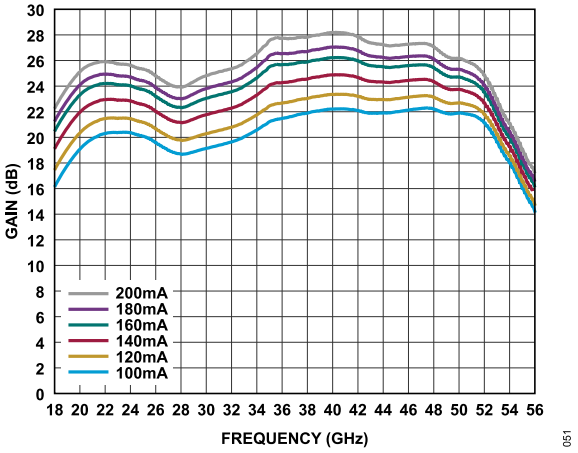

Figure 51. Gain vs. Frequency for Various I_{DQ} Values, V_{DD} = 2.5 V

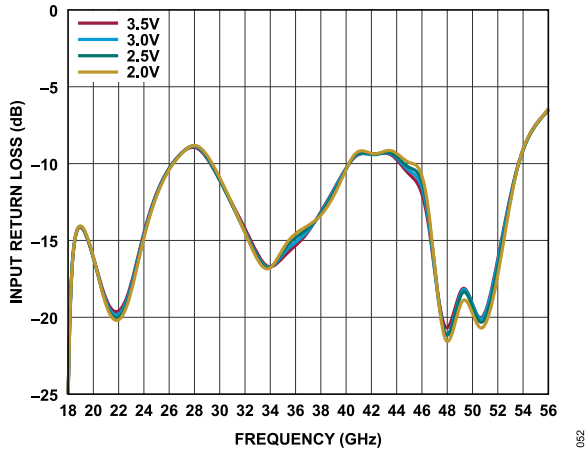

Figure 52. Input Return Loss vs. Frequency for Various V_{DD} Values, I_{DQ} = 160 mA

TYPICAL PERFORMANCE CHARACTERISTICS

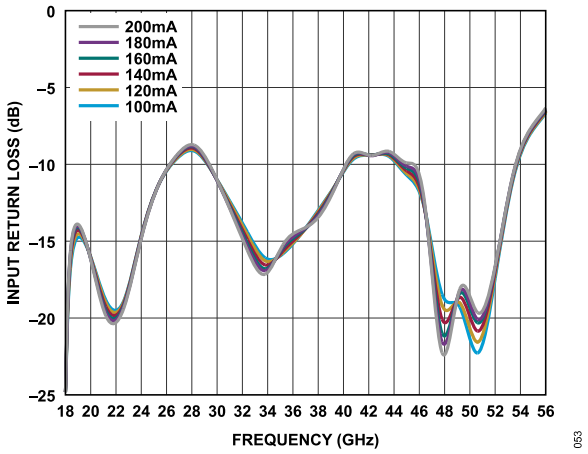

Figure 53. Input Return Loss vs. Frequency for Various I_{DQ} Values, V_{DD} = 2.5 V

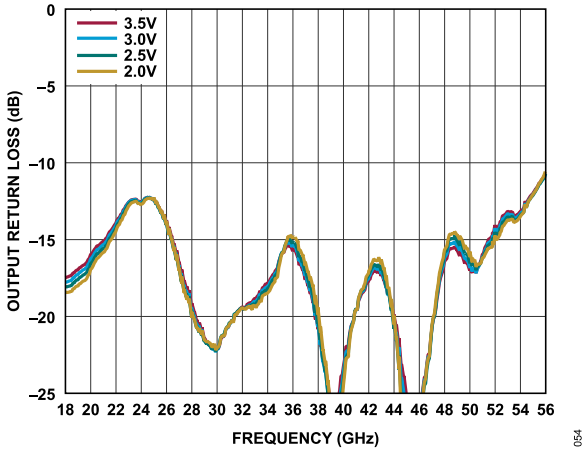

Figure 54. Output Return Loss vs. Frequency for Various V_{DD} Values, I_{DQ} = 160 mA

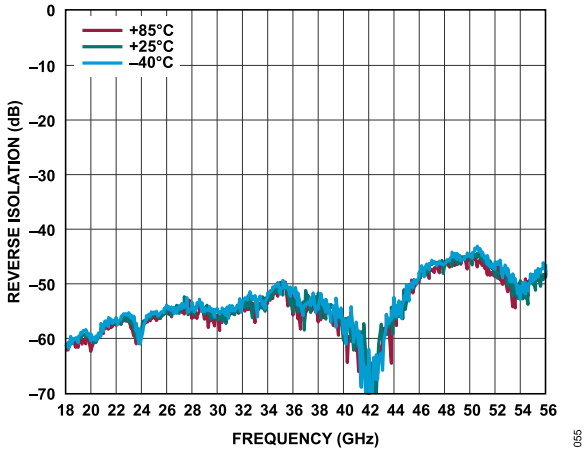

Figure 55. Reverse Isolation vs. Frequency for Various Temperatures, V_{DD} = 2.5 V, I_{DQ} = 160 mA

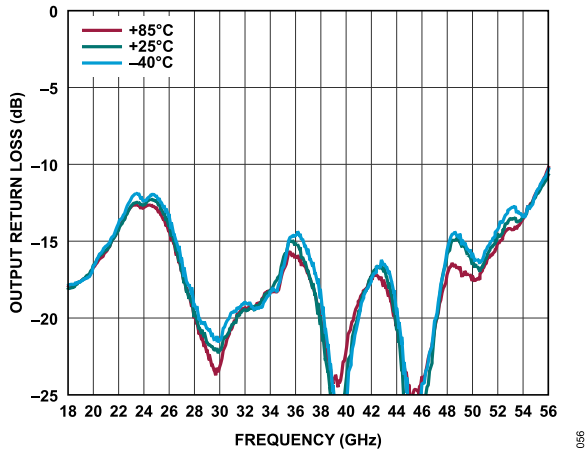

Figure 56. Output Return Loss vs. Frequency for Various Temperatures, V_{DD} = 2.5 V, I_{DQ} = 160 mA

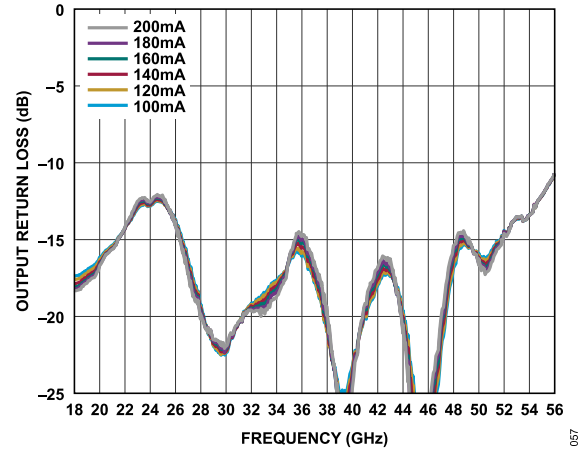

Figure 57. Output Return Loss vs. Frequency for Various I_{DQ} Values, V_{DD} = 2.5 V

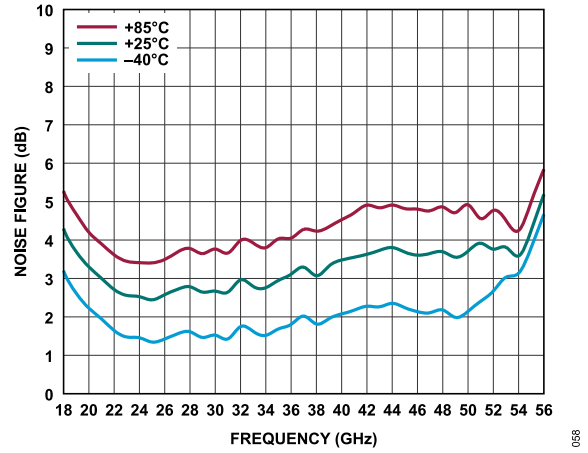

Figure 58. Noise Figure vs. Frequency for Various Temperatures, V_{DD} = 2.5 V, I_{DQ} = 160 mA

TYPICAL PERFORMANCE CHARACTERISTICS

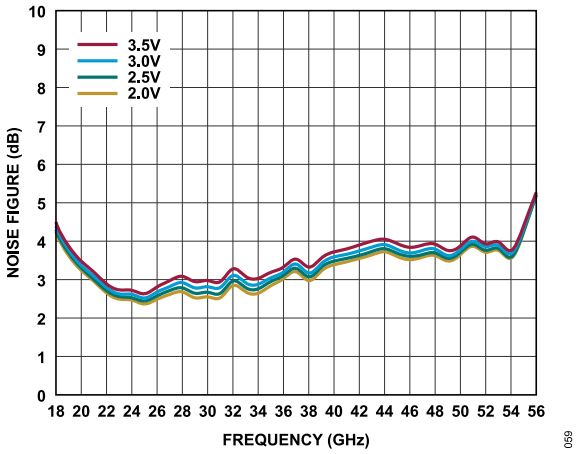

Figure 59. Noise Figure vs. Frequency for Various V_{DD} Values, I_{DQ} = 160 mA

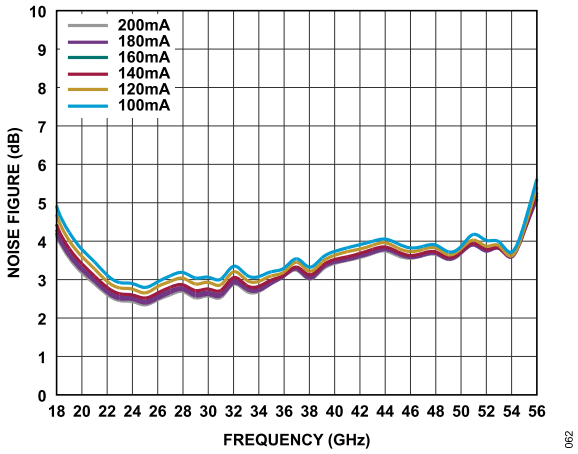

Figure 62. Noise Figure vs. Frequency for Various I_{DQ} Values, V_{DD} = 2.5 V

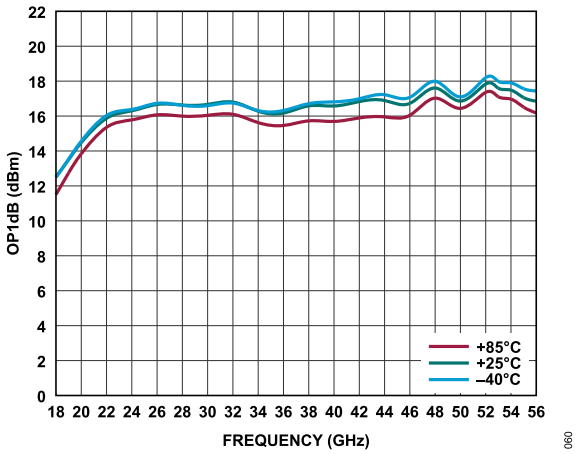

Figure 60. OP1dB vs. Frequency for Various Temperatures, V_{DD} = 2.5 V, I_{DQ} = 160 mA

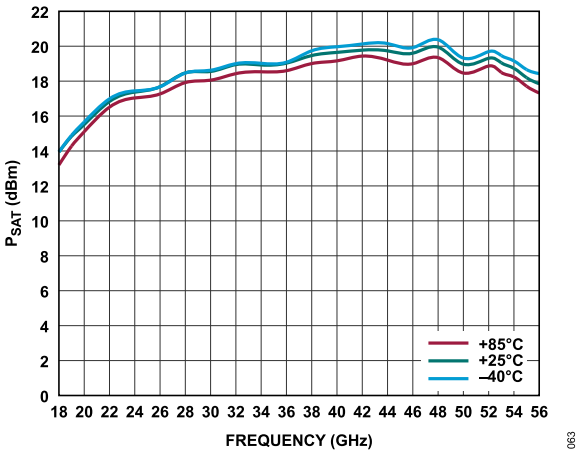

Figure 63. P_{SAT} vs. Frequency for Various Temperatures, V_{DD} = 2.5 V, I_{DQ} = 160 mA

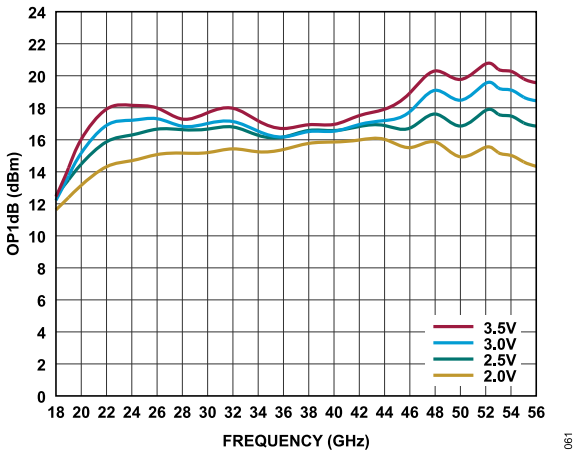

Figure 61. OP1dB vs. Frequency for Various V_{DD} Values, I_{DQ} = 160 mA

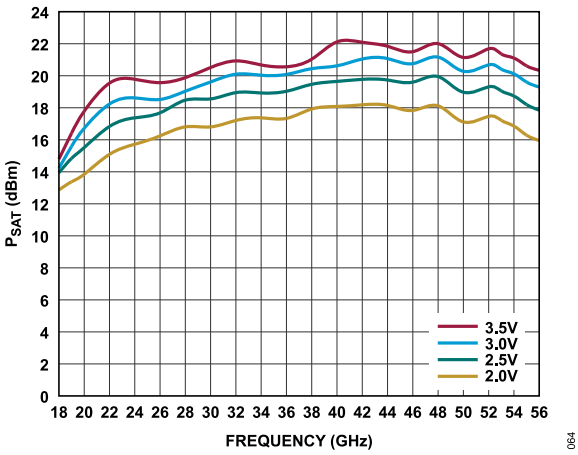

Figure 64. P_{SAT} vs. Frequency for Various V_{DD} Values, I_{DQ} = 160 mA

TYPICAL PERFORMANCE CHARACTERISTICS

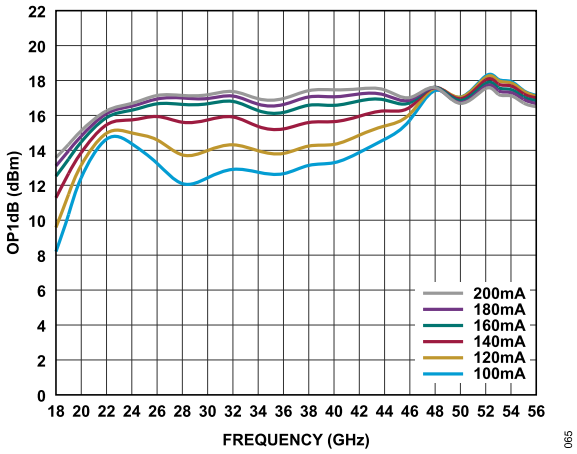

Figure 65. OP1dB vs. Frequency for Various I_{DQ} Values, V_{DD} = 2.5 V

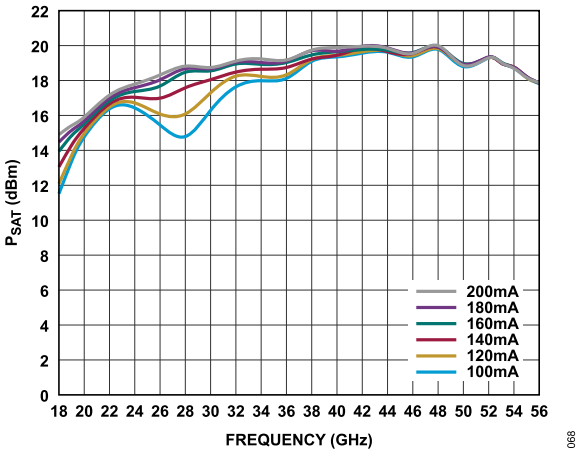

Figure 68. P_{SAT} vs. Frequency for Various I_{DQ} Values, V_{DD} = 2.5 V

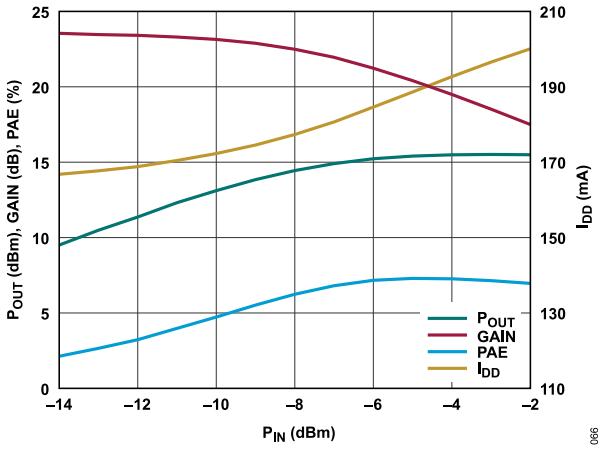

Figure 66. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, 20 GHz, V_{DD} = 2.5 V, I_{DQ} = 160 mA

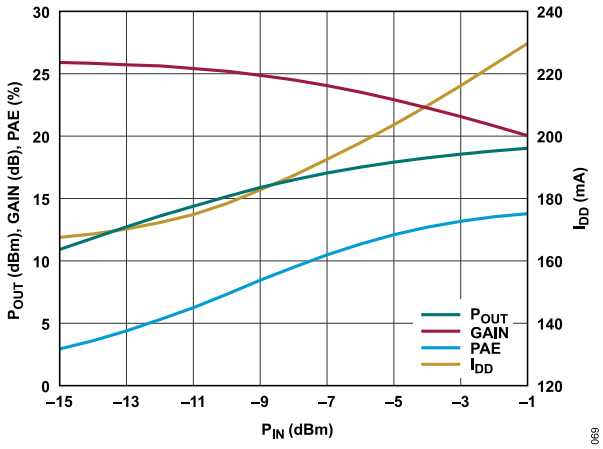

Figure 69. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, 36 GHz, V_{DD} = 2.5 V, I_{DQ} = 160 mA

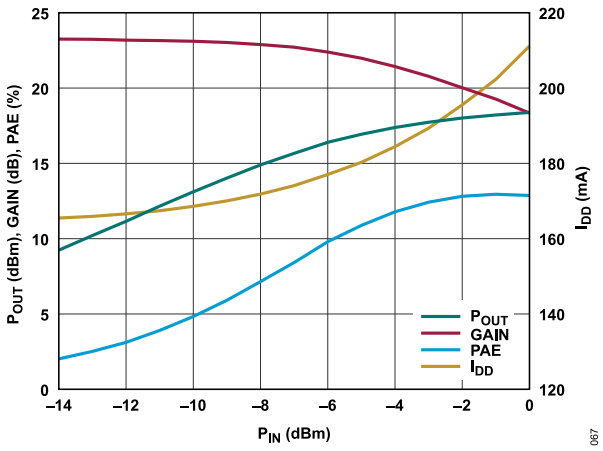

Figure 67. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, 28 GHz, V_{DD} = 2.5 V, I_{DQ} = 160 mA

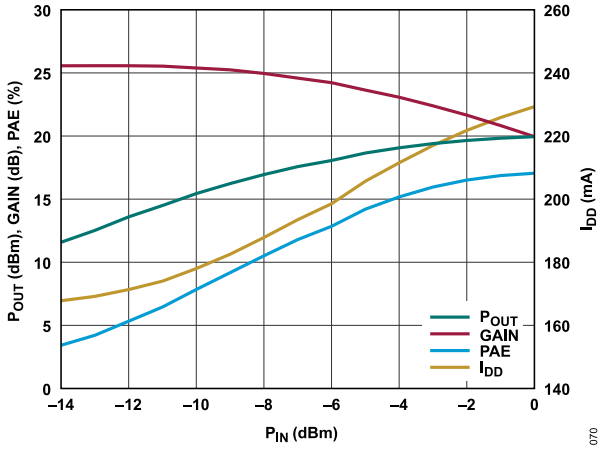

Figure 70. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, 48 GHz, V_{DD} = 2.5 V, I_{DQ} = 160 mA

TYPICAL PERFORMANCE CHARACTERISTICS

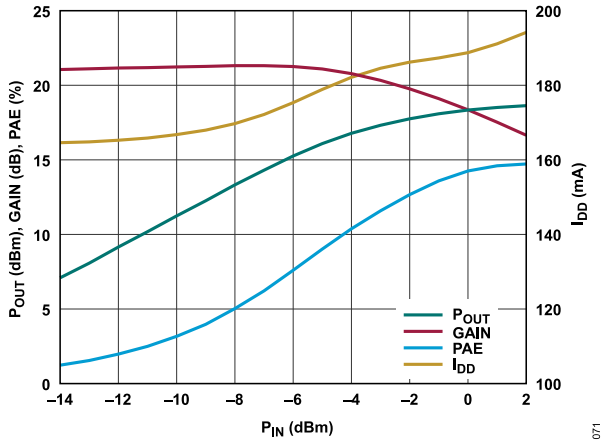

Figure 71. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, 54 GHz, V_{DD} = 2.5 V, I_{DQ} = 160 mA

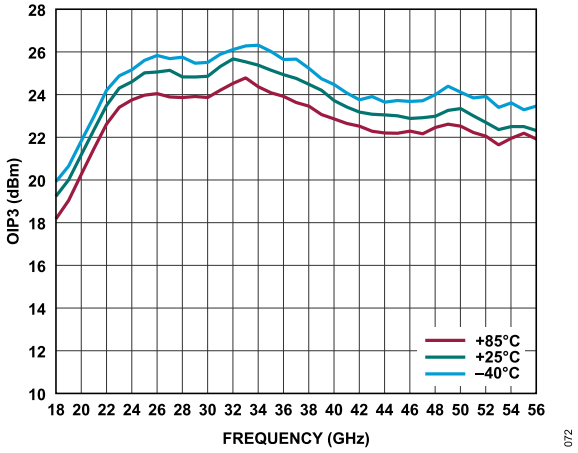

Figure 72. OIP3 vs. Frequency for Various Temperatures, P_{OUT} per Tone = 0 dBm, V_{DD} = 2.5 V, I_{DQ} = 160 mA

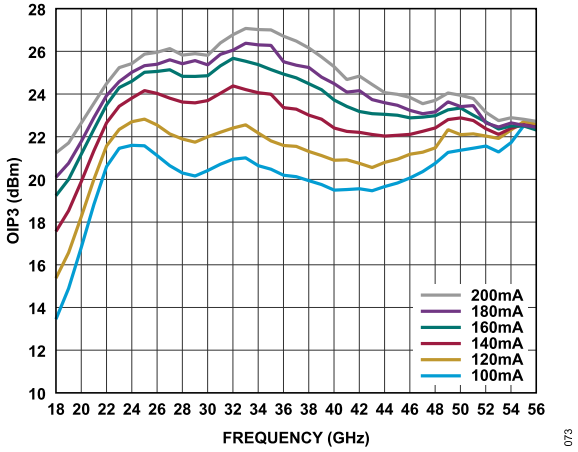

Figure 73. OIP3 vs. Frequency for Various I_{DQ} Values, P_{OUT} per Tone = 0 dBm, V_{DD} = 2.5 V

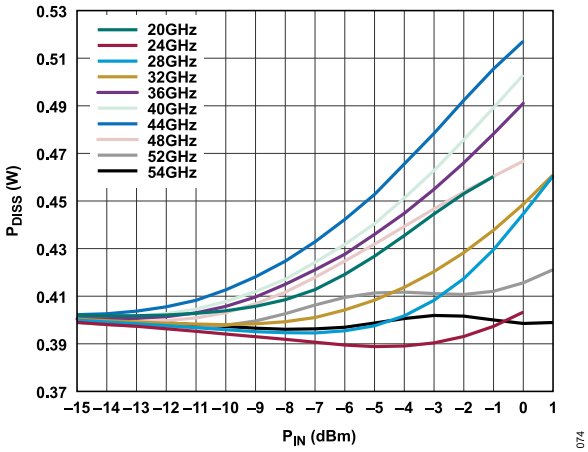

Figure 74. P_{DISS} vs. P_{IN} for Various Frequencies at T_{CASE} = 85°C, V_{DD} = 2.5 V, I_{DQ} = 160 mA

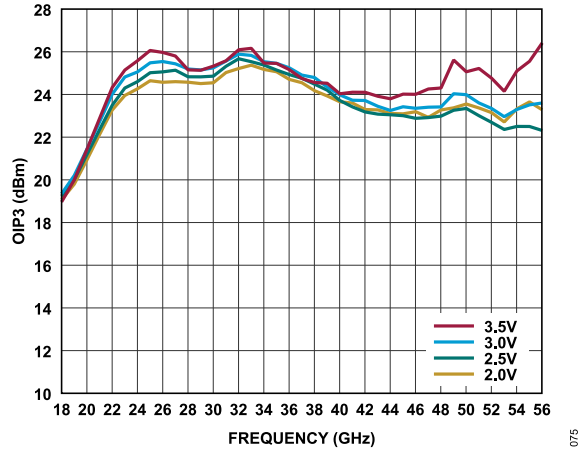

Figure 75. OIP3 vs. Frequency for Various V_{DD} Values, P_{OUT} per Tone = 0 dBm, I_{DQ} = 160 mA

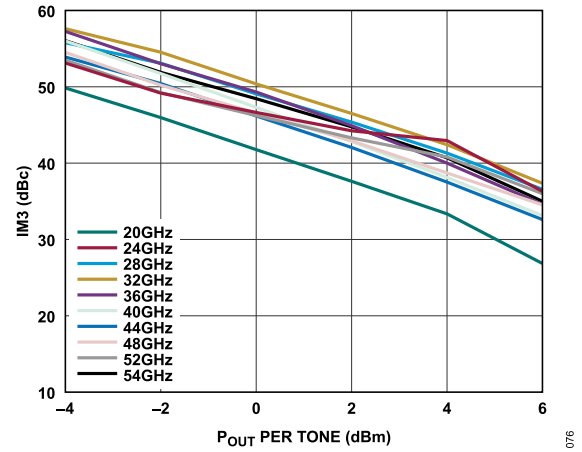

Figure 76. IM3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 2 V, I_{DQ} = 160 mA

TYPICAL PERFORMANCE CHARACTERISTICS

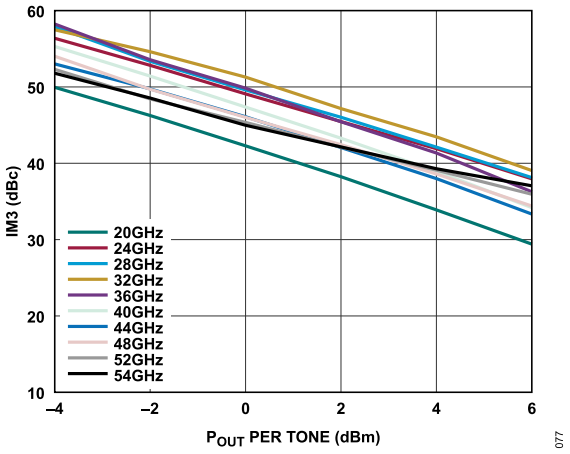

Figure 77. IM3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 2.5 V, I_{DQ} = 160 mA

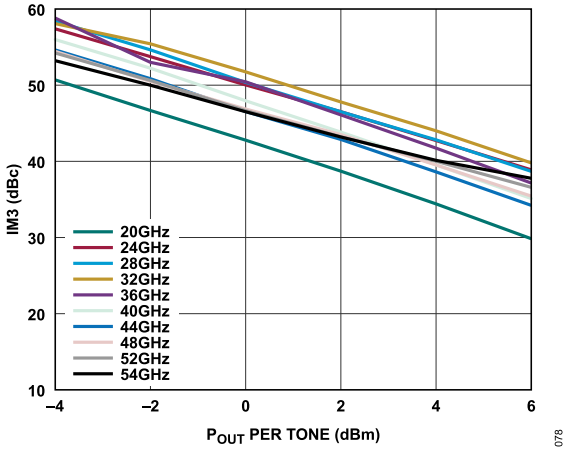

Figure 78. IM3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 3 V, I_{DQ} = 160 mA

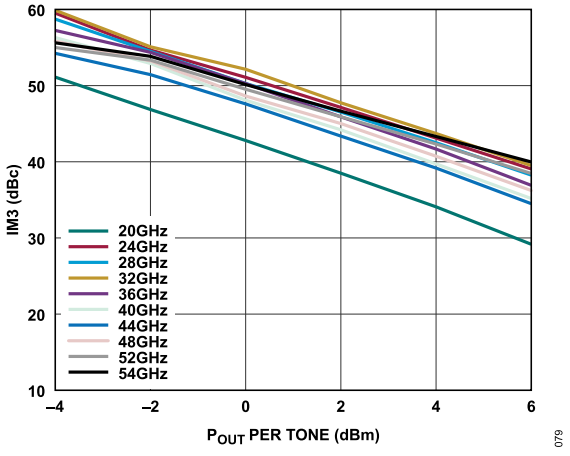

Figure 79. IM3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 3.5 V, I_{DQ} = 160 mA

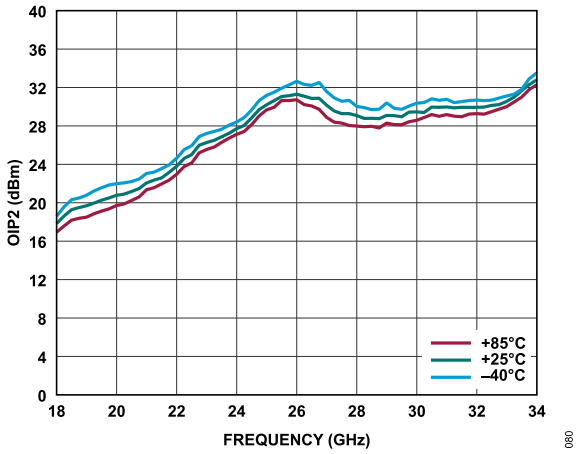

Figure 80. OIP2 vs. Frequency for Various Temperatures, P_{OUT} per Tone = 0 dBm, V_{DD} = 2.5 V, I_{DQ} = 160 mA

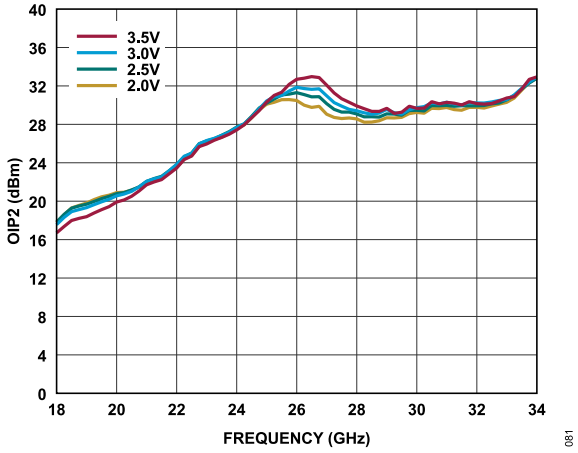

Figure 81. OIP2 vs. Frequency for Various V_{DD} Values, P_{OUT} per Tone = 0 dBm, I_{DQ} = 160 mA

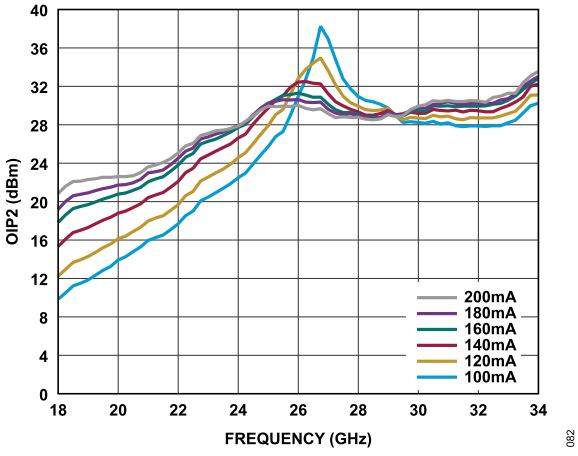

Figure 82. OIP2 vs. Frequency for Various I_{DQ} Values, P_{OUT} per Tone = 0 dBm, V_{DD} = 2.5 V

TYPICAL PERFORMANCE CHARACTERISTICS

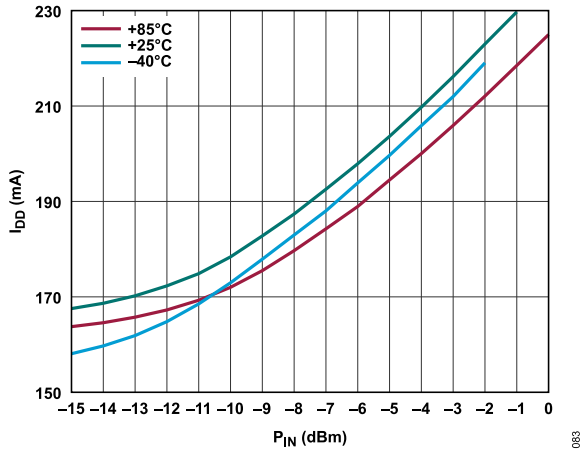

Figure 83. I_{DD} vs. P_{IN} at Various Temperatures, 36 GHz, V_{DD} = 2.5 V, I_{DQ} = 160 mA

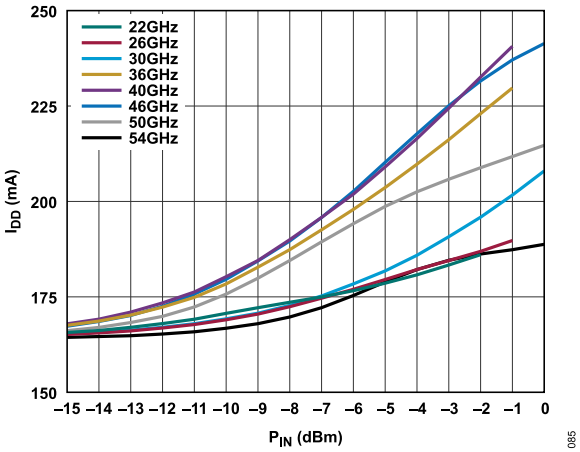

Figure 86. I_{DD} vs. P_{IN} at Various Frequencies, V_{DD} = 2.5 V, I_{DQ} = 160 mA

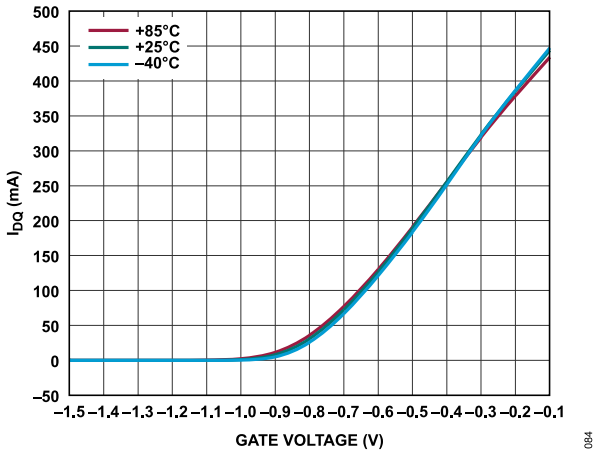

Figure 84. I_{DQ} vs. Gate Voltage for Various Temperature, V_{DD} = 2.5 V

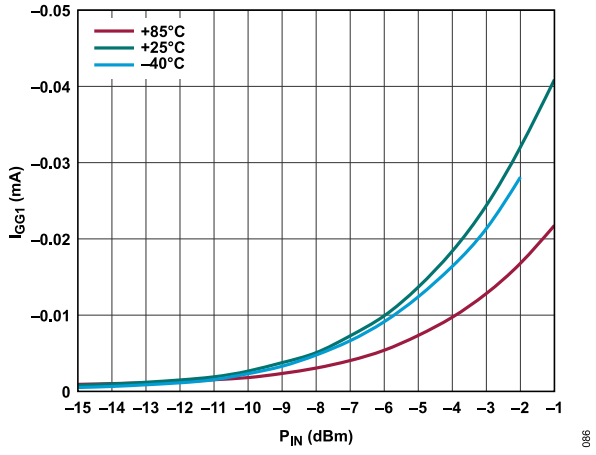

Figure 85. I_{GG1} vs. P_{IN} at Various Temperatures, 36 GHz, V_{DD} = 2.5 V, I_{DQ} = 160 mA

THEORY OF OPERATION

The ADL8106 is a wideband GaAs, pHEMT, low noise amplifier with integrated decoupling components. Figure 87 shows a simplified block diagram. The drain current is set by the negative voltage applied to the VGG1 pin. The drain bias voltage is applied through the VDD1 and VDD2 pins with the current split evenly between the two pins. Bias inductors and 0.1 µF and 100 pF decoupling capacitors are integrated.

The RFIN and RFOUT pins are ac-coupled and matched to 50 Ω. However, if these pins are connecting to devices with bias levels that are not equal to 0 V, externally ac-couple the RFIN and RFOUT pins.

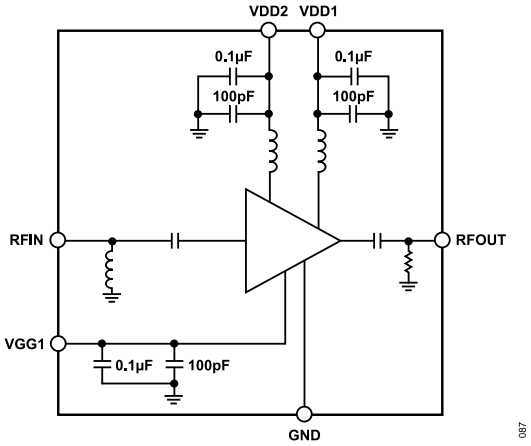

Figure 87. Simplified Block Diagram

APPLICATIONS INFORMATION

Figure 88 shows the basic connections for operating the ADL8106, and the configuration used to characterize and qualify the device. The RFIN and RFOUT pins are internally ac-coupled. However, if the dc bias level of the input signal is not equal to 0 V, externally ac-couple the RFIN pin. Likewise, if the RFOUT pin is driving an input with a bias level other than 0 V, externally ac-couple this pin.

Because VDD1, VDD2 and VGG1 are internally decoupled, no external decoupling components are required on these pins.

VGG1 sets the drain current of the amplifier (VGG1 ~ −0.65 V for an I_{DQ} of 120 mA). VDD1 and VDD2 provide the drain current (3 V nominal) with equal currents on each pin.

To avoid damaging the device, set VGG1 before VDD1 and VDD2 are applied. Set VGG1 to −2 V before turning on VDD1 and VDD2. VGG1 can then be adjusted upwards until the desired I_{DQ} is achieved. Then, apply the RF input signal. If the desired gate voltage is known, VGG1 can be set to that voltage value directly without taking it to the pinch off voltage (−2 V).

To turn off the device, turn off the RF input signal, turn off VDD1 and VDD2 and then turn off VGG1.

See the ADL8106-EVALZ user guide for information on using the evaluation board.

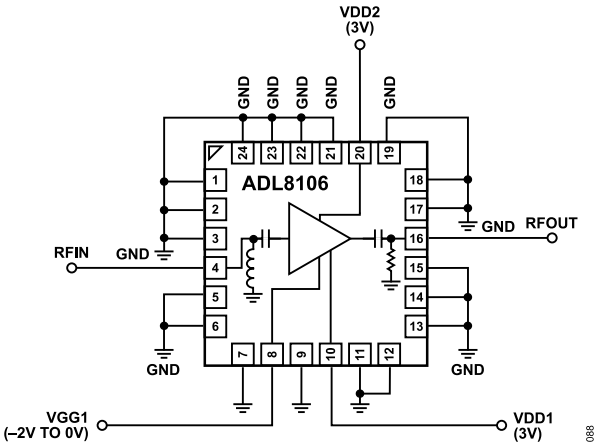

Figure 88. Basic Connections

BIASING THE ADL8106 WITH THE HMC920

The HMC920 is designed to provide active bias control for depletion mode amplifiers, such as the ADL8106. The HMC920 measures and regulates drain current to compensate for temperature changes and part to part variations in the drain current to gate voltage relationship. Additionally, the HMC920 properly sequences gate and drain voltages to ensure safe on and off operation and offers circuit self protection in the event of a short circuit. The active bias controller contains an internal charge pump that generates the negative voltage needed to drive the VGG1 pin on the ADL8106. Alternatively, an external negative voltage can be provided.

For more information regarding the use of the HMC920, refer to the HMC920 data sheet and the AN-1363 Application Note.

Application Circuit Setup

Figure 89 shows the application circuit for bias control of the ADL8106 using the HMC920. The HMC920 drain current is measured and the VGATE output voltage adjusts until the set point drain current is achieved. The various external component values around the HMC920 are calculated as follows.

The target drain current must first be determined and set. This current must be set based on the maximum drain current that is expected to be required during operation, including when the device is generating the maximum expected output power. This current is set by the resistor connected between the ISENSE pin on the HMC920 (Pin 25) and ground using the following equation:

$$I_{DRAIN}(A) = 166/R_{SENSE} + 0.0135$$

To ensure adequate headroom, the supply voltage for the HMC920 must be set higher than the target drain voltage to the ADL8106 (3 V). Accordingly, the supply voltage to HMC920 is set to 5 V.

The voltage on the LDOCC pin (Pin 29) on the HMC920 drives the VDRAIN pins which in turn drive the VDDx pins of the ADL8106. Because the LDOCC output is connected to the VDRAIN output through an internal metal-oxide semiconductor field effect transistor (MOSFET) switch with an on resistance of 0.5 Ω, the LDOCC voltage must be set slightly higher than the target drain voltage to the ADL8106. To determine the required LDOCC voltage, use the following equation:

$$VLDOCC = VDRAIN + IDRAIN \times 0.5$$

Therefore, VLDOCC = 3 V + (0.14 × 0.5) = 3.07 V.

To set VLDOCC to 3.07 V, use the following equation with R5 set to 10 kΩ:

$$R8 = (R5/2) \times (VLDOCC - 2)$$

Therefore, R8 = (10000/2) × (3.07 – 2) = 5.350 kΩ (choose 5.36 kΩ standard value).

APPLICATIONS INFORMATION

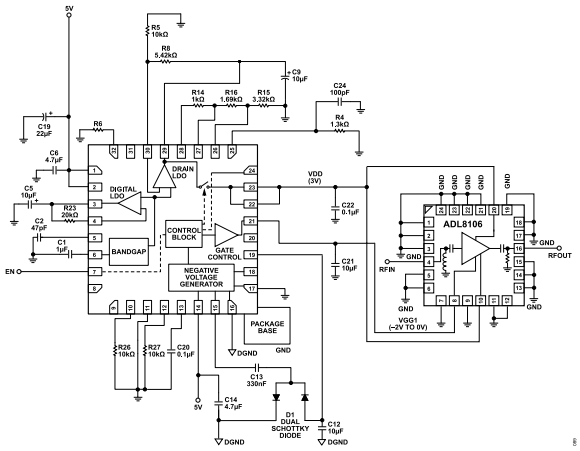

Figure 89. Active Bias Control of the ADL8106 Using the HMC920

HMC920 Bias Sequence

When the ADL8106 bias control circuit (HMC920) is set up, the bias can be toggled on and off by applying 3.5 V (high) or 0 V (low) to the EN pin. If EN is left floating, the pin floats high. When EN is set to 3.5 V, the gate voltage (V_{GATE}) initially drops to −2 V and the drain voltage (V_{DRAIN}) rises to +3 V. Then, V_{GATE} and the VGG1 voltage (V_{GG1}) increase until the drain current (I_{DRAIN}) reaches its target value. The closed control loop then regulates I_{DRAIN} to its target value. When the EN pin goes low, V_{GATE} and V_{GG1} drop back to −2 V, and V_{DRAIN} drops to 0 V.

Constant Drain Current Biasing vs. Constant Gate Voltage Biasing

In comparison to a constant gate voltage bias, where the current increases dynamically when RF power is applied, constant drain current bias results in constant power consumption.

The performance of the constant drain current circuit is summarized in Figure 90 to Figure 95. These figures include comparisons with constant gate voltage bias.

The OP1dB and P_{SAT} performance for the constant drain current bias can be varied by varying the drain current setpoint. By increasing the bias current, OP1dB and P_{SAT} improve as shown in Figure 92 and Figure 95. The trade-off with constant drain current is that the drain current is present for all RF input and output power levels.

Note that Figure 90 indicates a current consumption of 175 mA, which includes the complete current consumption of the circuit, that is, 140 mA drain current for the ADL8106 and an additional 35 mA of I_{DQ} in the HMC920. Also, the PAE for constant drain current bias in Figure 93 assumes a supply voltage of 5 V (the supply voltage to the HMC920) and a constant current of 175 mA.

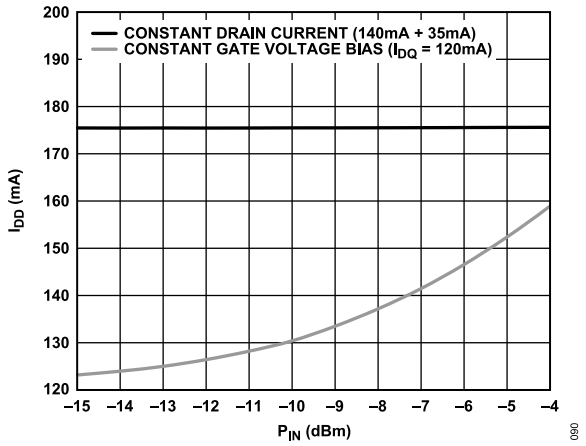

Figure 90. I_{DD} vs. P_{IN}, V_{DD} = 3 V, Frequency = 36 GHz, Constant Drain Current Bias (140 mA + 35 mA) and Constant Gate Voltage Bias (I_{DQ} = 120 mA)

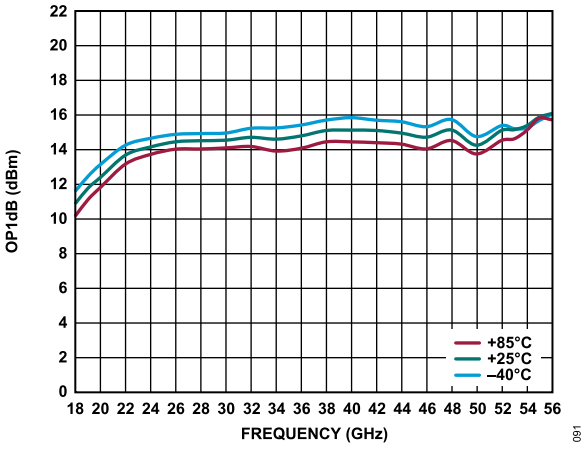

Figure 91. OP1dB vs. Frequency for Various Temperatures, Data Measured with Constant Drain Current of 140 mA

APPLICATIONS INFORMATION

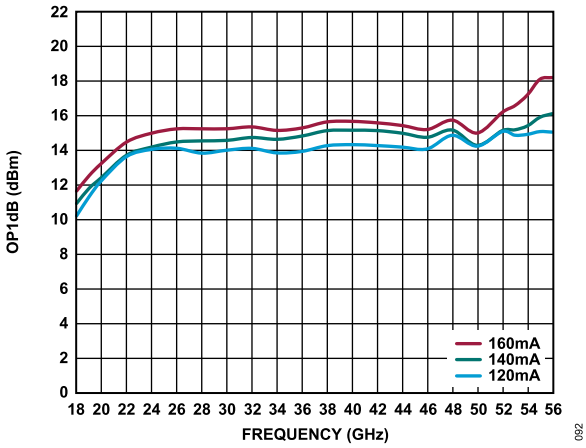

Figure 92. OP1dB vs. Frequency for Various Constant Drain Currents

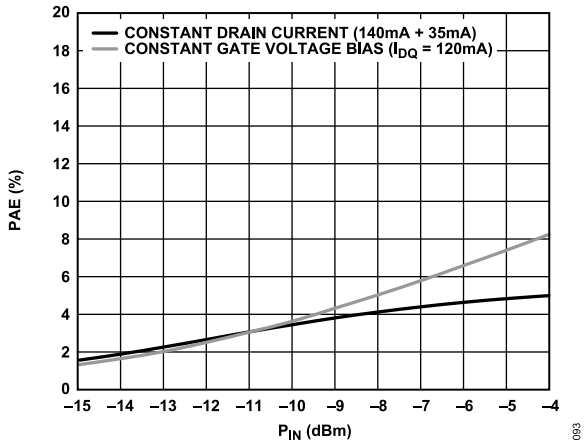

Figure 93. PAE vs. P_{IN}, V_{DD} = 3 V, Frequency = 36 GHz, Constant Drain Current Bias (140 mA + 35 mA) and Constant Gate Voltage Bias (I_{DQ}= 120 mA)

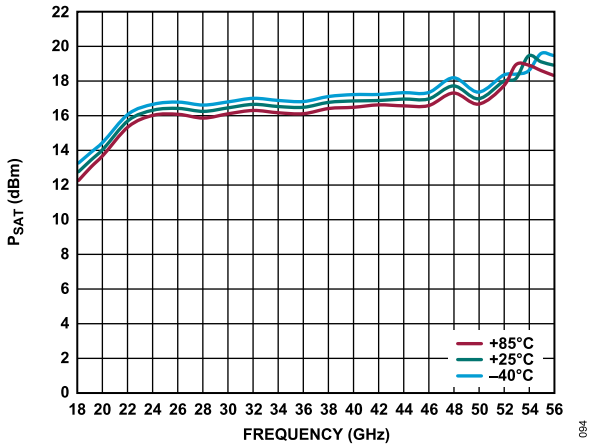

Figure 94. P_{SAT} vs. Frequency for Various Temperatures, Data Measured with I_{DD} = 140 mA

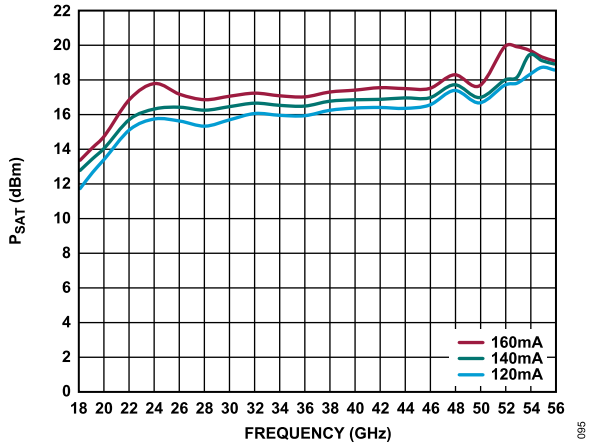

Figure 95. P_{SAT} vs. Frequency for Various Constant Drain Currents

OUTLINE DIMENSIONS

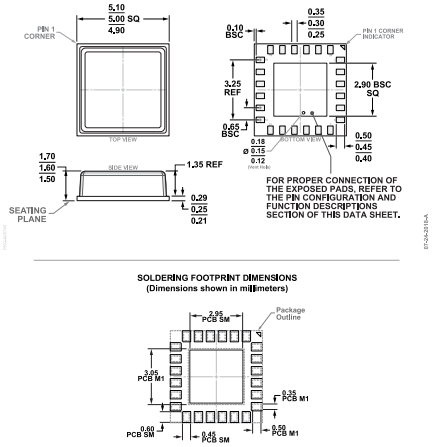

Figure 96. 24-Terminal Chip Array Small Outline No Lead [LGA_CAV]
5.00 mm × 5.00 mm Body and 1.60 mm Package Height
(CE-24-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADL8106ACEZ	−40°C to +85°C	24-Terminal Chip Array Small Outline No Lead Cavity [LGA_CAV]	Reel, 1	CE-24-2
ADL8106ACEZ-R7	−40°C to +85°C	24-Terminal Chip Array Small Outline No Lead Cavity [LGA_CAV]	Reel, 100	CE-24-2

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
ADL8106-EVALZ	Evaluation Board

[1] Z = RoHS Compliant Part.