TLC59116-Q1 16-Channel FM+ I²C-Bus Constant-Current LED Sink Driver

1 Features

- 16 LED Drivers (Each Output Programmable at Off, On, Programmable LED Brightness, or Programmable Group Dimming and Blinking Mixed With Individual LED Brightness)
- 16 Constant-Current Output Channels
- 256-Step (8-Bit) Linear Programmable Brightness Per LED Output Varying From Fully Off (Default) to Maximum Brightness Using a 97-kHz PWM Signal
- 256-Step Group Brightness Control Allows General Dimming [Using a 190-Hz PWM Signal From Fully Off to Maximum Brightness (Default)]
- 256-Step Group Blinking With Frequency Programmable From 24-Hz to 10.73 s and Duty Cycle From 0% to 99.6%
- Four Hardware Address Pins Allow 14 TLC59116-Q1 Devices to Be Connected to Same I²C Bus
- Four Software-Programmable I²C Bus Addresses (One LED Group Call Address and Three LED Sub Call Addresses) Allow Groups of Devices to Be Addressed at Same Time in Any Combination
- Software Reset Feature (SWRST Call) Allows Device to Be Reset Through I²C Bus
- Up to 14 Possible Hardware-Adjustable Individual I²C Bus Addresses Per Device, So That Each Device Can Be Programmed
- Open-Load and Overtemperature Detection Mode to Detect Individual LED Errors
- Output State Change Programmable on Acknowledge or Stop Command to Update Outputs Byte-by-Byte or All at Same Time (Default to Change on Stop)
- Output Current Adjusted Through an External Resistor
- Constant Output Current Range: 5-mA to 120-mA
- Maximum Output Voltage: 17 V
- 25-MHz Internal Oscillator Requires No External Components
- 1-MHz Fast-mode Plus (FMT) Compatible I²C-Bus Interface With 30-mA High-Drive Capability on SDA Output for Driving High-Capacitive Buses
- Internal Power-On Reset
- Noise Filter on SCL and SDA Inputs
- No Glitch on Power-Up
- Active-Low Reset
- Supports Hot Insertion
- Low Standby Current
- 3.3 V or 5 V Supply Voltage
- 5.5 V Tolerant Inputs
- 28-Pin Thin Shrink Small-Outline Package (TSSOP) (PW-28)
- –40°C to +105°C Operation

2 Applications

- General LED Lighting Applications
- Backlight for center stack buttons
- Backlight for cluster indicators

3 Description

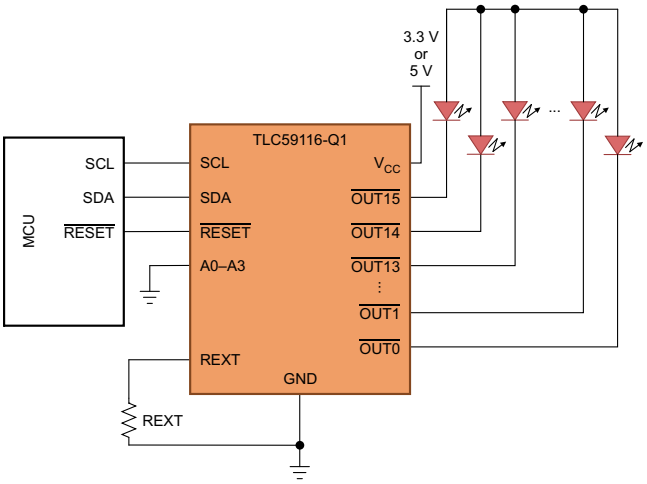
The TLC59116-Q1 is an I²C-Bus controlled 16-channel LED driver that is optimized for red/green/blue/amber (RGBA) color mixing and backlight application. Each LED output has its own 8-bit resolution (256 steps) fixed-frequency individual PWM controller that operates at 97-kHz, with a duty cycle that is adjustable from 0% to 99.6%.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLC59116-Q1	TSSOP (28)	9.70 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

TLC59116-Q1 Typical Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2016) to Revision A	Page
• Changed device status from *Product Preview* to *Production Data*	1

5 Description (continued)

The individual PWM controller allows each LED to be set to a specific brightness value. An additional 8-bit resolution (256 steps) group PWM controller has both a fixed frequency of 190-Hz and an adjustable frequency between 24-Hz to once every 10.73 seconds, with a duty cycle that is adjustable from 0% to 99.6%. The group PWM controller dims or blinks all LEDs with the same value.

Each LED output can be off, on (no PWM control), or set at its individual PWM controller value at both individual and group PWM controller values.

The TLC59116-Q1 operates with a supply voltage range of 3 V to 5.5 V and the outputs are 17 V tolerant. LEDs can be directly connected to the TLC59116-Q1 device outputs.

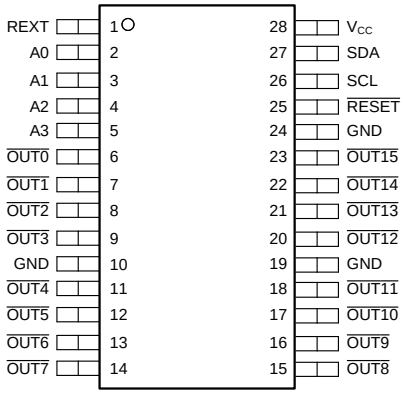
Software programmable LED Group and three Sub Call I^2C-Bus addresses allow all or defined groups of TLC59116-Q1 devices to respond to a common I^2C Bus address, allowing for example, all the same color LEDs to be turned on or off at the same time or marquee chasing effect, thus minimizing I^2C Bus commands.

Four hardware address pins allow up to 14 devices on the same Bus.

The Software Reset (SWRST) Call allows the master to perform a reset of the TLC59116-Q1 through the I^2C Bus, identical to the Power-On Reset (POR) that initializes the registers to their default state causing the outputs to be set high (LED off). This allows an easy and quick way to reconfigure all device registers to the same condition.

6 Pin Configuration and Functions

PW Package
28-Pin TSSOP
Top View



Pin Functions

PIN		I/O (1)	DESCRIPTION
NO.	NAME		
1	REXT	I	Input terminal used to connect an external resistor for setting up all output currents
2	A0	I	Address input 0
3	A1	I	Address input 1
4	A2	I	Address input 2
5	A3	I	Address input 3
6	$\overline{OUT0}$	O	Constant current output 0
7	$\overline{OUT1}$	O	Constant current output 1
8	$\overline{OUT2}$	O	Constant current output 2
9	$\overline{OUT3}$	O	Constant current output 3
10	GND	—	Ground
11	$\overline{OUT4}$	O	Constant current output 4
12	$\overline{OUT5}$	O	Constant current output 5
13	$\overline{OUT6}$	O	Constant current output 6
14	$\overline{OUT7}$	O	Constant current output 7
15	$\overline{OUT8}$	O	Constant current output 8
16	$\overline{OUT9}$	O	Constant current output 9
17	$\overline{OUT10}$	O	Constant current output 10
18	$\overline{OUT11}$	O	Constant current output 11
19	GND	—	Ground
20	$\overline{OUT12}$	O	Constant current output 12
21	$\overline{OUT13}$	O	Constant current output 13
22	$\overline{OUT14}$	O	Constant current output 14
23	$\overline{OUT15}$	O	Constant current output 15
24	GND	—	Ground
25	$\overline{RESET}$	I	Active-low reset input
26	SCL	I	Serial clock input
27	SDA	I/O	Serial data input/output
28	V_{CC}	—	Power supply

(1) I/O = input and Output

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	0	7	V
V_I	Input voltage	–0.4	V_{CC} + 0.4	V
V_O	Output voltage	–0.5	20	V
I_O	Output current per channel		120	mA
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation

				MIN	MAX	UNIT
V_{CC}	Supply voltage			3	5.5	V
V_{IH}	High-level input voltage	SCL, SDA, $\overline{RESET}$, A0, A1, A2, A3		0.7 × V_{CC}	V_{CC}	V
V_{IL}	Low-level input voltage	SCL, SDA, $\overline{RESET}$, A0, A1, A2, A3		0	0.3 × V_{CC}	V
V_O	Supply voltage to output pins	$\overline{OUT0}$ to $\overline{OUT15}$			17	V
I_{OL}	Low-level output current sink	SDA	V_{CC} = 3 V		20	mA
			V_{CC} = 5 V		30	
I_O	Output current per channel	$\overline{OUT0}$ to $\overline{OUT15}$		5	120	mA
T_A	Operating free-air temperature			–40	105	°C

7.4 Thermal Information

THERMAL METRIC (1)		TLC59116-Q1 PW (TSSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	78	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	35.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

V_{CC} = 3 V to 5.5 V, T_A = –40°C to +105°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP (1)	MAX	UNIT
I_I	Input / output leakage current	SCL, SDA, A0, A1, A2, A3, RESET	V_I = V_{CC} or GND				±0.3	µA
	Output leakage current	OUT0 to OUT15	V_O = 17 V, T_J = 25°C				0.5	µA
V_{POR}	Power-on reset voltage					2.5		V
I_{OL}	Low-level output current	SDA	V_{CC} = 3 V, V_{OL} = 0.4 V		20			mA
			V_{CC} = 5 V, V_{OL} = 0.4 V		30			
$I_{O(1)}$	Output current 1	OUT0 to OUT15	V_O = 0.6 V, R_{ext} = 720 Ω, CG = 0.992 (2)			26		mA
	Output current error	OUT0 to OUT15	I_O = 26 mA, V_O = 0.6 V, R_{ext} = 720 Ω, T_J = 25°C				±10%	
	Output channel to channel current error	OUT0 to OUT15	I_O = 26 mA, V_O = 0.6 V, R_{ext} = 720 Ω, T_J = 25°C				±6%	
$I_{O(2)}$	Output current 2	OUT0 to OUT15	V_O = 0.8 V, R_{ext} = 360 Ω, CG = 0.992 (2)			52		mA
	Output current error	OUT0 to OUT15	I_O = 52 mA, V_O = 0.8 V, R_{ext} = 360 Ω, T_J = 25°C				±8%	
	Output channel to channel current error	OUT0 to OUT15	I_O = 52 mA, V_O = 0.8 V, R_{ext} = 360 Ω, T_J = 25°C				±6%	
I_{OUT} vs V_{OUT}	Output current vs output voltage regulation	OUT0 to OUT15	V_O = 1 V to 3 V, I_O = 26 mA			±0.1		%/V
			V_O = 3 V to 5.5 V, I_O = 26 mA to 120 mA			±1		
$I_{OUT,Th1}$	Threshold current 1 for error detection	OUT0 to OUT15	$I_{OUT,target}$ = 26 mA			0.5 × I_{TARGET}%		
$I_{OUT,Th2}$	Threshold current 2 for error detection	OUT0 to OUT15	$I_{OUT,target}$ = 52 mA			0.5 × I_{TARGET}%		
$I_{OUT,Th3}$	Threshold current 3 for error detection	OUT0 to OUT15	$I_{OUT,target}$ = 104 mA			0.5 × I_{TARGET}%		
T_{SD}	Overtemperature shutdown (3)				150	175	200	°C
T_{HYS}	Restart hysteresis					15		°C
C_i	Input capacitance	SCL, A0, A1, A2, A3, RESET	V_I = V_{CC} or GND			5		pF
C_{io}	Input / output capacitance	SDA	V_I = V_{CC} or GND			8		pF
I_{CC}	Supply current		V_{CC} = 5.5 V	OUT0 to OUT15 = OFF, R_{ext} = Open			25	mA
				OUT0 to OUT15 = OFF, R_{ext} = 720 Ω			29	
				OUT0 to OUT15 = OFF, R_{ext} = 360 Ω			32	
				OUT0 to OUT15 = OFF, R_{ext} = 180 Ω			37	
				OUT0 to OUT15 = ON, R_{ext} = 720 Ω			29	
				OUT0 to OUT15 = ON, R_{ext} = 360 Ω			32	
				OUT0 to OUT15 = ON, R_{ext} = 180 Ω			37	

(1) All typical values are at T_A = 25°C.
(2) CG is the Current Gain and is defined in Table 13.
(3) Specified by design

7.6 Timing Requirements

T_A = –40°C to +105°C

		I²C BUS	MIN	MAX	UNIT
I²C INTERFACE					
f_{SCL}	SCL clock frequency (1)	STANDARD MODE	0	100	kHz
		FAST MODE	0	400	
		FAST MODE PLUS	0	1000	
t_{BUF}	I²C Bus free time between Stop and Start conditions	STANDARD MODE	4.7		µs
		FAST MODE	1.3		
		FAST MODE PLUS	0.5		
$t_{HD;STA}$	Hold time (repeated) Start condition	STANDARD MODE	4		µs
		FAST MODE	0.6		
		FAST MODE PLUS	0.26		
$t_{SU;STA}$	Set-up time for a repeated Start condition	STANDARD MODE	4.7		µs
		FAST MODE	0.6		
		FAST MODE PLUS	0.26		
$t_{SU;STO}$	Set-up time for Stop condition	STANDARD MODE	4		µs
		FAST MODE	0.6		
		FAST MODE PLUS	0.26		
$t_{HD;DAT}$	Data hold time	STANDARD MODE	0		ns
		FAST MODE	0		
		FAST MODE PLUS	0		
$t_{VD;ACK}$	Data valid acknowledge time (2)	STANDARD MODE	0.3	3.45	µs
		FAST MODE	0.1	0.9	
		FAST MODE PLUS	0.05	0.45	
$t_{VD;DAT}$	Data valid time (3)	STANDARD MODE	0.3	3.45	µs
		FAST MODE	0.1	0.9	
		FAST MODE PLUS	0.05	0.45	
$t_{SU;DAT}$	Data set-up time	STANDARD MODE	250		ns
		FAST MODE	100		
		FAST MODE PLUS	50		
t_{LOW}	Low period of SCL clock	STANDARD MODE	4.7		µs
		FAST MODE	1.3		
		FAST MODE PLUS	0.5		
t_{HIGH}	High period of SCL clock	STANDARD MODE	4		µs
		FAST MODE	0.6		
		FAST MODE PLUS	0.26		
t_f	Fall time of both SDA and SCL signals (4) (5)	STANDARD MODE		300	ns
		FAST MODE	$20+0.1C_b$ (6)	300	
		FAST MODE PLUS		120	
t_r	Rise time of both SDA and SCL signals	STANDARD MODE		1000	ns
		FAST MODE	$20+0.1C_b$ (6)	300	
		FAST MODE PLUS		120	

(1) The TLC59116-Q1 does not have a self timeout on the I²C Bus. The Master can issue a reset if needed.
(2) $t_{VD;ACK}$ = time for ACK signal from SCL low to SDA (out) low.
(3) $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL low.
(4) A master device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the V_{IL} of the SCL signal) in order to bridge the undefined region of the SCL falling edge.
(5) The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time (t_f) for the SDA output stage is specified at 250 ns. This allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.
(6) C_b = Total capacitance of one bus line in pF

Timing Requirements (continued)

T_A = –40°C to +105°C

		I²C BUS	MIN	MAX	UNIT
t_{SP}	Pulse width of spikes that must be suppressed by the input filter (7)	STANDARD MODE		50	ns
		FAST MODE		50	
		FAST MODE PLUS		50	
RESET					
t_W	Reset pulse width	STANDARD MODE	10		ns
		FAST MODE	10		
		FAST MODE PLUS	10		
t_{REC}	Reset recovery time	STANDARD MODE	0		ns
		FAST MODE	0		
		FAST MODE PLUS	0		
t_{RESET}	Time to reset (8) (9)	STANDARD MODE	400		ns
		FAST MODE	400		
		FAST MODE PLUS	400		

(7) Input filters on the SDA and SCL inputs suppress noise spikes less than 50 ns.
(8) Resetting the device while actively communicating on the bus may cause glitches or errant Stop conditions.
(9) Upon reset, the full delay will be the sum of t_{RESET} and the RC time constant of the SDA bus.

7.7 Typical Characteristics

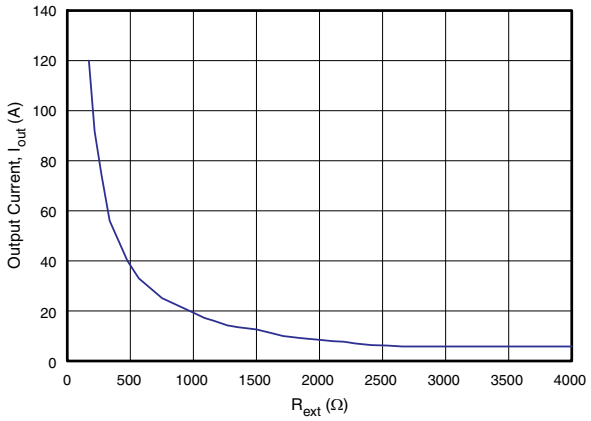


Figure 1. $I_{OUT,target}$ vs R_{ext}

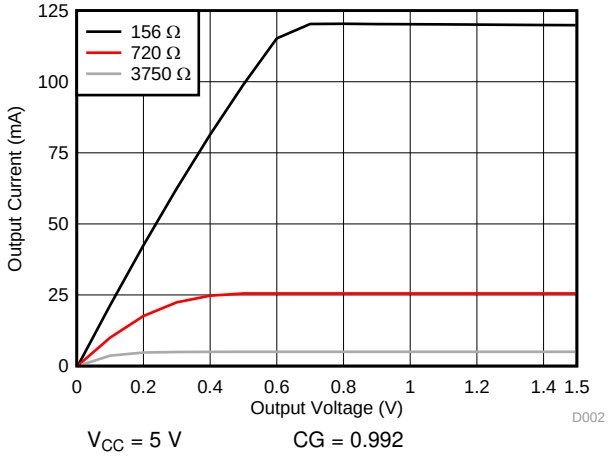


Figure 2. Output Current vs Output Voltage across Output Current

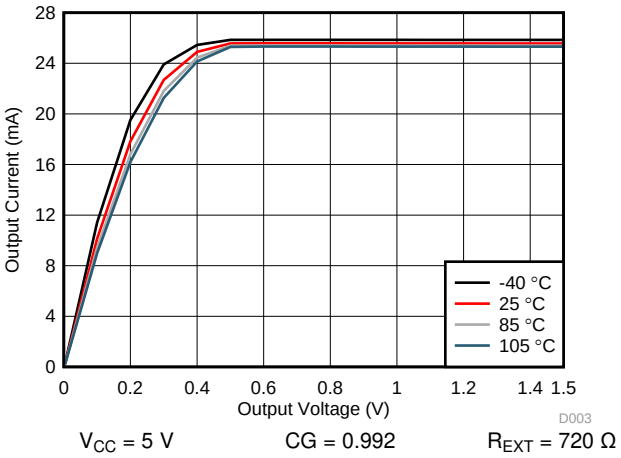


Figure 3. Output Current vs Output Voltage across Temp

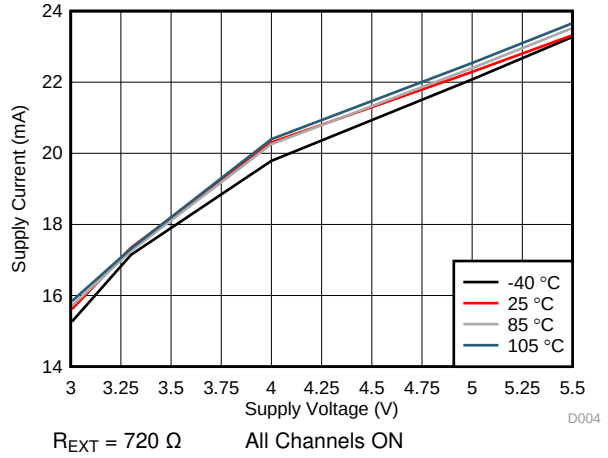


Figure 4. I_{CC} vs V_{CC} across Temp

8 Parameter Measurement Information

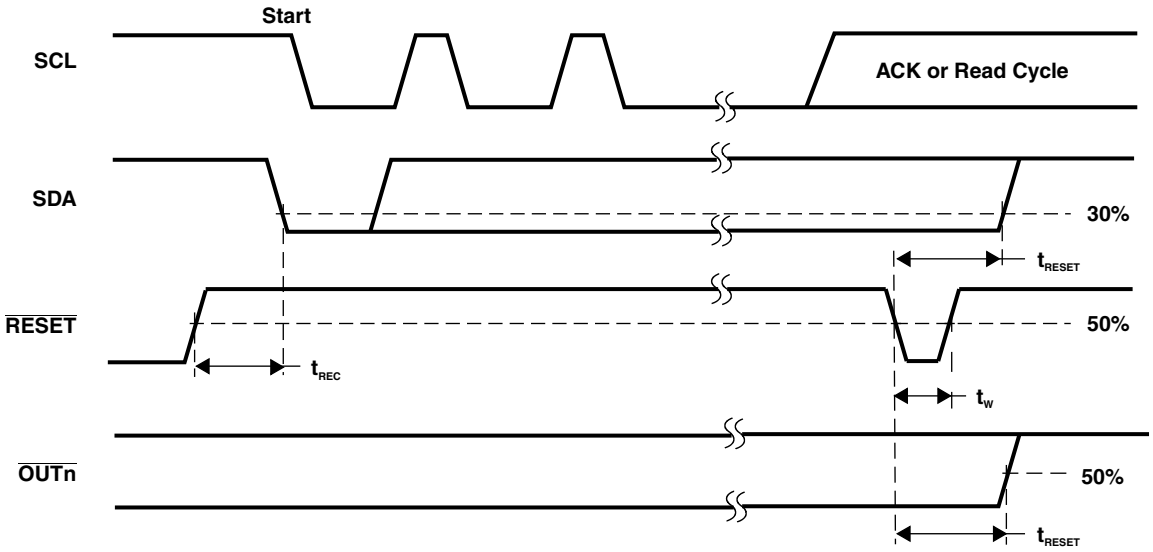


Figure 5. Reset Timing

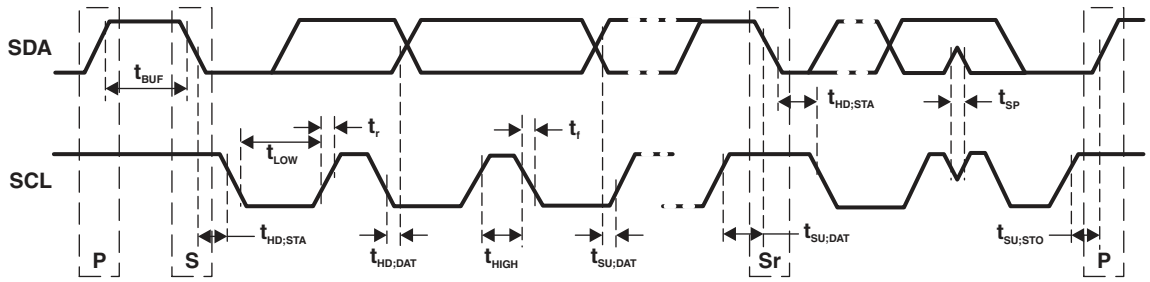
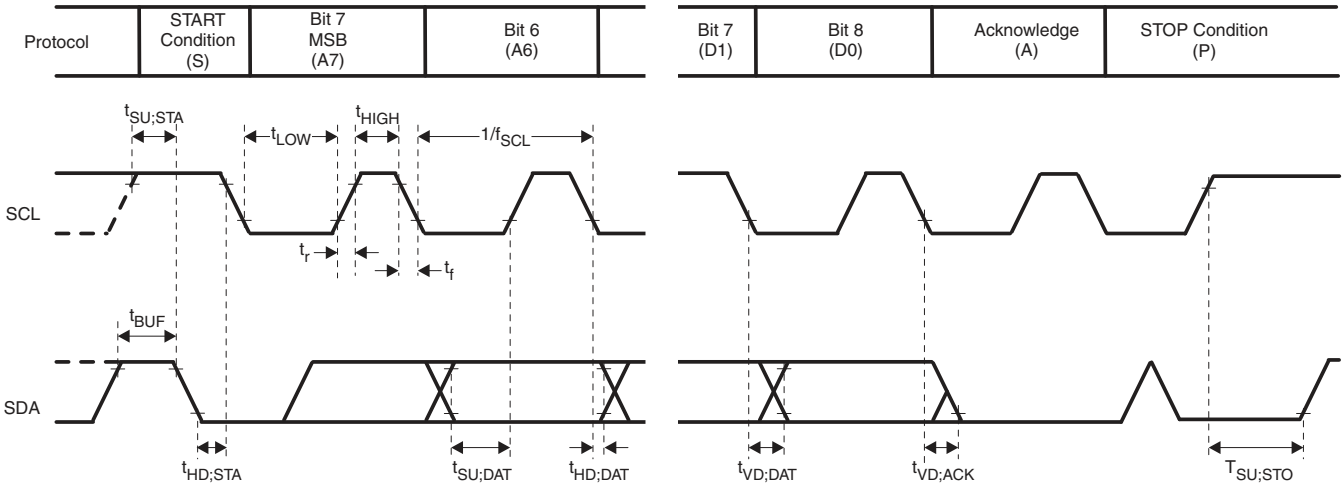


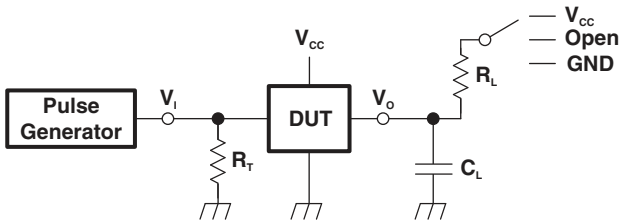
Figure 6. Definition of Timing



NOTE: Rise and fall times refer to V_{IL} and V_{IH}.

Figure 7. I²C Bus Timing

Parameter Measurement Information (continued)



NOTE:

- R_L = Load resistance for SDA and SCL; should be >1 kΩ at 3-mA or lower current
- C_L = Load capacitance; includes jig and probe capacitance
- R_T = Termination resistance; should be equal to the output impedance (Z_O) of the pulse generator

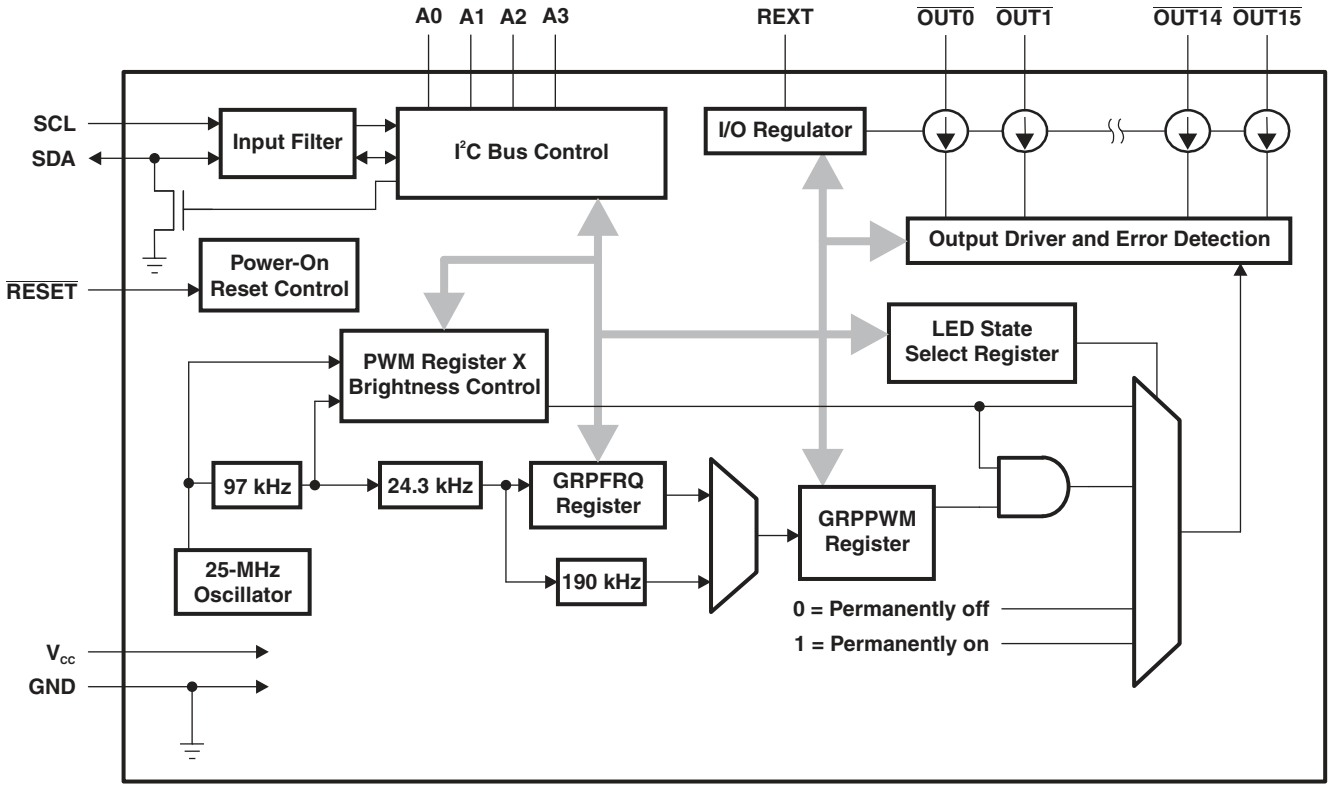
Figure 8. Test Circuit for Switching Characteristics

9 Detailed Description

9.1 Overview

The TLC59116-Q1 is an I²C Bus controlled 16-channel LED driver that is optimized for red/green/blue/amber (RGBA) color mixing and backlight application. Each LED output has its own 8-bit resolution (256 steps) fixed-frequency individual PWM controller that operates at 97-kHz, with a duty cycle that is adjustable from 0% to 99.6%. The individual PWM controller allows each LED to be set to a specific brightness value. An additional 8-bit resolution (256 steps) group PWM controller has both a fixed frequency of 190-Hz and an adjustable frequency between 24-Hz to once every 10.73 seconds, with a duty cycle that is adjustable from 0% to 99.6%. The group PWM controller dims or blinks all LEDs with the same value.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Open-Circuit Detection

The TLC59116-Q1 LED open-circuit detection compares the effective current level I_{OUT} with the open load detection threshold current $I_{OUT,Th}$. If I_{OUT} is below the threshold $I_{OUT,Th}$ the TLC59116-Q1 detects an open load condition. This error status can be read out as an error flag through the registers EFLAG1 and EFLAG2.

For open-circuit error detection, a channel must be on and the PWM must be off. See Table 1.

Feature Description (continued)

Table 1. Open-Circuit Detection

STATE OF OUTPUT PORT	CONDITION OF OUTPUT CURRENT	ERROR STATUS CODE	MEANING
Off	I_{OUT} = 0 mA	0	Detection not possible
On	$I_{OUT} < I_{OUT,Th}$ (1)	0	Open circuit
	$I_{OUT} \geq I_{OUT,Th}$ (1)	Channel n error status bit 1	Normal

(1) $I_{OUT,Th} = 0.5 \times I_{OUT,target}$ (typical)

9.3.2 Overtemperature Detection and Shutdown

The TLC59116-Q1 LED is equipped with a global overtemperature sensor and 16 individual channel-selective overtemperature sensors.

- When the global sensor reaches the trip temperature, all output channels are shut down, and the error status is stored in the internal Error Status register of every channel. After shutdown, the channels automatically restart after cooling down, if the control signal (output latch) remains on. The stored error status is not reset after cooling down and can be read out as the error status code in registers EFLAG1 and EFLAG2.
- When one of the channel-specific sensors reaches trip temperature, only the affected output channel is shut down, and the error status is stored only in the internal Error Status register of the affected channel. After shutdown, the channel automatically restarts after cooling down, if the control signal (output latch) remains on. The stored error status is not reset after cooling down and can be read out as error status code in registers EFLAG1 and EFLAG2.

For channel-specific overtemperature error detection, a channel must be on.

The error flags of open-circuit and overtemperature are ORed to set the EFLAG1 and EFLAG2 registers.

The error status code because of overtemperature is reset when the host writes 1 to bit 7 of the MODE2 register. The host must write 0 to bit 7 of the MODE2 register to enable the overtemperature error flag. See Table 2.

Table 2. Overtemperature Detection (1)

STATE OF OUTPUT PORT	CONDITION	ERROR STATUS CODE	MEANING
On On → all channels Off	$T_j < T_{j,trip}$ global	1	Normal
	$T_j > T_{j,trip}$ global	All error status bits = 0	Global overtemperature
On On → Off	$T_j < T_{j,trip}$ channel n	1	Normal
	$T_j > T_{j,trip}$ channel n	Channel n error status bit = 0	Channel n overtemperature

(1) The global shutdown threshold temperature is approximately 170°C.

9.3.3 Power-On Reset (POR)

When power is applied to V_{CC}, an internal power-on reset holds the TLC59116-Q1 in a reset condition until V_{CC} reaches V_{POR}. At this point, the reset condition is released and the TLC59116-Q1 registers, and I^2C Bus state machine are initialized to their default states (all zeroes), causing all the channels to be deselected. Thereafter, V_{CC} must be lowered below 0.2 V to reset the device.

9.3.4 External Reset

A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin low for a minimum of t_W. The TLC59116-Q1 registers and I^2C state machine are held in their default states until the $\overline{\text{RESET}}$ input is again high.

This input requires a pullup resistor to V_{CC} if no active connection is used.

9.3.5 Software Reset

The Software Reset Call (SWRST Call) allows all the devices in the I^2C Bus to be reset to the power-up state value through a specific I^2C Bus command.

The SWRST Call function is defined as the following:

1. A Start command is sent by the I^2C Bus master.

2. The reserved SWRST I^2C Bus address 1101 011 with the R/$\overline{W}$ bit set to 0 (write) is sent by the I^2C Bus master.
3. The TLC59116-Q1 device(s) acknowledge(s) after seeing the SWRST Call address 1101 0110 (D6h) only. If the R/$\overline{W}$ bit is set to 1 (read), no acknowledge is returned to the I^2C Bus master.
4. Once the SWRST Call address has been sent and acknowledged, the master sends two bytes with two specific values (SWRST data byte 1 and byte 2):
   (a) Byte1 = A5h: the TLC59116-Q1 acknowledges this value only. If byte 1 is not equal to A5h, the TLC59116-Q1 does not acknowledge it.
   (b) Byte 2 = 5Ah: the TLC59116-Q1 acknowledges this value only. If byte 2 is not equal to 5Ah, the TLC59116-Q1 does not acknowledge it.

   If more than two bytes of data are sent, the TLC59116-Q1 does not acknowledge any more.
5. Once the correct two bytes (SWRST data byte 1 and byte 2 only) have been sent and correctly acknowledged, the master sends a Stop command to end the SWRST Call. The TLC59116-Q1 then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time (t_{BUF}).

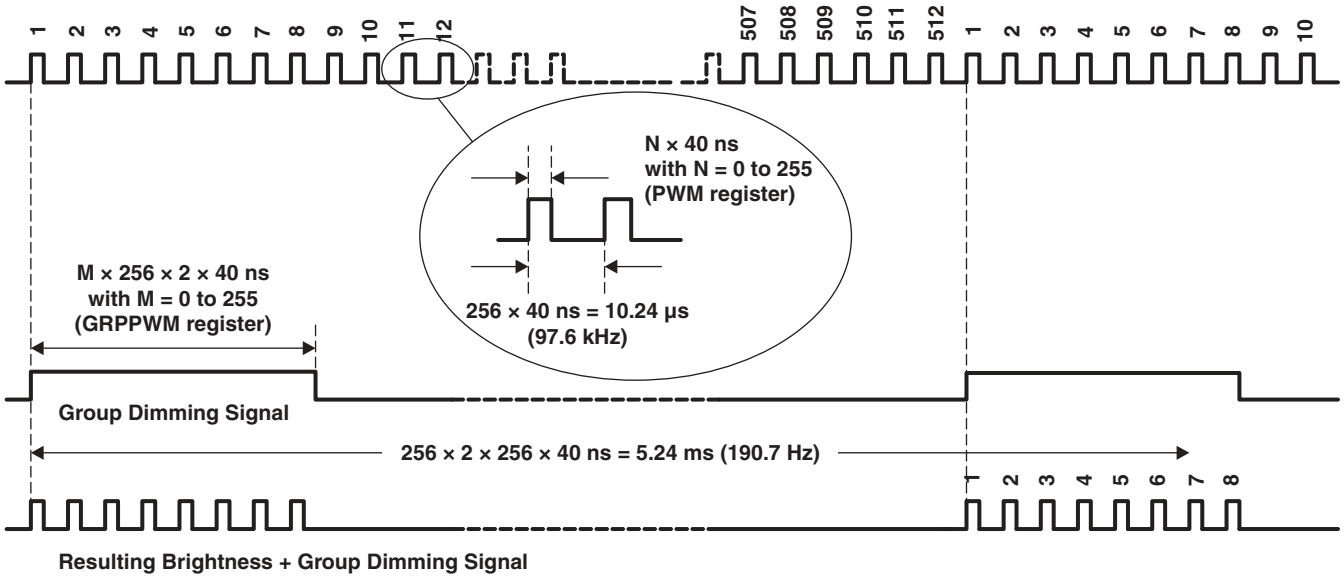
The I^2C Bus master may interpret a non-acknowledge from the TLC59116-Q1 (at any time) as a SWRST Call Abort. The TLC59116-Q1 does not initiate a reset of its registers. This happens only when the format of the Start Call sequence is not correct.

9.3.6 Individual Brightness Control With Group Dimming/Blinking

A 97-kHz fixed-frequency signal with programmable duty cycle (8 bits, 256 steps) is used to control the individual brightness for each LED.

On top of this signal, one of the following signals can be superimposed (this signal can be applied to the four LED outputs):

- A lower 190-Hz fixed-frequency signal with programmable duty cycle (8 bits, 256 steps) provides a global brightness control.
- A programmable frequency signal from 24-Hz to 1/10.73 s (8 bits, 256 steps) provides a global blinking control. See Figure 9.



NOTE:

- Minimum pulse width for LEDn brightness control is 40 ns.
- Minimum pulse width for group dimming is 20.48 µs.
- When M = 1 (GRPPWM register value), the resulting LEDn Brightness Control + Group Dimming signal has two pulses of the LED Brightness Control signal (pulse width = n × 40 ns, with n defined in the PWMx register).
- This resulting Brightness + Group Dimming signal shows a resulting control signal with M = 4 (8 pulses).

Figure 9. Brightness and Group Dimming Signals

9.4 Device Functional Modes

9.4.1 Active

Active mode occurs when one or more of the output channels is enabled.

9.4.2 Standby

Standby mode occurs when all output channels are disabled. Standby mode may be entered via I^2C command or by pulling the $\overline{\text{RESET}}$ pin low.

9.5 Programming

9.5.1 Characteristics of the I^2C Bus

The I^2C Bus is for two-way two-line communication between different devices or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

9.5.1.1 Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 10).

Programming (continued)

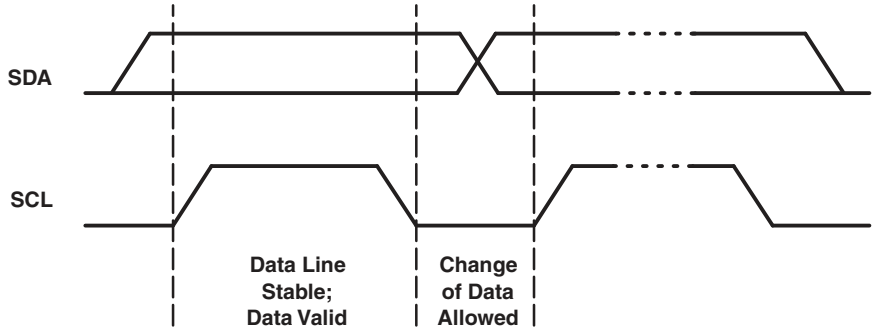


Figure 10. Bit Transfer

9.5.1.2 Start and Stop Conditions

Both data and clock lines remain high when the bus is not busy. A high-to-low transition of the data line while the clock is high is defined as the Start condition (S). A low-to-high transition of the data line while the clock is high is defined as the Stop condition (P) (see Figure 11).

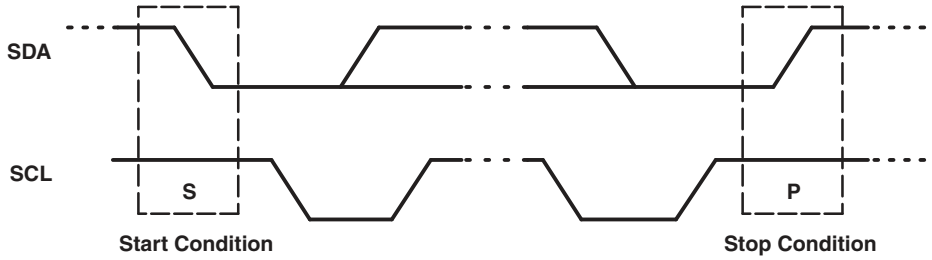


Figure 11. Start and Stop Conditions

9.5.1.3 Acknowledge

The number of data bytes transferred between the Start and the Stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a high level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse. See Figure 12.

A slave receiver that is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable low during the high period of the acknowledge related clock pulse; set-up time and hold time must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line high to enable the master to generate a Stop condition. See Figure 13.

Programming (continued)

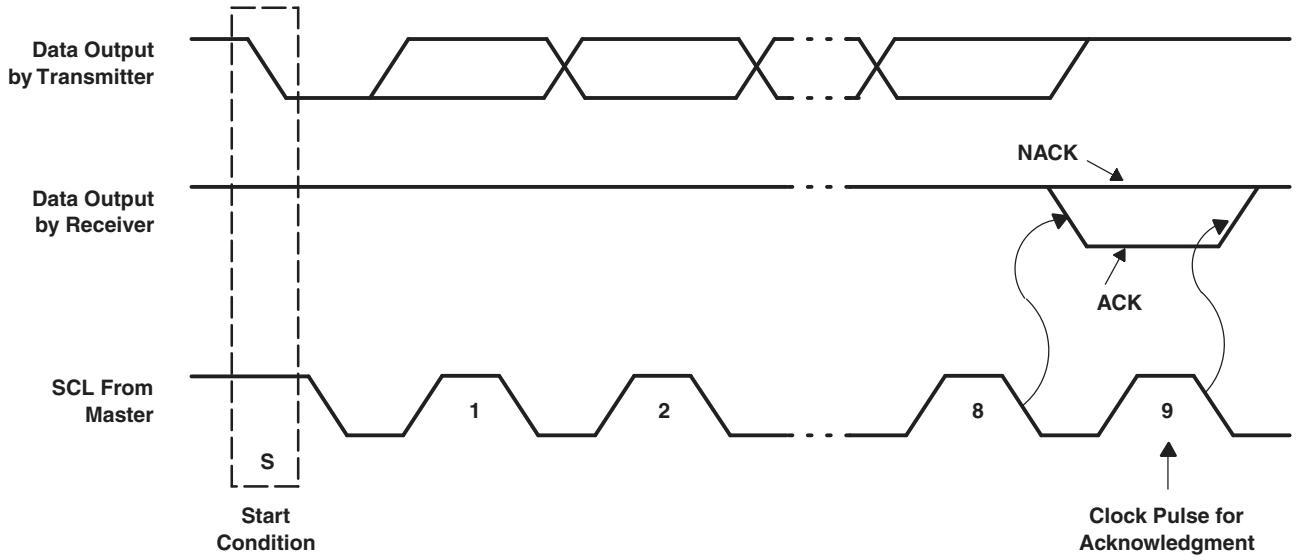


Figure 12. Acknowledge/Not Acknowledge on I²C Bus

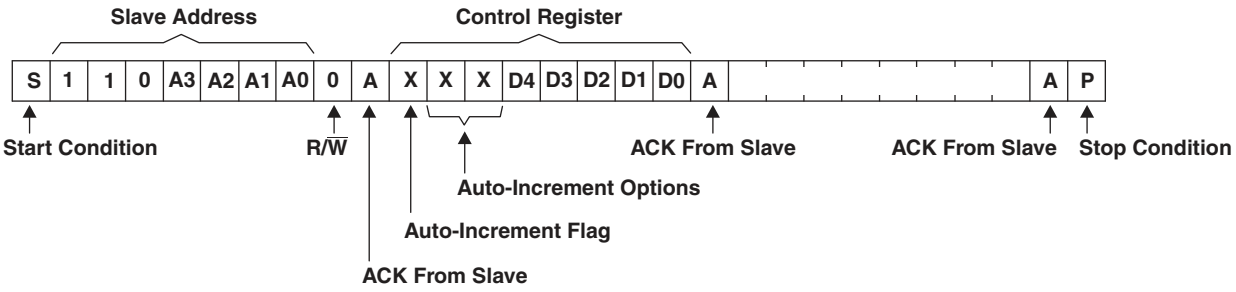
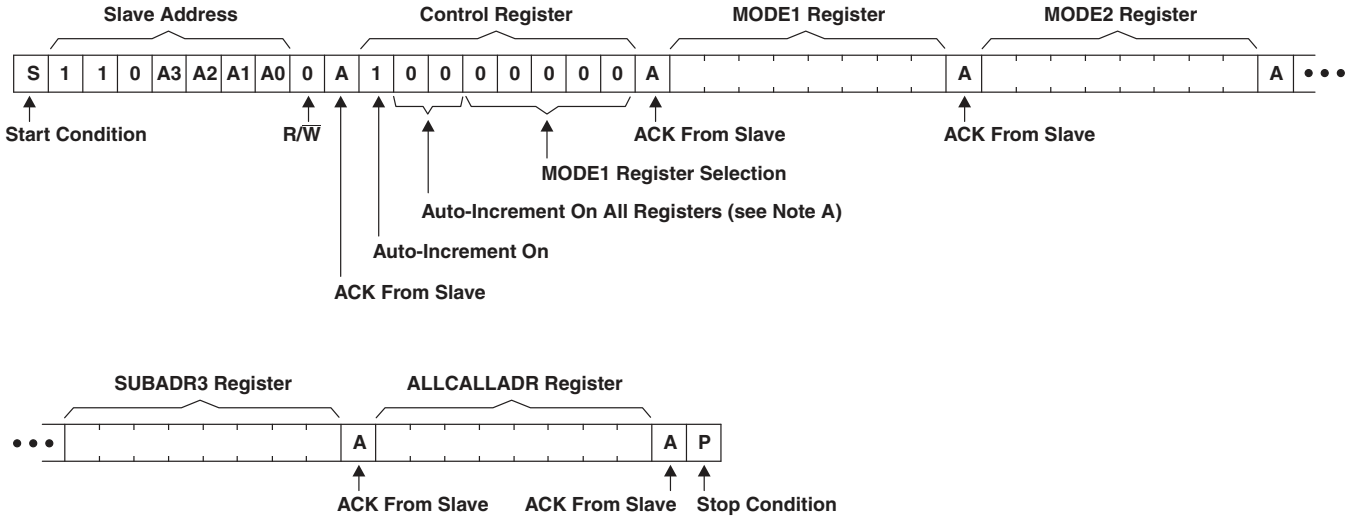


Figure 13. Write to a Specific Register



See Table 4 for register definitions.

Figure 14. Write to All Registers Using Auto-Increment

Programming (continued)

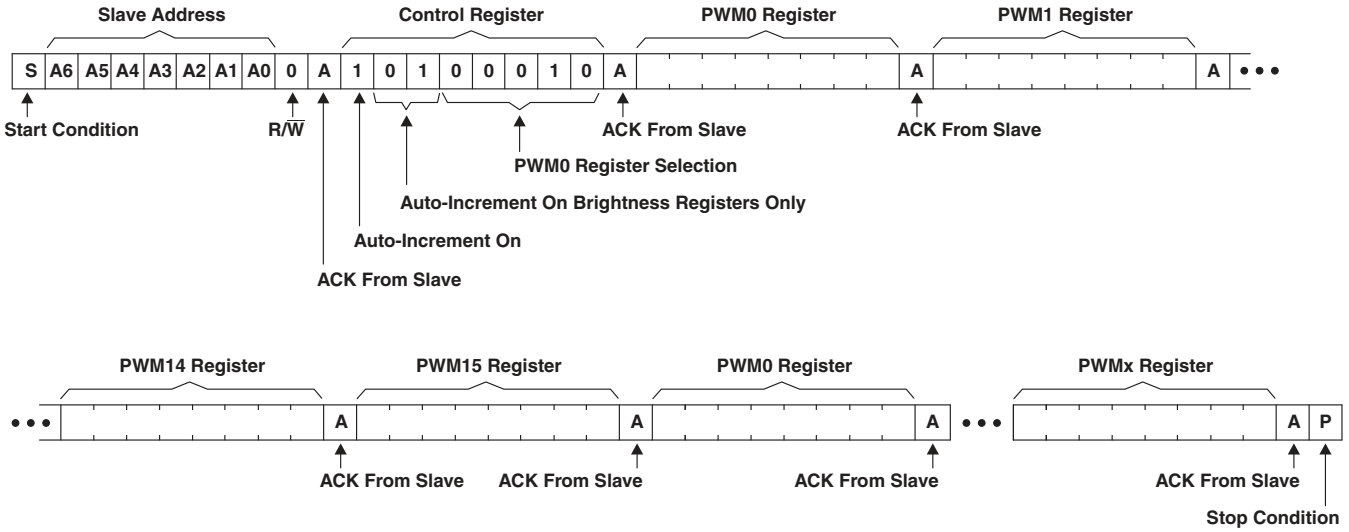


Figure 15. Multiple Writes to Individual Brightness Registers Using Auto-Increment

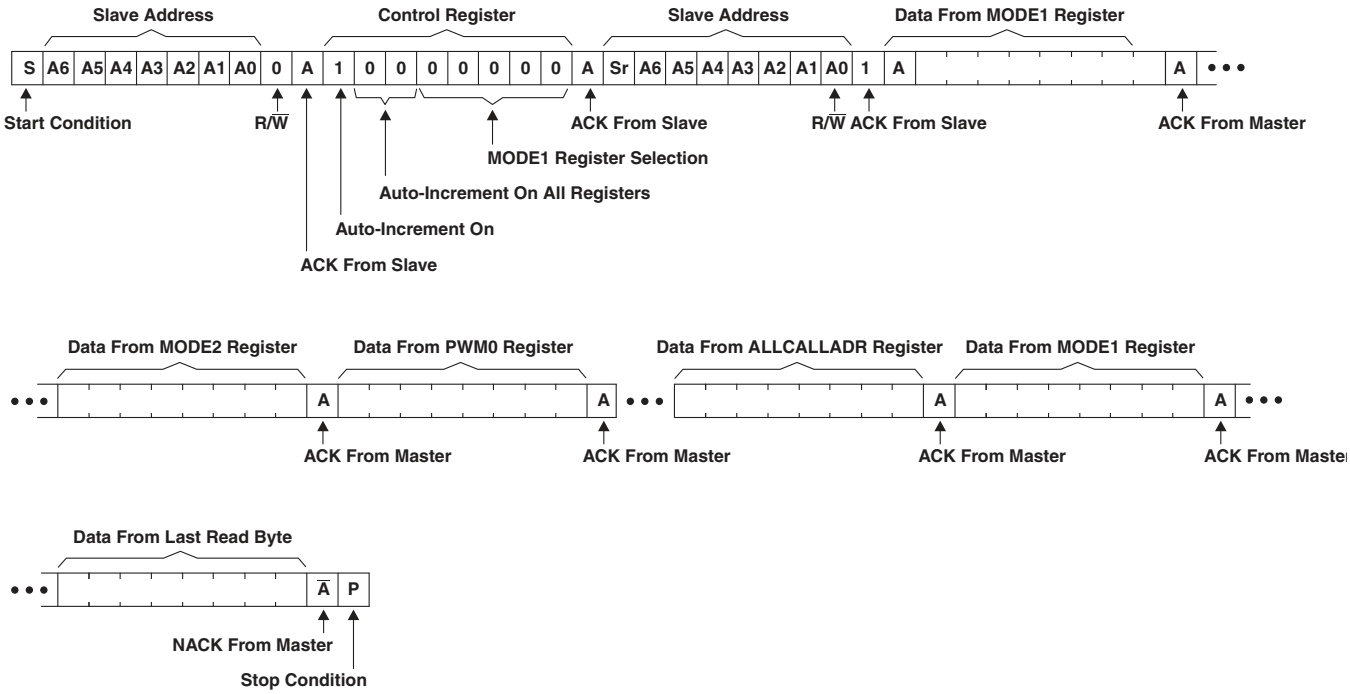
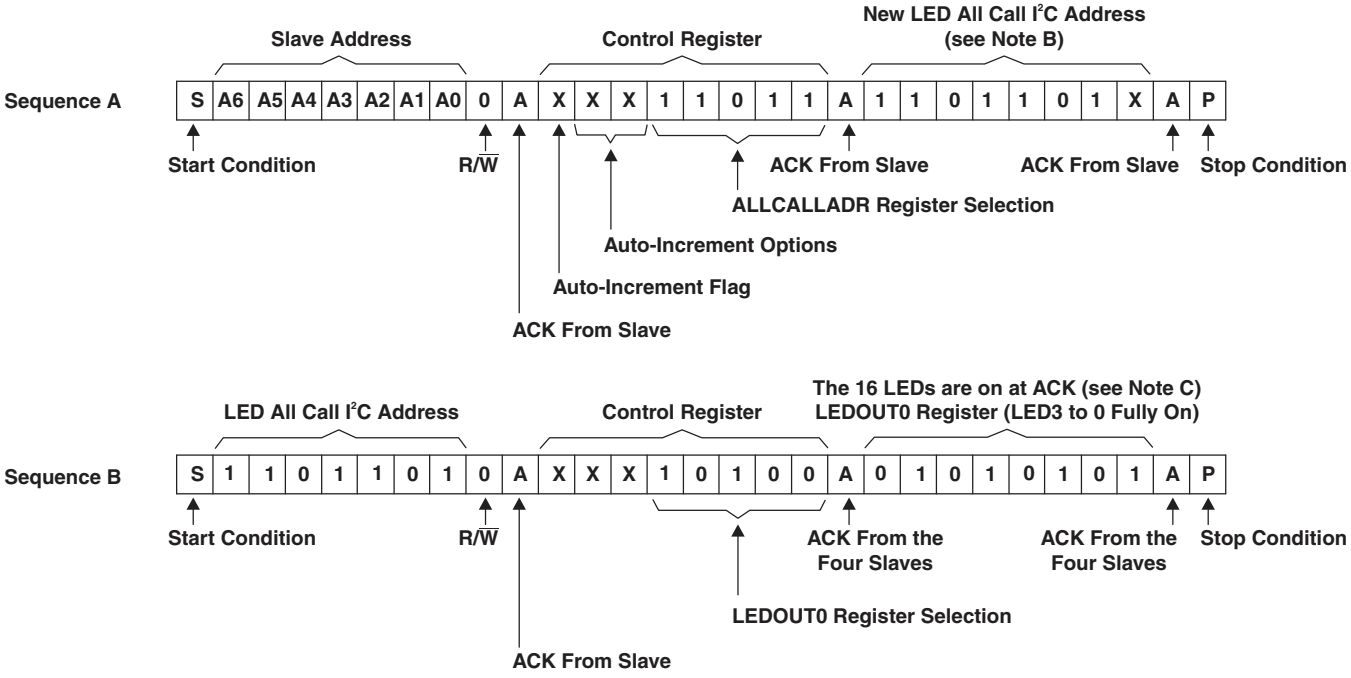


Figure 16. Read All Registers Auto-Increment

Programming (continued)



A. In this example, several TLC59116-Q1 devices are used, and the same Sequence A is sent to each of them.

B. The ALLCALL bit in the MODE1 register is equal to 1 for this example.

C. The OCH bit in the MODE2 register is equal to 1 for this example.

Figure 17. LED All Call I²C Bus Address Programming and LED All Call Sequence

9.5.2 System Configuration

A device generating a message is a transmitter; a device receiving is the receiver. The device that controls the message is the master and the devices that are controlled by the master are the slaves (see Figure 18).

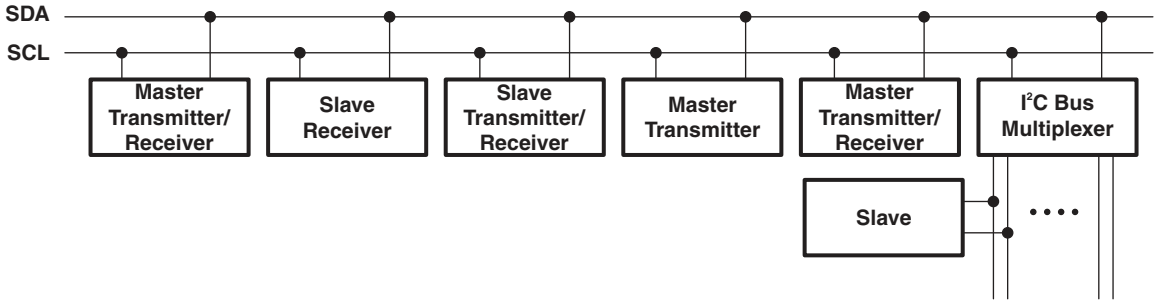


Figure 18. System Configuration

9.5.3 Device Address

Following a Start condition, the bus master must output the address of the slave it is accessing.

9.5.4 Regular I²C Bus Slave Address

The I²C Bus slave address of the TLC59116-Q1 is shown in Figure 19. To conserve power, no internal pullup resistors are incorporated on the hardware-selectable address pins, and they must be pulled high or low. For buffer management purposes, a set of sector information data should be stored.

Programming (continued)

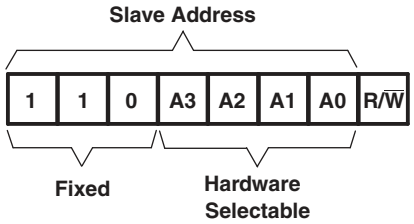


Figure 19. Slave Address

The last bit of the address byte defines the operation to be performed. When set to logic 1, a read operation is selected. When set to logic 0, a write operation is selected.

9.5.5 LED All Call I²C Bus Address

- Default power-up value (ALLCALLADR register): D0h or 1101 000
- Programmable through I²C Bus (volatile programming)
- At power-up, LED All Call I²C Bus address is enabled. TLC59116-Q1 sends an ACK when D0h (R/$\overline{W}$ = 0) or D1h (R/$\overline{W}$ = 1) is sent by the master.

See *LED All Call I2C Bus Address Register (ALLCALLADR)* for more detail.

NOTE

The default LED All Call I²C Bus address (D0h or 1101 000) must not be used as a regular I²C Bus slave address, since this address is enabled at power-up. All the TLC59116-Q1 devices on the I²C Bus will acknowledge the address if it is sent by the I²C Bus master.

Programming (continued)

9.5.6 LED Sub Call I²C Bus Address

- Three different I²C Bus addresses can be used
- Default power-up values:
  - SUBADR1 register: D2h or 1101 001
  - SUBADR2 register: D4h or 1101 010
  - SUBADR3 register: D8h or 1101 100
- Programmable through I²C Bus (volatile programming)
- At power-up, Sub Call I²C Bus address is disabled. TLC59116-Q1 does not send an ACK when D2h (R/$\overline{W}$ = 0) or D3h (R/$\overline{W}$ = 1) or D4h (R/$\overline{W}$ = 0) or D5h (R/$\overline{W}$ = 1) or D8h (R/$\overline{W}$ = 0) or D9h (R/$\overline{W}$ = 1) is sent by the master.

See *I2C Bus Subaddress Registers 1 to 3 (SUBADR1 to SUBADR3)* for more detail.

NOTE

The LED Sub Call I²C Bus addresses may be used as regular I²C Bus slave addresses if their corresponding enable bits are set to 0 in the *MODE1 Register*.

9.5.7 Software Reset I²C Bus Address

The address shown in Figure 20 is used when a reset of the TLC59116-Q1 is performed by the master. The software reset address (SWRST Call) must be used with R/$\overline{W}$ = 0. If R/$\overline{W}$ = 1, the TLC59116-Q1 does not acknowledge the SWRST. See *Software Reset* for more detail.

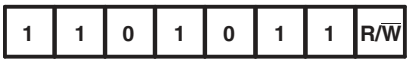


Figure 20. Software Reset Address

NOTE

The Software Reset I²C Bus address is reserved address and cannot be use as regular I²C Bus slave address or as an LED All Call or LED Sub Call address.

9.5.8 Control Register

Following the successful acknowledgment of the slave address, LED All Call address or LED Sub Call address, the bus master sends a byte to the TLC59116-Q1, which is stored in the Control register. The lowest five bits are used as a pointer to determine which register is accessed (D[4:0]). The highest three bits are used as auto-increment flag and auto-increment options (AI[2:0]). See Figure 21.

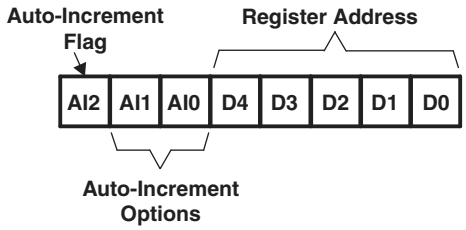


Figure 21. Control Register

When the auto-increment flag is set (AI2 = logic 1), the five low order bits of the Control register are automatically incremented after a read or write. This allows the user to program the registers sequentially. Four different types of auto-increment are possible, depending on AI1 and AI0 values as shown in Table 3.

Programming (continued)

Table 3. Auto-Increment Options

AI2	AI1	AI0	DESCRIPTION
0	0	0	No auto-increment
1	0	0	Auto-increment for all registers. D[4:0] roll over to 0 0000 after the last register (1 1011) is accessed.
1	0	1	Auto-increment for individual brightness registers only. D[4:0] roll over to 0 0010 after the last register (1 0001) is accessed.
1	1	0	Auto-increment for global control registers only. D[4:0] roll over to 1 0010 after the last register (1 0011) is accessed.
1	1	1	Auto-increment for individual and global control registers only. D[4:0] roll over to 0 0010 after the last register (1 0011) is accessed.

NOTE

Other combinations are not shown in Table 3. (AI[2:0] = 001, 010, and 011) are reserved and must not be used for proper device operation.

AI[2:0] = 000 is used when the same register must be accessed several times during a single I^2C Bus communication, for example, changing the brightness of a single LED. Data is overwritten each time the register is accessed during a write operation.

AI[2:0] = 100 is used when all the registers must be sequentially accessed, for example, power-up programming.

AI[2:0] = 101 is used when the four LED drivers must be individually programmed with different values during the same I^2C Bus communication, for example, changing a color setting to another color setting.

AI[2:0] = 110 is used when the LED drivers must be globally programmed with different settings during the same I^2C Bus communication, for example, global brightness or blinking change.

AI[2:0] = 111 is used when individually and global changes must be performed during the same I^2C Bus communication, for example, changing color and global brightness at the same time.

Only the five least significant bits D[4:0] are affected by the AI[2:0] bits.

When the Control register is written, the register entry point determined by D[4:0] is the first register that will be addressed (read or write operation), and can be anywhere between 0 0000 and 1 1011 (as defined in Table 4). When AI[2] = 1, the Auto-Increment flag is set and the rollover value at which the point where the register increment stops and goes to the next one is determined by AI[2:0]. See Table 3 for rollover values. For example, if the Control register = 1111 0100 (F4h), then the register addressing sequence will be (in hex):

14 → ... → 1B → 00 → ... → 13 → 02 → ... → 13 → 02 → ... as long as the master keeps sending or reading data.

9.6 Register Maps

Table 4 describes the registers in the TLC59116-Q1.

Table 4. Register Descriptions

REGISTER NUMBER (HEX)	NAME	ACCESS (1)	DESCRIPTION
00	MODE1	R/W	Mode 1
01	MODE2	R/W	Mode 2
02	PWM0	R/W	Brightness control LED0
03	PWM1	R/W	Brightness control LED1
04	PWM2	R/W	Brightness control LED2
05	PWM3	R/W	Brightness control LED3
06	PWM4	R/W	Brightness control LED4

(1) R = read, W = write

Register Maps (continued)

Table 4. Register Descriptions (continued)

REGISTER NUMBER (HEX)	NAME	ACCESS (1)	DESCRIPTION
07	PWM5	R/W	Brightness control LED5
08	PWM6	R/W	Brightness control LED6
09	PWM7	R/W	Brightness control LED7
0A	PWM8	R/W	Brightness control LED8
0B	PWM9	R/W	Brightness control LED9
0C	PWM10	R/W	Brightness control LED10
0D	PWM11	R/W	Brightness control LED11
0E	PWM12	R/W	Brightness control LED12
0F	PWM13	R/W	Brightness control LED13
10	PWM14	R/W	Brightness control LED14
11	PWM15	R/W	Brightness control LED15
12	GRPPWM	R/W	Group duty cycle control
13	GRPFREQ	R/W	Group frequency
14	LEDOUT0	R/W	LED output state 0
15	LEDOUT1	R/W	LED output state 1
16	LEDOUT2	R/W	LED output state 2
17	LEDOUT3	R/W	LED output state 3
18	SUBADR1	R/W	I^2C Bus subaddress 1
19	SUBADR2	R/W	I^2C Bus subaddress 2
1A	SUBADR3	R/W	I^2C Bus subaddress 3
1B	ALLCALLADR	R/W	LED All Call I^2C Bus address
1C	IREF	R/W	IREF configuration
1D	EFLAG1	R	Error flags 1
1E	EFLAG2	R	Error flags 2

9.6.1 Mode Register 1 (MODE1)

Table 5 describes Mode Register 1.

Table 5. MODE1 – Mode Register 1 (Address 00h) Bit Description

BIT	SYMBOL	ACCESS (1)	VALUE	DESCRIPTION
7	AI2	R	0 (2)	Register auto-increment disabled
			1	Register auto-increment enabled
6	AI1	R	0 (2)	Auto-increment bit 1 = 0
			1	Auto-increment bit 1 = 1
5	AI0	R	0 (2)	Auto-increment bit 0 = 0
			1	Auto-increment bit 0 = 1
4	OSC	R/W	0	Normal mode (3)
			1 (2)	Oscillator off.
3	SUB1	R/W	0 (2)	Device does not respond to I^2C Bus subaddress 1.
			1	Device responds to I^2C Bus subaddress 1.
2	SUB2	R/W	0 (2)	Device does not respond to I^2C Bus subaddress 2.
			1	Device responds to I^2C Bus subaddress 2.
1	SUB3	R/W	0 (2)	Device does not respond to I^2 CBus subaddress 3.
			1	Device responds to I^2C Bus subaddress 3.
0	ALLCALL	R/W	0	Device does not respond to LED All Call I^2C Bus address.
			1 (2)	Device responds to LED All Call I^2C Bus address.

(1) R = read, W = write
(2) Default value
(3) Requires 500 µs maximum for the oscillator to be up and running once OSC bit has been set to logic 1. Timings on LED outputs are not ensured if PWMx, GRPPWM, or GRPFREQ registers are accessed within the 500-µs window.

NOTE

The OSC bit (Bit 4) must be set to 0 before any outputs will turn on. Proper operation requires this bit to be 0. Setting the bit to a 1 will turn all channels off.

9.6.2 Mode Register 2 (MODE2)

Table 6 describes Mode Register 2.

Table 6. MODE2 – Mode Register 2 (Address 01h) Bit Description

BIT	SYMBOL	ACCESS (1)	VALUE	DESCRIPTION
7	EFCLR	R/W	0 (2)	Enable error status flag
			1	Clear error status flag
6		R	0 (2)	Reserved
5	DMBLNK	R/W	0 (2)	Group control = dimming
			1	Group control = blinking
4		R	0 (2)	Reserved
3	OCH	R/W	0 (2)	Outputs change on Stop command (3)
			1	Outputs change on ACK
2:0		R	000 (2)	Reserved

(1) R = read, W = write
(2) Default value
(3) Change of the outputs at the Stop command allows synchronizing outputs of more than one TLC59116-Q1. Applicable to registers from 02h (PWM0) to 17h (LEDOUT3) only.

9.6.3 Brightness Control Registers 0 to 15 (PWM0 to PWM15)

Table 7 describes Brightness Control Registers 0 to 15.

Table 7. PWM0 to PWM15 – Brightness Control Registers 0 to 15 (Address 02h to 11h) Bit Description

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS (1)	VALUE	DESCRIPTION
02h	PWM0	7:0	IDC0[7:0]	R/W	0000 0000 (2)	PWM0 individual duty cycle
03h	PWM1	7:0	IDC1[7:0]	R/W	0000 0000 (2)	PWM1 individual duty cycle
04h	PWM2	7:0	IDC2[7:0]	R/W	0000 0000 (2)	PWM2 individual duty cycle
05h	PWM3	7:0	IDC3[7:0]	R/W	0000 0000 (2)	PWM3 individual duty cycle
06h	PWM4	7:0	IDC4[7:0]	R/W	0000 0000 (2)	PWM4 individual duty cycle
07h	PWM5	7:0	IDC5[7:0]	R/W	0000 0000 (2)	PWM5 individual duty cycle
08h	PWM6	7:0	IDC6[7:0]	R/W	0000 0000 (2)	PWM6 individual duty cycle
09h	PWM7	7:0	IDC7[7:0]	R/W	0000 0000 (2)	PWM7 individual duty cycle
0Ah	PWM8	7:0	IDC8[7:0]	R/W	0000 0000 (2)	PWM8 individual duty cycle
0Bh	PWM9	7:0	IDC9[7:0]	R/W	0000 0000 (2)	PWM9 individual duty cycle
0Ch	PWM10	7:0	IDC10[7:0]	R/W	0000 0000 (2)	PWM10 individual duty cycle
0Dh	PWM11	7:0	IDC11[7:0]	R/W	0000 0000 (2)	PWM11 individual duty cycle
0Eh	PWM12	7:0	IDC12[7:0]	R/W	0000 0000 (2)	PWM12 individual duty cycle
0Fh	PWM13	7:0	IDC13[7:0]	R/W	0000 0000 (2)	PWM13 individual duty cycle
10h	PWM14	7:0	IDC14[7:0]	R/W	0000 0000 (2)	PWM14 individual duty cycle
11h	PWM15	7:0	IDC15[7:0]	R/W	0000 0000 (2)	PWM15 individual duty cycle

(1) R = read, W = write
(2) Default value

A 97-kHz fixed frequency signal is used for each output. Duty cycle is controlled through 256 linear steps from 00h (0% duty cycle = LED output off) to FFh (99.6% duty cycle = LED output at maximum brightness). Applicable to LED outputs programmed with LDRx = 10 or 11 (LEDOUT0, LEDOUT1, LEDOUT2 and LEDOUT3 registers).

$$\text{Duty cycle} = \text{IDCn}[7:0] / 256 \quad (1)$$

9.6.4 Group Duty Cycle Control Register (GRPPWM)

Table 8 describes the Group Duty Cycle Control Register.

Table 8. GRPPWM – Group Brightness Control Register (Address 12h) Bit Description

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS (1)	VALUE	DESCRIPTION
12h	GRPPWM	7:0	GDC0[7:0]	R/W	1111 1111 (2)	GRPPWM register

(1) R = read, W = write
(2) Default value

When the DMBLNK bit (MODE2 register) is programmed with logic 0, a 190-Hz fixed-frequency signal is superimposed with the 97-kHz individual brightness control signal. GRPPWM is then used as a global brightness control, allowing the LED outputs to be dimmed with the same value. The value in GRPFREQ is then a Don't care.

General brightness for the 16 outputs is controlled through 256 linear steps from 00h (0% duty cycle = LED output off) to FFh (99.6% duty cycle = maximum brightness). This is applicable to LED outputs programmed with LDRx = 11 (LEDOUT0, LEDOUT1, LEDOUT2 and LEDOUT3 registers).

When DMBLNK bit is programmed with logic 1, the GRPPWM and GRPFREQ registers define a global blinking pattern, where GRPFREQ defines the blinking period (from 24-Hz to 10.73 s) and GRPPWM defines the duty cycle (ON/OFF ratio in %).

$$\text{Duty cycle} = \text{GDC0}[7:0] / 256 \quad (2)$$

9.6.5 Group Frequency Register (GRPFREQ)

Table 9 describes the Group Frequency Register.

Table 9. GRPFREQ – Group Frequency Register (Address 13h) Bit Description

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS (1)	VALUE	DESCRIPTION
13h	GRPFREQ	7:0	GFRQ[7:0]	R/W	0000 0000 (2)	GRPFREQ register

(1) R = read, W = write
(2) Default value

GRPFREQ is used to program the global blinking period when the DMBLNK bit (MODE2 register) is equal to 1. Value in this register is a Don't care when DMBLNK = 0. This is applicable to LED output programmed with LDRx = 11 (LEDOUT0, LEDOUT1, LEDOUT2 and LEDOUT3 registers).

The blinking period is controlled through 256 linear steps from 00h (41 ms, frequency 24 Hz) to FFh (10.73 s).

Global blinking period (seconds) = (GFRQ[7:0] + 1) / 24

9.6.6 LED Driver Output State Registers 0 to 3 (LEDOUT0 to LEDOUT3)

Table 10 describes LED Driver Output State Registers 0 to 3.

Table 10. LEDOUT0 to LEDOUT3 – LED Driver Output State Registers 0 to 3 (Address 14h to 17h) Bit Description

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS (1)	VALUE	DESCRIPTION
14h	LEDOUT0	7:6	LDR3[1:0]	R/W	00 (2)	LED3 output state control
		5:4	LDR2[1:0]	R/W	00 (2)	LED2 output state control
		3:2	LDR1[1:0]	R/W	00 (2)	LED1 output state control
		1:0	LDR0[1:0]	R/W	00 (2)	LED0 output state control
15h	LEDOUT1	7:6	LDR7[1:0]	R/W	00 (2)	LED7 output state control
		5:4	LDR6[1:0]	R/W	00 (2)	LED6 output state control
		3:2	LDR5[1:0]	R/W	00 (2)	LED5 output state control
		1:0	LDR4[1:0]	R/W	00 (2)	LED4 output state control
16h	LEDOUT2	7:6	LDR11[1:0]	R/W	00 (2)	LED11 output state control
		5:4	LDR10[1:0]	R/W	00 (2)	LED10 output state control
		3:2	LDR9[1:0]	R/W	00 (2)	LED9 output state control
		1:0	LDR8[1:0]	R/W	00 (2)	LED8 output state control
17h	LEDOUT3	7:6	LDR15[1:0]	R/W	00 (2)	LED15 output state control
		5:4	LDR14[1:0]	R/W	00 (2)	LED14 output state control
		3:2	LDR13[1:0]	R/W	00 (2)	LED13 output state control
		1:0	LDR12[1:0]	R/W	00 (2)	LED12 output state control

(1) R = read, W = write
(2) Default value

LDRx = 00: LED driver x is off (default power-up state).

LDRx = 01: LED driver x is fully on (individual brightness and group dimming/blinking not controlled).

LDRx = 10: LED driver x is individual brightness can be controlled through its PWMx register.

LDRx = 11: LED driver x is individual brightness and group dimming/blinking can be controlled through its PWMx register and the GRPPWM registers.

9.6.7 I²C Bus Subaddress Registers 1 to 3 (SUBADR1 to SUBADR3)

Table 11 describes I²C Bus Subaddress Registers 1 to 3.

Table 11. SUBADR1 to SUBADR3 – I²C Bus Subaddress Registers 1 to 3 (Address 18h to 1Ah) Bit Description

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS (1)	VALUE	DESCRIPTION
18h	SUBADR1	7:1	A1[7:1]	R/W	1101 001 (2)	I²C Bus subaddress 1
		0	A1[0]	R	0 (2)	Reserved
19h	SUBADR2	7:1	A2[7:1]	R/W	1101 010 (2)	I²C Bus subaddress 2
		0	A2[0]	R	0 (2)	Reserved
1Ah	SUBADR3	7:1	A3[7:1]	R/W	1101 100 (2)	I²C Bus subaddress 3
		0	A3[0]	R	0 (2)	Reserved

(1) R = read, W = write
(2) Default value

Subaddresses are programmable through the I²C Bus. Default power-up values are D2h, D4h, D8h. The TLC59116-Q1 does not acknowledge these addresses immediately after power-up (the corresponding SUBx bit in MODE1 register is equal to 0).

Once subaddresses have been programmed to valid values, the SUBx bits (MODE1 register) must be set to 1 to allows the device to acknowledge these addresses.

Only the 7 MSBs representing the I²C Bus subaddress are valid. The LSB in SUBADRx register is a read-only bit (0).

When SUBx is set to 1, the corresponding I²C Bus subaddress can be used during either an I²C Bus read or write sequence.

9.6.8 LED All Call I²C Bus Address Register (ALLCALLADR)

Table 12 describes the LED All Call I²C Bus Address Register.

Table 12. ALLCALLADR – LED All Call I²C Bus Address Register (Address 1Bh) Bit Description

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS (1)	VALUE	DESCRIPTION
1Bh	ALLCALLADR	7:1	AC[7:1]	R/W	1101 000 (2)	All Call I²C Bus address
		0	AC[0]	R	0 (2)	Reserved

(1) R = read, W = write
(2) Default value

The LED All Call I²C Bus address allows all the TLC59116-Q1 devices in the bus to be programmed at the same time (ALLCALL bit in register MODE1 must be equal to 1, which is the power-up default state). This address is programmable through the I²C Bus and can be used during either an I²C Bus read or write sequence. The register address can also be programmed as a Sub Call.

Only the seven MSBs representing the All Call I²C bus address are valid. The LSB in ALLCALLADR register is a read-only bit (0).

If ALLCALL bit = 0, the device does not acknowledge the address programmed in register ALLCALLADR.

9.6.9 Output Gain Control Register (IREF)

Table 13 describes the Output Gain Control Register.

Table 13. IREF – Output Gain Control Register (Address 1Ch) Bit Description

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS (1)	VALUE	DESCRIPTION
1Ch	IREF	7	CM	R/W	1 (2)	High/low current multiplier
		6	HC	R/W	1 (2)	Subcurrent
		5:0	CC[5:0]	R/W	11 1111 (2)	Current multiplier

(1) R = read, W = write
(2) Default value

IREF determines the voltage gain (VG), which affects the voltage at the REXT terminal and indirectly the reference current (I_{ref}) flowing through the external resistor at terminal REXT. Bit 0 is the Current Multiplier (CM) bit, which determines the ratio $I_{OUT,target}/I_{ref}$. Each combination of VG and CM sets a Current Gain (CG).

- VG: the relationship between {HC,CC[0:5]} and the voltage gain is calculated as shown:
  $VG = (1 + HC) \times (1 + D/64) / 4$
  $D = CC0 \times 2^5 + CC1 \times 2^4 + CC2 \times 2^3 + CC3 \times 2^2 + CC4 \times 2^1 + CC5 \times 2^0$
  Where HC is 1 or 0, and D is the binary value of CC[0:5]. So, the VG could be regarded as a floating-point number with 1-bit exponent HC and 6-bit mantissa CC[0:5]. {HC,CC[0:5]} divides the programmable voltage gain (VG) into 128 steps and two sub-bands:
  Low-voltage subband (HC = 0): VG = 1/4 to 127/256, linearly divided into 64 steps
  High-voltage subband (HC = 1): VG = 1/2 to 127/128, linearly divided into 64 steps
- CM: In addition to determining the ratio $I_{OUT,target}/I_{ref}$, CM limits the output current range.
  High Current Multiplier (CM = 1): $I_{OUT,target}/I_{ref} = 15$, suitable for output current range I_{OUT} = 10 mA to 120 mA.
  Low Current Multiplier (CM = 0): $I_{OUT,target}/I_{ref} = 5$, suitable for output current range I_{OUT} = 5 mA to 40 mA
- CG: The total Current Gain is defined as:
  $V_{REXT} = 1.26\ V \times VG$
  $I_{ref} = V_{REXT}/R_{ext}$, if the external resistor (R_{ext}) is connected to ground.
  $I_{OUT,target} = I_{ref} \times 15 \times 3^{CM-1} = 1.26\ V/R_{ext} \times VG \times 15 \times 3^{CM-1} = (1.26\ V/R_{ext} \times 15) \times CG$
  $CG = VG \times 3^{CM-1}$
  Therefore, CG = (1/12) to (127/128), divided into 256 steps.

Examples

- IREF Code {CM, HC, CC[0:5]} = {1,1,111111}
  $VG = 127/128 = 0.992$ and $CG = VG \times 3^0 = VG = 0.992$
- IREF Code {CM, HC, CC[0:5]} = {1,1,000000}
  $VG = (1 + 1) \times (1 + 0/64)/4 = 1/2 = 0.5$, and $CG = 0.5$
- IREF Code {CM, HC, CC[0:5]} = {0,0,000000}
  $VG = (1 + 0) \times (1 + 0/64)/4 = 1/4$, and $CG = (1/4) \times 3^{-1} = 1/12$

After power-on, the default value of the Configuration Code {CM, HC, CC[0:5]} is {1,1,111111}. Therefore, VG = CG = 0.992. The relationship between the Configuration Code and the Current Gain is shown in Figure 22.

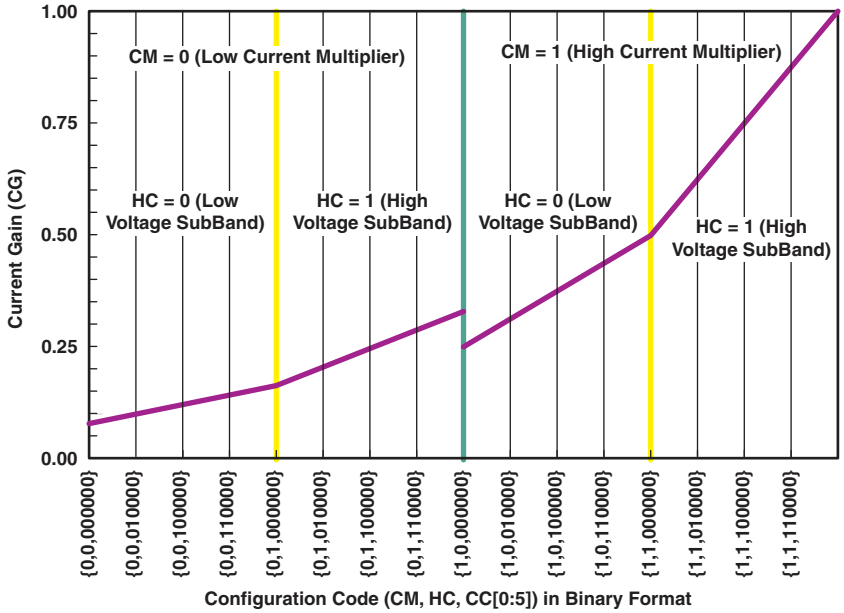


Figure 22. Current Gain vs Configuration Code

9.6.10 Error Flags Registers (EFLAG1, EFLAG2)

Table 14 describes Error Flags Registers 1 and 2.

Table 14. EFLAG1, EFLAG2 – Error Flags Registers (Address 1Dh and 1Eh) Bit Description

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS (1)	VALUE (2)	DESCRIPTION (3)
1Dh	EFLAG1	0	EFLAG1[0]	R	0	Channel 0
		1	EFLAG1[1]		0	Channel 1
		2	EFLAG1[2]		0	Channel 2
		3	EFLAG1[3]		0	Channel 3
		4	EFLAG1[4]		0	Channel 4
		5	EFLAG1[5]		0	Channel 5
		6	EFLAG1[6]		0	Channel 6
		7	EFLAG1[7]		0	Channel 7
1Eh	EFLAG2	0	EFLAG1[0]	R	0	Channel 8
		1	EFLAG1[1]		0	Channel 9
		2	EFLAG1[2]		0	Channel 10
		3	EFLAG1[3]		0	Channel 11
		4	EFLAG1[4]		0	Channel 12
		5	EFLAG1[5]		0	Channel 13
		6	EFLAG1[6]		0	Channel 14
		7	EFLAG1[7]		0	Channel 15

(1) R = read, W = write
(2) Default value
(3) At power-up, in order to initialize the Error Flags registers, the host must write 1 to bit 7 of the MODE2 register and then write 0 to bit 7 of the MODE2 register.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Constant Current Output

In LED display applications, TLC59116-Q1 provides nearly no current variations from channel to channel and from device to device. While $I_{OUT} \leq 52$ mA, the maximum current skew between channels is less than ±6% and less than ±10% between devices.

10.1.2 Adjusting Output Current

TLC59116-Q1 scales up the reference current (I_{ref}) set by the external resistor (R_{ext}) to sink the output current (I_{out}) at each output port. Table 13 shows the Configuration Code and discusses bits CM, HC, and CC[5:0]. The following formulas can be used to calculate the target output current $I_{OUT,target}$ in the saturation region:

$$V_{REXT} = 1.26\ V \times VG \quad (3)$$

$$I_{ref} = V_{REXT}/R_{ext}, \text{ if another end of the external resistor } R_{ext} \text{ is connected to ground} \quad (4)$$

$$I_{OUT,target} = I_{ref} \times 15 \times 3^{CM-1} \quad (5)$$

Where R_{ext} is the resistance of the external resistor connected to the REXT terminal, and V_{REXT} is the voltage of REXT, which is controlled by the programmable voltage gain (VG), which is defined by the Configuration Code.

The Current Multiplier bit (CM) sets the ratio $I_{OUT,target}/I_{ref}$ to 15 or 5 (sets the exponent *CM – 1* to either 0 or –1). After power-on, the default value of VG is 127/128 = 0.992, and the default value of CM is 1, so that the ratio $I_{OUT,target}/I_{ref}$ = 15. Based on the default VG and CM:

$$V_{REXT} = 1.26\ V \times 127/128 = 1.25\ V \quad (6)$$

$$I_{OUT,target} = (1.25\ V/R_{ext}) \times 15 \quad (7)$$

Therefore, the default current is approximately 20 mA at 931 Ω. The default relationship after power-on between $I_{OUT,target}$ and R_{ext} is shown in Figure 24.

shows the output voltage versus the output current with several different resistor values on REXT. This shows the minimum voltage required at the device to have full VF across the LED. The VLED voltage must be higher than the VF plus the VOL of the driver. If the VLED is too high, more power will be dissipated in the driver. If this is the case, a resistor can be inserted in series with the LED to dissipate the excess power and reduce the thermal conditions on the driver.

If a single driver is used with LEDs that have different VF values, resistors can also be used in series with the LED to remove the excess power from the driver. In cases where not all outputs are being used, the unused outputs can be left floating without issue.

10.2 Typical Application

The TLC59116-Q1 outputs can be wired in parallel to increase the current per LED string.

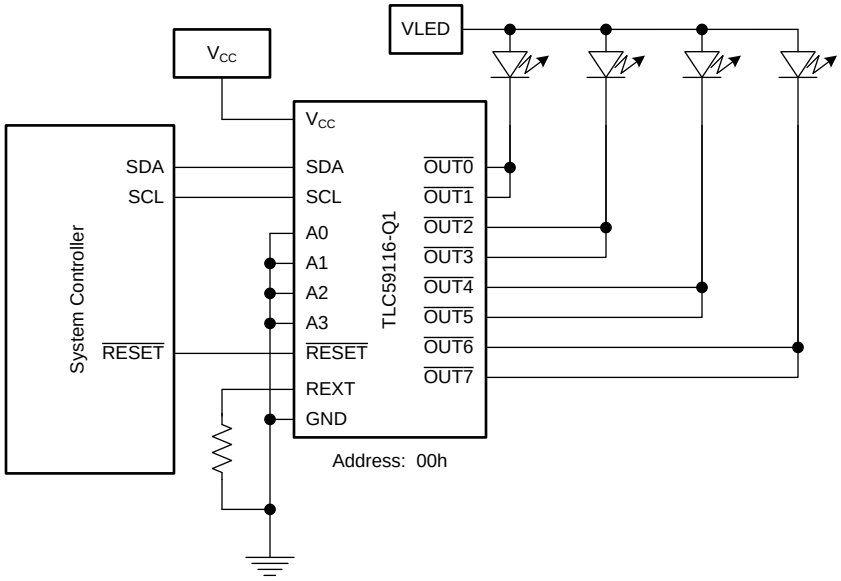


Figure 23. Parallel Channels

10.2.1 Design Requirements

Set the LED current to 50 mA while the IREF register is at the default value (CG = 0.992).

10.2.2 Detailed Design Procedure

The goal of this design is to set the LED current to 50 mA. Because two outputs are in parallel, the LED current should actually be set to 25 mA. With the IREF register at the default value:

$$I_{OUT,target} = (1.25 \text{ V} / R_{EXT}) \times 15 \quad (8)$$

Using this equation, the appropriate R_{EXT} is calculated to be 750 Ω.

Typical Application (continued)

10.2.3 Application Curve

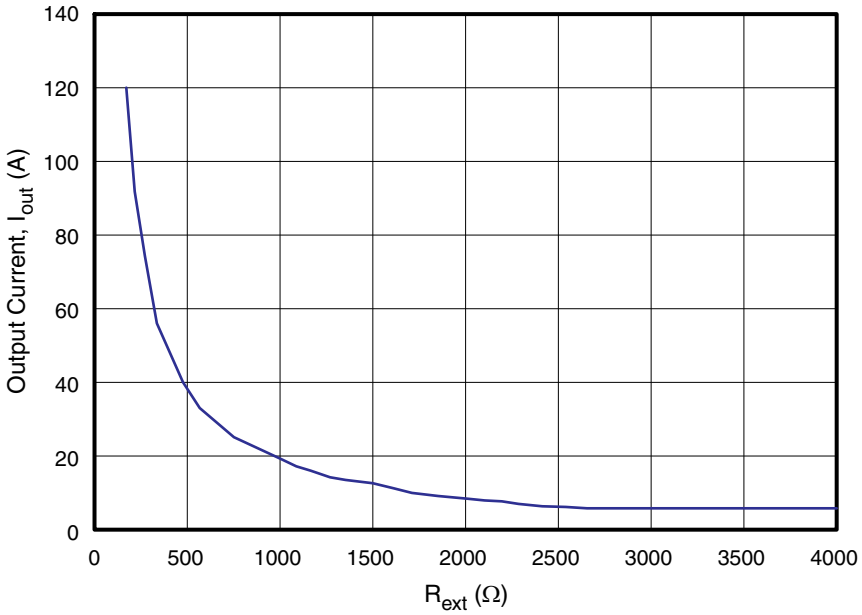


Figure 24. $I_{OUT,target}$ vs R_{ext}

11 Power Supply Recommendations

TLC59116-Q1 is designed to operate from a V_{CC} range of 3 V to 5.5 V.

12 Layout

12.1 Layout Guidelines

The I^2C signals (SDA / SCL) should be kept away from potential noise sources.

The traces carrying power through the LEDs should be wide enough to the handle necessary current.

All LED current passes through the device and into the ground node. The connection between the device ground and the circuit board ground must be a strong connection.

12.2 Layout Example

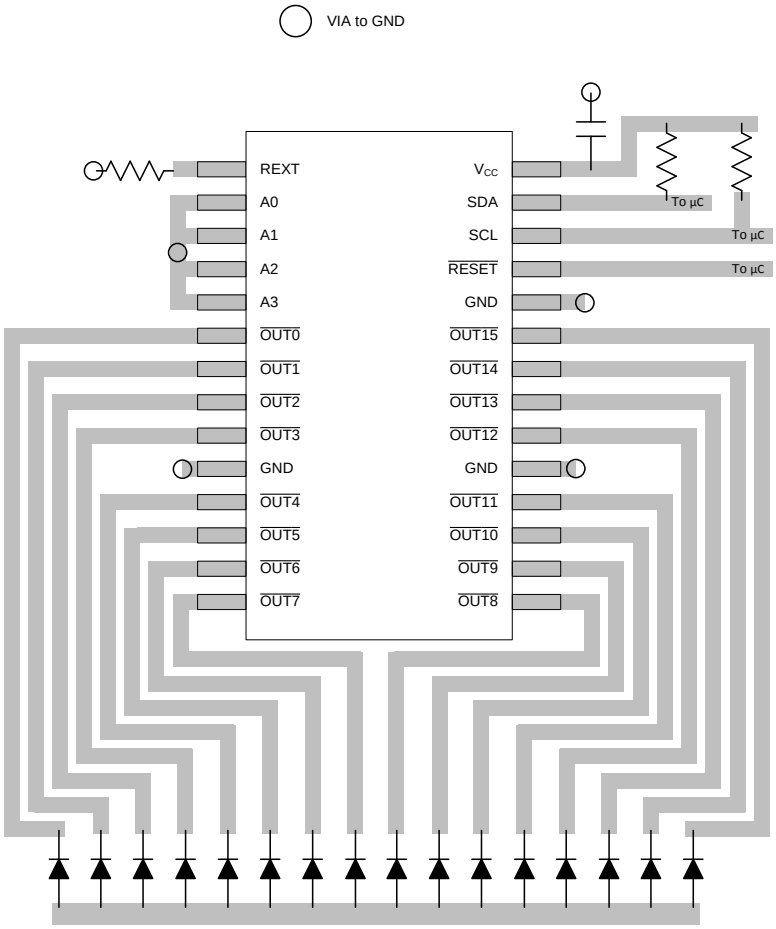


Figure 25. PW-28 Layout Example

12.3 Thermal Considerations

The maximum IC junction temperature should be restricted to 150°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given ambient temperature, use Equation 9 as a guideline:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\theta_{JA}} \quad (9)$$

where

- $P_{D(max)}$ = maximum allowable power dissipation
- $T_{J(max)}$ = maximum allowable junction temperature (150°C for the TLC59116-Q1)
- T_A = ambient temperature of the device
- Θ_{JA} = junction to air thermal impedance.

See *Thermal Information* section. This parameter is highly dependent upon board layout.

Power dissipation in the device is determined by the LED current and the voltage at the $\overline{OUTx}$ pins. For example, if the LED current is 50 mA continuous through each channel and the output voltage is 1 V on each channel, then the total power dissipation is 50 mA × 1 V × 16 ch = 0.8 W.

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- TLC59116EVM-390 User's Guide, SLVU296
- TLC59116FEVM-571, SLVU367

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC59116ITPWRQ1	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	Y59116Q	Samples
TLC59116ITPWTQ1	ACTIVE	TSSOP	PW	28	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	Y59116Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

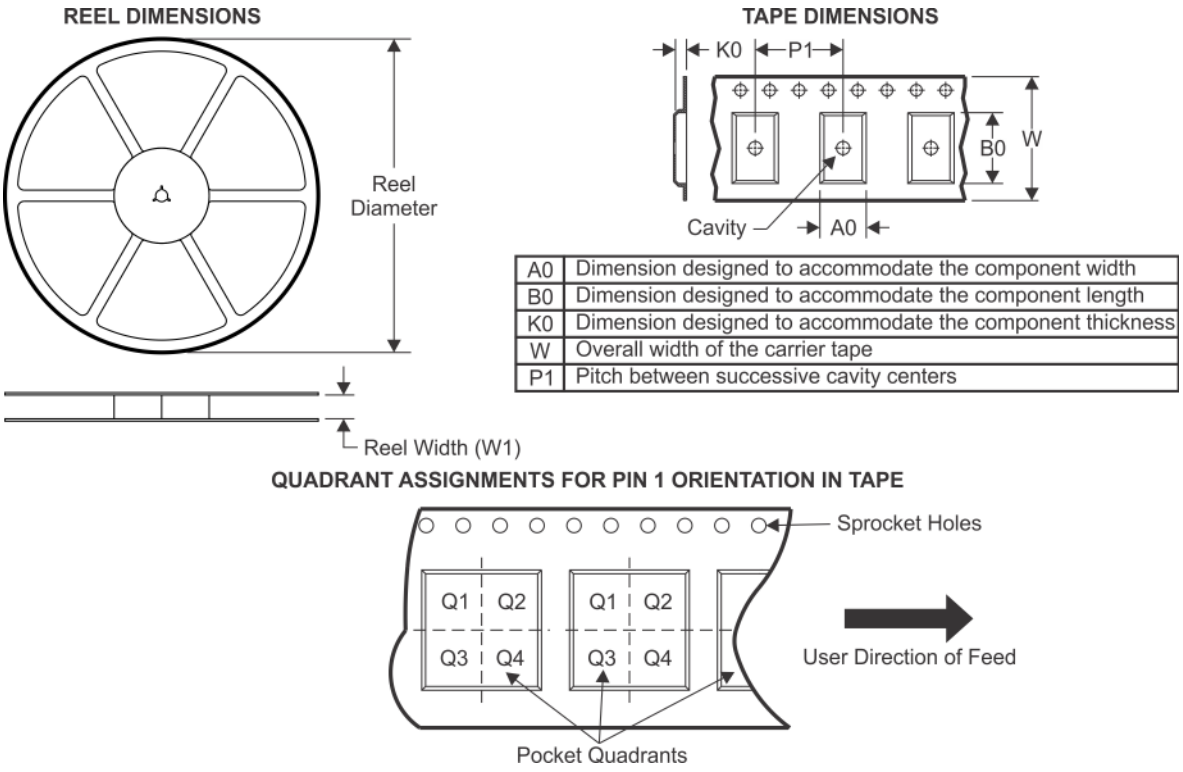
OTHER QUALIFIED VERSIONS OF TLC59116-Q1 :

- Catalog: TLC59116

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

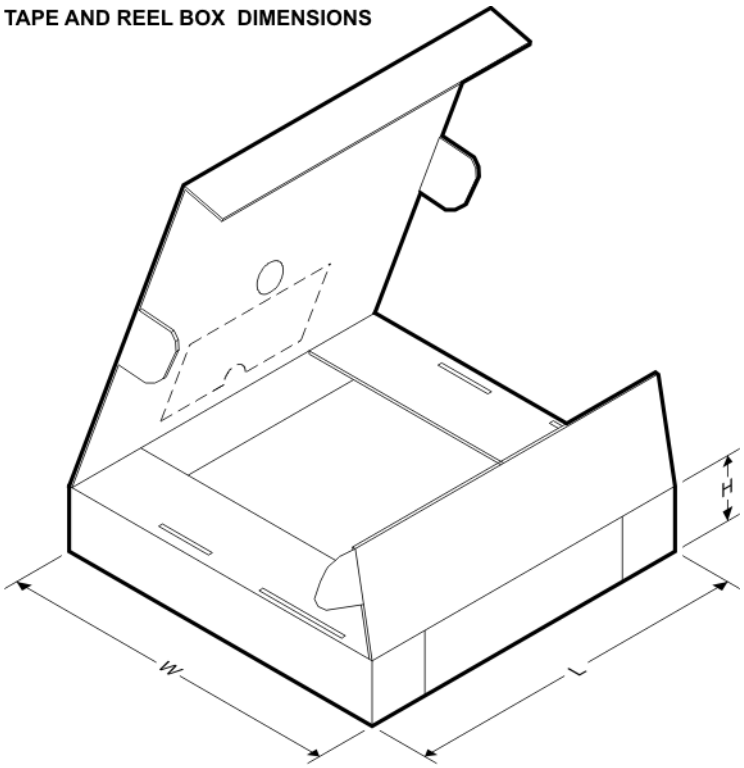


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC59116ITPWRQ1	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TLC59116ITPWTQ1	TSSOP	PW	28	250	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

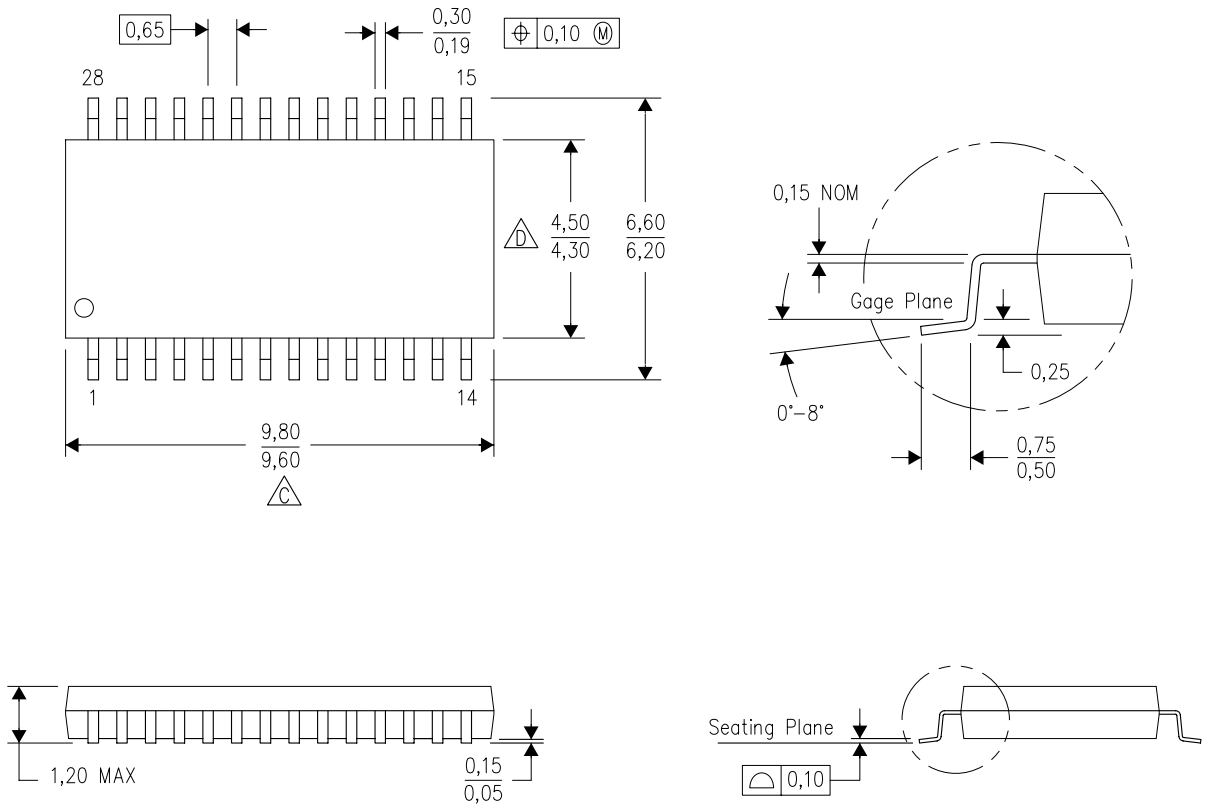
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC59116ITPWRQ1	TSSOP	PW	28	2000	350.0	350.0	43.0
TLC59116ITPWTQ1	TSSOP	PW	28	250	350.0	350.0	43.0

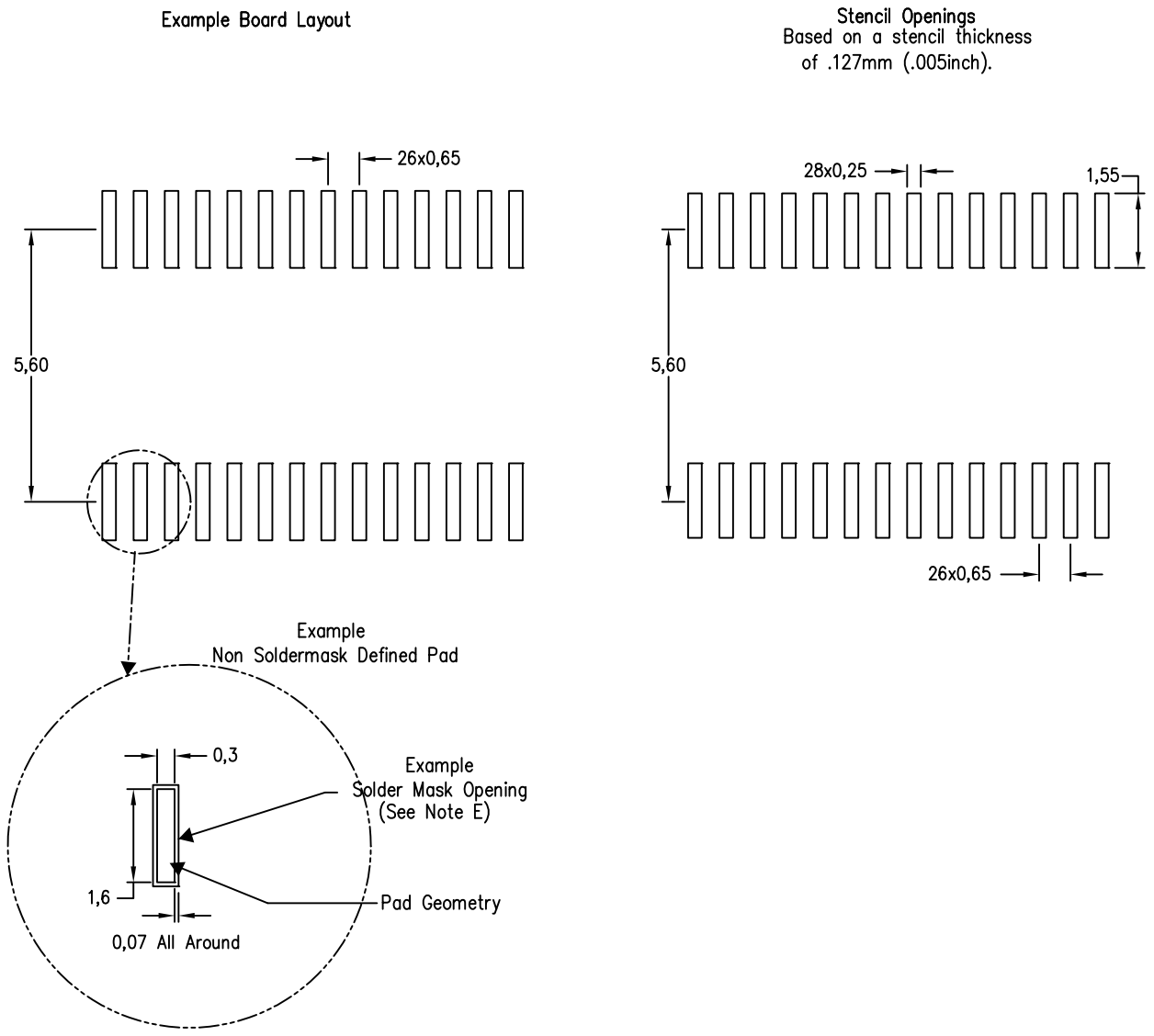
PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



4040064–7/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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