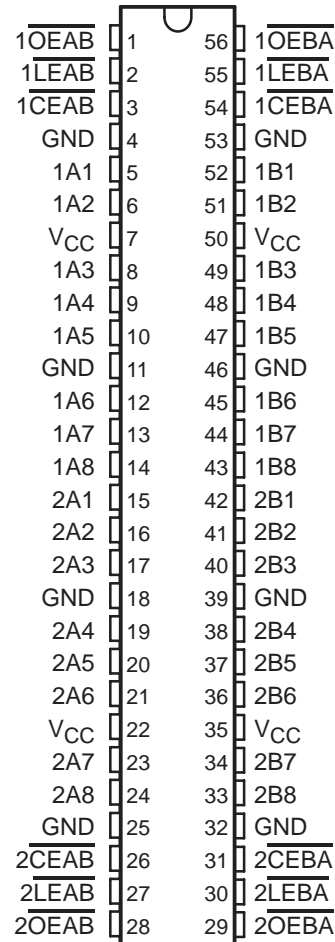


# SN54LVT16543, SN74LVT16543 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS148C – MAY 1992 – REVISED JULY 1995

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments *Widebus*™ Family
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Support Unregulated Battery Operation Down to 2.7 V
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200$  pF,  $R = 0$ )
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVT16543 . . . WD PACKAGE  
SN74LVT16543 . . . DGG OR DL PACKAGE  
(TOP VIEW)



## description

The 'LVT16543 are 16-bit registered transceivers designed for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable ( $\overline{LEAB}$  or  $\overline{LEBA}$ ) and output-enable ( $\overline{OEAB}$  or  $\overline{OEBA}$ ) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ( $\overline{CEAB}$ ) input must be low in order to enter data from A or to output data from B. If  $\overline{CEAB}$  is low and  $\overline{LEAB}$  is low, the A-to-B latches are transparent; a subsequent low-to-high transition of  $\overline{LEAB}$  puts the A latches in the storage mode. With  $\overline{CEAB}$  and  $\overline{OEAB}$  both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the  $\overline{CEBA}$ ,  $\overline{LEBA}$ , and  $\overline{OEBA}$  inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments Incorporated.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265  
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251-1443

Copyright © 1995, Texas Instruments Incorporated

# SN54LVT16543, SN74LVT16543

## 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS

### WITH 3-STATE OUTPUTS

SCBS148C – MAY 1992 – REVISED JULY 1995

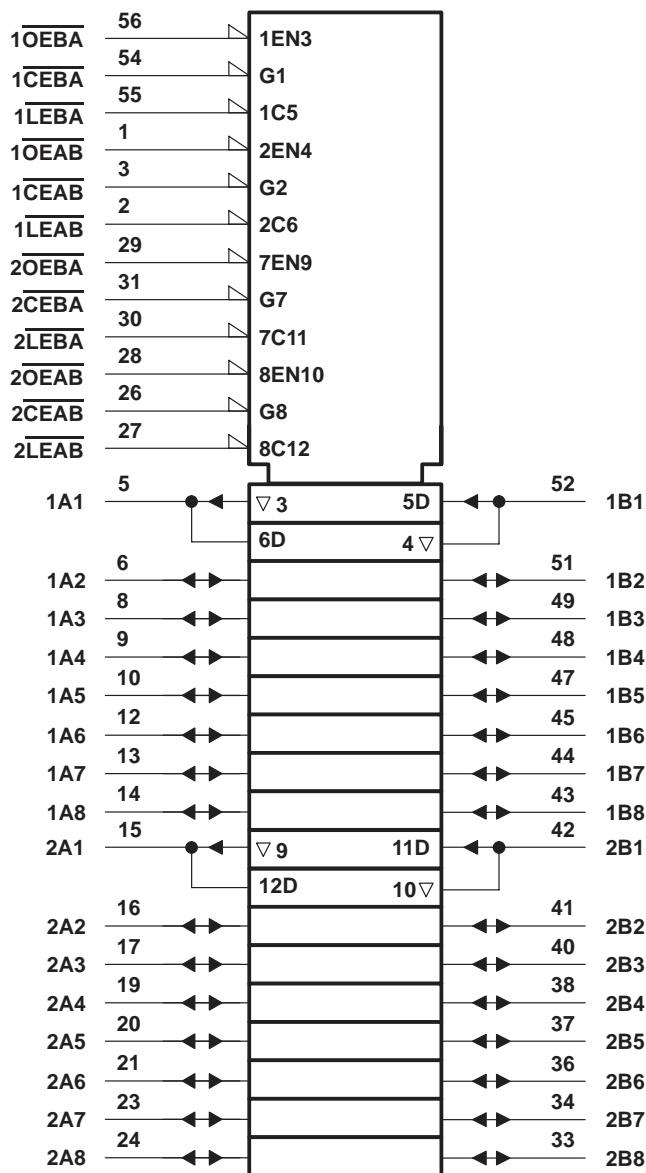
#### description (continued)

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT16543 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16543 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74LVT16543 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

#### logic symbol†



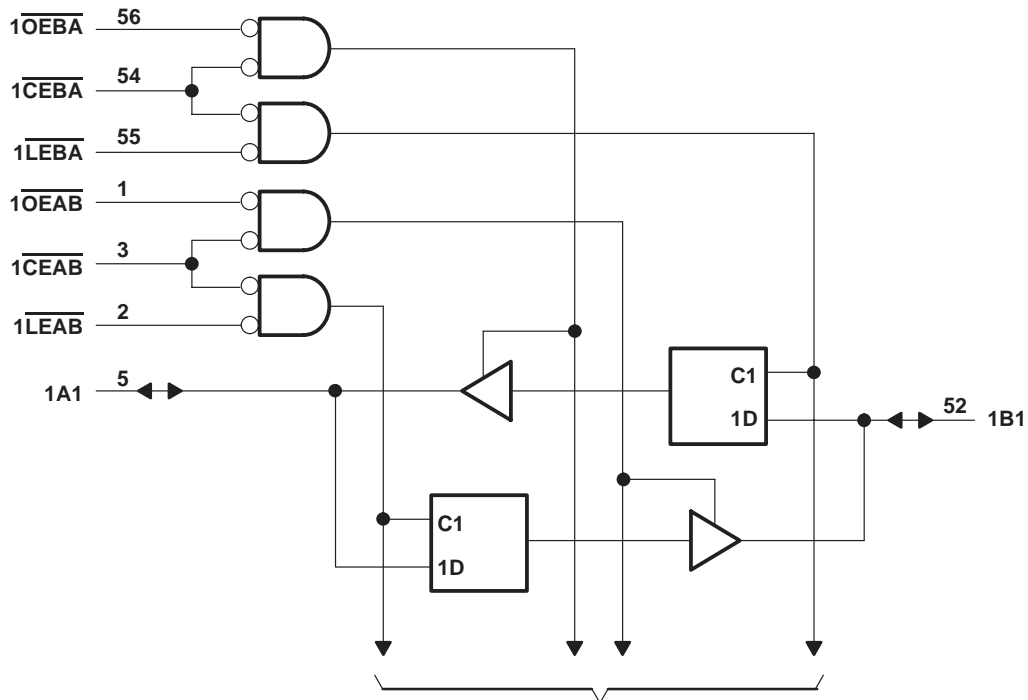
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



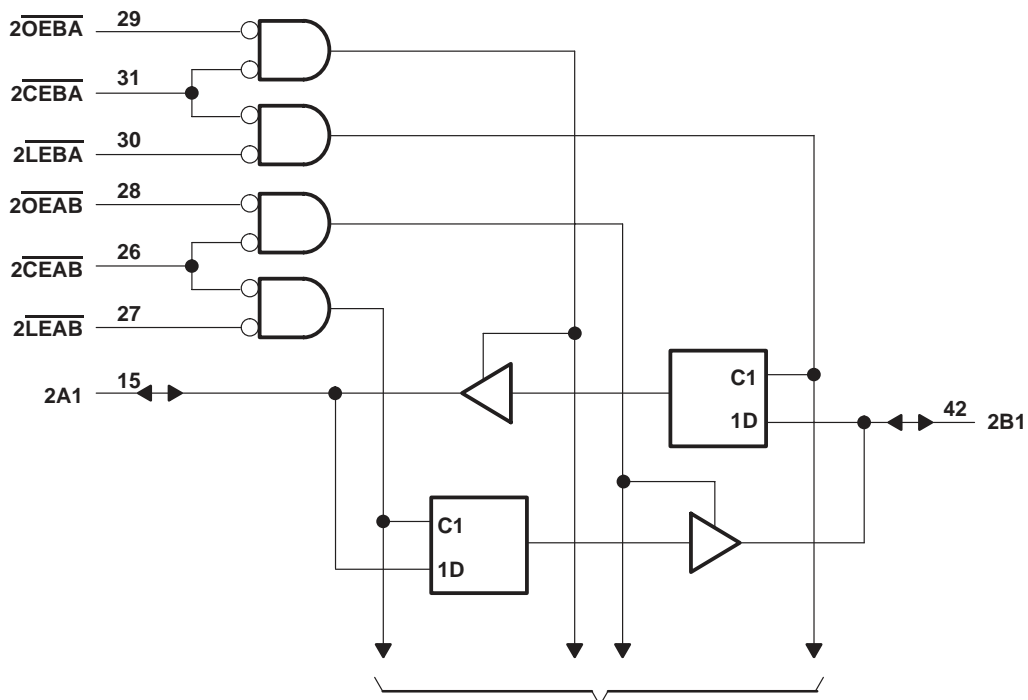
**SN54LVT16543, SN74LVT16543**  
**3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS**  
**WITH 3-STATE OUTPUTS**

SCBS148C - MAY 1992 - REVISED JULY 1995

logic diagram (positive logic)



To Seven Other Channels



To Seven Other Channels



# SN54LVT16543, SN74LVT16543

## 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS

### WITH 3-STATE OUTPUTS

SCBS148C – MAY 1992 – REVISED JULY 1995

FUNCTION TABLE†  
(each 8-bit section)

INPUTS				OUTPUT B
CEAB	LEAB	OEAB	A	
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B <sub>0</sub> ‡
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses  $\overline{CEBA}$ ,  $\overline{LEBA}$ , and  $\overline{OEBA}$ .

‡ Output level before the indicated steady-state input conditions were established

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, $V_{CC}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$ (see Note 1)	–0.5 V to 7 V
Current into any output in the low state, $I_{OL}$ : SN54LVT16543	96 mA
SN74LVT16543	128 mA
Current into any output in the high state, $I_{OH}$ (see Note 2): SN54LVT16543	48 mA
SN74LVT16543	64 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

§ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .  
 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

### recommended operating conditions (see Note 4)

		SN54LVT16543		SN74LVT16543		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2.7	3.6	2.7	3.6	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage		5.5		5.5	V
$I_{OH}$	High-level output current		–24		–32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265  
 POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251-1443

**SN54LVT16543, SN74LVT16543**  
**3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS**  
**WITH 3-STATE OUTPUTS**

SCBS148C – MAY 1992 – REVISED JULY 1995

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		SN54LVT16543		SN74LVT16543		UNIT
			MIN	TYP†	MAX	MIN	
$V_{IK}$	$V_{CC} = 2.7\text{ V}$ , $I_I = -18\text{ mA}$		-1.2		-1.2		V
$V_{OH}$	$V_{CC} = \text{MIN to MAX}^\ddagger$ , $I_{OH} = -100\ \mu\text{A}$		$V_{CC} - 0.2$		$V_{CC} - 0.2$		V
	$V_{CC} = 2.7\text{ V}$ , $I_{OH} = -8\text{ mA}$		2.4		2.4		
	$V_{CC} = 3\text{ V}$	$I_{OH} = -24\text{ mA}$	2		2		
$I_{OH} = -32\text{ mA}$							
$V_{OL}$	$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\ \mu\text{A}$	0.2		0.2		V
		$I_{OL} = 24\text{ mA}$	0.5		0.5		
	$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$	0.4		0.4		
		$I_{OL} = 32\text{ mA}$	0.5		0.5		
		$I_{OL} = 48\text{ mA}$	0.55				
		$I_{OL} = 64\text{ mA}$			0.55		
$I_I$	$V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}$ or GND		Control inputs		$\pm 1$		$\mu\text{A}$
	$V_{CC} = 0$ or $\text{MAX}^\ddagger$ , $V_I = 5.5\text{ V}$				10		
	$V_{CC} = 3.6\text{ V}$	$V_I = 5.5\text{ V}$	A or B ports $^\S$		20		
		$V_I = V_{CC}$			5		
		$V_I = 0$			-10		
$I_{off}$	$V_{CC} = 0$ , $V_I$ or $V_O = 0$ to $4.5\text{ V}$				$\pm 100$		$\mu\text{A}$
$I_{I(\text{hold})}$	$V_{CC} = 3\text{ V}$	$V_I = 0.8\text{ V}$	A or B ports		75		$\mu\text{A}$
		$V_I = 2\text{ V}$			-75		
$I_{OZH}$	$V_{CC} = 3.6\text{ V}$ , $V_O = 3\text{ V}$		1		1		$\mu\text{A}$
$I_{OZL}$	$V_{CC} = 3.6\text{ V}$ , $V_O = 0.5\text{ V}$		-1		-1		$\mu\text{A}$
$I_{CC}$	$V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}$ or GND, $I_O = 0$ ,		Outputs high		0.12		$\text{mA}$
			Outputs low		5		
			Outputs disabled		0.12		
$\Delta I_{CC}^\parallel$	$V_{CC} = 3\text{ V to } 3.6\text{ V}$ , One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}$ or GND		0.2		0.2		$\text{mA}$
$C_i$	$V_I = 3\text{ V or } 0$		4		4		$\text{pF}$
$C_{io}$	$V_O = 3\text{ V or } 0$		13		13		$\text{pF}$

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ Unused pins at  $V_{CC}$  or GND

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



# SN54LVT16543, SN74LVT16543

## 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS

### WITH 3-STATE OUTPUTS

SCBS148C – MAY 1992 – REVISED JULY 1995

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN54LVT16543				SN74LVT16543				UNIT
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{w}$	Pulse duration, $\overline{LEAB}$ or $\overline{LEBA}$ low		3.3		3.3		3.3		3.3	ns	
$t_{su}$	Setup time	A or B before $\overline{LEAB}\uparrow$ or $\overline{LEBA}\uparrow$	Data high	0.8	0.5		0.8	0.5		ns	
			Data low	1.5	1.9		1.5	1.9			
	A or B before $\overline{CEAB}\uparrow$ or $\overline{CEBA}\uparrow$	Data high	0.7	0.4		0.7	0.4		ns		
		Data low	1.6	1.9		1.6	1.9				
$t_h$	Hold time	A or B after $\overline{LEAB}\uparrow$ or $\overline{LEBA}\uparrow$	Data high	0.8	0		0.8	0		ns	
			Data low	1.2	1.3		1.2	1.3			
	A or B after $\overline{CEAB}\uparrow$ or $\overline{CEBA}\uparrow$	Data high	0.8	0		0.8	0		ns		
		Data low	1.3	1.4		1.3	1.4				

switching characteristics over recommended operating free-air temperature range,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT16543				SN74LVT16543				UNIT	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
$t_{PLH}$	A or B	B or A	1.4	5		5.8	1.4	2.7	4.6		5.5	ns
$t_{PHL}$			1.3	4.7		5.9	1.3	2.9	4.6		5.8	
$t_{PLH}$	$\overline{LE}$	A or B	1.3	6.8		8.5	1.7	3.7	6.3		8.1	ns
$t_{PHL}$			1.5	6.5		8.3	1.9	3.7	6		7.8	
$t_{PZH}$	$\overline{OE}$	A or B	1.4	6		7.7	1.5	3.3	5.8		7.6	ns
$t_{PZL}$			1.6	6.3		8.4	1.6	3.3	6.2		8.2	
$t_{PHZ}$	$\overline{OE}$	A or B	2	6.7		7.3	2	4.1	6.5		7.1	ns
$t_{PLZ}$			2.7	6		6.2	2.7	3.9	5.8		5.9	
$t_{PZH}$	$\overline{CE}$	A or B	1.4	6.2		7.7	1.5	3.3	6		7.6	ns
$t_{PZL}$			1.6	6.6		8.5	1.7	3.3	6.4		8.3	
$t_{PHZ}$	$\overline{CE}$	A or B	2	6.6		7.2	2	4.1	6.4		7.1	ns
$t_{PLZ}$			2.6	5.6		5.9	2.6	4	5.4		5.6	

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

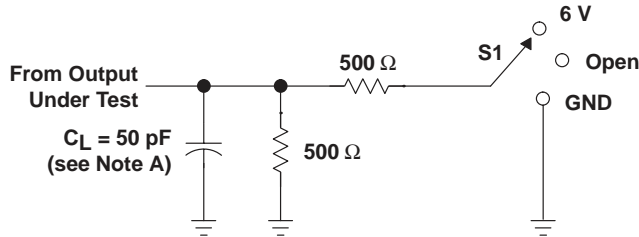
PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



# SN54LVT16543, SN74LVT16543 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

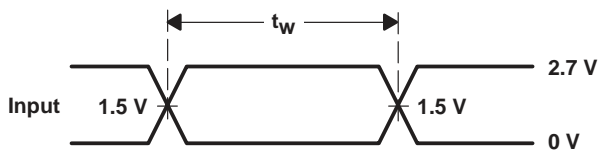
SCBS148C – MAY 1992 – REVISED JULY 1995

## PARAMETER MEASUREMENT INFORMATION

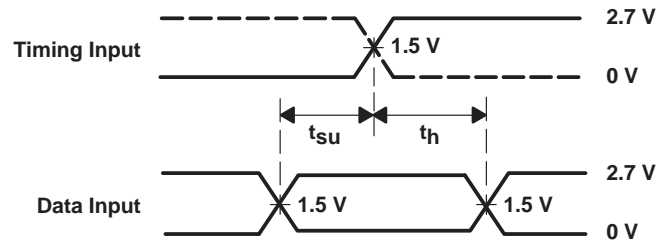


TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND

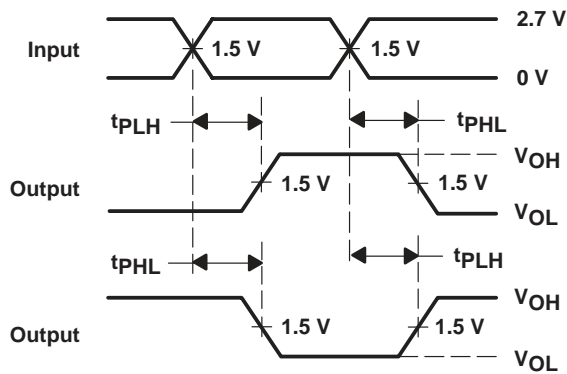
LOAD CIRCUIT FOR OUTPUTS



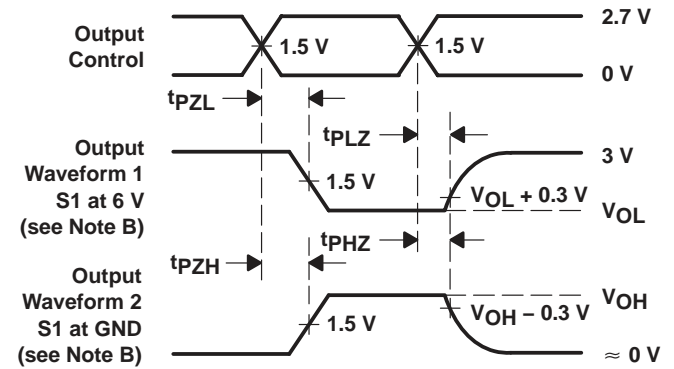
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

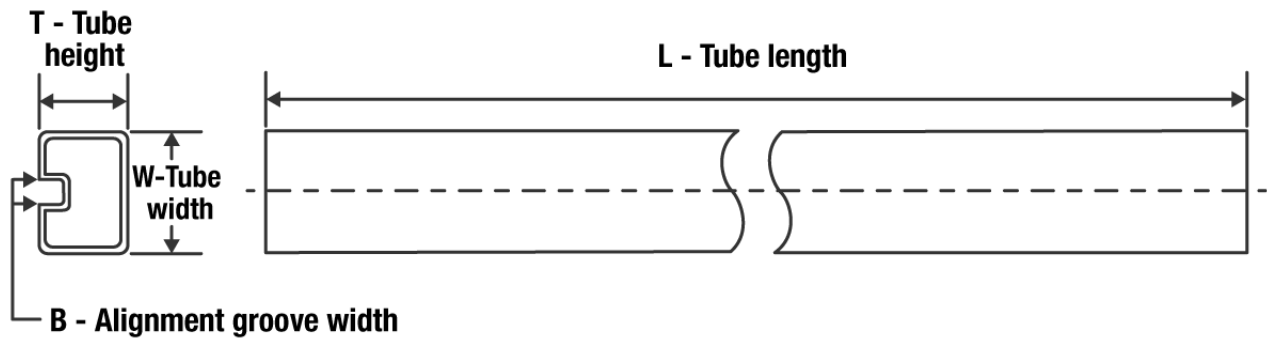
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVT16543DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74LVT16543DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVT16543DGGR	TSSOP	DGG	56	2000	367.0	367.0	45.0
SN74LVT16543DLR	SSOP	DL	56	1000	367.0	367.0	55.0

**TUBE**


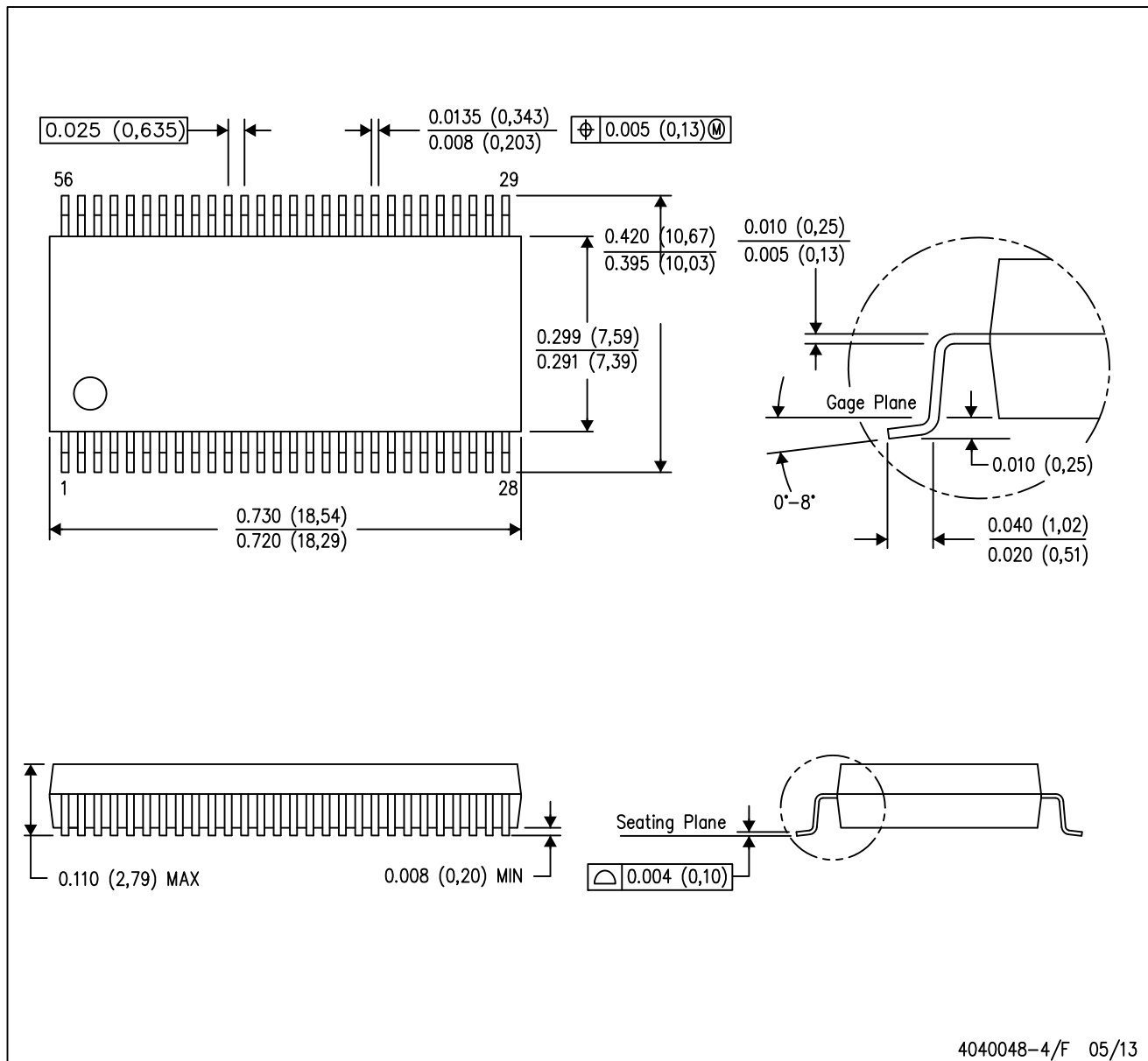
\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LVT16543DL	DL	SSOP	56	20	473.7	14.24	5110	7.87

# MECHANICAL DATA

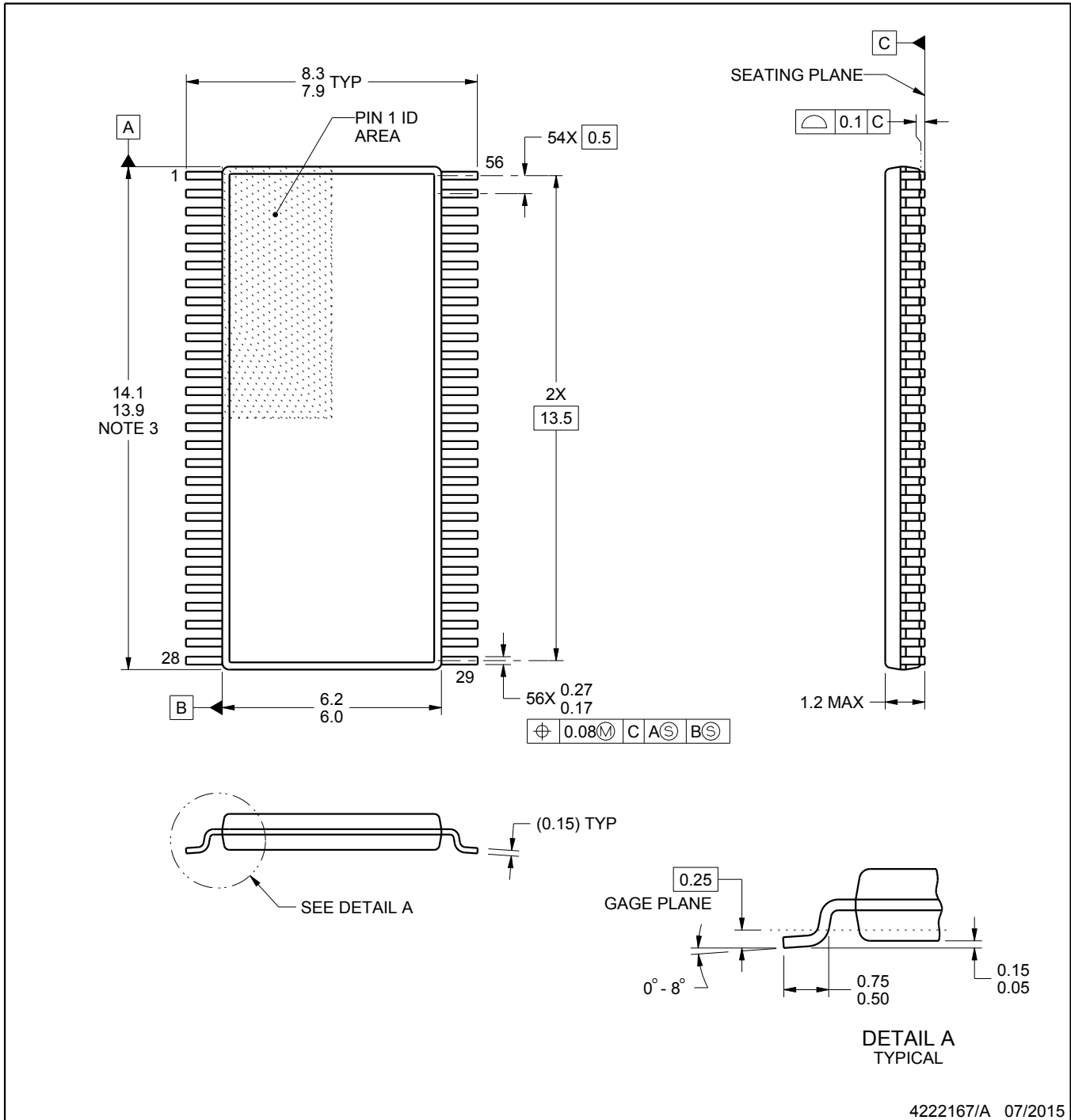
DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.



4222167/A 07/2015

NOTES:

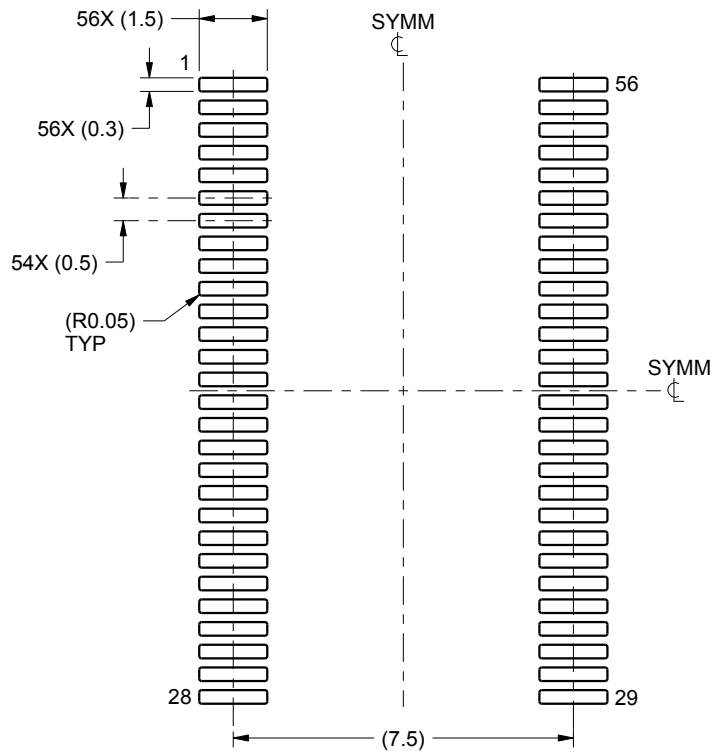
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

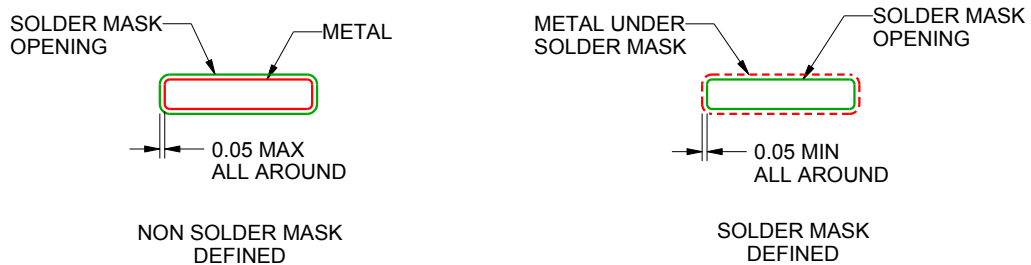
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

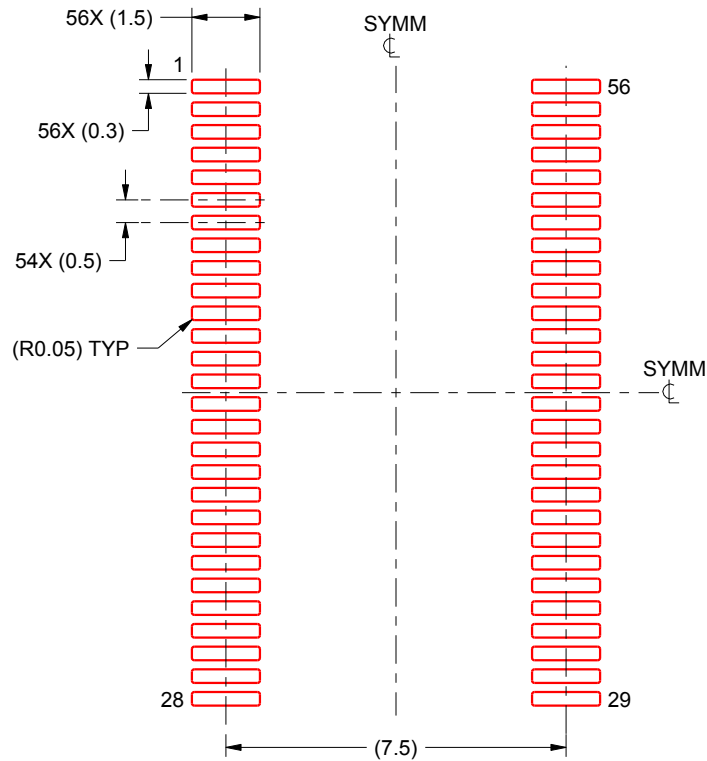
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated