19-3587; Rev 1; 1/12

Pin-Selectable, Hex Power-Supply Supervisory Circuit

General Description

The MAX6886 pin-selectable, multivoltage supply supervisor monitors six voltage-detector inputs and one watchdog input, asserting a $\overline{RESET}$ when inputs drop below the selected voltage thresholds or the watchdog timer expires. Manual reset and margin disable inputs offer additional flexibility.

Five logic inputs select the MAX6886 thresholds. Logic inputs select a supply tolerance (5% or 10%) and 1 of 32 factory-set threshold settings. Connect external capacitors or use the factory default setting to set the watchdog timeout periods and reset time delay.

The MAX6886 is available in a 20-pin TQFN (5mm x 5mm x 0.8mm) package and operates over the extended -40°C to +85°C temperature range.

Applications

Multivoltage Systems

Telecom

Networking

Servers/Workstations/Storage Systems

Pin Configuration appears at end of data sheet.

Features

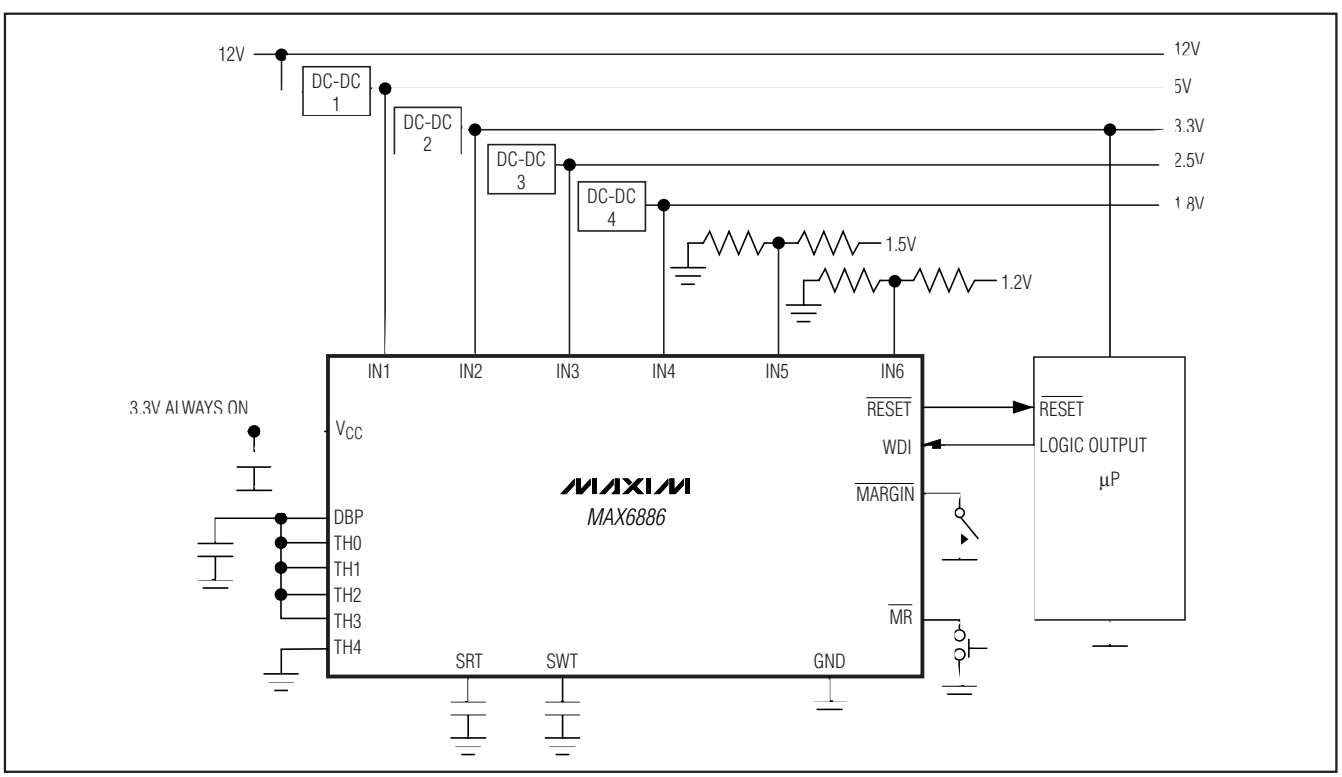
- **32 Pin-Selectable Undervoltage Detector Thresholds**
- **Capacitor-Adjustable Reset and Watchdog Timeout Periods**
- **Factory Default Reset and Watchdog Timeout Periods**
- **Margining Disable and Manual Reset Controls**
- **-40°C to +85°C Operating Temperature Range**
- **Small 5mm x 5mm 20-Pin Thin QFN Package**
- **Few External Components**
- **±1% Threshold Accuracy**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX6886ETP+	-40°C to +85°C	20 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

Typical Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Pin-Selectable, Hex Power-Supply Supervisory Circuit

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
IN1–IN6, V_{CC}, $\overline{RESET}$, SRT, SWT .....-0.3V to +6V
TH0–TH4, WDI, $\overline{MR}$, $\overline{MARGIN}$ .....-0.3V to +6V
DBP .....-0.3V to +3V
Input/Output Current (all pins).....±20mA
Continuous Power Dissipation (T_A = +70°C)
20-Pin 5mm x 5mm Thin QFN
(derate 21.3mW/°C above +70°C).....1702mW

Maximum Junction Temperature .....+150°C
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN1}–V_{IN4} or V_{CC} = 2.7V to 5.8V, WDI = GND, TH0–TH4 = $\overline{MARGIN}$ = $\overline{MR}$ = DBP, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range (Note 3)		Voltage on either one of IN1–IN4 or V_{CC} to guarantee the part is fully operational		2.7		5.8	V
Supply Current	I_{CC}	V_{IN1} = 5.8V, IN2–IN6 = GND, no load			0.9	1.2	mA
Digital Bypass Voltage	V_{DBP}			2.48	2.55	2.67	V
Threshold Accuracy (Table 2)	V_{TH}	IN1–IN6, $V_{IN_}$ falling	T_A = +25°C to +85°C	-1		+1	% V_{TH}
			T_A = -40°C to +85°C	-1.5		+1.5	
Threshold Hysteresis	V_{TH-HYS}				0.3		% V_{TH}
Threshold Tempco	ΔV_{TH}/°C				10		ppm/°C
IN_ Input Impedance	R_{IN}	For $V_{IN_}$ < highest $V_{IN1–IN4}$ and $V_{IN_}$ < V_{CC} (not ADJ), thresholds are not set as adjustable		130	200	300	kΩ
IN_ Input Leakage Current	I_{IN}	IN5, IN6		-150		+150	nA
		IN1–IN4 set as adjustable thresholds					
Power-Up Delay	t_{D-PO}	V_{CC} ≥ 2.5V				2.5	ms
IN_ to $\overline{RESET}$ Delay	t_{D-R}	IN_ falling/rising, 100mV overdrive			20		µs
Reset Default Timeout Period	t_{RP}	V_{SRT} = V_{CC}		180	200	220	ms
Reset Adjustable Timeout Period	t_{RP-ADJ}	C_{SRT} = 47nF		135	207	280	ms
SRT Adjustable Timeout Current	I_{SRT}	V_{SRT} = V_{GND}		180	230	280	nA
SRT Default Timeout Threshold	$V_{SRT-DEF}$	V_{SRT} ≥ $V_{SRT-DEF}$, selects reset default		1.1	1.25	1.5	V
SRT Adjustable Timeout Threshold	$V_{SRT-ADJ}$	(Note 4)		0.95	1.00	1.05	V
SRT Adjustable Timeout Discharge Threshold	$V_{SRT-DIS}$	(Note 5)			100		mV
SRT Adjustable Timeout Output-Low Discharge Current	$I_{SRT-DIS}$	V_{SRT} = 0.3V		0.7			mA
$\overline{RESET}$ Output Low	$V_{OLRESET}$	I_{SINK} = 4mA, output asserted				0.4	V
$\overline{RESET}$ Output Open-Drain Leakage Current	I_{LKG}	Output tri-stated		-1		+1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1}–V_{IN4} or V_{CC} = 2.7V to 5.8V, WDI = GND, TH0–TH4 = $\overline{MARGIN}$ = $\overline{MR}$ = DBP, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{MR}$, $\overline{MARGIN}$, TH0–TH4, WDI Input Voltage	V_{IL}					0.6	V
	V_{IH}			1.4			
$\overline{MR}$ Input Pulse Width	$t_{\overline{MR}}$			1			µs
$\overline{MR}$ Glitch Rejection					100		ns
$\overline{MR}$ to $\overline{RESET}$ Delay	$t_{D\text{-}\overline{MR}}$				200		ns
$\overline{MR}$ to Internal DBP Pullup Current	$I_{\overline{MR}}$	$V_{\overline{MR}}$ = 1.4V		5	10	15	µA
$\overline{MARGIN}$ to Internal DBP Pullup Current	$I_{\overline{MARGIN}}$	$V_{\overline{MARGIN}}$ = 1.4V		5	10	15	µA
TH0–TH4 Input Current				-100		+100	nA
WDI Pulldown Current	I_{WDI}	V_{WDI} = 0.6V		5	10	15	µA
WDI Input Pulse Width	t_{WDI}			50			ns
Watchdog Default Timeout Period	t_{WD}	V_{SWT} = V_{CC}	Initial mode	92.16	102.4	112.64	s
			Normal mode	1.44	1.6	1.76	
Watchdog Adjustable Timeout Period	$t_{WD\text{-}ADJ}$	C_{SWT} = 0.33µF	Initial mode	53.7	82.5	111.9	s
			Normal mode	0.93	1.43	1.94	
SWT Adjustable Timeout Current	I_{SWT}	SWT = GND		180	230	280	nA
SWT Default Timeout Threshold	$V_{SWT\text{-}DEF}$	$V_{SWT} \geq V_{SWT\text{-}DEF}$, selects watchdog default timeout		1.1	1.25	1.5	V
SWT Adjustable Timeout Threshold	$V_{SWT\text{-}ADJ}$	(Note 4)		0.95	1.00	1.05	V
SWT Adjustable Timeout Discharge Threshold	$V_{SWT\text{-}DIS}$	(Note 5)			100		mV
SWT Adjustable Timeout Output-Low Discharge Current	$I_{SWT\text{-}DIS}$	V_{SWT} = 0.3V		0.7			mA

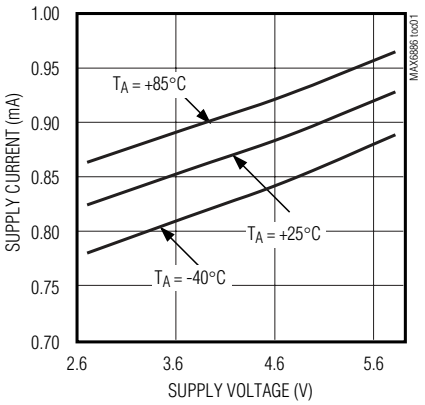
Note 1: Device may be supplied from IN1–IN4 or V_{CC}.
Note 2: 100% production tested at T_A = +25°C and T_A = +85°C. Specifications at T_A = -40°C are guaranteed by design.
Note 3: The internal supply voltage, measured at V_{CC}, equals the maximum of IN1–IN4.
Note 4: External capacitor is charged by I_{S_T} when $V_{S_T\text{-}DIS} < V_{S_T} < V_{S_T\text{-}ADJ}$.
Note 5: External capacitor is discharged by $I_{S_T\text{-}DIS}$ down to $V_{S_T\text{-}DIS}$ after V_{S_T} reaches $V_{S_T\text{-}ADJ}$.

Pin-Selectable, Hex Power-Supply Supervisory Circuit

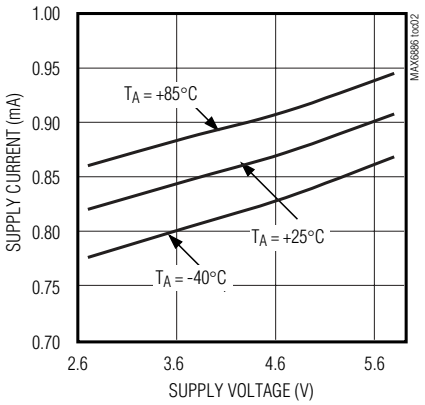
Typical Operating Characteristics

(V_{IN1}–V_{IN4} or V_{CC} = 5V, WDI = GND, TH0–TH4 = $\overline{MARGIN}$ = $\overline{MR}$ = DBP, T_A = +25°C, unless otherwise noted.)

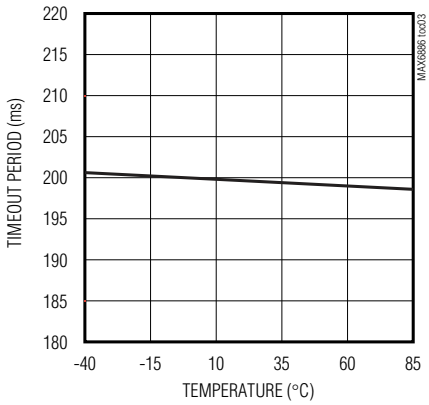
IN1–IN4 SUPPLY CURRENT vs. IN1–IN4 SUPPLY VOLTAGE



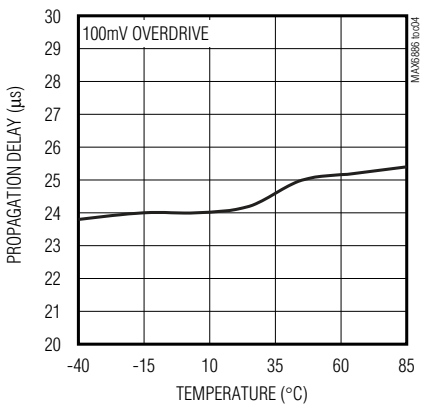
V_{CC} SUPPLY CURRENT vs. V_{CC} SUPPLY VOLTAGE



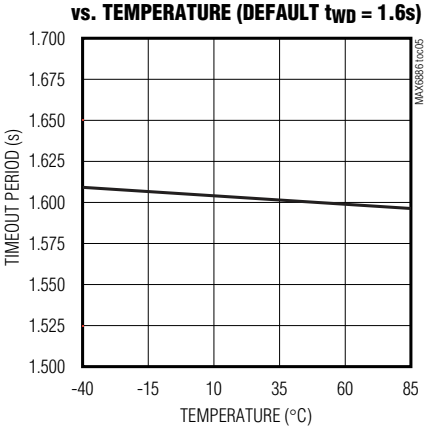
RESET TIMEOUT PERIOD vs. TEMPERATURE (DEFAULT t_{RP} = 200ms)



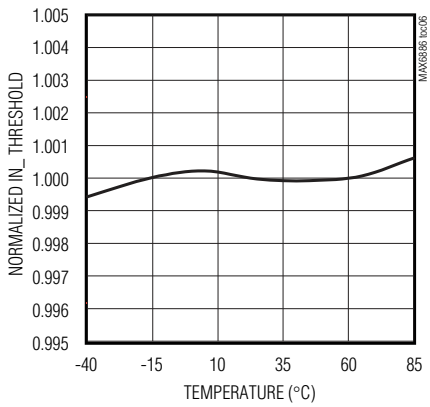
IN_ TO $\overline{RESET}$ PROPAGATION DELAY vs. TEMPERATURE



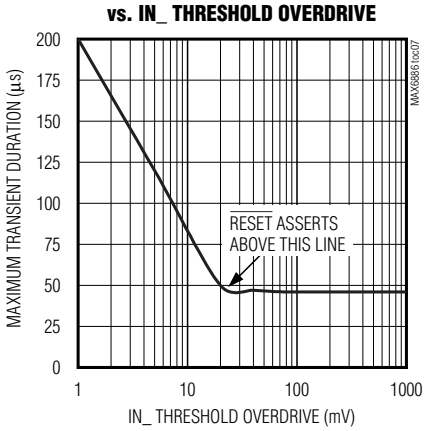
WATCHDOG TIMEOUT PERIOD vs. TEMPERATURE (DEFAULT t_{WD} = 1.6s)



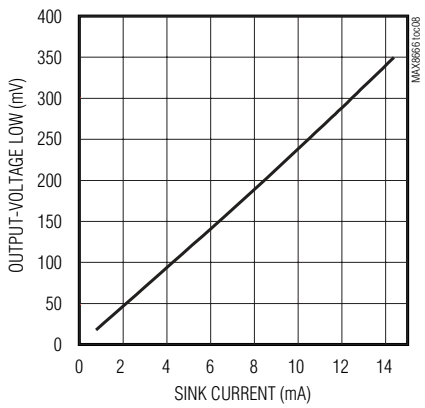
NORMALIZED IN_ THRESHOLD vs. TEMPERATURE



MAXIMUM IN_ TRANSIENT vs. IN_ THRESHOLD OVERDRIVE



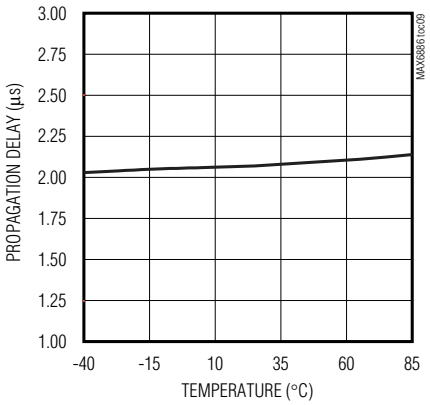
OUTPUT-VOLTAGE LOW vs. SINK CURRENT



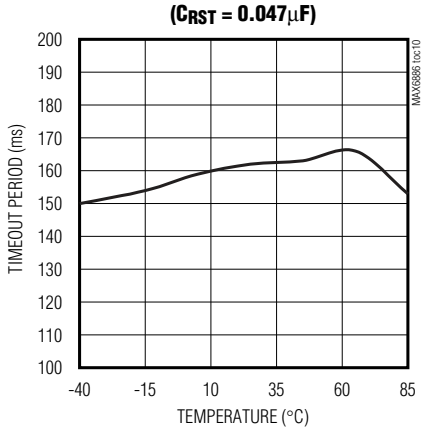
Typical Operating Characteristics (continued)

(V_{IN1}–V_{IN4} or V_{CC} = 5V, WDI = GND, TH0–TH4 = $\overline{MARGIN}$ = $\overline{MR}$ = DBP, T_A = +25°C, unless otherwise noted.)

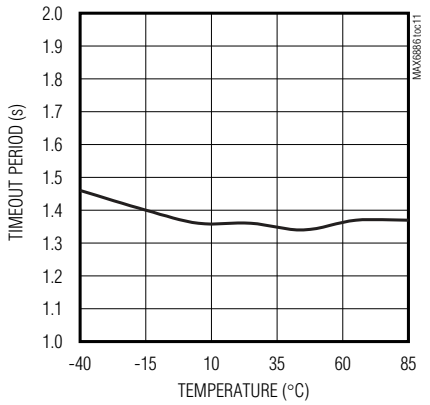
$\overline{MR}$ TO $\overline{RESET}$ OUTPUT PROPAGATION DELAY vs. TEMPERATURE



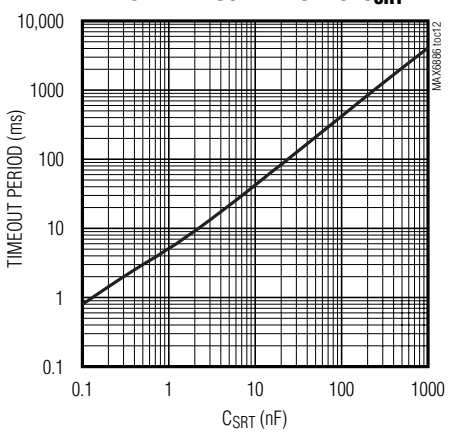
RESET TIMEOUT PERIOD vs. TEMPERATURE (C_{RST} = 0.047µF)



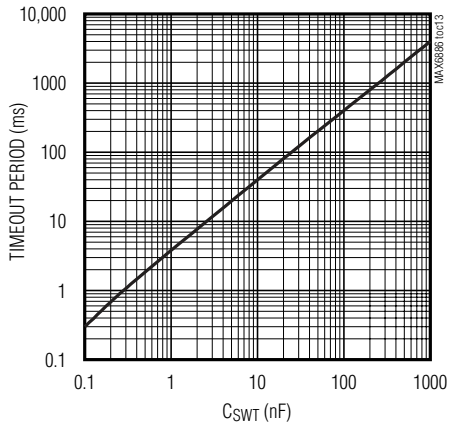
WATCHDOG TIMEOUT PERIOD vs. TEMPERATURE (C_{SWT} = 0.33µF)



RESET TIMEOUT PERIOD vs. C_{SRT}



WATCHDOG TIMEOUT PERIOD vs. C_{SWT}



Pin Description

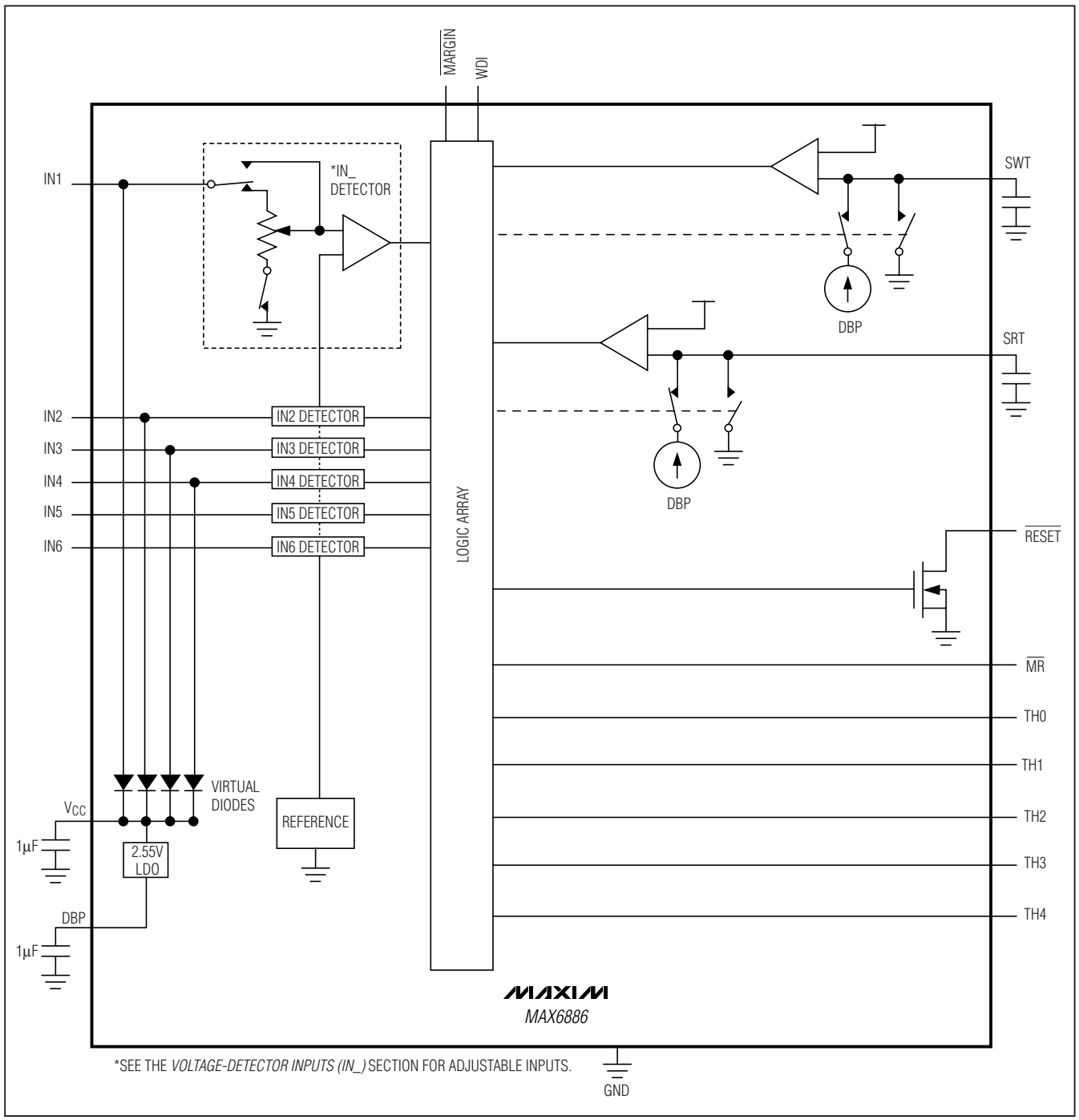
PIN	NAME	FUNCTION
1	$\overline{RESET}$	Open-Drain, Active-Low Reset Output. $\overline{RESET}$ asserts when any input voltage falls below the selected threshold, the watchdog timer expires, or when $\overline{MR}$ is pulled low. $\overline{RESET}$ remains asserted for default (200ms) or adjustable reset timeout period after all assertion-causing conditions are cleared. An external pullup resister is required.
2	SRT	Reset Timeout Adjust Input. Connect an external capacitor between SRT and GND to set the reset timeout period. The timeout period is calculated by t_{RP} = 4.348E6 x C_{SRT} (t_{RP} in seconds and C_{SRT} in Farads). To use the factory default period of 200ms connect SRT to V_{CC}.
3	SWT	Watchdog Timeout Adjust Input. Connect an external capacitor between SWT and GND to set the watchdog timeout period. The adjustable timeout period is calculated by t_{WD} = 4.348E6 x C_{SWT} (t_{WD} in seconds and C_{SWT} in Farads). Disable the watchdog timer by connecting SWT to GND. Connect SWT to V_{CC} to use the factory-default normal and initial periods of 1.6s and 102.4s, respectively.

Pin-Selectable, Hex Power-Supply Supervisory Circuit

Pin Description (continued)

PIN	NAME	FUNCTION
4	GND	Ground
5	WDI	Watchdog Timer Input. Logic input for the watchdog timer function. If WDI is not strobed with a valid low-to-high or high-to-low transition within the selected timeout period, $\overline{RESET}$ asserts. WDI is internally pulled down to GND through a 10µA current sink.
6	$\overline{MR}$	Active-Low Manual Reset Input. Pull $\overline{MR}$ low to assert $\overline{RESET}$. $\overline{RESET}$ will remain asserted for its preset/adjustable reset timeout period when $\overline{MR}$ is driven high. Leave $\overline{MR}$ unconnected or connect to DBP if unused. $\overline{MR}$ is internally pulled up to DBP through a 10µA current source.
7	$\overline{MARGIN}$	Margin Input. When $\overline{MARGIN}$ is pulled low, $\overline{RESET}$ is held in its existing state independent of subsequent changes in monitored input voltages or the watchdog timer expiration. $\overline{MARGIN}$ is internally pulled up to DBP through a 10µA current source. $\overline{MARGIN}$ overrides $\overline{MR}$ if both are asserted at the same time.
8	TH4	Threshold Selection Input 4. Logic input to select desired threshold. Connect TH4 to GND or DBP. See Table 2 for available thresholds. Input has no internal pullup or pulldown.
9	TH3	Threshold Selection Input 3. Logic input to select desired threshold. Connect TH3 to GND or DBP. See Table 2 for available thresholds. Input has no internal pullup or pulldown.
10	TH2	Threshold Selection Input 2. Logic input to select desired threshold. Connect TH2 to GND or DBP. See Table 2 for available thresholds. Input has no internal pullup or pulldown.
11	TH1	Threshold Selection Input 1. Logic input to select desired threshold. Connect TH1 to GND or DBP. See Table 2 for available thresholds. Input has no internal pullup or pulldown.
12	TH0	Threshold Selection Input 0. Logic input to select desired threshold. Connect TH0 to GND or DBP. See Table 2 for available thresholds. Input has no internal pullup or pulldown.
13	V_{CC}	Internal Power-Supply Voltage. Bypass V_{CC} to GND with a 1µF ceramic capacitor as close to the device as possible. V_{CC} supplies power to the internal circuitry. V_{CC} is internally powered from the highest of the monitored IN1–IN4 voltages. Do not use V_{CC} to supply power to external circuitry. To externally supply V_{CC}, see the *Powering the MAX6886* section.
14	DBP	Digital Bypass Voltage. The internally generated voltage at DBP supplies power to internal logic and output $\overline{RESET}$. Connect a 1µF capacitor from DBP to GND as close to the device as possible. Do not use DBP to supply power to external circuitry.
15	IN6	Input Voltage Detector 6. Select the undervoltage threshold using TH0–TH4. See Table 2. IN6 cannot supply power to the device. For improved noise immunity, bypass IN6 to GND with a 0.1µF capacitor installed as close to the device as possible.
16	IN5	Input Voltage Detector 5. Select the undervoltage threshold using TH0–TH4. See Table 2. IN5 cannot supply power to the device. For improved noise immunity, bypass IN5 to GND with a 0.1µF capacitor installed as close to the device as possible.
17	IN4	Input Voltage Detector 4. Select the undervoltage threshold using TH0–TH4. See Table 2. For improved noise immunity, bypass IN4 to GND with a 0.1µF capacitor installed as close to the device as possible. Power the device through IN1–IN4 or V_{CC} (see the *Powering the MAX6886* section).
18	IN3	Input Voltage Detector 3. Select the undervoltage threshold using TH0–TH4. See Table 2. For improved noise immunity, bypass IN3 to GND with a 0.1µF capacitor installed as close to the device as possible. Power the device through IN1–IN4 or V_{CC} (see the *Powering the MAX6886* section).
19	IN2	Input Voltage Detector 2. Select the undervoltage threshold using TH0–TH4. See Table 2. For improved noise immunity, bypass IN2 to GND with a 0.1µF capacitor installed as close to the device as possible. Power the device through IN1–IN4 or V_{CC} (see the *Powering the MAX6886* section).
20	IN1	Input Voltage Detector 1. Select the undervoltage threshold using TH0–TH4. See Table 2. For improved noise immunity, bypass IN1 to GND with a 0.1µF capacitor installed as close to the device as possible. Power the device through IN1–IN4 or V_{CC} (see the *Powering the MAX6886* section).
—	EP	Exposed Paddle. Internally connected to GND. Connect EP to GND or leave unconnected.

Functional Diagram



Pin-Selectable, Hex Power-Supply Supervisory Circuit

Detailed Description

The MAX6886 pin-selectable, multivoltage supply supervisor monitors six voltage-detector inputs and one watchdog input. $\overline{RESET}$ asserts when any of the configured input thresholds have been reached, $\overline{MR}$ is asserted, or the watchdog timer expires. $\overline{MARGIN}$ allows a system to be tested without $\overline{RESET}$ being asserted.

Logic inputs TH0–TH4 select 1 of 32 threshold sets for inputs IN1–IN6 (see Table 2, Threshold Options). Inputs in Table 2 that contain ADJ for inputs allow external resistor voltage-dividers to be connected to create additional thresholds.

$\overline{RESET}$ is an open-drain acitve-low output and asserts when $\overline{MR}$ is low, the watchdog timer expires, or any voltage at IN1–IN6 falls below its respective threshold. The default $\overline{RESET}$ time delay is 200ms and custom timeout periods are set by connecting an external capacitor from SRT to GND. The default watchdog normal and initial timeout periods are 1.6s and 102.4s, respectively. The normal and initial watchdog timeout periods can be adjusted by connecting an external capacitor from SWT to GND.

Powering the MAX6886

The MAX6886 derives power from the voltage-detector inputs IN1–IN4 or through an externally supplied V_{CC}. A virtual diode-ORing scheme selects the positive input that supplies power to the device (see the *Functional Diagram*). The highest input voltage on IN1–IN4 supplies power to the device. One of IN1–IN4 must be at least 2.7V to ensure proper operation.

Internal hysteresis ensures that the supply input that initially powered the device continues to power the device when multiple input voltages are within 50mV of each other.

V_{CC} powers the analog circuitry and is the bypass connection for the MAX6886 internal supply. Bypass V_{CC} to GND with a 1µF ceramic capacitor installed as close to the device as possible. The internal supply voltage, measured at V_{CC}, equals the maximum of IN1–IN4. If V_{CC} is externally supplied, V_{CC} must be at least 200mV higher than any voltage applied to IN1–IN4 and V_{CC} must be brought up first. V_{CC} always powers the device when all IN_ are factory set as "ADJ." Do not use the internally generated V_{CC} to provide power to external circuitry.

The MAX6886 generates a digital supply voltage at DBP for the internal logic circuitry and $\overline{RESET}$. Bypass DBP to GND with a 1µF ceramic capacitor installed as close to the device as possible. The nominal DBP output voltage is 2.55V. Do not use DBP to provide power to external circuitry.

Inputs

The MAX6886 contains multiple logic and voltage-detector inputs. Each voltage-detector input is monitored for undervoltage thresholds.

Voltage-Detector Inputs (IN_)

The MAX6886 offers several monitor options with both pin-selectable and adjustable reset thresholds. The threshold voltage at each adjustable IN_ input is typically 0.6V. To monitor a voltage >0.6V, connect a resistor-divider network to the circuit as shown in Figure 1.

$$V_{IN_TH} = V_{TH} (R_1 + R_2) / R_2 \quad \text{(Equation 1)}$$

where V_{IN_TH} is the desired reset threshold voltage for the respective IN_ and V_{TH} is the input threshold (0.6V).

Resistors R_1 and R_2 can have very high values to minimize current consumption due to low-leakage currents. Set R_2 to some conveniently high value (10kΩ, for example) and calculate R_1 based on the desired reset threshold voltage, using the following formula:

$$R_1 = R_2 \times (V_{IN_TH}/V_{TH} - 1)$$

Threshold Logic Inputs (TH0–TH4)

The TH0–TH4 logic inputs select the undervoltage thresholds and tolerance of the IN1–IN6 voltage-detector inputs. TH0–TH4 define 32 unique options for the supervisor functionality. Connect the respective TH_ to GND for a logic 0 or to DBP for a logic 1. Tables 1 and 2 show the 32 unique threshold options available. TH4 sets the threshold tolerance of the undervoltage threshold. A logic 1 selects a 5% supply tolerance and a logic 0 selects a 10% supply tolerance. The MAX6886 logic determines which thresholds should be used for

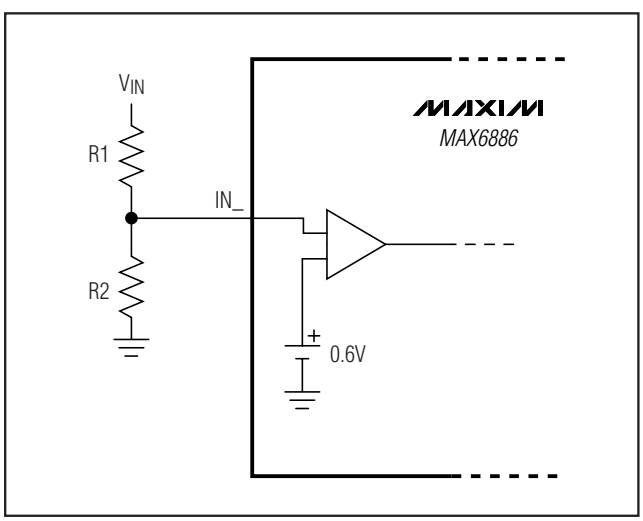


Figure 1. Adjusting the Monitored Threshold

the IN inputs only at power-up. Use the voltage-divider circuit of Figure 1 and Equation 1 to set the threshold for the user-adjustable inputs as described in the *Voltage-Detector Inputs (IN_)* section.

Manual Reset ($\overline{MR}$)

Many microprocessor-based (µP) products require manual reset capability to allow an operator or external logic circuitry to initiate a reset. The manual reset input ($\overline{MR}$) can be connected directly to a switch without an external pullup resistor or debouncing network. $\overline{MR}$ is internally pulled up to DBP. Leave unconnected if not used. $\overline{MR}$ is internally pulled up to DBP through a 10µA current source. $\overline{MR}$ is designed to reject fast, falling transients (typically 100ns pulses) and must be held low for a minimum of 1µs to assert $\overline{RESET}$. After $\overline{MR}$ transitions from low to high, $\overline{RESET}$ remains asserted for the duration of its timeout period.

Table 1. Nominal Monitored Supply Voltages

SELECTION	TH4–TH0*	NOMINAL SUPPLY VOLTAGES (V)						SUPPLY TOLERANCE (%)
		IN1	IN2	IN3	IN4	IN5	IN6	
1	11111	5.0	3.3	2.5	1.8	ADJ	ADJ	5
2	11110	5.0	3.0	2.5	1.8	ADJ	ADJ	5
3	11101	5.0	3.3	2.5	ADJ	ADJ	ADJ	5
4	11100	5.0	3.0	2.5	ADJ	ADJ	ADJ	5
5	11011	5.0	3.3	1.8	ADJ	ADJ	ADJ	5
6	11010	5.0	3.0	1.8	ADJ	ADJ	ADJ	5
7	11001	5.0	3.3	ADJ	ADJ	ADJ	ADJ	5
8	11000	5.0	3.0	ADJ	ADJ	ADJ	ADJ	5
9	10111	3.3	2.5	1.8	ADJ	ADJ	ADJ	5
10	10110	3.0	2.5	1.8	ADJ	ADJ	ADJ	5
11	10101	3.3	2.5	ADJ	ADJ	ADJ	ADJ	5
12	10100	3.0	2.5	ADJ	ADJ	ADJ	ADJ	5
13	10011	3.3	1.8	ADJ	ADJ	ADJ	ADJ	5
14	10010	3.0	1.8	ADJ	ADJ	ADJ	ADJ	5
15	10001	3.3	2.5	1.8	1.5	ADJ	ADJ	5
16	10000	3.0	2.5	1.8	1.5	ADJ	ADJ	5
17	01111	5.0	3.3	2.5	1.8	ADJ	ADJ	10
18	01110	5.0	3.0	2.5	1.8	ADJ	ADJ	10
19	01101	5.0	3.3	2.5	ADJ	ADJ	ADJ	10
20	01100	5.0	3.0	2.5	ADJ	ADJ	ADJ	10
21	01011	5.0	3.3	1.8	ADJ	ADJ	ADJ	10
22	01010	5.0	3.0	1.8	ADJ	ADJ	ADJ	10
23	01001	5.0	3.3	ADJ	ADJ	ADJ	ADJ	10
24	01000	5.0	3.0	ADJ	ADJ	ADJ	ADJ	10
25	00111	3.3	2.5	1.8	ADJ	ADJ	ADJ	10
26	00110	3.0	2.5	1.8	ADJ	ADJ	ADJ	10
27	00101	3.3	2.5	ADJ	ADJ	ADJ	ADJ	10
28	00100	3.0	2.5	ADJ	ADJ	ADJ	ADJ	10
29	00011	3.3	1.8	ADJ	ADJ	ADJ	ADJ	10
30	00010	3.0	1.8	ADJ	ADJ	ADJ	ADJ	10
31	00001	3.3	2.5	1.8	1.5	ADJ	ADJ	10
32	00000	ADJ	ADJ	ADJ	ADJ	ADJ	ADJ	—

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Table 2. Threshold Options

SELECTION	TH4–TH0*	THRESHOLD VOLTAGES (V)					
		IN1	IN2	IN3	IN4	IN5	IN6
1	11111	4.62	3.06	2.31	1.67	0.60	0.60
2	11110	4.62	2.78	2.31	1.67	0.60	0.60
3	11101	4.62	3.06	2.31	0.60	0.60	0.60
4	11100	4.62	2.78	2.31	0.60	0.60	0.60
5	11011	4.62	3.06	1.67	0.60	0.60	0.60
6	11010	4.62	2.78	1.67	0.60	0.60	0.60
7	11001	4.62	3.06	0.60	0.60	0.60	0.60
8	11000	4.62	2.78	0.60	0.60	0.60	0.60
9	10111	3.06	2.31	1.67	0.60	0.60	0.60
10	10110	2.78	2.31	1.67	0.60	0.60	0.60
11	10101	3.06	2.31	0.60	0.60	0.60	0.60
12	10100	2.78	2.31	0.60	0.60	0.60	0.60
13	10011	3.06	1.67	0.60	0.60	0.60	0.60
14	10010	2.78	1.67	0.60	0.60	0.60	0.60
15	10001	3.06	2.31	1.67	1.39	0.60	0.60
16	10000	2.78	2.31	1.67	1.39	0.60	0.60
17	01111	4.38	2.88	2.19	1.58	0.60	0.60
18	01110	4.38	2.62	2.19	1.58	0.60	0.60
19	01101	4.38	2.88	2.19	0.60	0.60	0.60
20	01100	4.38	2.62	2.19	0.60	0.60	0.60
21	01011	4.38	2.88	1.58	0.60	0.60	0.60
22	01010	4.38	2.62	1.58	0.60	0.60	0.60
23	01001	4.38	2.88	0.60	0.60	0.60	0.60
24	01000	4.38	2.62	0.60	0.60	0.60	0.60
25	00111	2.88	2.19	1.58	0.60	0.60	0.60
26	00110	2.62	2.19	1.58	0.60	0.60	0.60
27	00101	2.88	2.19	0.60	0.60	0.60	0.60
28	00100	2.62	2.19	0.60	0.60	0.60	0.60
29	00011	2.88	1.58	0.60	0.60	0.60	0.60
30	00010	2.62	1.58	0.60	0.60	0.60	0.60
31	00001	2.88	2.19	1.58	1.31	0.60	0.60
32	00000	0.60	0.60	0.60	0.60	0.60	0.60

**TH4 = '1' selects 7.5% threshold tolerance, TH4 = '0' selects 12.5% threshold tolerance.*

Contact factory for alternative thresholds.

Margin Output Disable ($\overline{MARGIN}$)

$\overline{MARGIN}$ allows system-level testing while power supplies exceed the normal operating ranges. Drive $\overline{MARGIN}$ low to hold $\overline{RESET}$ in its existing state while system-level testing occurs. Leave $\overline{MARGIN}$ unconnected or connect to DBP if unused. An internal 10µA current source pulls $\overline{MARGIN}$ to DBP. $\overline{MARGIN}$ overrides $\overline{MR}$ if both are asserted at the same time.

Watchdog Timer

The MAX6886's watchdog circuit monitors the µP's activity. If the µP does not toggle the watchdog input (WDI) within the watchdog timeout period, $\overline{RESET}$ asserts. The internal watchdog timer is cleared by a reset, or by a transition at WDI (which can detect pulses as short as 50ns.) The watchdog timer remains cleared while $\overline{RESET}$ is asserted. The timer starts counting as soon as $\overline{RESET}$ goes high (see Figure 2).

The MAX6886 features two modes of watchdog timer operation: normal and initial modes. At power-up, after a reset event, or after the watchdog timer expires, the initial watchdog timeout is active (t_{WDI}). After the first transition on WDI, the normal watchdog timeout is active (t_{WD}). The initial and normal watchdog timeouts are determined by the value of the capacitor connected between SWT and ground. The initial watchdog timeout is approximately 64 times the normal watchdog timeout.

Connect a capacitor from SWT to GND to determine the normal watchdog timeout period according to the following equation:

$$C_{SWT} = \frac{t_{WD}}{4.348 \times 10^6}$$

where t_{WD} is in seconds and C_{SWT} is in Farads. As an example, a 1µF capacitor gives a normal timeout period of 4.68s and an initial watchdog timeout period of approximately 4.5 minutes. Connect SWT to V_{CC} to use the factory-default watchdog normal and initial timeouts of 1.6s and 102.4s, respectively. Choose a low-leakage capacitor for C_{SWT}. Disable the watchdog timer by connecting SWT to GND. WDI is internally pulled down to GND through a 10µA current sink.

$\overline{RESET}$ Output

The reset output is typically connected to the reset input of a µP. A µP's reset input starts or restarts the µP in a known state. $\overline{RESET}$ goes low whenever one or more input voltage (IN1–IN6) monitors drop below their respective thresholds, when $\overline{MR}$ is pulled low for a minimum of 1µs, or when the watchdog timer expires. $\overline{RESET}$ remains low for its reset timeout period (t_{RP}) after all assertion-causing conditions have been cleared (see Figure 2).

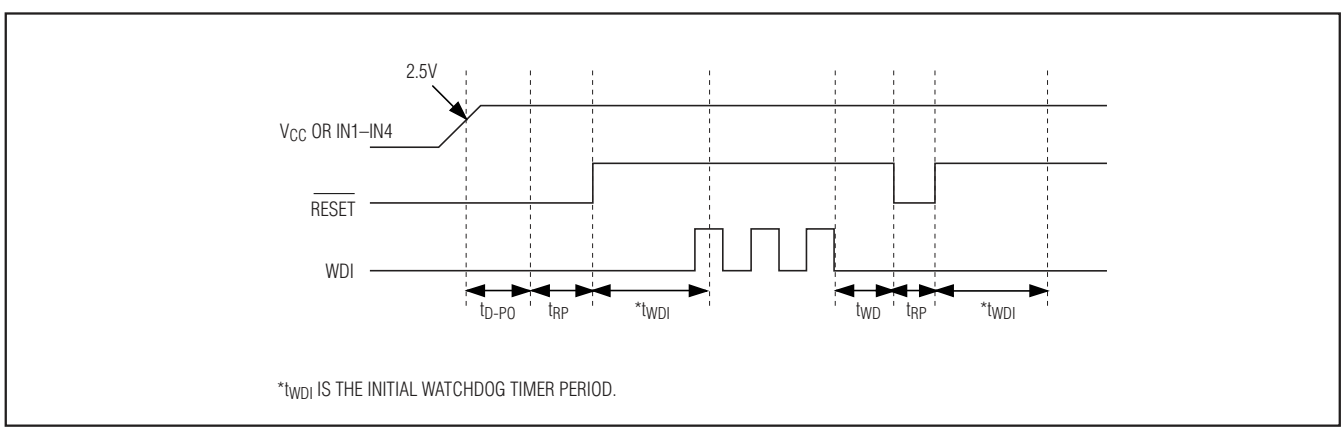

Figure 2. Watchdog, Reset, and Power-Up Timing Diagram

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Set the $\overline{RESET}$ time delay by connecting a capacitor from SRT to GND using the following equation:

$$C_{SRT} = \frac{t_{WD}}{4.348 \times 10^6}$$

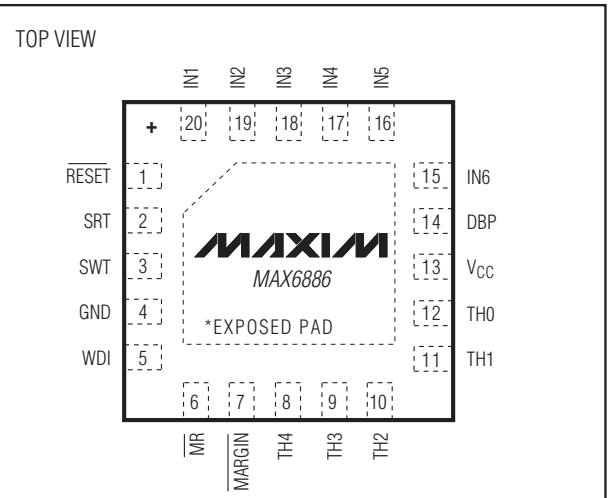
where t_{RP} is in seconds and C_{SRT} is in Farads. Connect SRT to V_{CC} for a factory-default reset timeout of 200ms. $\overline{RESET}$ is open-drain and requires an external pullup resistor. $\overline{RESET}$ remains low for $1V \le V_{CC} \le 2.5V$.

Applications Information

Layout and Bypassing

For better noise immunity, bypass each of the voltage-detector inputs to GND with 0.1µF capacitors installed as close to the device as possible. Bypass V_{CC} and DBP to GND with 1µF capacitors installed as close to the device as possible.

Pin Configuration



TQFN

*EXPOSED PAD CONNECTED TO GND.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 TQFN-EP	T2055+5	21-0140	90-0010

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/05	Initial release	—
1	1/12	Updated Table 2.	10

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