# Isolated, Single-Channel RS-232 Line Driver/Receiver

Data Sheet

# ADM3251E

## FEATURES

- 2.5 kV fully isolated (power and data) RS-232 transceiver
- *iso*Power integrated, isolated dc-to-dc converter
- 460 kbps data rate
- 1 Tx and 1 Rx
- Meets EIA/TIA-232E specifications
- ESD protection on $R_{IN}$ and $T_{OUT}$ pins
  - ±8 kV: contact discharge
  - ±15 kV: air gap discharge
- 0.1 µF charge pump capacitors
- High common-mode transient immunity: >25 kV/µs
- Safety and regulatory approvals
  - UL recognition
    - 2500 V rms for 1 minute per UL 1577
  - VDE Certificate of Conformity
    - DIN EN 60747-5-2 (VDE 0884 Teil 2): 2003-01
  - CSA Component Acceptance Notice #5A
- Operating temperature range: −40°C to +85°C
- Wide body, 20-lead SOIC package

## APPLICATIONS

- High noise data communications
- Industrial communications
- General-purpose RS232 data links
- Industrial/telecommunications diagnostic ports
- Medical equipment

## FUNCTIONAL BLOCK DIAGRAM

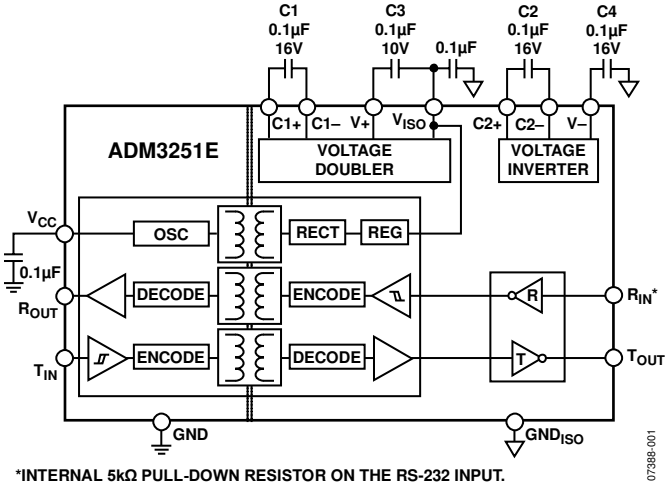


*Figure 1.*

## GENERAL DESCRIPTION

The ADM3251E[1] is a high speed, 2.5 kV fully isolated, single-channel RS-232/V.28 transceiver device that operates from a single 5 V power supply. Due to the high ESD protection on the $R_{IN}$ and $T_{OUT}$ pins, the device is ideally suited for operation in electrically harsh environments or where RS-232 cables are frequently being plugged and unplugged.

The ADM3251E incorporates dual-channel digital isolators with *iso*Power™ integrated, isolated power. There is no requirement to use a separate isolated dc-to-dc converter. Chip-scale transformer *i*Coupler® technology from Analog Devices, Inc., is used both for the isolation of the logic signals as well as for the integrated dc-to-dc converter. The result is a total isolation solution.

The ADM3251E contains *iso*Power technology that uses high frequency switching elements to transfer power through the transformer. Special care must be taken during printed circuit board (PCB) layout to meet emissions standards. Refer to Application Note AN-0971, *Control of Radiated Emissions with isoPower Devices*, for details on board layout considerations.

The ADM3251E conforms to the EIA/TIA-232E and ITU-T V. 28 specifications and operates at data rates up to 460 kbps.

Four external 0.1 µF charge pump capacitors are used for the voltage doubler/inverter, permitting operation from a single 5 V supply.

The ADM3251E is available in a 20-lead, wide body SOIC package and is specified over the −40°C to +85°C temperature range.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; and 7,075,329.

Rev. G


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## REVISION HISTORY

**10/13—Rev. F to Rev. G**

Added Patents Information, Note 1 ... 1
Changed Minimum External Tracking (Creepage) Value to 7.6 mm, Table 5 ... 5
Changes to Pin 9 Description and Pin 11 Descriptions, Table 8 ... 8
Changes to Isolation of Power and Data Section ... 11
Changes to Pollution Degree and Input–to-Output Test Voltage Parameters, Table 6 ... 6
Added Applications Information Section and Example PCB for Reduced EMI Section; Added Table 9 and Table 10; Renumbered Sequentially ... 13
Changes to PCB Layout Section ... 13
Added Isolated Power Supply Circuit Section, and Figure 22; Renumbered Sequentially ... 14

**6/12—Rev. E to Rev. F**

Changes to Endnote 1 in Table 4 ... 5
Added DC Correctness and Magnetic Field Immunity Section ... 13
Added Figure 22 and Figure 23; Renumbered Sequentially ... 14
Updated Outline Dimensions and Changes to Ordering Guide ... 15

**5/10—Rev. D to Rev. E**

Changes to Features Section ... 1
Changes to Table 4 ... 5

**3/10—Rev. C to Rev. D**

Changes to Features and General Description Sections ... 1
Changes to Table 4 and Table 5 ... 5
Changed DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 Insulation Characteristics (Pending) Heading to DIN EN 60747-5-2 (VDE 0884 Teil 2): 2003-01 Insulation Characteristics ... 6

**1/10—Rev. B to Rev. C**

Changes to Table 4 ... 5

11/09—Rev. A to Rev. B

Changes to Figure 1 ... 1
Changed to Primary Side Supply Input Current, $I_{CC(DISABLE)}$ Maximum Limit to 2.5 mA ... 4
Changes to Table 4 ... 5
Changes to Figure 13 ... 11

**9/08—Rev. 0 to Rev. A**

Changes to Timing Parameters in Table 1 ... 3
Changes to Timing Parameters in Table 2 ... 4
Changes to Ordering Guide ... 14

**7/08—Revision 0: Initial Version**

# SPECIFICATIONS

All voltages are relative to their respective ground; all minimum/maximum specifications apply over the entire recommended operating range; $T_A$ = 25°C and $V_{CC}$ = 5.0 V (dc-to-dc converter enabled), unless otherwise noted.

**Table 1.**

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| DC CHARACTERISTICS | | | | | |
| $V_{CC}$ Operating Voltage Range | 4.5 | | 5.5 | V | |
| DC-to-DC Converter Enable Threshold, $V_{CC(ENABLE)}$[1] | 4.5 | | | V | |
| DC-to-DC Converter Disable Threshold, $V_{CC(DISABLE)}$[1] | | | 3.7 | V | |
| DC-to-DC Converter Enabled | | | | | |
| Input Supply Current, $I_{CC(ENABLE)}$ | | | 110 | mA | $V_{CC}$ = 5.5 V, no load |
| | | | 145 | mA | $V_{CC}$ = 5.5 V, $R_L$ = 3 kΩ |
| $V_{ISO}$ Output[2] | | 5.0 | | V | $I_{ISO}$ = 0 µA |
| LOGIC | | | | | |
| Transmitter Input, $T_{IN}$ | | | | | |
| Logic Input Current, $I_{TIN}$ | −10 | +0.01 | +10 | µA | |
| Logic Low Input Threshold, $V_{TINL}$ | | | 0.3 $V_{CC}$ | V | |
| Logic High Input Threshold, $V_{TINH}$ | 0.7 $V_{CC}$ | | | V | |
| Receiver Output, $R_{OUT}$ | | | | | |
| Logic High Output, $V_{ROUTH}$ | $V_{CC}$ − 0.1 | $V_{CC}$ | | V | $I_{ROUTH}$ = −20 µA |
| | $V_{CC}$ − 0.5 | $V_{CC}$ − 0.3 | | V | $I_{ROUTH}$ = −4 mA |
| Logic Low Output, $V_{ROUTL}$ | | 0.0 | 0.1 | V | $I_{ROUTH}$ = 20 µA |
| | | 0.3 | 0.4 | V | $I_{ROUTH}$ = 4 mA |
| RS-232 | | | | | |
| Receiver, $R_{IN}$ | | | | | |
| EIA-232 Input Voltage Range[3] | −30 | | +30 | V | |
| EIA-232 Input Threshold Low | 0.6 | 2.0 | | V | |
| EIA-232 Input Threshold High | | 2.1 | 2.4 | V | |
| EIA-232 Input Hysteresis | | 0.1 | | V | |
| EIA-232 Input Resistance | 3 | 5 | 7 | kΩ | |
| Transmitter, $T_{OUT}$ | | | | | |
| Output Voltage Swing (RS-232) | ±5 | ±5.7 | | V | $R_L$ = 3 kΩ to GND |
| Transmitter Output Resistance | 300 | | | Ω | $V_{ISO}$ = 0 V |
| Output Short-Circuit Current (RS-232) | | ±12 | | mA | |
| TIMING CHARACTERISTICS | | | | | |
| Maximum Data Rate | 460 | | | kbps | $R_L$ = 3 kΩ to 7 kΩ, $C_L$ = 50 pF to 1000 pF |
| Receiver Propagation Delay | | | | | |
| $t_{PHL}$ | | 190 | | ns | |
| $t_{PLH}$ | | 135 | | ns | |
| Transmitter Propagation Delay | | 650 | | ns | $R_L$ = 3 kΩ, $C_L$ = 1000 pF |
| Transmitter Skew | | 80 | | ns | |
| Receiver Skew | | 70 | | ns | |
| Transition Region Slew Rate[3] | 5.5 | 10 | 30 | V/µs | +3 V to −3 V or −3 V to +3 V, $V_{CC}$ = +3.3 V, $R_L$ = 3 kΩ, $C_L$ = 1000 pF, $T_A$ = 25°C |
| AC SPECIFICATIONS | | | | | |
| Output Rise/Fall Time, $t_R/t_F$ (10% to 90%) | | 2.3 | | ns | $C_L$ = 15 pF, CMOS signal levels |
| Common-Mode Transient Immunity at Logic High Output[4] | 25 | | | kV/µs | $V_{CM}$ = 1 kV, transient magnitude = 800 V |
| Common-Mode Transient Immunity at Logic Low Output[4] | 25 | | | kV/µs | $V_{CM}$ = 1 kV, transient magnitude = 800 V |
| ESD PROTECTION ($R_{IN}$ And $T_{OUT}$ PINS) | | ±15 | | kV | Human body model air discharge |
| | | ±8 | | kV | Human body model contact discharge |

[1] Enable/disable threshold is the $V_{CC}$ voltage at which the internal dc-to-dc converter is enabled/disabled.
[2] To maintain data sheet specifications, do not draw current from $V_{ISO}$.
[3] Guaranteed by design.
[4] $V_{CM}$ is the maximum common-mode voltage slew rate that can be sustained while maintaining specification-compliant operation. $V_{CM}$ is the common-mode potential difference between the logic and bus sides. The transient magnitude is the range over which the common mode is slewed. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

All voltages are relative to their respective ground; all minimum/maximum specifications apply over the entire recommended operating range; $T_A$ = 25°C, $V_{CC}$ = 3.3 V (dc-to-dc converter disabled), and the secondary side is powered externally by $V_{ISO}$ = 3.3 V, unless otherwise noted.

**Table 2.**

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| DC CHARACTERISTICS | | | | | |
| $V_{CC}$ Operating Voltage Range | 3.0 | | 3.7 | V | |
| DC-to-DC Converter Disable Threshold, $V_{CC(DISABLE)}$[1] | | | 3.7 | V | |
| DC-to-DC Converter Disabled | | | | | |
| $V_{ISO}$[2] | 3.0 | | 5.5 | V | |
| Primary Side Supply Input Current, $I_{CC(DISABLE)}$ | | | 2.5 | mA | No load |
| Secondary Side Supply Input Current, $I_{ISO(DISABLE)}$ | | | 12 | mA | $V_{ISO}$ = 5.5 V, $R_L$ = 3 kΩ |
| Secondary Side Supply Input Current, $I_{ISO(DISABLE)}$ | | 6.2 | | mA | $R_L$ = 3 kΩ |
| LOGIC | | | | | |
| Transmitter Input, $T_{IN}$ | | | | | |
| Logic Input Current, $I_{TIN}$ | −10 | +0.01 | +10 | µA | |
| Logic Low Input Threshold, $V_{TINL}$ | | | 0.3 $V_{CC}$ | V | |
| Logic High Input Threshold, $V_{TINH}$ | 0.7 $V_{CC}$ | | | V | |
| Receiver Output, $R_{OUT}$ | | | | | |
| Logic High Output, $V_{ROUTH}$ | $V_{CC}$ − 0.1 | $V_{CC}$ | | V | $I_{ROUTH}$ = −20 µA |
| | $V_{CC}$ − 0.5 | $V_{CC}$ − 0.3 | | V | $I_{ROUTH}$ = −4 mA |
| Logic Low Output, $V_{ROUTL}$ | | 0.0 | 0.1 | V | $I_{ROUTH}$ = 20 µA |
| | | 0.3 | 0.4 | | $I_{ROUTH}$ = 4 mA |
| RS-232 | | | | V | |
| Receiver, $R_{IN}$ | | | | | |
| EIA-232 Input Voltage Range[3] | −30 | | +30 | V | |
| EIA-232 Input Threshold Low | 0.6 | 1.3 | | V | |
| EIA-232 Input Threshold High | | 1.6 | 2.4 | V | |
| EIA-232 Input Hysteresis | | 0.3 | | V | |
| EIA-232 Input Resistance | 3 | 5 | 7 | kΩ | |
| Transmitter, $T_{OUT}$ | | | | | |
| Output Voltage Swing (RS-232) | ±5 | ±5.7 | | V | $R_L$ = 3 kΩ to GND |
| Transmitter Output Resistance | 300 | | | Ω | $V_{ISO}$ = 0 V |
| Output Short-Circuit Current (RS-232) | | ±11 | | mA | |
| TIMING CHARACTERISTICS | | | | | |
| Maximum Data Rate | 460 | | | kbps | $R_L$ = 3 kΩ to 7 kΩ, $C_L$ = 50 pF to 1000 pF |
| Receiver Propagation Delay | | | | | |
| $t_{PHL}$ | | 190 | | ns | |
| $t_{PLH}$ | | 135 | | ns | |
| Transmitter Propagation Delay | | 650 | | ns | $R_L$ = 3 kΩ, $C_L$ = 1000 pF |
| Transmitter Skew | | 80 | | ns | |
| Receiver Skew | | 55 | | ns | |
| Transition Region Slew Rate[3] | 5.5 | 10 | 30 | V/µs | +3 V to −3 V or −3 V to +3 V, $V_{CC}$ = 3.3 V, $R_L$ = 3 kΩ, $C_L$ = 1000 pF, $T_A$ = 25°C |
| AC SPECIFICATIONS | | | | | |
| Output Rise/Fall Time, $t_R/t_F$ (10% to 90%) | | 2.3 | | ns | $C_L$ = 15 pF, CMOS signal levels |
| Common-Mode Transient Immunity at Logic High Output[4] | 25 | | | kV/µs | $V_{CM}$ = 1 kV, transient magnitude = 800 V |
| Common-Mode Transient Immunity at Logic Low Output[4] | 25 | | | kV/µs | $V_{CM}$ = 1 kV, transient magnitude = 800 V |
| ESD PROTECTION ($R_{IN}$ AND $T_{OUT}$ PINS) | | ±15 | | kV | Human body model air discharge |
| | | ±8 | | kV | Human body model contact discharge |

[1] Enable/disable threshold is the $V_{CC}$ voltage at which the internal dc-to-dc converter is enabled/disabled.
[2] To maintain data sheet specifications, do not draw current from $V_{ISO}$.
[3] Guaranteed by design.
[4] $V_{CM}$ is the maximum common-mode voltage slew rate that can be sustained while maintaining specification-compliant operation. $V_{CM}$ is the common-mode potential difference between the logic and bus sides. The transient magnitude is the range over which the common mode is slewed. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

## PACKAGE CHARACTERISTICS

**Table 3.**

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Resistance (Input-to-Output) | $R_{I-O}$ | | $10^{12}$ | | Ω | |
| Capacitance (Input-to-Output) | $C_{I-O}$ | | 2.2 | | pF | f = 1 MHz |
| Input Capacitance | $C_I$ | | 4.0 | | pF | |
| IC Junction-to-Air Thermal Resistance | $\theta_{JA}$ | | 47.05 | | °C/W | |

## REGULATORY INFORMATION

**Table 4.**

| UL[1] | VDE[2] | CSA |
|---|---|---|
| Recognized under 1577 Component Recognition Program<br>File E214100 | Certified according to DIN EN 60747-5-2 (VDE 0884 Teil 2):2003-01<br>File 2471900-4880-0001/123328 | Approved under CSA Component Acceptance Notice #5A<br>Basic Insulation per CSA 60950-1-07 and IEC 60950-1, 400 V rms (566 V peak) maximum working voltage<br>File 2268268 |

[1] In accordance with UL 1577, each ADM3251E is proof tested by applying an insulation test voltage ≥3000 V rms for 1 sec (current leakage detection limit = 6 μA).
[2] Each ADM3251E is proof tested by applying an insulation test voltage ≥4000 V peak for 1 sec (partial discharge detection limit = 5 pC).

## INSULATION AND SAFETY-RELATED SPECIFICATIONS

**Table 5.**

| Parameter | Symbol | Value | Unit | Conditions |
|---|---|---|---|---|
| Rated Dielectric Insulation Voltage | | 2500 | V rms | 1 minute duration |
| Minimum External Air Gap (Clearance) | L(I01) | 7.7 | mm | Measured from input terminals to output terminals, shortest distance through air |
| Minimum External Tracking (Creepage) | L(I02) | 7.6 | mm | Measured from input terminals to output terminals, shortest distance path along body |
| Minimum Internal Gap (Internal Clearance) | | 0.017 | mm | Distance through insulation |
| Tracking Resistance (Comparative Tracking Index) | CTI | >175 | V | DIN IEC 112/VDE 0303 Part 1 |
| Isolation Group | | IIIa | | |
| Maximum Working Voltage Compatible with 50-Year Service Life | $V_{IORM}$ | 425 | V peak | Continuous peak voltage across the isolation barrier |

## DIN EN 60747-5-2 (VDE 0884 TEIL 2): 2003-01 INSULATION CHARACTERISTICS

This isolator is suitable for reinforced isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits.

**Table 6.**

| Description | Conditions | Symbol | Characteristic | Unit |
|---|---|---|---|---|
| Installation Classification per DIN VDE 0110 | | | | |
| For Rated Mains Voltage ≤ 150 V rms | | | I to IV | |
| For Rated Mains Voltage ≤ 300 V rms | | | I to III | |
| Climatic Classification | | | 40/105/21 | |
| Pollution Degree | | | 2 | |
| Maximum Working Insulation Voltage | | $V_{IORM}$ | 424 | V peak |
| Input-to-Output Test Voltage | | | | |
| Method b1 | $V_{IORM} \times 1.875 = V_{PR}$, 100% production test, $t_m$ = 1 sec, partial discharge < 5 pC | $V_{PR}$ | 795 | V peak |
| Highest Allowable Overvoltage | Transient overvoltage, $t_{TR}$ = 10 sec | $V_{TR}$ | 4000 | V peak |
| Safety-Limiting Values | Maximum value allowed in the event of a failure | | | |
| Case Temperature | | $T_S$ | 150 | °C |
| Supply Current | | $I_{S1}$ | 531 | mA |
| Insulation Resistance at $T_S$ | $V_{IO}$ = 500 V | $R_S$ | $>10^9$ | Ω |

# ABSOLUTE MAXIMUM RATINGS

**Table 7.**

| Parameter | Rating |
|---|---|
| $V_{CC}$, $V_{ISO}$ | −0.3 V to +6 V |
| V+ | ($V_{CC}$ − 0.3 V ) to +13 V |
| V− | −13 V to +0.3 V |
| Input Voltages | |
| $T_{IN}$ | −0.3 V to ($V_{CC}$ + 0.3 V ) |
| $R_{IN}$ | ±30 V |
| Output Voltages | |
| $T_{OUT}$ | ±15 V |
| $R_{OUT}$ | −0.3 V to ($V_{CC}$ + 0.3 V ) |
| Short-Circuit Duration | |
| $T_{OUT}$ | Continuous |
| Power Dissipation | |
| $\theta_{JA}$, Thermal Impedance | 47.05°C/W |
| Operating Temperature Range | |
| Industrial | −40°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Pb-Free Temperature (Soldering, 30 sec) | 260°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

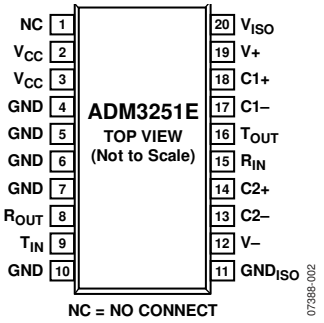


*Figure 2. Pin Configuration*

**Table 8. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | NC | No Connect. This pin should always remain unconnected. |
| 2, 3 | $V_{CC}$ | Power Supply Input. A 0.1 µF decoupling capacitor is required between $V_{CC}$ and ground. When a voltage between 4.5 V and 5.5 V is applied to the $V_{CC}$ pin, the integrated dc-to-dc converter is enabled. If this voltage is lowered to between 3.0 V and 3.7 V, the integrated dc-to-dc converter is disabled. |
| 4, 5, 6, 7, 10 | GND | Ground. |
| 8 | $R_{OUT}$ | Receiver Output. This pin outputs CMOS logic levels. |
| 9 | $T_{IN}$ | Transmitter (Driver) Input. This pin accepts CMOS levels. |
| 11 | $GND_{ISO}$ | Ground Reference for Isolated RS-232 Side. |
| 12 | V– | Internally Generated Negative Supply. |
| 13, 14 | C2–, C2+ | Positive and Negative Connections for Charge Pump Capacitors. External Capacitor C2 is connected between these pins; a 0.1 µF capacitor is recommended, but larger capacitors up to 10 µF can be used. |
| 15 | $R_{IN}$ | Receiver Input. This input accepts RS-232 signal levels. |
| 16 | $T_{OUT}$ | Transmitter (Driver) Output. This outputs RS-232 signal levels. |
| 17, 18 | C1–, C1+ | Positive and Negative Connections for Charge Pump Capacitors. External Capacitor C1 is connected between these pins; a 0.1 µF capacitor is recommended, but larger capacitors up to 10 µF can be used. |
| 19 | V+ | Internally Generated Positive Supply. |
| 20 | $V_{ISO}$ | Isolated Supply Voltage for Isolator Secondary Side. A 0.1 µF decoupling capacitor is required between $V_{ISO}$ and ground. When the integrated dc-to-dc converter is enabled, the $V_{ISO}$ pin should not be used to power external circuitry. If the integrated dc-to-dc converter is disabled, power the secondary side by applying a voltage in the range of 3.0 V to 5.5 V to this pin. |

# TYPICAL PERFORMANCE CHARACTERISTICS

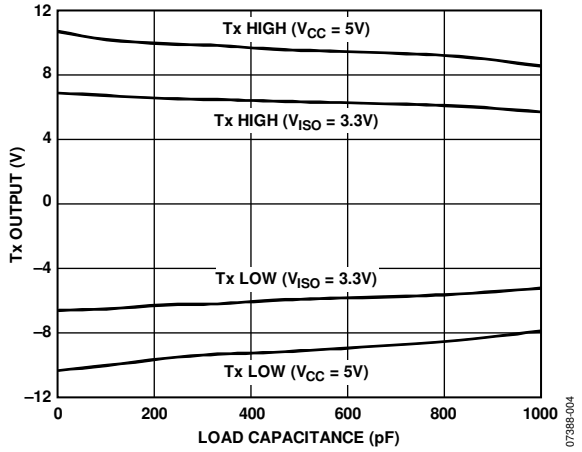


*Figure 3. Transmitter Output Voltage High/Low vs. Load Capacitance at 460 kbps*

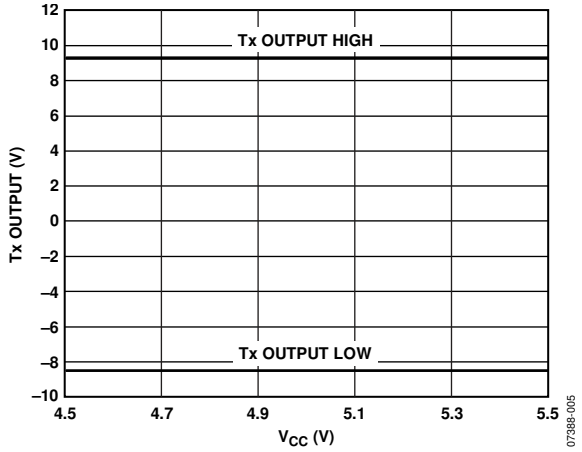


*Figure 4. Transmitter Output Voltage High/Low vs. $V_{CC}$, $R_L$ = 3 kΩ*

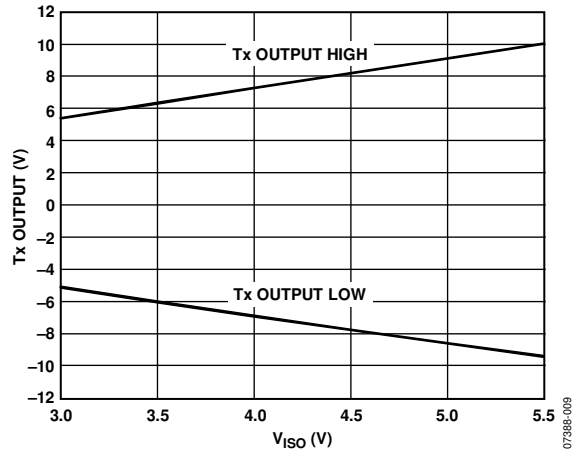


*Figure 5. Transmitter Output Voltage High/Low vs. $V_{ISO}$, $R_L$ = 3 kΩ*

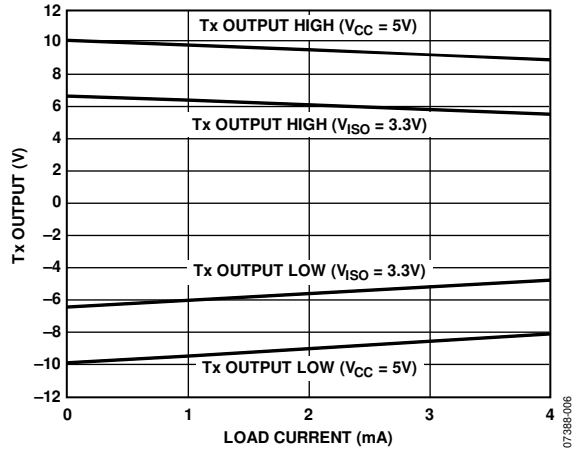


*Figure 6. Transmitter Output Voltage High/Low vs. Load Current*

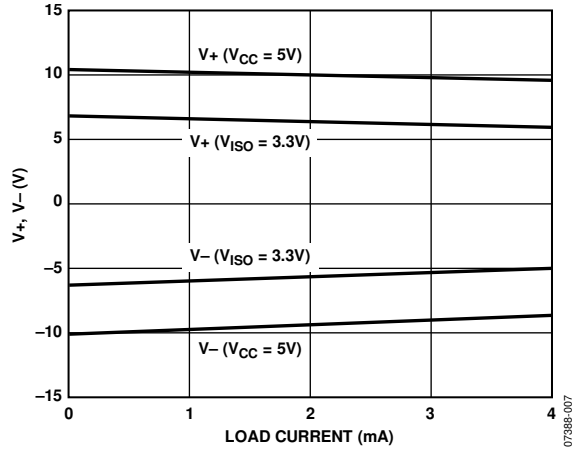


*Figure 7. Charge Pump V+, V– vs. Load Current*

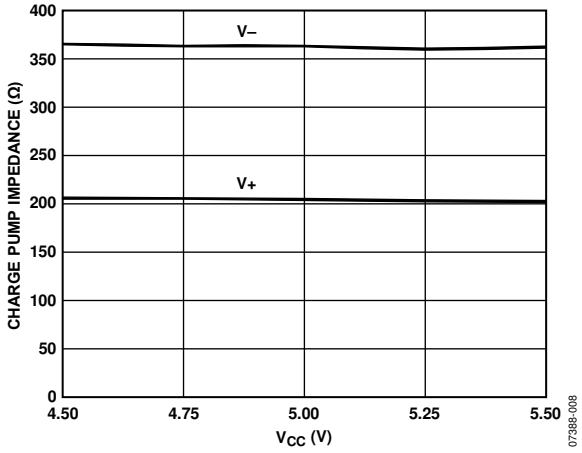


*Figure 8. Charge Pump Impedance vs. $V_{CC}$*

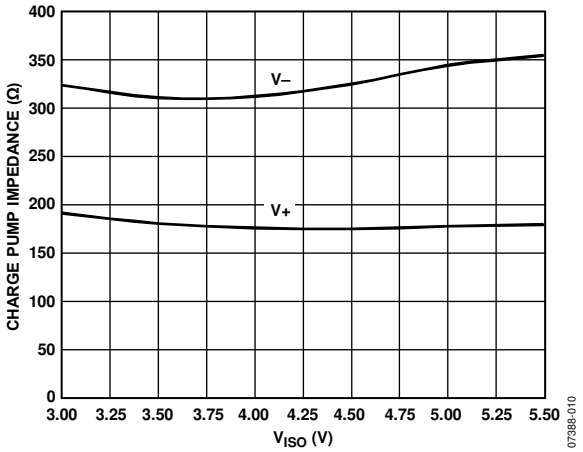


Figure 9. Charge Pump Impedance vs. $V_{ISO}$

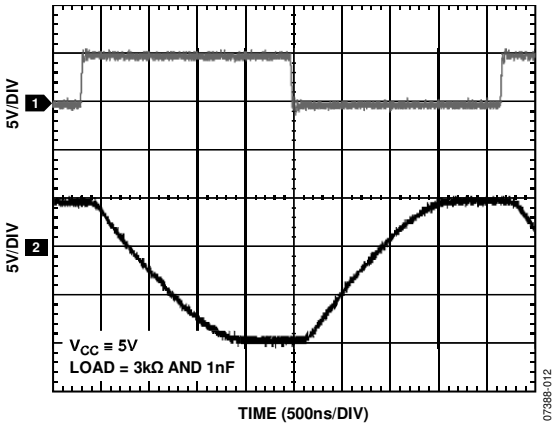


Figure 11. 460 kbps Data Transmission

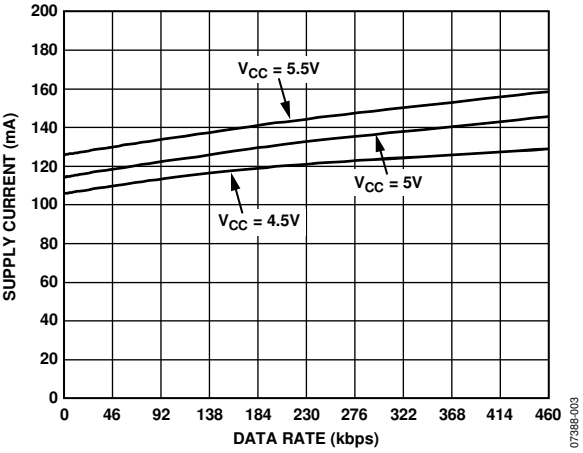


Figure 10. Primary Supply Current vs. Data Rate

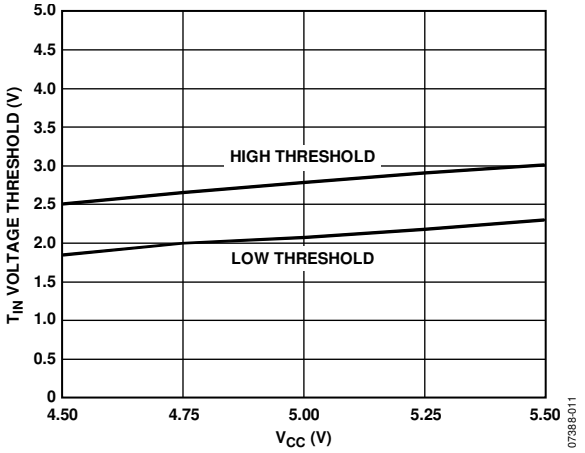


Figure 12. $T_{IN}$ Voltage Threshold vs. $V_{CC}$

# THEORY OF OPERATION

The ADM3251E is a high speed, 2.5 kV fully isolated, single-channel RS-232 transceiver device that operates from a single power supply.

The internal circuitry consists of the following main sections:

- Isolation of power and data
- A charge pump voltage converter
- A 5.0 V logic to EIA/TIA-232E transmitter
- A EIA/TIA-232E to 5.0 V logic receiver

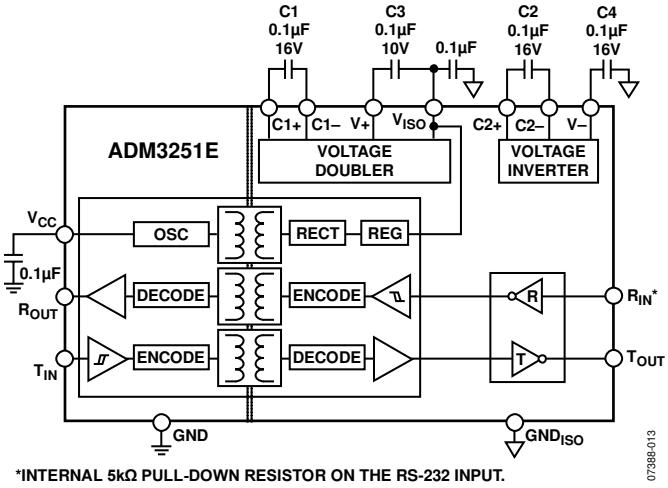


*Figure 13. Functional Block Diagram*

## ISOLATION OF POWER AND DATA

The ADM3251E incorporates a dc-to-dc converter section, which works on principles that are common to most modern power supply designs. $V_{CC}$ power is supplied to an oscillating circuit that switches current into a chip-scale air core transformer. Power is transferred to the secondary side, where it is rectified to a high dc voltage. The power is then linearly regulated to about 5.0 V and supplied to the secondary side data section and to the $V_{ISO}$ pin. The $V_{ISO}$ pin should not be used to power external circuitry.

Because the oscillator runs at a constant high frequency independent of the load, excess power is internally dissipated in the output voltage regulation process. Limited space for transformer coils and components also adds to internal power dissipation. This results in low power conversion efficiency.

The ADM3251E can be operated with the dc-to-dc converter enabled or disabled. The internal dc-to-dc converter state of the ADM3251E is controlled by the input $V_{CC}$ voltage. In normal operating mode, $V_{CC}$ is set between 4.5 V and 5.5 V and the internal dc-to-dc converter is enabled. To disable the dc-to-dc converter, lower $V_{CC}$ to a value between 3.0 V and 3.7 V. In this mode, the user must externally supply isolated power to the $V_{ISO}$ pin. An isolated secondary side voltage of between 3.0 V and 5.5 V and a secondary side input current, $I_{ISO}$, of 12 mA (maximum) is required on the $V_{ISO}$ pin. The signal channels of the ADM3251E then continue to operate normally.

The $T_{IN}$ pin accepts CMOS input levels (and TTL levels at $V_{CC}$ = 3.3 V). The driver input signal that is applied to the $T_{IN}$ pin is referenced to logic ground (GND). It is coupled across the isolation barrier, inverted, and then appears at the transceiver section, referenced to isolated ground ($GND_{ISO}$). Similarly, the receiver input ($R_{IN}$) accepts RS-232 signal levels that are referenced to isolated ground. The $R_{IN}$ input is inverted and coupled across the isolation barrier to appear at the $R_{OUT}$ pin, referenced to logic ground.

The digital signals are transmitted across the isolation barrier using *i*Coupler technology. Chip-scale transformer windings couple the digital signals magnetically from one side of the barrier to the other. Digital inputs are encoded into waveforms that are capable of exciting the primary transformer of the winding. At the secondary winding, the induced waveforms are decoded into the binary value that was originally transmitted.

There is hysteresis in the $V_{CC}$ input voltage detect circuit. Once the dc-to-dc converter is active, the input voltage must be decreased below the turn-on threshold to disable the converter. This feature ensures that the converter does not go into oscillation due to noisy input power.

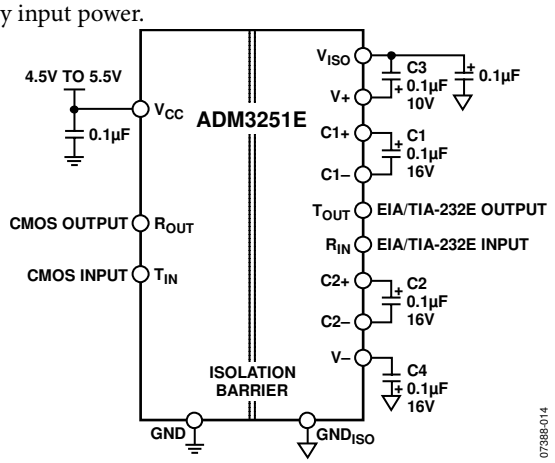


*Figure 14. Typical Operating Circuit with the DC-to-DC Converter Enabled ($V_{CC}$ = 4.5 V to 5.5 V)*

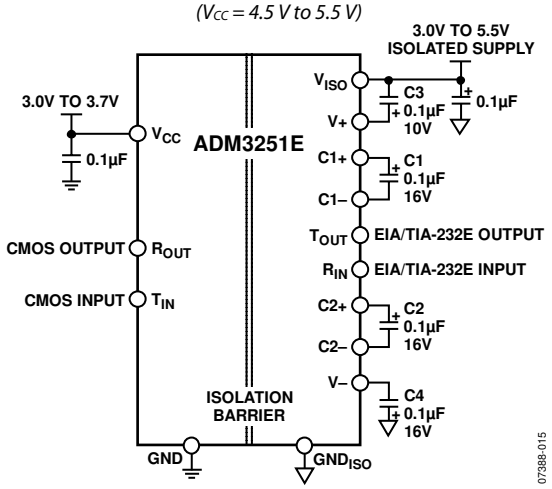


*Figure 15. Typical Operating Circuit with the DC-to-DC Converter Disabled ($V_{CC}$ = 3.0 V to 3.7 V)*

## CHARGE PUMP VOLTAGE CONVERTER

The charge pump voltage converter consists of a 200 kHz oscillator and a switching matrix. The converter generates a ±10.0 V supply from the input 5.0 V level. This is done in two stages by using a switched capacitor technique as illustrated in Figure 16 and Figure 17. First, the 5.0 V input supply is doubled to 10.0 V by using C1 as the charge storage element. The +10.0 V level is then inverted to generate −10.0 V using C2 as the storage element. C3 is shown connected between V+ and $V_{ISO}$, but is equally effective if connected between V+ and $GND_{ISO}$.

Capacitor C3 and Capacitor C4 are used to reduce the output ripple. Their values are not critical and can be increased, if desired. Larger capacitors (up to 10 µF) can be used in place of C1, C2, C3, and C4.

## 5.0 V LOGIC TO EIA/TIA-232E TRANSMITTER

The transmitter driver converts the 5.0 V logic input levels into RS-232 output levels. When driving an RS-232 load with $V_{CC}$ = 5.0 V, the output voltage swing is typically ±10 V.

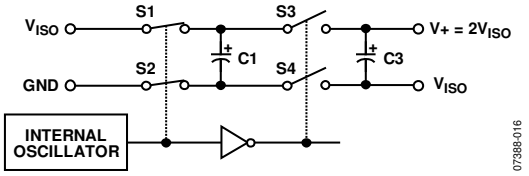


*Figure 16. Charge Pump Voltage Doubler*

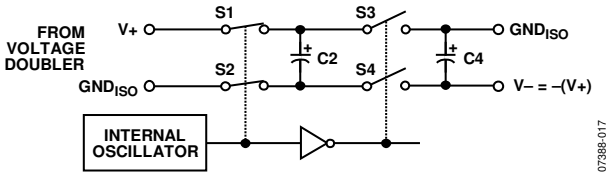


*Figure 17. Charge Pump Voltage Inverter*

## EIA/TIA-232E TO 5 V LOGIC RECEIVER

The receiver is an inverting level-shifter that accepts the RS-232 input level and translates it into a 5.0 V logic output level. The input has an internal 5 kΩ pull-down resistor to ground and is also protected against overvoltages of up to ±30 V. An unconnected input is pulled to 0 V by the internal 5 kΩ pull-down resistor. This, therefore, results in a Logic 1 output level for an unconnected input or for an input connected to GND. The receiver has a Schmitt-trigger input with a hysteresis level of 0.1 V. This ensures error-free reception for both a noisy input and for an input with slow transition times.

## HIGH BAUD RATE

The ADM3251E offers high slew rates, permitting data transmission at rates well in excess of the EIA/TIA-232E specifications. The RS-232 voltage levels are maintained at data rates up to 460 kbps.

## THERMAL ANALYSIS

Each ADM3251E device consists of three internal die, attached to a split-paddle lead frame. For the purposes of thermal analysis, it is treated as a thermal unit with the highest junction temperature reflected in the $\theta_{JA}$ value from Table 7. The value of $\theta_{JA}$ is based on measurements taken with the part mounted on a JEDEC standard 4-layer PCB with fine-width traces in still air. Following the recommendations in the PCB Layout section decreases the thermal resistance to the PCB, allowing increased thermal margin at high ambient temperatures.

## INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADM3251E.

The insulation lifetime of the ADM3251E depends on the voltage waveform type imposed across the isolation barrier. The iCoupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 18, Figure 19, and Figure 20 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower.

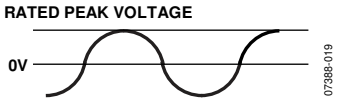


*Figure 18. Bipolar AC Waveform*

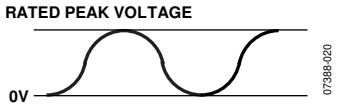


*Figure 19. Unipolar AC Waveform*

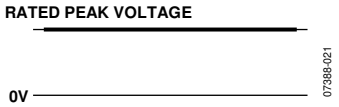


*Figure 20. DC Waveform Outline Dimensions*

# APPLICATIONS INFORMATION

## PCB LAYOUT

The ADM3251E requires no external circuitry for its logic interfaces. Power supply bypassing is required at the input and output supply pins (see Figure 21). Bypass capacitors are conveniently connected between Pin 3 and Pin 4 for $V_{CC}$ and between Pin 19 and Pin 20 for $V_{ISO}$. The capacitor value should be between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm.

Because it is not possible to apply a heat sink to an isolation device, the device primarily depends on heat dissipating into the PCB through the ground pins. If the device is used at high ambient temperatures, care should be taken to provide a thermal path from the ground pins to the PCB ground plane. The board layout in Figure 21 shows enlarged pads for Pin 4, Pin5, Pin 6, Pin 7, Pin 10, and Pin 11. Multiple vias should be implemented from each of the pads to the ground plane, which significantly reduce the temperatures inside the chip. The dimensions of the expanded pads are left to the discretion of the designer and the available board space.

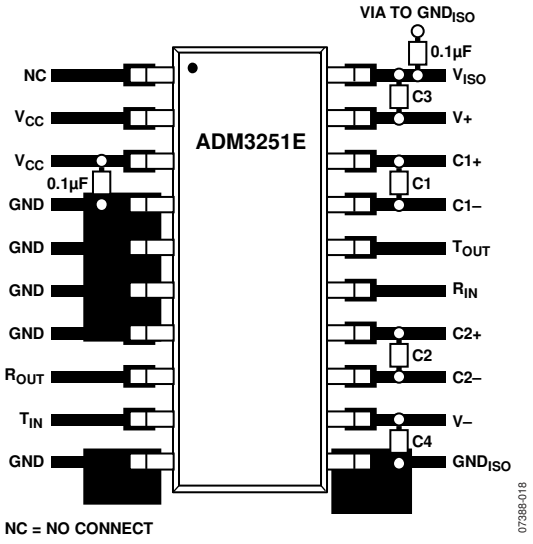


*Figure 21. Recommended Printed Circuit Board Layout*

In applications involving high common-mode transients, care should be taken to ensure that board coupling across the isolation barrier is minimized. Furthermore, the board layout should be designed such that any coupling that does occur equally affects all pins on a given component side.

The power supply section of the ADM3251E uses a 300 MHz oscillator frequency to pass power through its chip-scale transformers. Operation at these high frequencies may raise concerns about radiated emissions and conducted noise. PCB layout and construction is a very important tool for controlling radiated emissions. Refer to Application Note AN-0971, *Control of Radiated Emissions with isoPower Devices*, for extensive guidance on radiation mechanisms and board layout considerations.

## EXAMPLE PCB FOR REDUCED EMI

The choice of how aggressively EMI must be addressed for a design to pass emissions levels depends on the requirements of the design as well as cost and performance trade-offs.

The starting point for this example is a 2-layer PCB. EMI reductions are relative to the emissions and noise from this board. To conform to FCC Class B levels, the emissions at these two frequencies must be less than 46 dBµV/m, normalized to 3 m antenna distance. As expected, EMI testing confirmed that the largest emissions peaks occur at the tank frequency and rectifier frequency.

A 6-layer PCB that employs edge guarding and buried capacitive bypassing, which are EMI mitigation techniques described in detail in Application Note AN-0971, was manufactured. The stackup of the 6-layer test PCB is shown in Table 9. PCB layout Gerber files are available upon request.

**Table 9. PCB Layers**

| Layer | Description |
|---|---|
| Top | Components and ground planes |
| Inner Layer 1 | $V_{CC}$ planes |
| Inner Layer 2 | All tracks |
| Inner Layer 3 | Blank |
| Inner Layer 4 | Buried capacitive plane |
| Bottom | Ground planes |

EMI testing was repeated on the optimized board. The resulting reduction in radiated emissions is shown in Table 10. This board meets FCC Class B standards with no external shielding by utilizing buried stitching capacitors and edge fencing.

**Table 10. EMI Test Results**

| EMI Test Results | 300 MHz | 600 MHz |
|---|---|---|
| 2-Layer PCB Emissions | 48 dB | 53 dB |
| 6-Layer PCB Emissions | 36 dB | 32 dB |
| Achieved EMI Reduction | 12 dB | 21 dB |

## DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions.

In the absence of logic transitions at the input for more than 1 µs, periodic sets of refresh pulses (indicative of the correct input state) are sent to ensure dc correctness at the output. If the decoder receives no internal pulses for more than approximately 5 µs, the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default state by the watchdog timer circuit. This situation should occur in the ADM3251E during power-up and power-down operations only.

The limitation on the ADM3251E magnetic field immunity is set by the condition in which induced voltage in the receiving coil of the transformer is sufficiently large to falsely set or reset the decoder. The following analysis defines the conditions under which this can occur.

The pulses at the transformer output have an amplitude of >1.0 V. The decoder has a sensing threshold of about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\Sigma\pi r_n^2; \text{ n} = 1, 2, \ldots, N$$

where:
$\beta$ is the magnetic flux density (gauss).
$N$ is the number of turns in the receiving coil.
$r_n$ is the radius of the n$^{th}$ turn in the receiving coil (cm).

Given the geometry of the receiving coil internally and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 22.

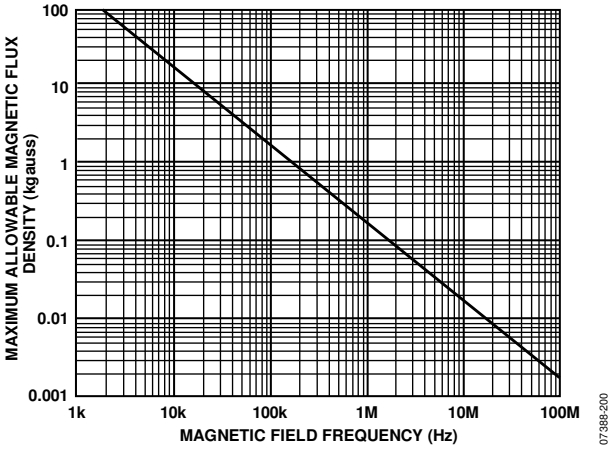


*Figure 22. Maximum Allowable External Magnetic Flux Density*

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is approximately 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and is of the worst-case polarity), the received pulse is reduced from >1.0 V to 0.75 V, which is still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the transformers. Figure 23 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown in Figure 23, the ADM3251E is extremely immune and can be affected only by extremely large currents operated at high frequency very close to the component. For example, at a magnetic field frequency of 1 MHz, a 0.5 kA current placed 5 mm away from the ADM3251E is required to affect the operation of the component.

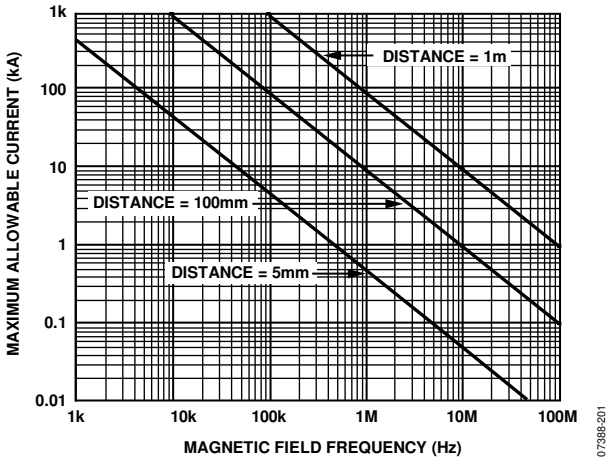


*Figure 23. Maximum Allowable Current for Various Current-to-ADM3251E Spacings*

In the presence of strong magnetic fields and high frequencies, any loops formed by PCB traces may induce error voltages sufficiently large to trigger the thresholds of succeeding circuitry. Exercise care in the layout of such traces to avoid this possibility.

## ISOLATED POWER SUPPLY CIRCUIT

To operate the ADM3251E with its internal dc-to-dc converter disabled, connect a voltage of between 3.0 V and 3.7 V to the $V_{CC}$ pin and apply an isolated power of between 3.0 V and 5.5 V to the $V_{ISO}$ pin, referenced to $GND_{ISO}$.

A transformer driver circuit with a center-tapped transformer and LDO can be used to generate the isolated supply, as shown in Figure 24. The center-tapped transformer provides electrical isolation of the 5 V power supply. The primary winding of the transformer is excited with a pair of square waveforms that are 180° out of phase with each other. A pair of Schottky diodes and a smoothing capacitor are used to create a rectified signal from the secondary winding. The ADP3330 linear voltage regulator provides a regulated power supply to the bus side circuitry ($V_{ISO}$) of the ADM3251E.

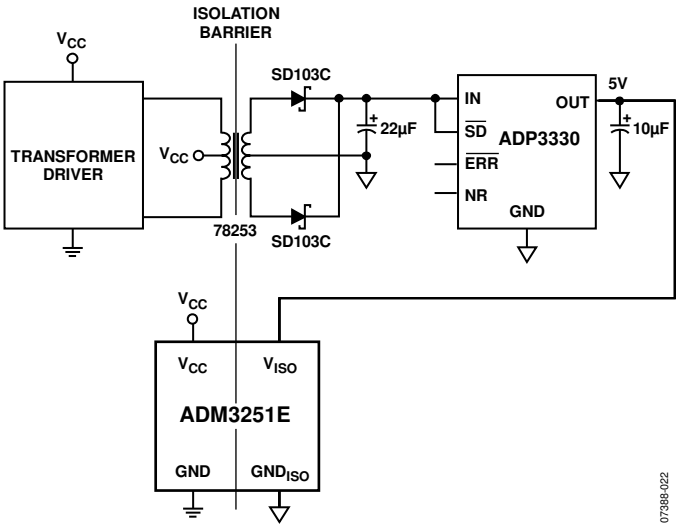


*Figure 24. Isolated Power Supply Circuit*

# OUTLINE DIMENSIONS

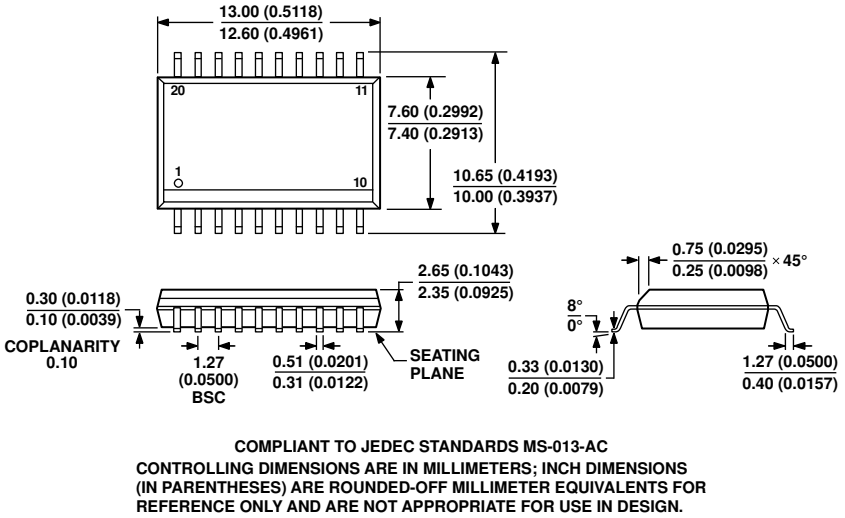


*Figure 25. 20-Lead Standard Small Outline Package [SOIC_W]*
*Wide Body (RW-20)*
*Dimensions shown in millimeters and (inches)*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| ADM3251EARWZ | −40°C to +85°C | 20-Lead Standard Small Outline Package [SOIC_W] | RW-20 |
| ADM3251EARWZ-REEL | −40°C to +85°C | 20-Lead Standard Small Outline Package [SOIC_W] | RW-20 |
| EVAL-ADM3251EEB1Z | | Evaluation Board | |

[1] Z = RoHS Compliant Part.

## NOTES


D07388-0-10/13(G)