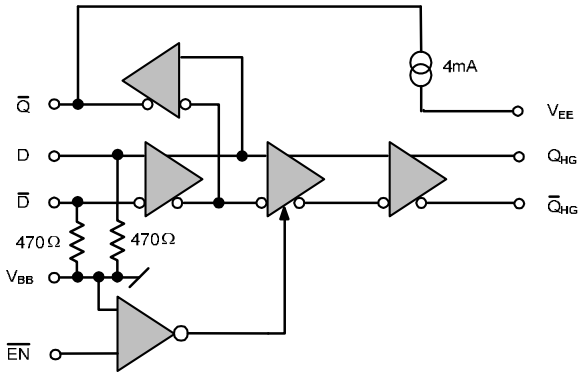
PECL/ECL Oscillator Gain Stage & Buffer with Selectable Enable

MLP8

FEATURES

- Minimizes External Components
- High Bandwidth for ≥1GHz
- Similar Operation as CTSLVEL16VR
  - Except in Disabled Condition Q_{HG} is High
- -147 dBc/Hz Typical Noise Floor

BLOCK DIAGRAM



DESCRIPTION

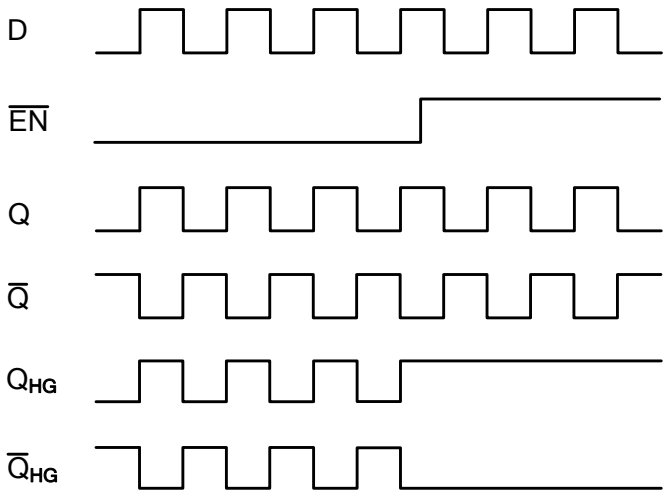
The CTSLVEL16VT is a specialized oscillator gain stage with a high gain output buffer including an enable function. The $Q_{HG}/\overline{Q}_{HG}$ outputs have voltage gain several times greater than the $\overline{Q}$ output. It provides a $Q_{HG}/\overline{Q}_{HG}$ enable that allows continuous oscillator operation via the $\overline{Q}$ outputs.

The CTSLVEL16VT also provides a 4mA internal pull-down current source for $\overline{Q}$ outputs. Internal input biasing further reduces the number of needed external components.

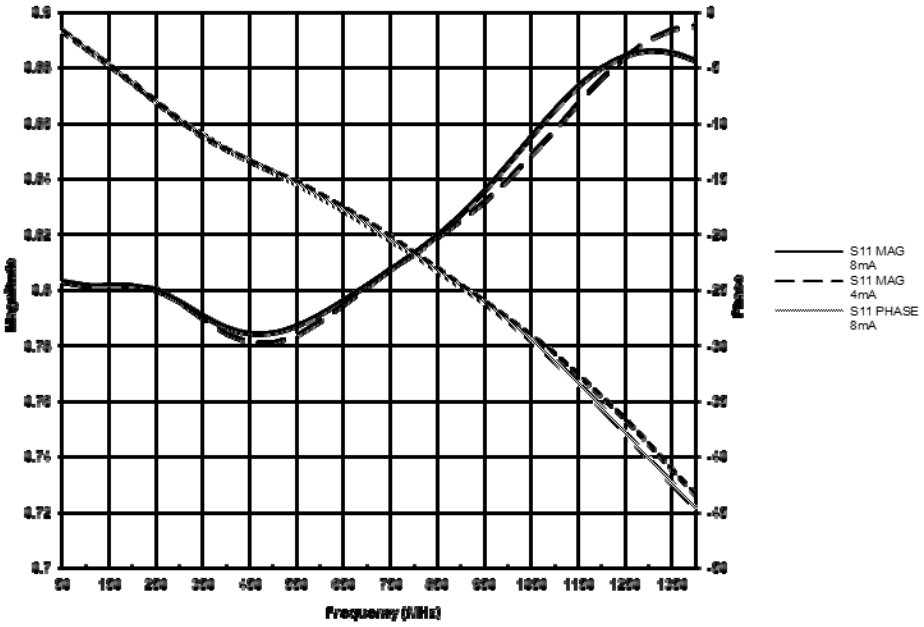
ENGINEERING NOTES

The CTSLVEL16VT is a specialized oscillator gain stage with a high gain output buffer including an enable. The $Q_{HG}/\overline{Q}_{HG}$ outputs have a voltage gain several times greater than the $\overline{Q}$ output. When the $\overline{EN}$ input is LOW, the $\overline{Q}$ and $Q_{HG}/\overline{Q}_{HG}$ outputs follow the data inputs. When $\overline{EN}$ is HIGH, the Q_{HG} output is forced high and the $\overline{Q}_{HG}$ output is forced low.

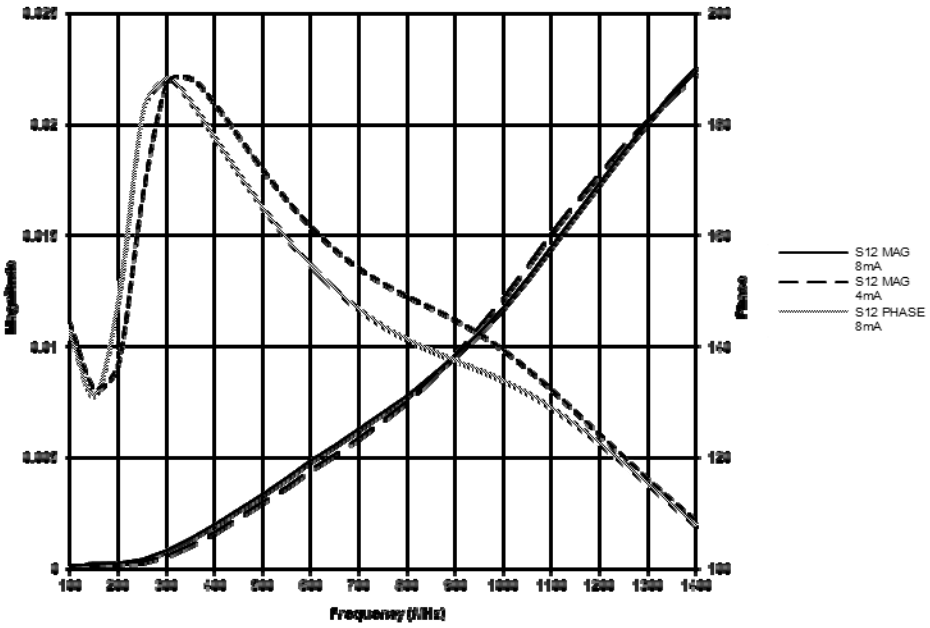
In the CTSLVEL16VT, the $\overline{D}$ input is internally tied directly to the V_{BB} pin and the D input is tied to the V_{BB} pin through a 470Ω internal bias resistor. Bypassing V_{BB} to ground with a 0.01 µF capacitor is recommended.



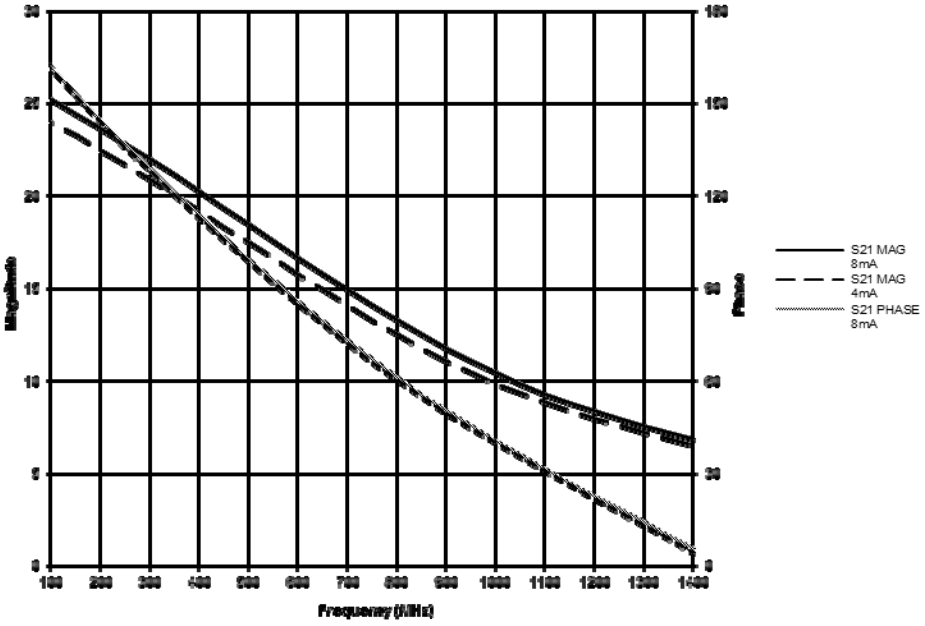
Timing Diagram


S11 MAG
8mA
S11 MAG
4mA
S11 PHASE
8mA
Frequency (MHz)

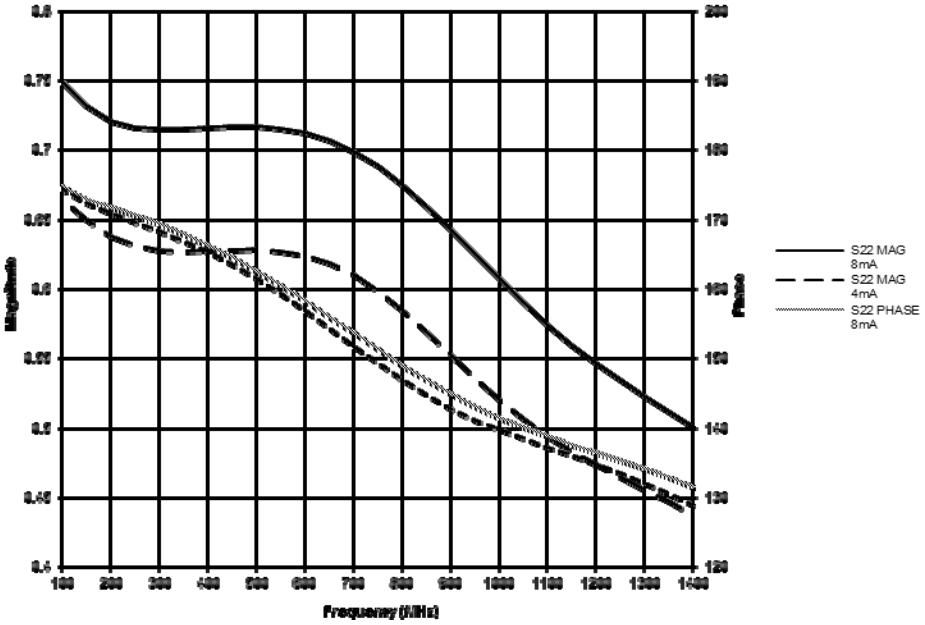
S11


S12 MAG
8mA
S12 MAG
4mA
S12 PHASE
8mA
Frequency (MHz)

S12


S21 MAG
8mA
S21 MAG
4mA
S21 PHASE
8mA
Frequency (MHz)

S21


S22 MAG
8mA
S22 MAG
4mA
S22 PHASE
8mA
Frequency (MHz)

S22

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Condition	Rating	Unit
V_{CC}	PECL Power Supply	V_{EE} = 0V	0 to + 6.0	V
V_{D_PECL}	PECL D Input Voltage	Referenced to V_{BB}	±0.75	V
V_{EN_PECL}	PECL D Input Voltage	V_{EE} = 0V	0 to + 6.0	V
V_{EE}	ECL Power Supply	V_{CC} = 0V	-6.0 to 0	V
V_{D_ECL}	ECL D Input Voltage	Referenced to V_{BB}	±0.75	V
V_{EN_ECL}	ECL D Input Voltage	V_{CC} = 0V	-6.0 to 0	V
I_{OUT}	Output Current	Continuous Q	25	mA
		Surge Q	50	
		Continuous Q_{HG}	50	
		Surge Q_{HG}	100	
T_A	Operating Temperature Range	-	-40 to +85	°C
T_{STG}	Storage Temperature Range	-	-65 to +150	°C
ESD_{HBM}	Human Body Model Electro Static Discharge	-	2500	V
ESD_{MM}	Machine Model Electro Static Discharge	-	200	V
ESD_{CDM}	Charged Device Model Electro Static Discharge	-	2000	V

ECL DC Characteristics (V_{EE} = -3.0V to -5.5V, V_{CC} = GND)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1]	-1045	-835	-1025	-835	-1025	-835	-1025	-835	mV
V_{OL}	Output LOW Voltage[1]	-1925	-1555	-1900	-1620	-1900	-1620	-1900	-1620	mV
V_{IH}	Input HIGH Voltage D,EN	-1165	-740	-1165	-740	-1165	-740	-1165	-740	mV
V_{IL}	Input LOW Voltage D,EN	-1900	-1475	-1900	-1475	-1900	-1475	-1900	-1475	mV
V_{BB}	Reference Voltage	-1390	-1250	-1390	-1250	-1390	-1250	-1390	-1250	mV
I_{IH}	Input HIGH Current EN		150		150		150		150	µA
I_{IL}	Input LOW Current EN	0.5		0.5		0.5		0.5		µA
I_{EE}	Power Supply Current[1]		48		48		48		54	mA

1 Specified with each output terminated through 50Ω resistors to V_{CC} -2V.

LVPECL DC Characteristics (V_{EE} = GND, V_{CC} = +3.3V)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1,2]	2255	2465	2275	2465	2275	2465	2275	2465	mV
V_{OL}	Output LOW Voltage[1,2]	1375	1745	1400	1680	1400	1680	1400	1680	mV
V_{IH}	Input HIGH Voltage D,EN	2135	2560	2135	2560	2135	2560	2135	2560	mV
V_{IL}	Input LOW Voltage D,EN	1400	1825	1400	1825	1400	1825	1400	1825	mV
V_{BB}	Reference Voltage[1]	1910	2050	1910	2050	1910	2050	1910	2050	mV
I_{IH}	Input HIGH Current EN		150		150		150		150	µA
I_{IL}	Input LOW Current EN	0.5		0.5		0.5		0.5		µA
I_{EE}	Power Supply Current[2]		48		48		48		54	mA

1 For supply voltages other than 3.3V, use the ECL table values and ADD supply voltage value.

2 Specified with each output terminated through 50 Ω resistors to V_{CC} -2V.

PECL DC Characteristics (V_{EE} = GND, V_{CC} = +5.0V)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1,2]	3955	4165	3975	4165	3975	4165	3975	4165	mV
V_{OL}	Output LOW Voltage[1,2]	3075	3445	3100	3380	3100	3380	3100	3380	mV
V_{IH}	Input HIGH Voltage D,EN	3835	4260	3835	4260	3835	4260	3835	4260	mV
V_{IL}	Input LOW Voltage D,EN	3100	3525	3100	3525	3100	3525	3100	3525	mV
V_{BB}	Reference Voltage[1]	3610	3750	3610	3750	3610	3750	3610	3750	mV
I_{IH}	Input HIGH Current EN		150		150		150		150	µA
I_{IL}	Input LOW Current EN	0.5		0.5		0.5		0.5		µA
I_{EE}	Power Supply Current[2]		48		48		48		54	mA

1 For supply voltages other than 3.3V, use the ECL table values and ADD supply voltage value.

2 Specified with each output terminated through 50Ω resistors to V_{CC} -2V.

AC Characteristics (V_{EE} = -3.0V to -5.5V; V_{CC}=GND or V_{EE}=GND; V_{CC} = +3.0V to +5.5V)

Symbol	Characteristic	40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH}/t_{PHL}	Propagation Del y													
	D toQ[1]			350			350			350			350	ps
	D to Q_{HG}[2]			450			450			450			450	ps
t_{SKEW}	Duty Cycle Skew[3]		5	20		5	20		5	20		5	20	ps
Vpp (AC)	Input Swing[4] Differential	80		1000	80		1000	80		1000	80		1000	mV
	Input Swing[4] Single Ended	160		1500	160		1500	160		1500	160		1500	
t_r/t_f	Output Rise/Fall[1,2] (20% - 80%)	100		240	100		240	100		240	100		240	ps

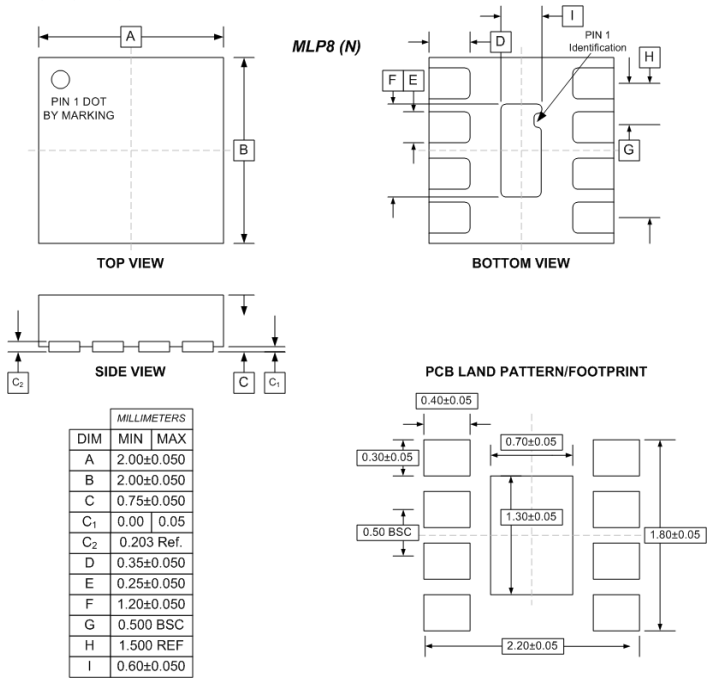
1 Specified with each output terminated through 50Ω resistors to V_{CC} -2V.

2 Specified with each output terminated through 50Ω resistors to V_{CC} -2V.

3 Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.

4 The peak-to-peak input swing is the range for which AC parameters are guaranteed. D and $\overline{D}$ must remain within the range of ± 750 mV with respect to V_{BB}. The device has a voltage gain of ~20 to the $\overline{Q}$ outputs and a voltage gain of ~100 to the $Q_{HG}/\overline{Q}_{HG}$ outputs.

PACKAGE DIMENSIONS

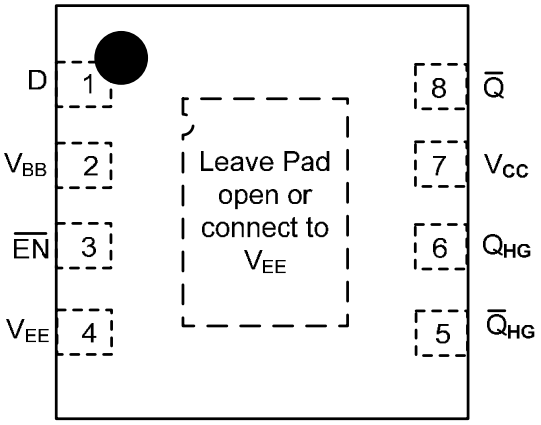


DIM	MILLIMETERS MIN	MAX
A	2.00±0.050	
B	2.00±0.050	
C	0.75±0.050	
C_1	0.00	0.05
C_2	0.203 Ref.	
D	0.35±0.050	
E	0.25±0.050	
F	1.20±0.050	
G	0.500 BSC	
H	1.500 REF	
I	0.60±0.050	

Pin Description and Configuration

Pin Assignments for CTSLVEL16VTNNG

Pin	Name	Type	Function
1	D	Input	Data Input
2	V_{BB}	Output	Reference Voltage
3	EN	Input	Output Enable
4	V_{EE}	Power	Negative Supply
5	$\overline{Q}_{HG}$	Output	High Gain Inverting PECL Output
6	Q_{HG}	Output	High Gain PECL Output
7	V_{CC}	Power	Positive Supply
8	$\overline{Q}$	Output	Inverting PECL Output
9	NC	-	N/A



CTSLVEL16VTNNG

PART ORDERING NUMBER

Part Number	Package	Marking
CTSLVEL16VTNNG	MLP8	P8G YYWW