NUF9002FC

Low Capacitance 10 Line EMI Filter with ESD Protection

This device is a ten−line EMI filter array for wireless applications. Greater than −25 dB attenuation is obtained at frequencies from 900 MHz to 3.0 GHz. ESD protection is provided across all capacitors.

Features

- EMI Filtering and ESD Protection
- Integration of 50 Discretes
- Provides Protection for IEC61000−4−2 (Level 4)
  - 8.0 kV (Contact)
- Flip−Chip Package
- Moisture Sensitivity Level 1
- ESD Rating: Machine Model = C; Human Body Model = 3B
- Pb−Free Package is Available*

Benefits

- Reduces EMI/RFI Emissions on a Data Line
- Integrated Solution Offers Cost and Space Savings
- Reduces Parasitic Inductances Which Offer a More “Ideal” Low Pass Filter Response
- Integrated Solution Improves System Reliability

Applications

- LCD for Cell Phones and PDAs
- Computers and Printers
- Communication Systems
- MP3 Players

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating		Symbol	Value	Unit
ESD Discharge IEC61000−4−2	Contact Discharge	V_{PP}	8.0	kV
Steady−State Power per Resistor		P_R	100	mW
Steady−State Power per Package		P_T	200	mW
Operating Temperature Range		T_{OP}	−40 to +85	°C
Storage Temperature Range		T_{STG}	−55 to +150	°C
Junction Temperature		T_J	+125	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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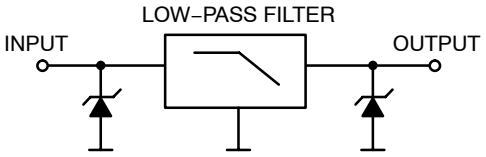
http://onsemi.com



$R_{I/O}$ = 100 Ω
C_{input} = 28 pF

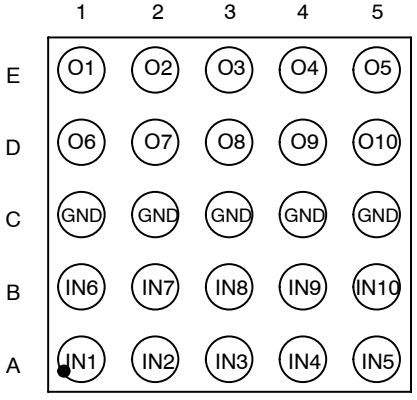
MARKING DIAGRAM

Flip−Chip
CASE 499G

NUF9002 = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONFIGURATION
(Ball Side)



ORDERING INFORMATION

Device	Package	Shipping†
NUF9002FCT1	Flip−Chip	3000 Tape & Reel
NUF9002FCT1G	Flip−Chip (Pb−Free)	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Reverse Working Voltage	V_{RWM}	–	–	–	5.0	V
Breakdown Voltage	V_{BR}	I_R = 1.0 mA	6.0	7.0	8.0	V
Leakage Current	I_R	V_{RM} = 3.0 V	–	–	0.1	μA
Series Resistance	R_A	–	85	100	115	Ω
Capacitance	$C_{LINE\ 1}$	f = 1.0 MHz, 0 Vdc	–	28	35	pF
Cut−Off Frequency	f_{3dB}	(Above this frequency, appreciable attenuation occurs)	–	110	–	MHz

TYPICAL PERFORMANCE CURVE

(T_A = 25°C unless otherwise specified)

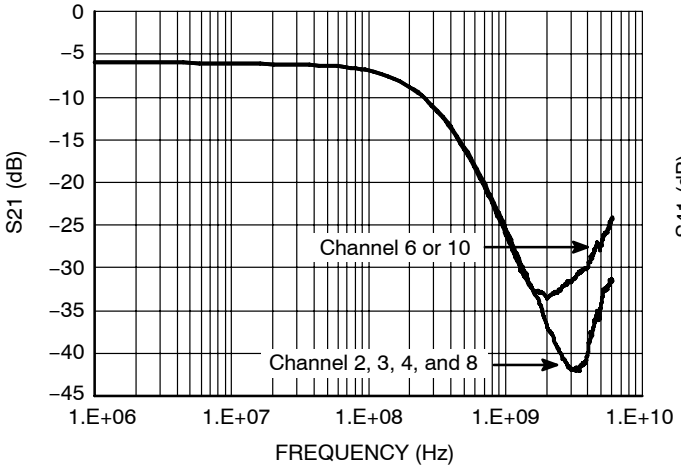


Figure 1. Insertion Loss Characteristics (S21 Measurement)

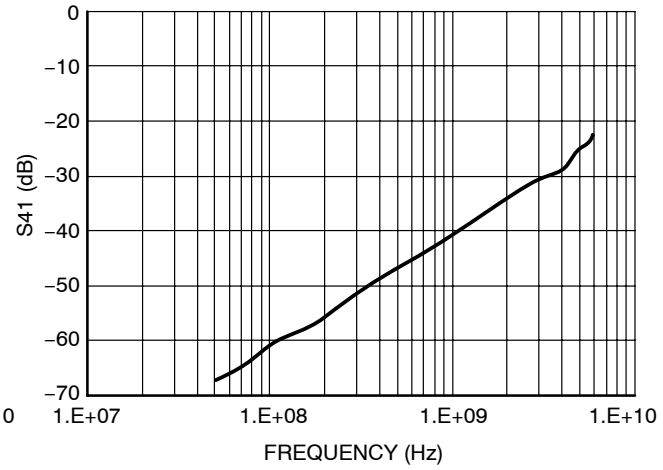


Figure 2. Analog Crosstalk Curve (S41 Measurement)

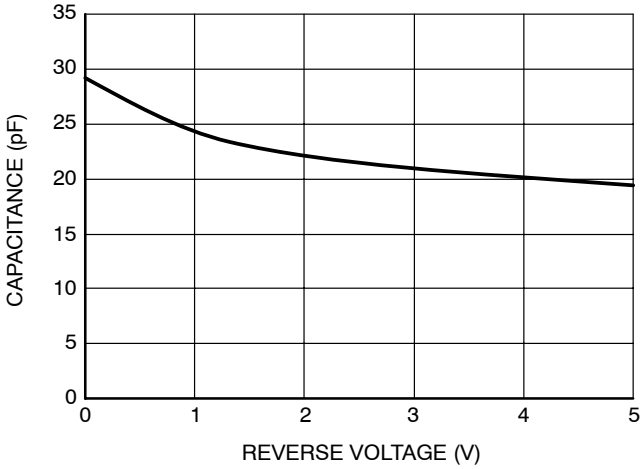


Figure 3. Typical Line Capacitance vs. Reverse Bias Voltage

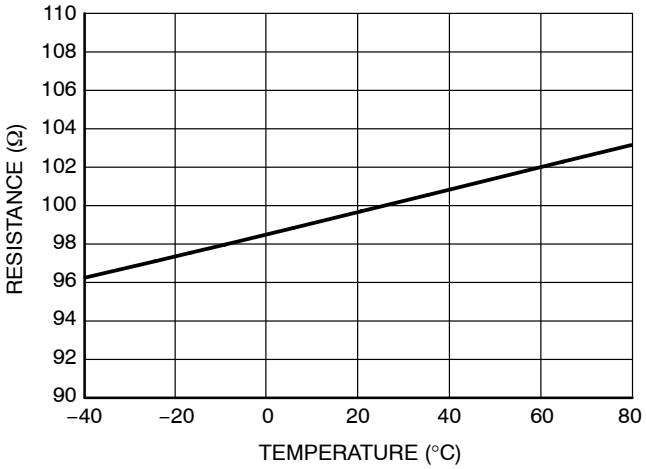


Figure 4. Typical Resistance Over Temperature

PRINTED CIRCUIT BOARD RECOMMENDATIONS

Parameter	500 μm Pitch 300 or 350 μm Solder Ball
PCB Pad Size	250 μm +25 −0
Pad Shape	Round
Pad Type	NSMD
Solder Mask Opening	350 μm ±25
Solder Stencil Thickness	125 μm
Stencil Aperture	250 x 250 μm sq.
Solder Flux Ratio	50/50
Solder Paste Type	No Clean Type 3 or Finer
Trace Finish	OSP Cu
Trace Width	150 μm Max

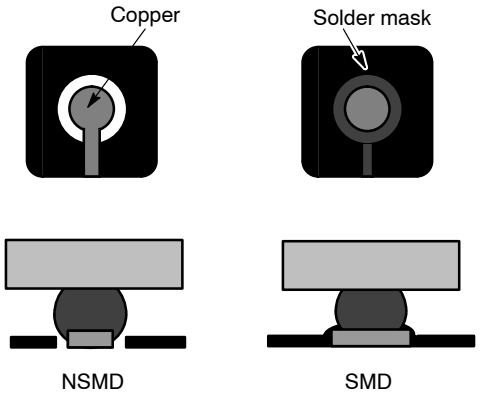
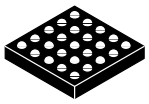


Figure 5. NSMD vs. SMD

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®



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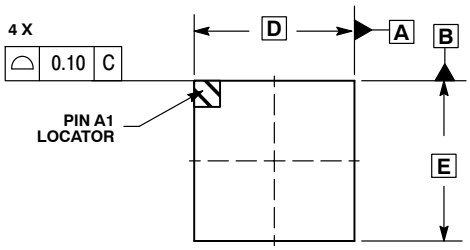
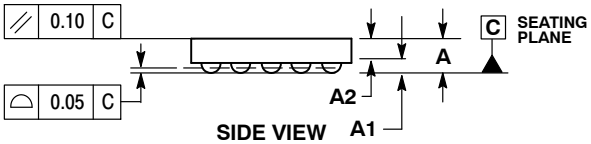
SCALE 4:1

FLIP−CHIP−25 CSP
CASE 499G−01
ISSUE B

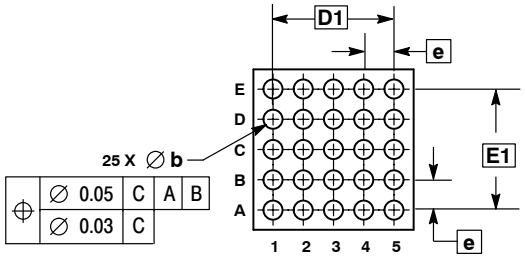
DATE 03 MAY 2005



TOP VIEW



SIDE VIEW



BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	0.700
A1	0.210	0.270
A2	0.380	0.430
D	2.650 BSC	
E	2.650 BSC	
b	0.290	0.340
e	0.500 BSC	
D1	2.000 BSC	
E1	2.000 BSC	

GENERIC MARKING DIAGRAM*

xxxxxx = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	**98AON13902D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**FLIP−CHIP−25 CSP, 0.265 *0.265 MM, 0.500 PITCH**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

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