



# FDPC1012S

## PowerTrench® Power Clip

### 25V Asymmetric Dual N-Channel MOSFET

#### Features

- Q1: N-Channel
  - Max  $r_{DS(on)}$  = 7.0 m $\Omega$  at  $V_{GS}$  = 4.5 V,  $I_D$  = 12 A
- Q2: N-Channel
  - Max  $r_{DS(on)}$  = 2.2 m $\Omega$  at  $V_{GS}$  = 4.5 V,  $I_D$  = 23 A
  - Low inductance packaging shortens rise/fall times, resulting in lower switching losses
  - MOSFET integration enables optimum layout for lower circuit inductance and reduced switch node ringing
  - RoHS Compliant

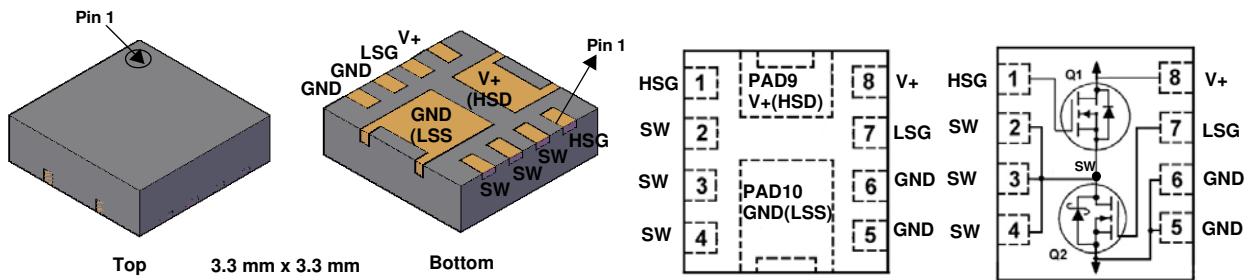


#### General Description

This device includes two specialized N-Channel MOSFETs in a dual package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFET™ (Q2) have been designed to provide optimal power efficiency.

#### Applications

- Computing
- Communications
- General Purpose Point of Load



#### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
$V_{DS}$	Drain to Source Voltage	25	25	V
$V_{GS}$	Gate to Source Voltage	12	12	V
$I_D$	Drain Current -Continuous	$T_C = 25^\circ\text{C}$ 35	88	A
	-Continuous	$T_A = 25^\circ\text{C}$ 13 <sup>1a</sup>	26 <sup>1b</sup>	
	-Pulsed	(Note 4) 40	120	
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3) 50	181	mJ
$P_D$	Power Dissipation for Single Operation	$T_A = 25^\circ\text{C}$ 1.6 <sup>1a</sup>	2.0 <sup>1b</sup>	W
	Power Dissipation for Single Operation	$T_A = 25^\circ\text{C}$ 0.8 <sup>1c</sup>	0.9 <sup>1d</sup>	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150		$^\circ\text{C}$

#### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	77 <sup>1a</sup>	63 <sup>1b</sup>	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	151 <sup>1c</sup>	135 <sup>1d</sup>	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	5.0	3.5	

#### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
01OD/03OD	FDPC1012S	Power Clip 33	13"	12 mm	3000 units

**Electrical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
--------	-----------	-----------------	------	-----	-----	-----	-------

**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$ $I_D = 1\text{ mA}$ , $V_{GS} = 0\text{ V}$	Q1 Q2	25 25			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$ $I_D = 10\text{ mA}$ , referenced to $25\text{ }^\circ\text{C}$	Q1 Q2		18 22		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 20\text{ V}$ , $V_{GS} = 0\text{ V}$ $V_{DS} = 20\text{ V}$ , $V_{GS} = 0\text{ V}$	Q1 Q2			1 500	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current, Forward	$V_{GS} = 12\text{ V/-8 V}$ , $V_{DS} = 0\text{ V}$ $V_{GS} = 12\text{ V/-8 V}$ , $V_{DS} = 0\text{ V}$	Q1 Q2			$\pm 100$ $\pm 100$	nA nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$ $V_{GS} = V_{DS}$ , $I_D = 1\text{ mA}$	Q1 Q2	0.8 1.1	1.3 1.6	2.2 2.2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$ $I_D = 10\text{ mA}$ , referenced to $25\text{ }^\circ\text{C}$	Q1 Q2		-4 -4		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 4.5\text{ V}$ , $I_D = 12\text{ A}$ $V_{GS} = 4.5\text{ V}$ , $I_D = 12\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$ $V_{GS} = 4.5\text{ V}$ , $I_D = 23\text{ A}$ $V_{GS} = 4.5\text{ V}$ , $I_D = 23\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$	Q1 Q2		5.2 7.5 1.6 2.3	7.0 10.5 2.2 3.2	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}$ , $I_D = 13\text{ A}$ $V_{DS} = 5\text{ V}$ , $I_D = 26\text{ A}$	Q1 Q2		79 200		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	Q1: $V_{DS} = 13\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$	Q1 Q2		1075 3456		pF
$C_{oss}$	Output Capacitance	Q2: $V_{DS} = 13\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$	Q1 Q2		250 885		pF
$C_{rss}$	Reverse Transfer Capacitance	$V_{DS} = 13\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$	Q1 Q2		50 130		pF
$R_g$	Gate Resistance		Q1 Q2	0.1 0.1	0.4 0.5	2.0 2.0	$\Omega$

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time		Q1 Q2		6 12		ns
$t_r$	Rise Time	Q1: $V_{DD} = 13\text{ V}$ , $I_D = 13\text{ A}$ , $R_{GEN} = 6\text{ }\Omega$	Q1 Q2		2 3		ns
$t_{d(off)}$	Turn-Off Delay Time	Q2: $V_{DD} = 13\text{ V}$ , $I_D = 26\text{ A}$ , $R_{GEN} = 6\text{ }\Omega$	Q1 Q2		19 34		ns
$t_f$	Fall Time		Q1 Q2		2 3		ns
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{ V to } 4.5\text{ V}$	Q1 Q2		8 25		nC
$Q_{gs}$	Gate to Source Gate Charge	Q1 $V_{DD} = 13\text{ V}$ , $I_D = 13\text{ A}$ Q2	Q1 Q2		2.3 7.8		nC
$Q_{gd}$	Gate to Drain "Miller" Charge	Q1 $V_{DD} = 13\text{ V}$ , $I_D = 26\text{ A}$ Q2	Q1 Q2		2.0 6.4		nC

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

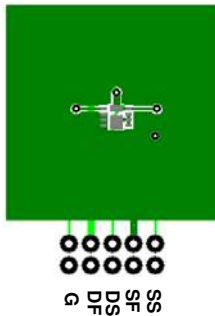
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
--------	-----------	-----------------	------	-----	-----	-----	-------

### Drain-Source Diode Characteristics

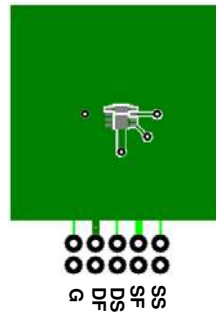
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 13\text{ A}$ (Note 2)	Q1		0.8	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 26\text{ A}$ (Note 2)	Q2		0.8	1.2	
$t_{rr}$	Reverse Recovery Time	Q1 $I_F = 13\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	Q1		20	35	ns
			Q2		27	43	
$Q_{rr}$	Reverse Recovery Charge	Q2 $I_F = 26\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$	Q1		6	12	nC
			Q2		27	43	

Notes:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a. 77 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 63 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



c. 151 °C/W when mounted on a minimum pad of 2 oz copper



d. 135 °C/W when mounted on a minimum pad of 2 oz copper

2 Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

3. Q1 :  $E_{AS}$  of 50 mJ is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ; N-ch:  $L = 3\text{ mH}, I_{AS} = 5.8\text{ A}, V_{DD} = 25\text{ V}, V_{GS} = 10\text{ V}$ . 100% test at  $L = 0.1\text{ mH}, I_{AS} = 14.5\text{ A}$ .

Q2:  $E_{AS}$  of 181 mJ is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ; N-ch:  $L = 3\text{ mH}, I_{AS} = 11\text{ A}, V_{DD} = 25\text{ V}, V_{GS} = 10\text{ V}$ . 100% test at  $L = 0.1\text{ mH}, I_{AS} = 32.9\text{ A}$ .

4. Pulsed Id limited by junction temperature,  $t_d \leq 10\mu\text{s}$ . Please refer to SOA curve for more details.

**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted

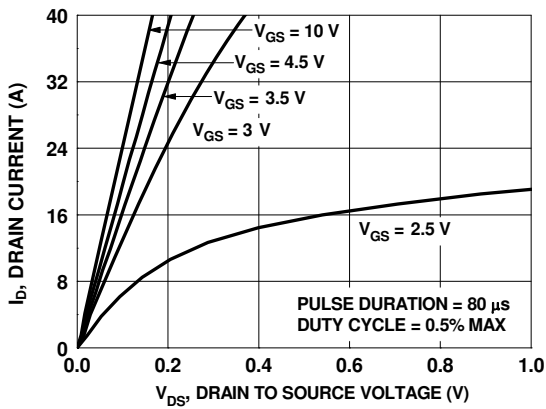


Figure 1. On Region Characteristics

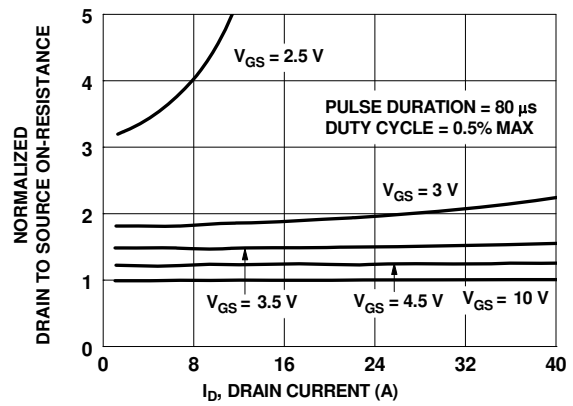


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

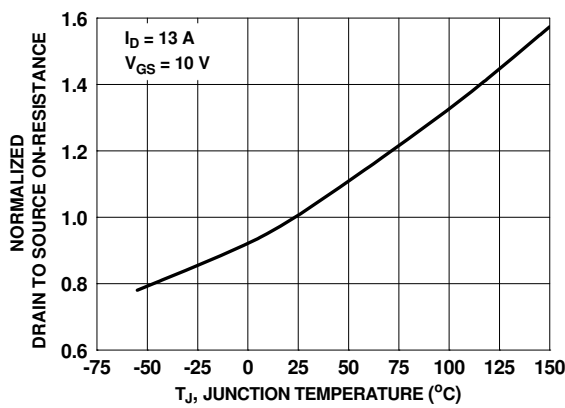


Figure 3. Normalized On Resistance vs Junction Temperature

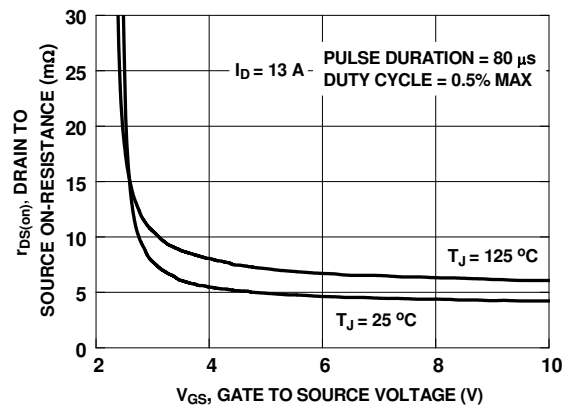


Figure 4. On-Resistance vs Gate to Source Voltage

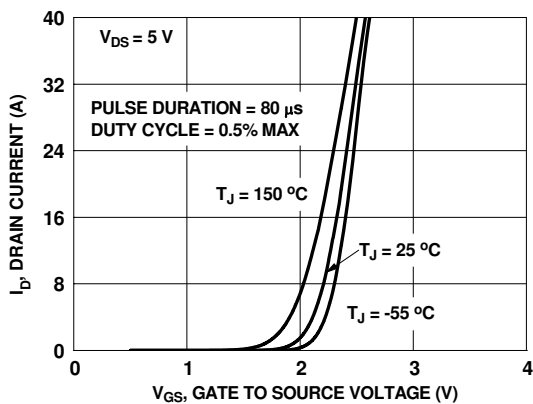


Figure 5. Transfer Characteristics

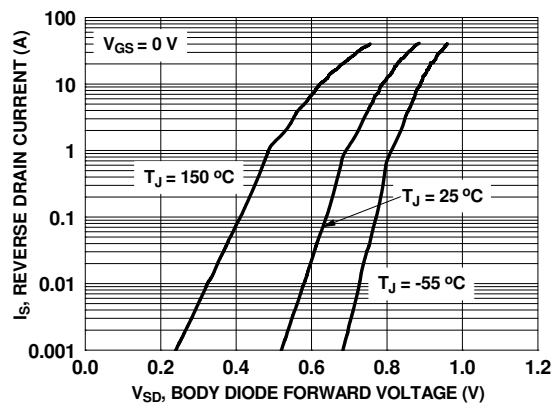
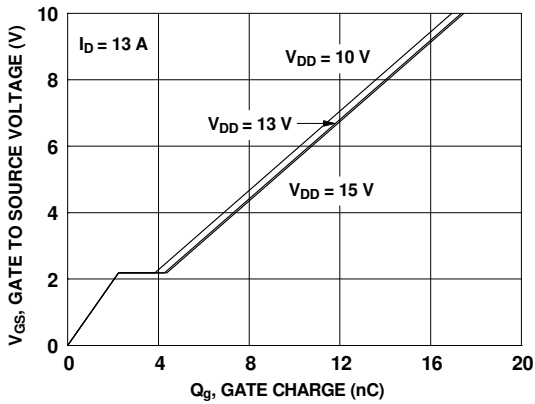
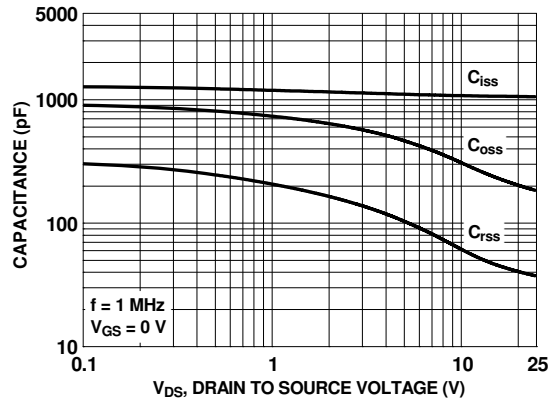


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

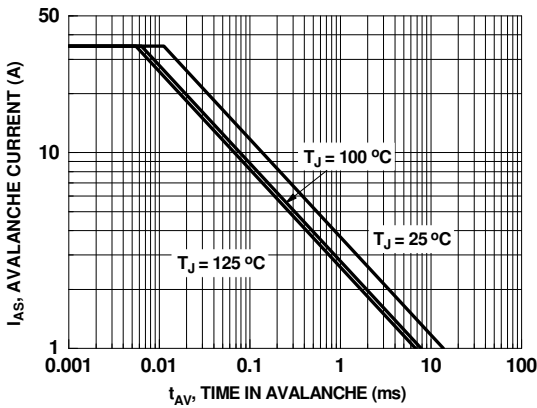
**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted



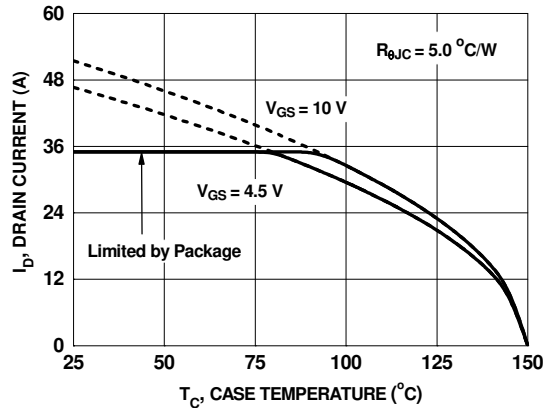
**Figure 7. Gate Charge Characteristics**



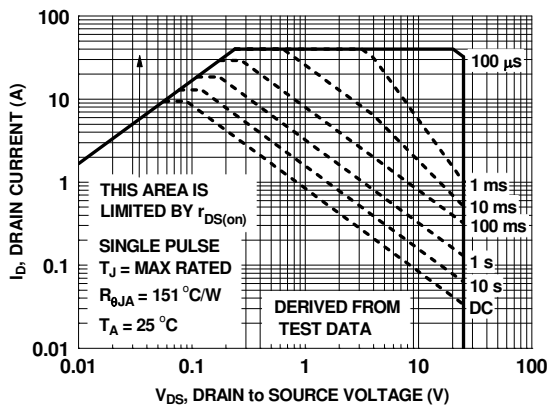
**Figure 8. Capacitance vs Drain to Source Voltage**



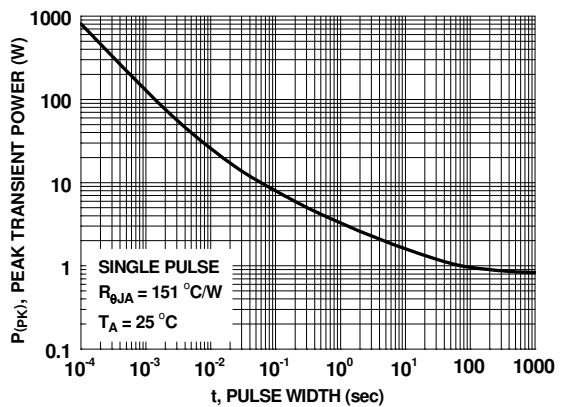
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

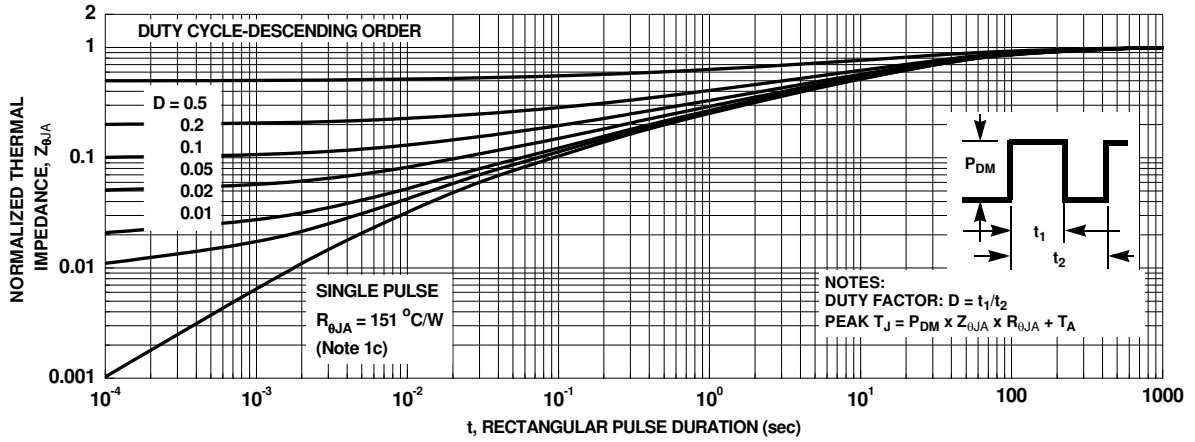


**Figure 11. Forward Bias Safe Operating Area**



**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted



**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**

**Typical Characteristics (Q2 N-Channel)**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

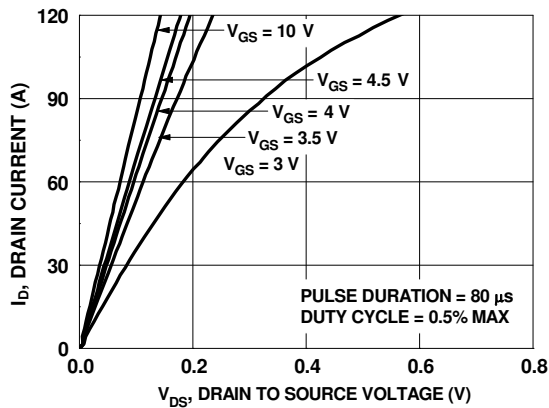


Figure 14. On-Region Characteristics

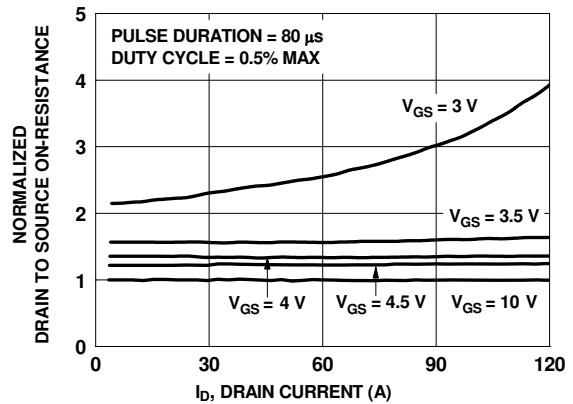


Figure 15. Normalized on-Resistance vs Drain Current and Gate Voltage

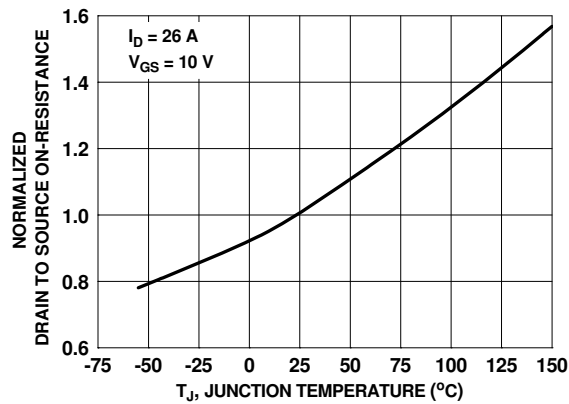


Figure 16. Normalized On-Resistance vs Junction Temperature

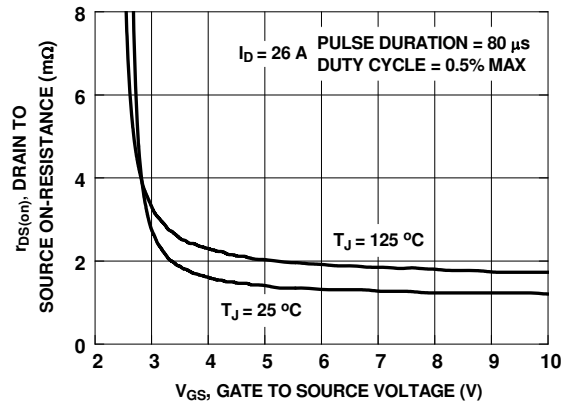


Figure 17. On-Resistance vs Gate to Source Voltage

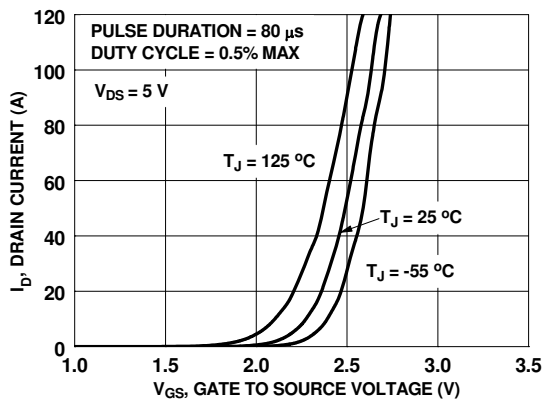


Figure 18. Transfer Characteristics

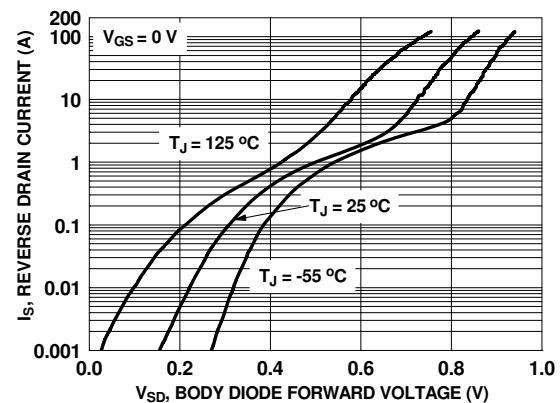
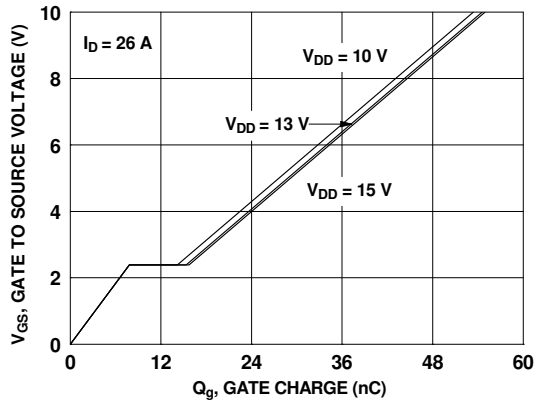
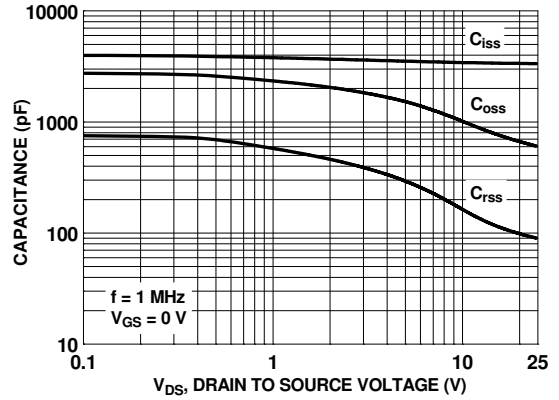


Figure 19. Source to Drain Diode Forward Voltage vs Source Current

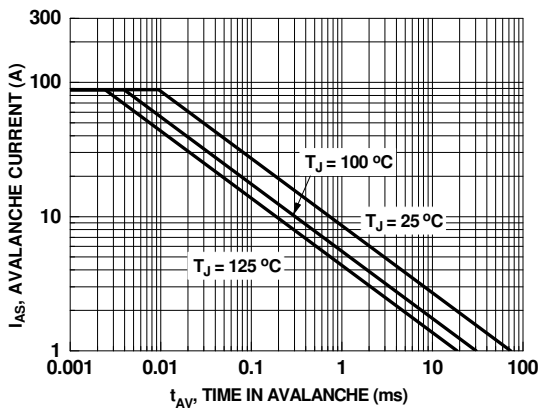
**Typical Characteristics (Q2 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted



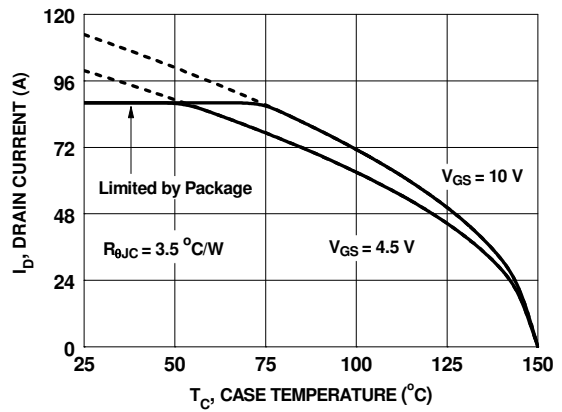
**Figure 20. Gate Charge Characteristics**



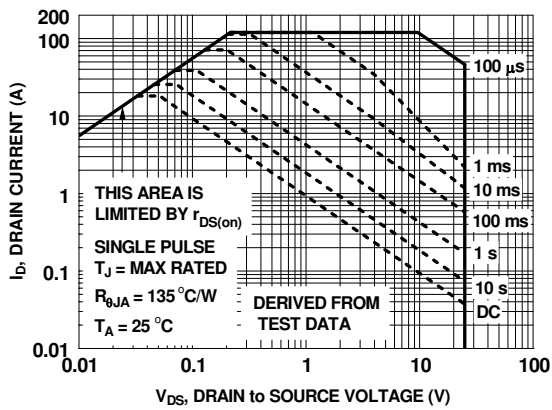
**Figure 21. Capacitance vs Drain to Source Voltage**



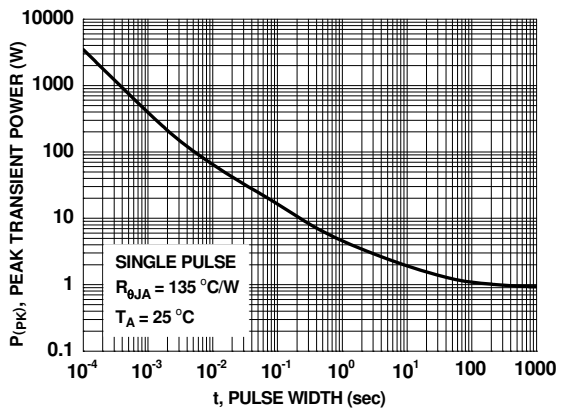
**Figure 22. Unclamped Inductive Switching Capability**



**Figure 23. Maximum Continuous Drain Current vs Case Temperature**



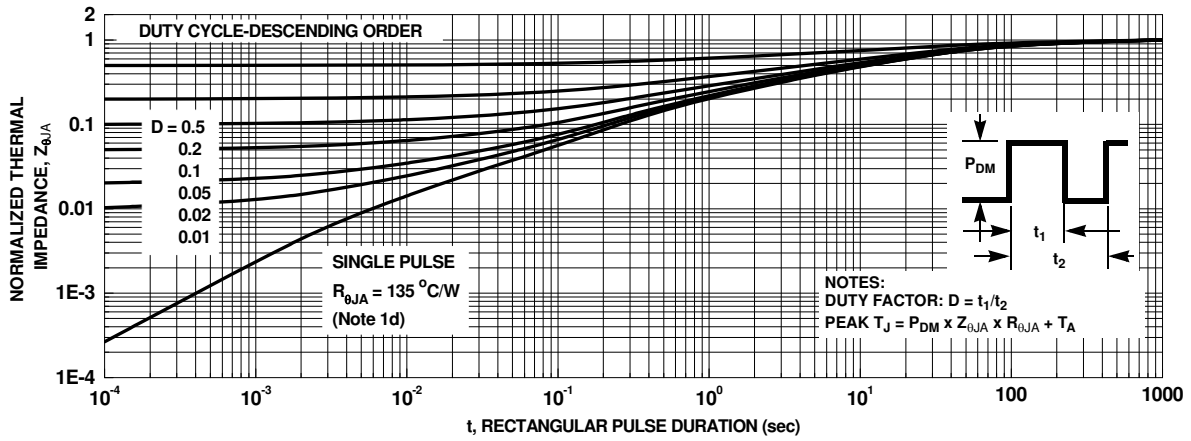
**Figure 24. Forward Bias Safe Operating Area**



**Figure 25. Single Pulse Maximum Power Dissipation**



**Typical Characteristics (Q2 N-Channel)**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 26. Junction-to-Ambient Transient Thermal Response Curve**

## Typical Characteristics (continued)

### SyncFET™ Schottky body diode Characteristics

Fairchild's SyncFET™ process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDPC1012S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

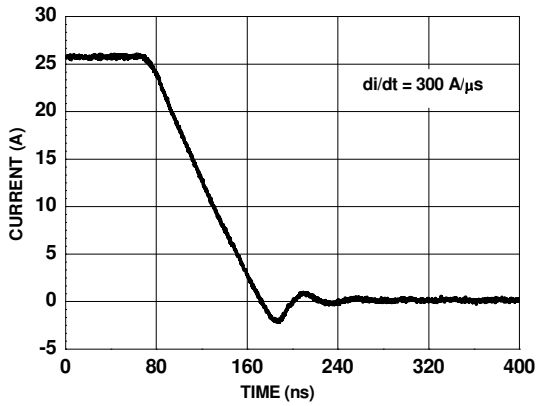


Figure 27. FDPC1012S SyncFET™ body diode reverse recovery characteristic

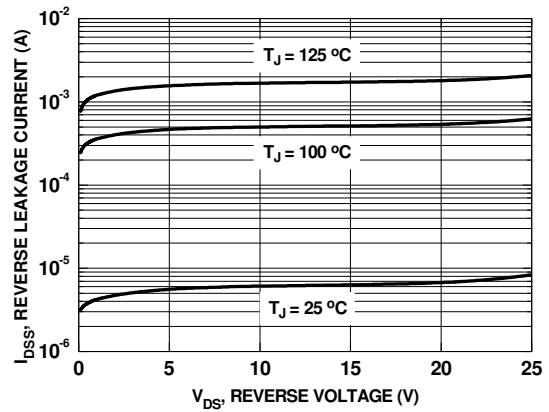
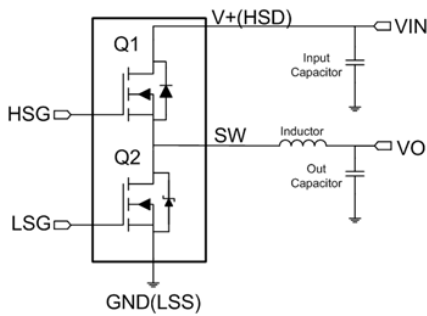


Figure 28. SyncFET™ body diode reverse leakage versus drain-source voltage

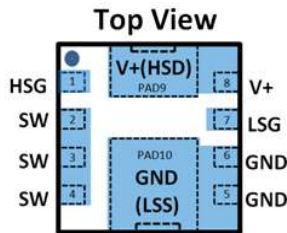
## Application Information

### Typical Application Diagram (Synchronous Rectifier Buck Converter)



**Figure 1. Power Clip in Buck Converter Topology**

As shown in Figure 1, in the Power Clip package Q1 is the High Side MOSFET (Control MOSFET) and Q2 is the Low Side MOSFET (Synchronous MOSFET). Figure 2 below shows the package pin out. The blue overlay on the drawing indicates a typical PCB land pattern for the part.



**Figure 2. Top View of Power Clip**

Table 1 Pin Information shows the name and description of each pin.

PIN		Description
Number	Name	
1	HSG	Gate signal input of Q1 Gate
2,3,4	SW	Switch or Phase node, Source of Q1 and Drain of Q2
5,6,PAD 10	GND,GND(LSS) PAD	Ground, Source of Q2
7	LSG	Gate signal input of Q2 Gate
8,PAD 9	V+, V+(HSD) PAD	Input voltage of SR Buck converter, Drain of Q1

**Table 1. Pin Information**

## Recommended PCB Layout Guidelines

As a PCB designer, it is necessary to address critical issues in layout to minimize losses and optimize the performance of the power train. Power Clip is a high power density solution and all high current flow paths, such as V+(HSD), SW and GND(LSS) should be short and wide for minimal resistance and inductance. V+(HSD) and GND(LSS) are the primary heat flow paths for the Power Clip. A recommended layout procedure is discussed below to maximize the electrical and thermal performance of the part.

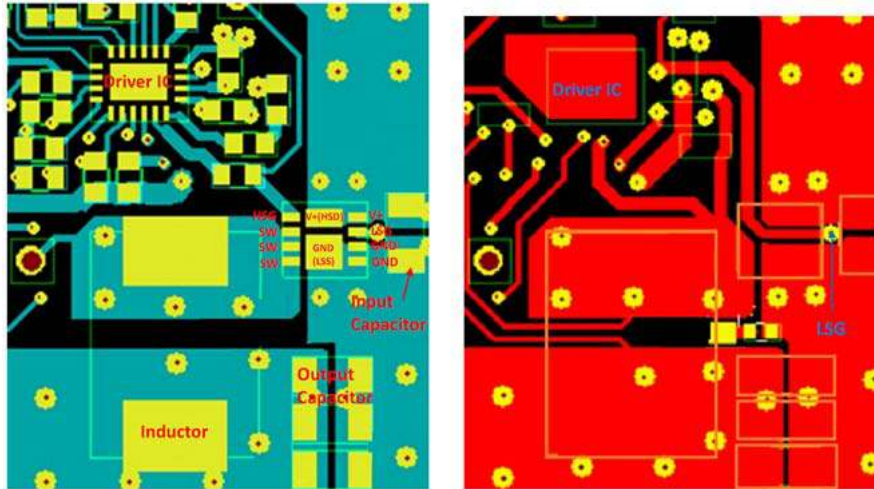


Figure 3. Top/Component (green) View and Bottom (red) PCB View

Following is a guideline, not a requirement which the PCB designer should consider.

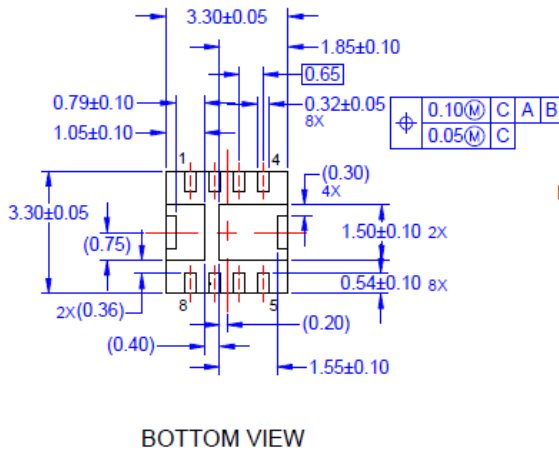
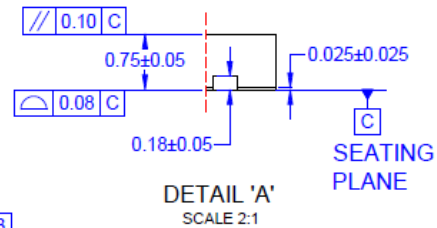
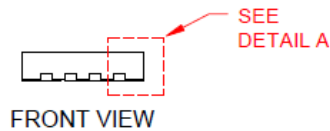
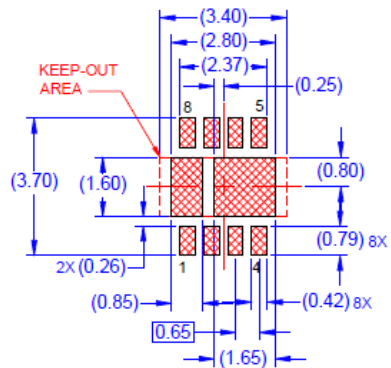
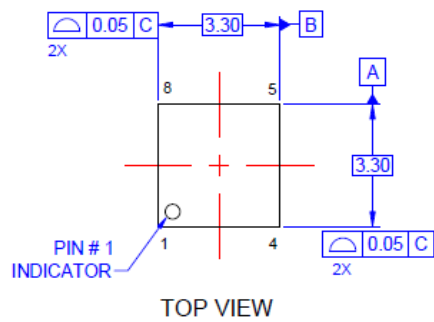
Figure 3 shows an example of a well designed layout. The discussion that follows summarizes the key features of this layout.

- "The input ceramic bypass capacitor between VIN and GND should be placed as close as possible to the pins V+ / V+(HSD) PAD and GND / GND(LSS) PAD to help reduce parasitic inductance and high frequency ringing. Several capacitors may be placed in parallel, and capacitors may be placed on both the top and bottom side of the board. The capacitor located immediately adjacent to the Power Clip will be the most effective at reducing HF parasitic. Caps located farther away, or on the opposite side of the board will also assist, but will be less effective due to increased trace inductance.
- "The Power Clip package design, with very short distance between pins V+ and GND, allows for a short connect distance to the input cap. This is a factor that enables the Power Clip switch loop to have very low parasitic inductance.
- "Use large copper areas on the component side to connect the V+ pin and V+ (HSD) pad, and the GND and GND(LSS) PAD.
- "The SW to inductor copper trace is a high current path. It will also be a high noise region due to switching voltage transients. The trace should be short and wide to enable a low resistance path and to minimize the size of the noise region. Care should be taken to minimize coupling of this trace to adjacent traces. The layout in Figure 3 shows a good example of this short, wide path.
- "The Power Trench® Technology MOSFETs used in the Power Clip are effective at minimizing SW node ringing. They incorporate a proprietary design<sup>1</sup> that minimizes the peak overshoot ring voltage on the switch node (SW). They allow the part to operate well within the breakdown voltage limits. For most layouts, this eliminates the need to add an external snubber circuit. If the designer chooses to use an RC snubber, it should be placed close to the part between the SW pins and GND / GND (LSS) PAD to dampen the high frequency ringing.
- "The Driver IC should be placed relatively closed to HSG pin and LSG pin to minimize G drive trace inductance. Excessive G trace length may slow the switching speed of the HS drive. And it may lead to excessive ringing on the LS G. If the designer must place the driver a significant distance away from the Power Clip, it would be a good practice to include a 0 Ohm resistor in the LS G path as a place holder. In the final design, if the LS G exhibits excessive LF ringing, efficiency can often be improved by changing this resistor to a few Ohms to dampen the LS G LF ringing.
- "The Power Clip has very good Junction-PCB heat transfer from all power pins. It has much better heat transfer Junction-GND (LSS) than traditional dual FET packages. In most cases, board ground will be the most effective heat transfer path on the PCB. Use a large copper area between GND / GND(LSS) PAD pins and board ground. To ensure the best thermal and electrical connection to ground, we recommend using multiple vias to interconnect ground plane layers as shown in Figure 3.

1. Patent Pending

- "Use multiple vias in parallel on each copper region to interconnect top, inner and bottom layers. This will reduce resistance and inductance of the vias and will improve thermal conductivity. Vias should be relatively large, around 8 mils to 10 mils.
- "Avoid using narrow thermal relief traces on the V+ / V+(HSD) PAD and GND / GND(LSS)PAD pins. These will increase HF switch loop inductance. And these will increase ringing of the HF power loop and the SW node.

## Dimensional Outline and Pad Layout



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE IS REFERENCED FROM JEDEC MO-240, VARIATION BA.
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
  - D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
  - E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
  - F) DRAWING FILE NAME: MKT-PQFN08GREV4








Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:  
[https://www.fairchildsemi.com/evaluate/package-specifications/packageDetails.html?id=PN\\_PQDEU-X08](https://www.fairchildsemi.com/evaluate/package-specifications/packageDetails.html?id=PN_PQDEU-X08).



TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

- AccuPower™
- Awinda®
- AX-CAP®\*
- BitSiC™
- Build it Now™
- CorePLUS™
- CorePOWER™
- CROSSVOLT™
- CTL™
- Current Transfer Logic™
- DEUXPEED®
- Dual Cool™
- EcoSPARK®
- EfficientMax™
- ESBC™
-  Fairchild®
- Fairchild Semiconductor®
- FACT Quiet Series™
- FACT®
- FAST®
- FastvCore™
- FETBench™
- FPS™
- F-PFST™
- FRFET®
- Global Power ResourceSM
- GreenBridge™
- Green FPS™
- Green FPS™ e-Series™
- Gmax™
- GTO™
- IntelliMAX™
- ISOPLANAR™
- Marking Small Speakers Sound Louder and Better™
- MegaBuck™
- MICROCOUPLER™
- MicroFET™
- MicroPak™
- MicroPak2™
- MillerDrive™
- MotionMax™
- MotionGrid®
- MTi®
- MTx®
- MVN®
- mWSaver®
- OptoHiT™
- OPTOLOGIC®
- OPTOPLANAR®
-  PowerTrench®
- PowerXS™
- Programmable Active Droop™
- QFET®
- QS™
- Quiet Series™
- RapidConfig™
-  Saving our world, 1mW/W/kW at a time™
- SignalWise™
- SmartMax™
- SMART START™
- Solutions for Your Success™
- SPM®
- STEALTH™
- SuperFET®
- SuperSOT™-3
- SuperSOT™-6
- SuperSOT™-8
- SupreMOS®
- SyncFET™
- Sync-Lock™
-  SYSTEM®
- TinyBoost®
- TinyBuck®
- TinyCalc™
- TinyLogic®
- TINYOPTO™
- TinyPower™
- TinyPWM™
- TinyWire™
- TranSiC™
- TriFault Detect™
- TRUECURRENT®\*
- µSerDes™
-  SerDes™
- UHC®
- Ultra FRFET™
- UniFET™
- VCX™
- VisualMax™
- VoltagePlus™
- XS™
- Xsens™
- 仙童™

\*Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. TO OBTAIN THE LATEST, MOST UP-TO-DATE DATASHEET AND PRODUCT INFORMATION, VISIT OUR WEBSITE AT [HTTP://WWW.FAIRCHILDSEMI.COM](http://www.fairchildsemi.com). FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used here in:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, [www.fairchildsemi.com](http://www.fairchildsemi.com), under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufactures of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed application, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address and warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms






Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I72



## TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

AccuPower™	F-PFS™	OPTOPLANAR®	
AttitudeEngine™	FRFET®		TinyBoost®
Awinda®	Global Power Resource <sup>SM</sup>	PowerTrench®	TinyBuck®
AX-CAP®*	GreenBridge™	PowerXS™	TinyCalc™
BitSiC™	Green FPS™	Programmable Active Droop™	TinyLogic®
Build it Now™	Green FPS™ e-Series™	QFET®	TINYOPTO™
CorePLUS™	Gmax™	QS™	TinyPower™
CorePOWER™	GTO™	Quiet Series™	TinyPWM™
CROSSVOLT™	IntelliMAX™	RapidConfigure™	TinyWire™
CTL™	ISOPLANAR™		TranSiC™
Current Transfer Logic™	Making Small Speakers Sound Louder and Better™	Saving our world, 1mW/W/kW at a time™	TriFault Detect™
DEUXPEED®	MegaBuck™	SignalWise™	TRUECURRENT®*
Dual Cool™	MICROCOUPLER™	SmartMax™	SerDes™
EcoSPARK®	MicroFET™	SMART START™	
EfficientMax™	MicroPak™	Solutions for Your Success™	UHC®
ESBC™	MicroPak2™	SPM®	Ultra FRFET™
	MillerDrive™	STEALTH™	UniFET™
Fairchild®	MotionMax™	SuperFET®	VCX™
Fairchild Semiconductor®	MotionGrid®	SuperSOT™-3	VisualMax™
FACT Quiet Series™	MTI®	SuperSOT™-6	VoltagePlus™
FACT®	MTX®	SuperSOT™-8	XS™
FAST®	MVN®	SupreMOS®	Xsens™
FastvCore™	mWSaver®	SyncFET™	仙童™
FETBench™	OptoHiT™	Sync-Lock™	
FPS™	OPTOLOGIC®		

\* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

## DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. TO OBTAIN THE LATEST, MOST UP-TO-DATE DATASHEET AND PRODUCT INFORMATION, VISIT OUR WEBSITE AT [HTTP://WWW.FAIRCHILDSEMI.COM](http://www.fairchildsemi.com). FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

## LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, [www.fairchildsemi.com](http://www.fairchildsemi.com), under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I73