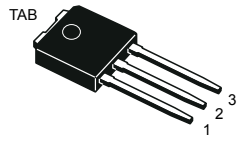
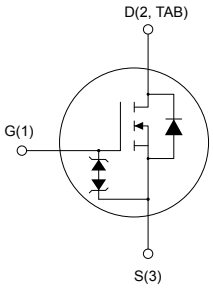
STU3N65M6

Datasheet

N-channel 650 V, 1.4 Ω typ., 3.5 A MDmesh M6 Power MOSFET in an IPAK package



IPAK



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Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STU3N65M6	650 V	1.5 Ω	3.5 A

- Reduced switching losses
- Lower $R_{DS(on)}$ per area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

The new MDmesh M6 technology incorporates the most recent advancements to the well-known and consolidated MDmesh family of SJ MOSFETs. STMicroelectronics builds on the previous generation of MDmesh devices through its new M6 technology, which combines excellent $R_{DS(on)}$ per area improvement with one of the most effective switching behaviors available, as well as a user-friendly experience for maximum end-application efficiency.

Product status link
STU3N65M6

Product summary	
Order code	STU3N65M6
Marking	3N65M6
Package	IPAK
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	3.5	A
I_D	Drain current (continuous) at T_C = 100 °C	2.2	A
I_{DM} (1)	Drain current (pulsed)	14	A
P_{TOT}	Total power dissipation at T_C = 25 °C	45	W
dv/dt(2)	Peak diode recovery voltage slope	5	V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	100	
T_J	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		

1. *Pulse width limited by safe operating area*
2. *I_{SD} ≤ 3.5 A, di/dt=400 A/µs; $V_{DS}(peak) < V_{(BR)DSS}$, V_{DD} = 400 V*
3. *V_{DS} ≤ 520 V*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	2.78	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	100	

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	1	A
E_{as}	Single pulse avalanche energy (starting T_j=25°C, I_D= I_{AR}, V_{DD}=50 V)	78	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 4. On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS}= 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_C = 125 °C (1)			100	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±5	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.25	3	3.75	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 1.75 A		1.4	1.5	Ω

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	150	-	pF
C_{oss}	Output capacitance		-	13	-	
C_{rss}	Reverse transfer capacitance		-	0.7	-	
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 520 V, V_{GS} = 0 V	-	31	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D=0 A	-	5.2	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 3.5 A, V_{GS}= 0 to 10 V, (see Figure 14. Test circuit for gate charge behavior)	-	6	-	nC
Q_{gs}	Gate-source charge		-	1	-	
Q_{gd}	Gate-drain charge		-	3.2	-	

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 325 V, I_D = 1.75 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	5.2	-	ns
t_r	Rise time		-	5.4	-	
$t_{d(off)}$	Turn-off delay time		-	14.1	-	
t_f	Fall time		-	17.1	-	

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		3.5	A
I_{SDM} (1)	Source-drain current (pulsed)		-		14	A
V_{SD} (2)	Forward on voltage	I_{SD} = 3.5 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 3.5 A, di/dt = 100 A/µs, V_{DD} = 60 V, (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	159		ns
Q_{rr}	Reverse recovery charge		-	0.7		µC
I_{RRM}	Reverse recovery current		-	8.9		A
t_{rr}	Reverse recovery time	I_{SD} = 3.5 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	190		ns
Q_{rr}	Reverse recovery charge		-	0.8		µC
I_{RRM}	Reverse recovery current		-	8.5		A

1. *Pulse width limited by safe operating area*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

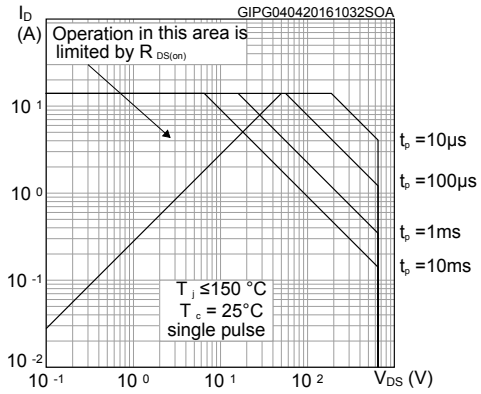


Figure 2. Thermal impedance

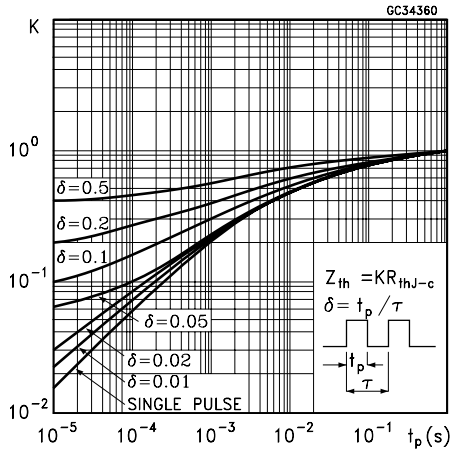


Figure 3. Output characteristics

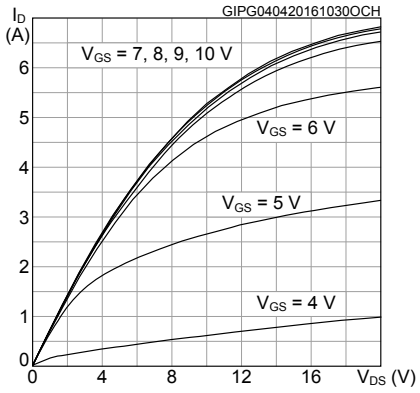


Figure 4. Transfer characteristics

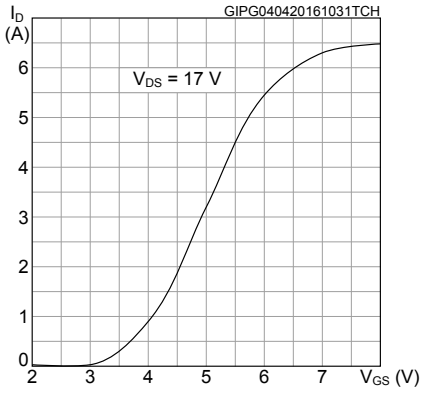


Figure 5. Gate charge vs gate-source voltage

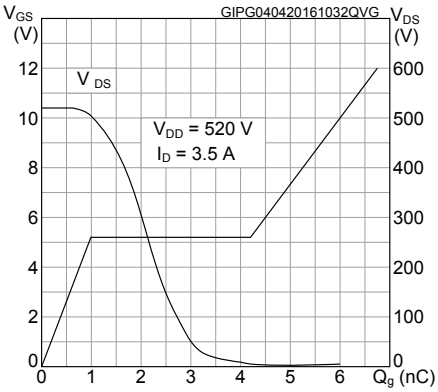


Figure 6. Static drain-source on-resistance

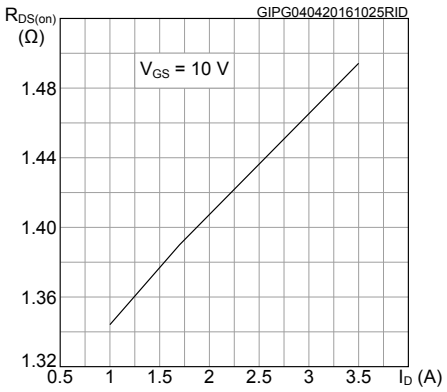


Figure 7. Capacitance variations

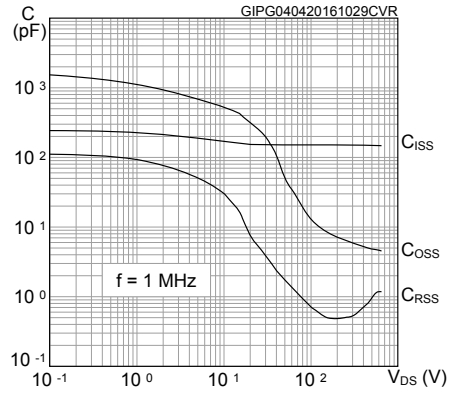


Figure 8. Normalized gate threshold voltage vs temperature

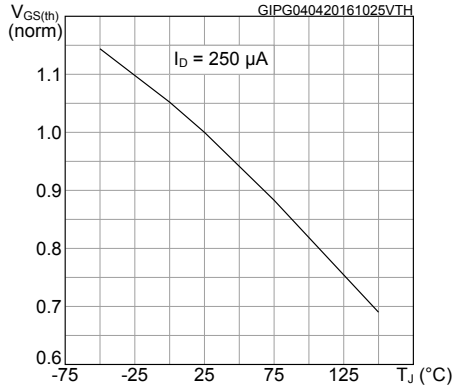


Figure 9. Normalized on-resistance vs temperature

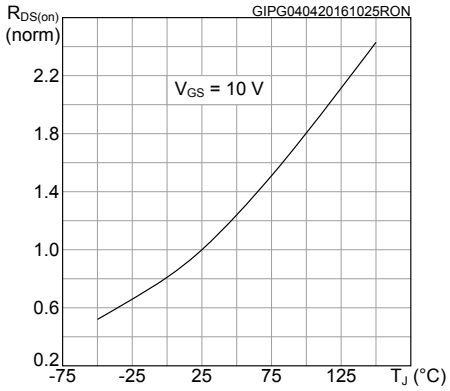


Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

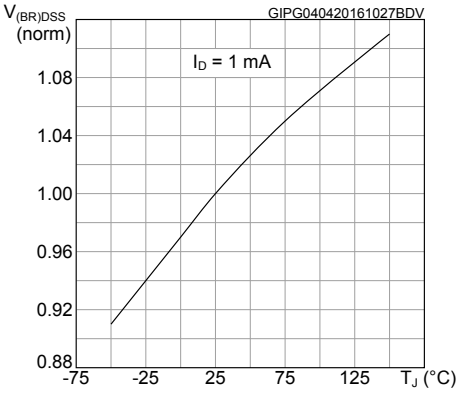


Figure 11. Output capacitance stored energy

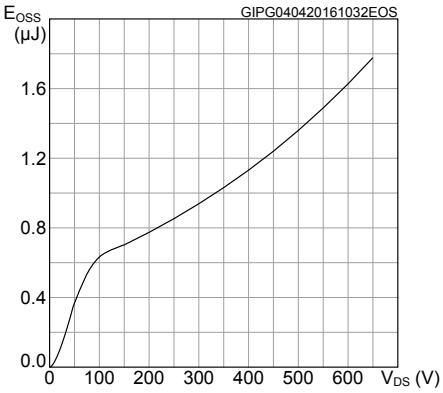
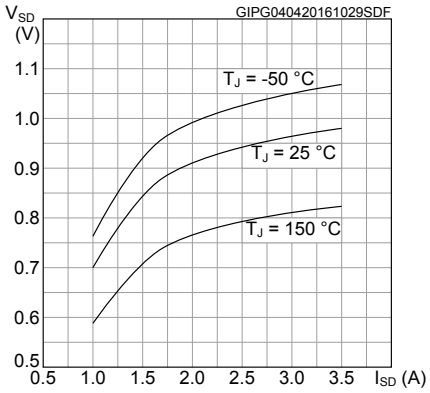


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Test circuit for resistive load switching times

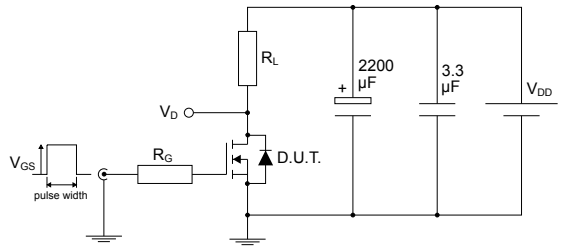


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Figure 14. Test circuit for gate charge behavior

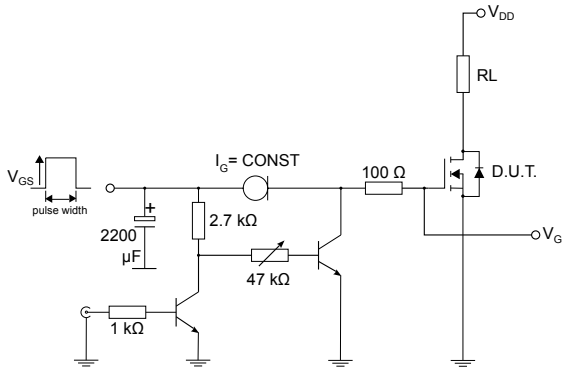

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Figure 15. Test circuit for inductive load switching and diode recovery times

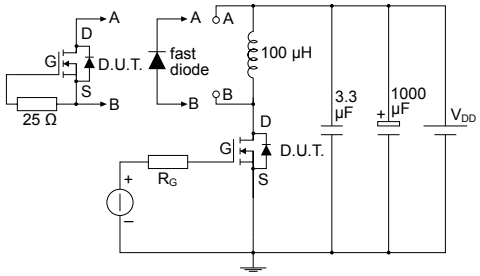

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Figure 16. Unclamped inductive load test circuit

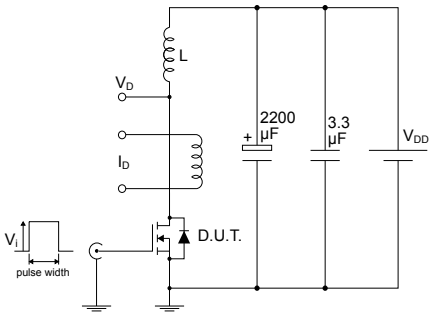

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Figure 17. Unclamped inductive waveform

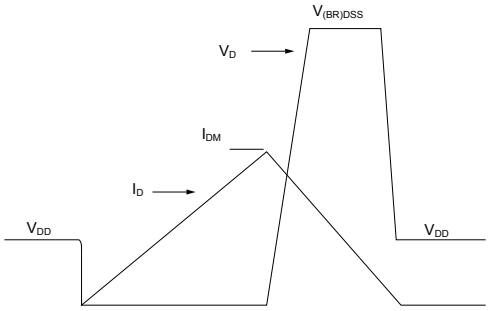

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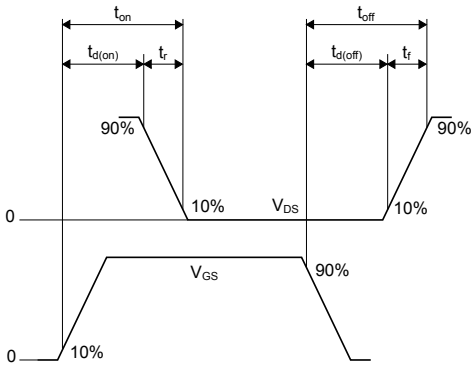
Figure 18. Switching time waveform



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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 IPAK (TO-251) type C package information

Figure 19. **IPAK (TO-251) type C package outline**

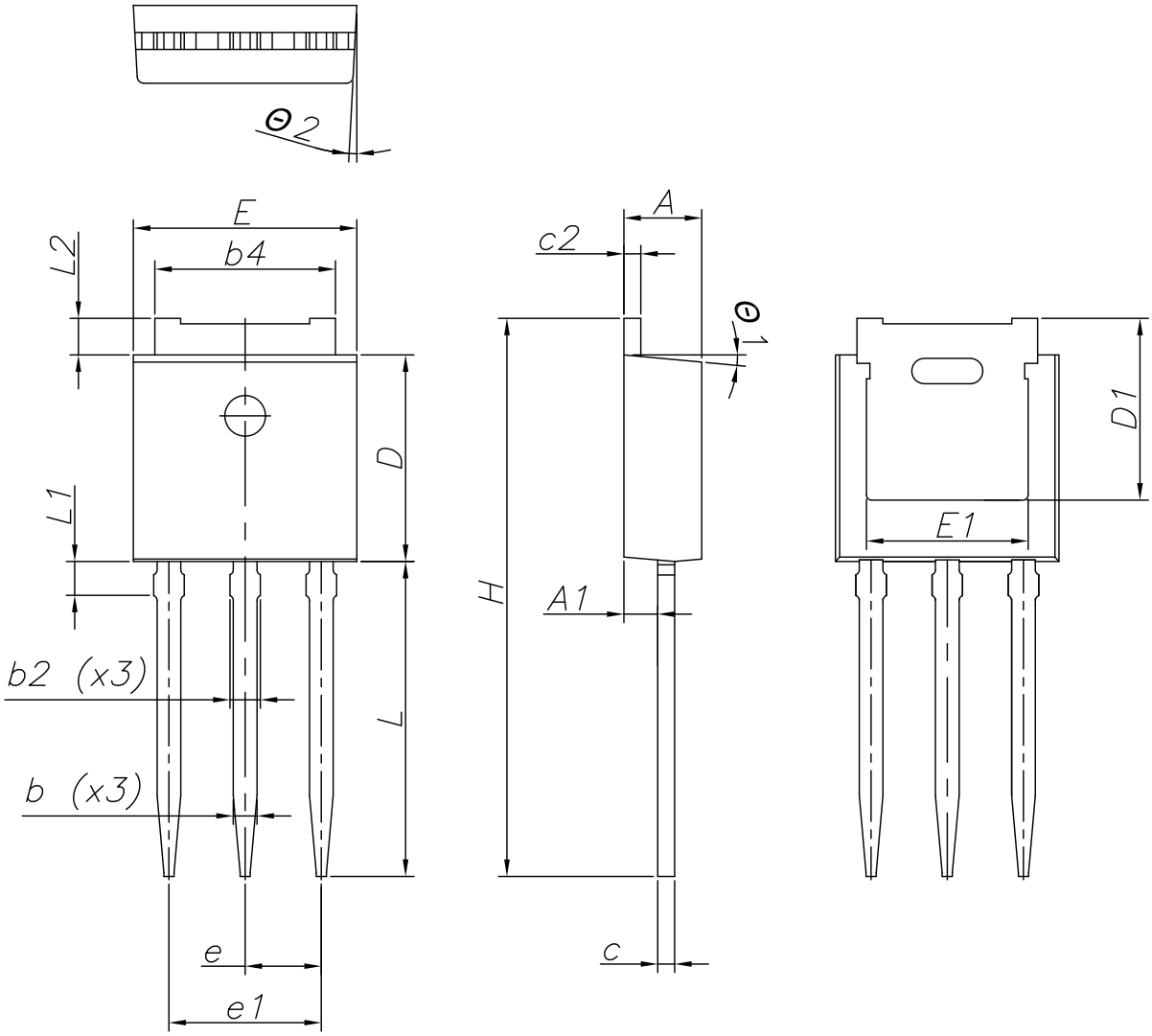

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Table 8. **IPAK (TO-251) type C package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.35
A1	0.90	1.00	1.10
b	0.66		0.79
b2			0.90
b4	5.23	5.33	5.43
c	0.46		0.59
c2	0.46		0.59
D	6.00	6.10	6.20
D1	5.20	5.37	5.55
E	6.50	6.60	6.70
E1	4.60	4.78	4.95
e	2.20	2.25	2.30
e1	4.40	4.50	4.60
H	16.18	16.48	16.78
L	9.00	9.30	9.60
L1	0.80	1.00	1.20
L2	0.90	1.08	1.25
θ1	3°	5°	7°
θ2	1°	3°	5°

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
02-May-2016	1	Initial release.
18-Dec-2018	2	Added *Section 4.2 IPAK (TO-251) type C package information*.
18-Jul-2023	3	Updated Section 4.1 IPAK (TO-251) type C package information. Minor text changes.

Contents