

To our customers,

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## Old Company Name in Catalogs and Other Documents

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On April 1<sup>st</sup>, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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**EOL announced Product**

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SWITCHING P-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

This product is P-Channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Super Low On-State Resistance  
 $R_{DS(on)1} = 50 \text{ m}\Omega \text{ Max. (} V_{GS} = -10 \text{ V, } I_D = -10 \text{ A)}$   
 $R_{DS(on)2} = 88 \text{ m}\Omega \text{ Max. (} V_{GS} = -4 \text{ V, } I_D = -10 \text{ A)}$
- Low  $C_{iss}$   $C_{iss} = 2360 \text{ pF Typ.}$
- Built-in Gate Protection Diode

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ )

Drain to Source Voltage	$V_{DSS}$	-60	V
Gate to Source Voltage*	$V_{GSS(AC)}$	$\pm 20$	V
Gate to Source Voltage	$V_{GSS(DC)}$	-20, 0	V
Drain Current (DC)	$I_D(DC)$	$\pm 20$	A
Drain Current (pulse)**	$I_D(pulse)$	$\pm 80$	A
Total Power Dissipation ( $T_c = 25^\circ\text{C}$ )	$P_T$	35	W
Total Power Dissipation ( $T_A = 25^\circ\text{C}$ )	$P_T$	2.0	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

\*  $f = 20 \text{ kHz, Duty Cycle} \leq 10\% (+\text{Side})$

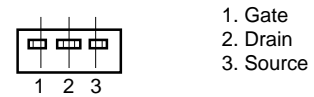
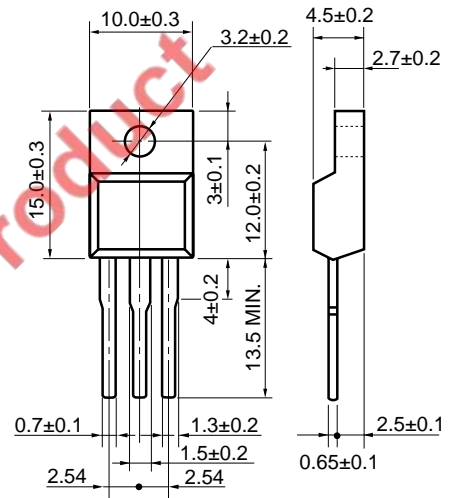
\*\*  $PW \leq 10 \mu\text{s, Duty Cycle} \leq 1\%$

THERMAL RESISTANCE

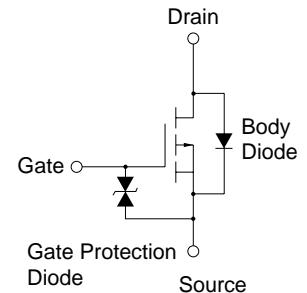
Channel to Case	$R_{th(ch-C)}$	3.57 $^\circ\text{C/W}$
Channel to Ambient	$R_{th(ch-A)}$	62.5 $^\circ\text{C/W}$

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

PACKAGE DIMENSIONS  
(in millimeter)



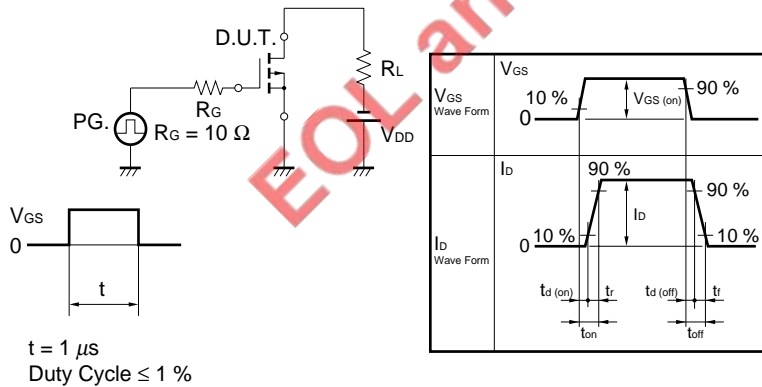
ISOLATED TO-220 (MP-45F)



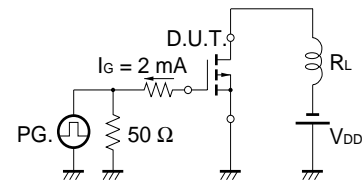
ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R <sub>DS(on)1</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -10 A		39	50	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = -4 V, I <sub>D</sub> = -10 A		61	88	mΩ
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1 mA	-1.0	-1.5	-2.0	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -10 A	8.0	15		S
Drain Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> = -60 V, V <sub>GS</sub> = 0			-10	μA
Gate to Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0			±10	μA
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -10 V V <sub>GS</sub> = 0 f = 1 MHz		2360		pF
Output Capacitance	C <sub>oss</sub>			1060		pF
Reverse Transfer Capacitance	C <sub>rss</sub>			350		pF
Turn-On Delay Time	t <sub>d(on)</sub>	I <sub>D</sub> = -10 A V <sub>GS(on)</sub> = -10 V V <sub>DD</sub> = -30 V R <sub>G</sub> = 10 Ω		25		ns
Rise Time	t <sub>r</sub>			160		ns
Turn-Off Delay Time	t <sub>d(off)</sub>			310		ns
Fall Time	t <sub>f</sub>			240		ns
Total Gate Charge	Q <sub>G</sub>	I <sub>D</sub> = -20 A V <sub>DD</sub> = -48 V V <sub>GS</sub> = -10 V		74		nC
Gate to Source Charge	Q <sub>GS</sub>			12		nC
Gate to Drain Charge	Q <sub>GD</sub>			16		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 20 A, V <sub>GS</sub> = 0		1.0	1.5	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 20 A, V <sub>GS</sub> = 0 di/dt = 100 A/μs		130		ns
Reverse Recovery Charge	Q <sub>rr</sub>			290		nC

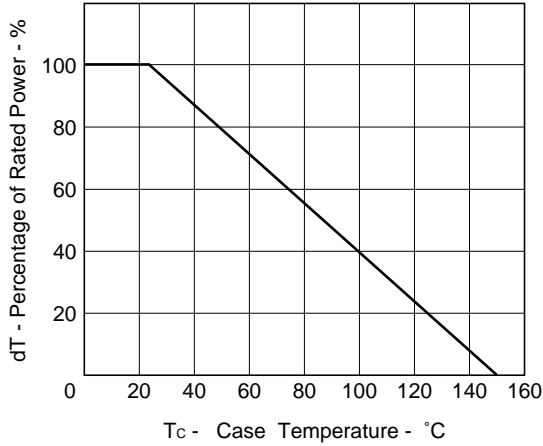
Test Circuit 1 Switching Time



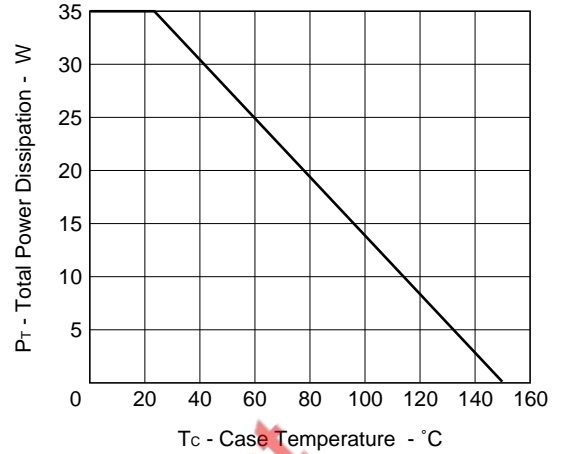
Test Circuit 2 Gate Charge



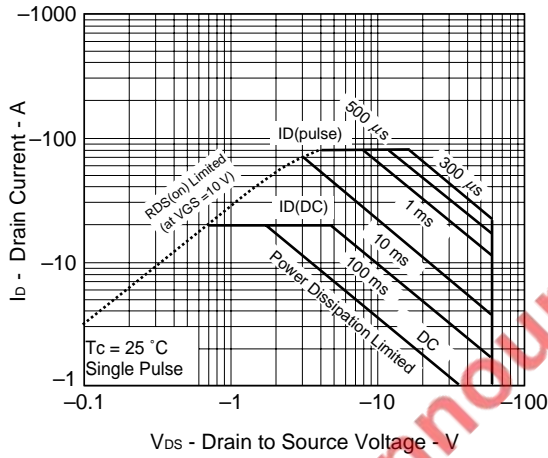
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



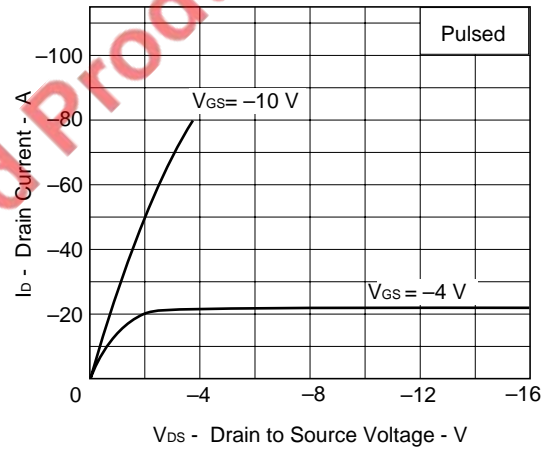
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



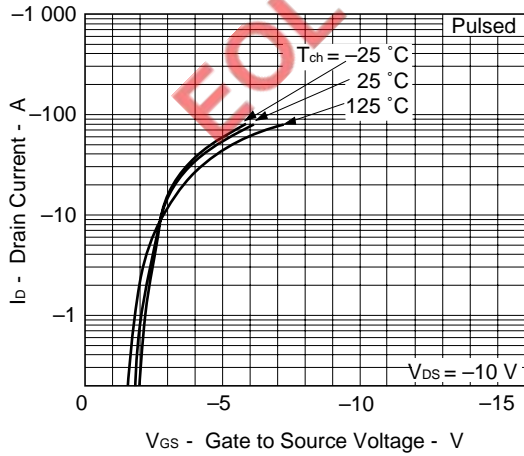
FORWARD BIAS SAFE OPERATING AREA



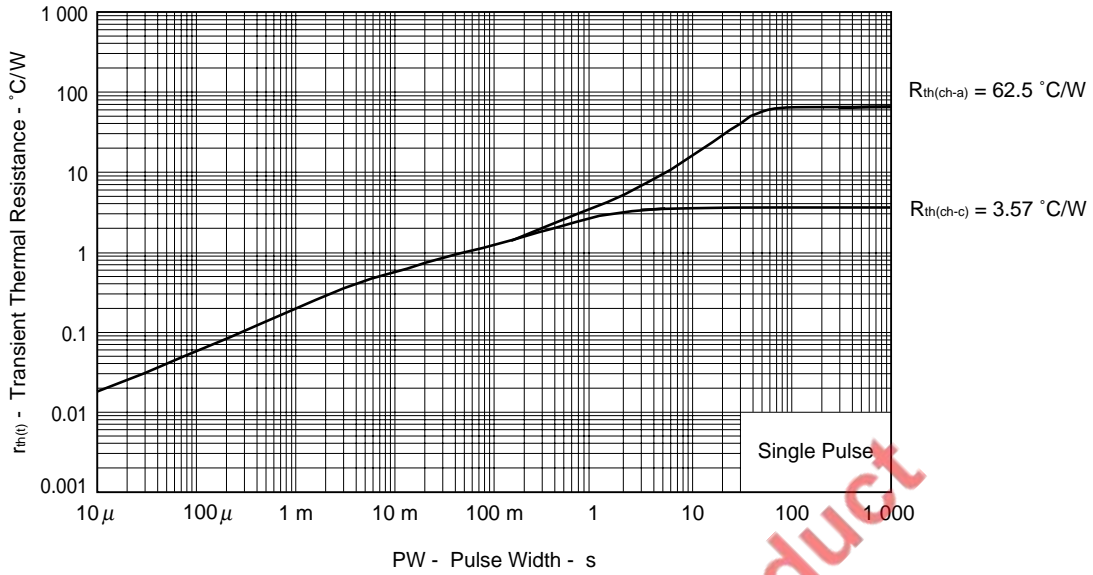
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



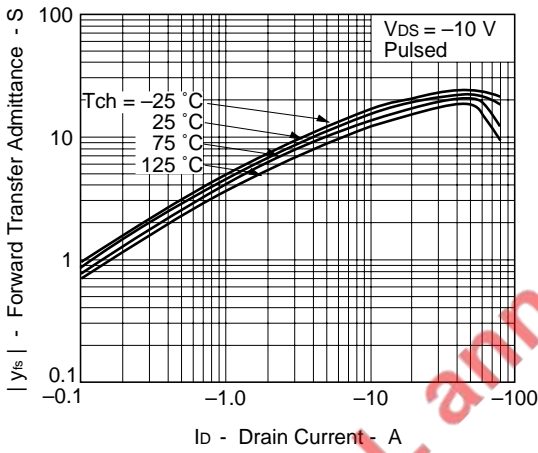
FORWARD TRANSFER CHARACTERISTICS



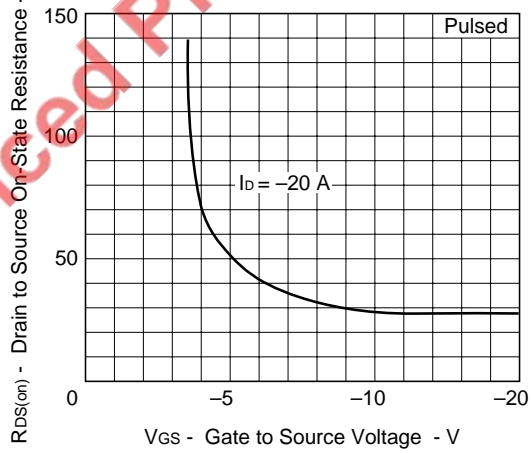
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



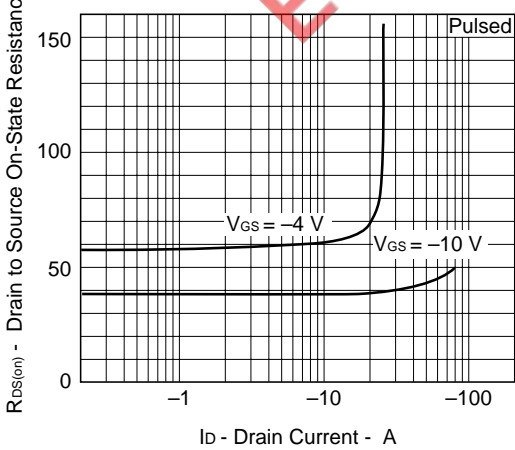
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



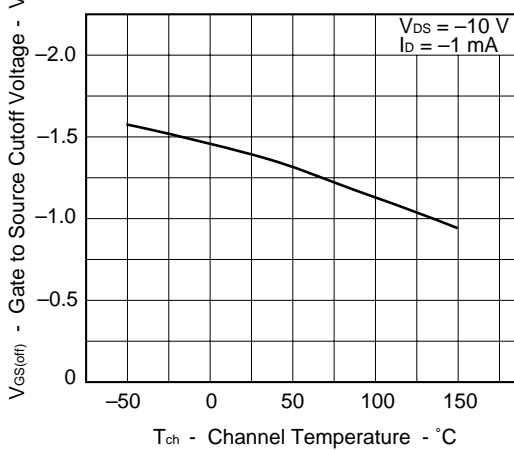
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

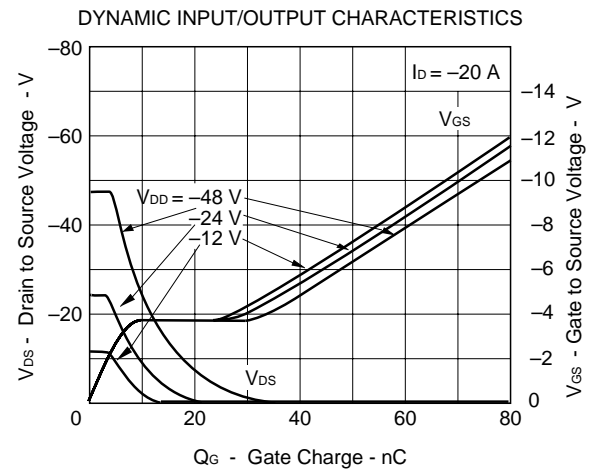
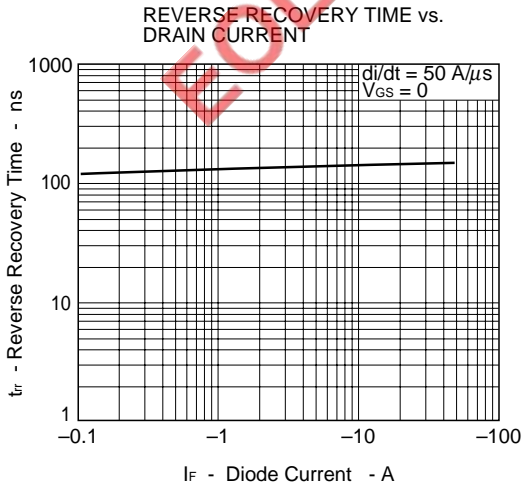
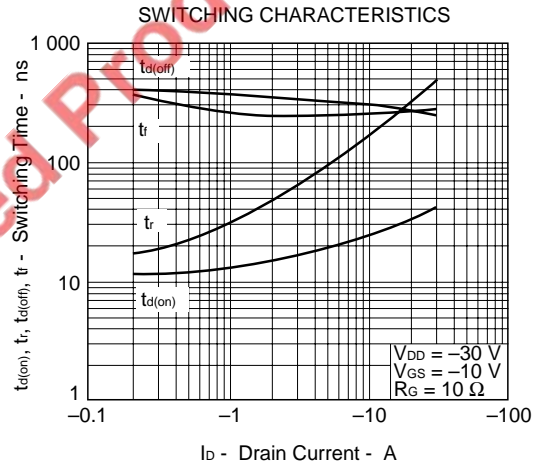
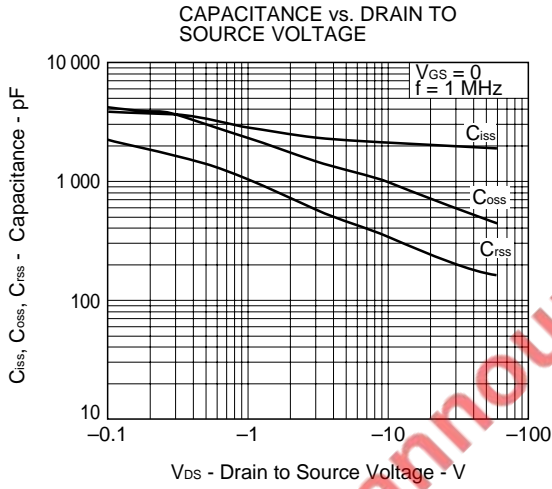
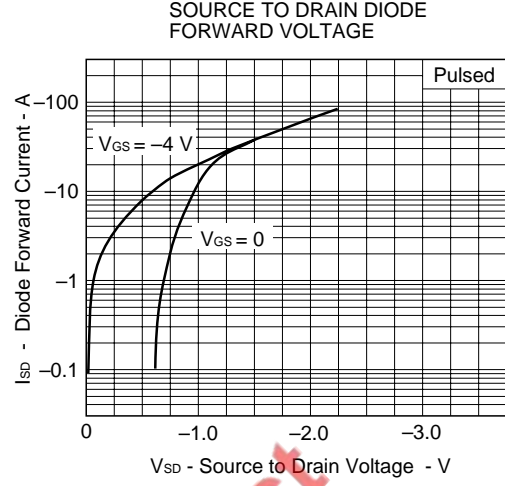
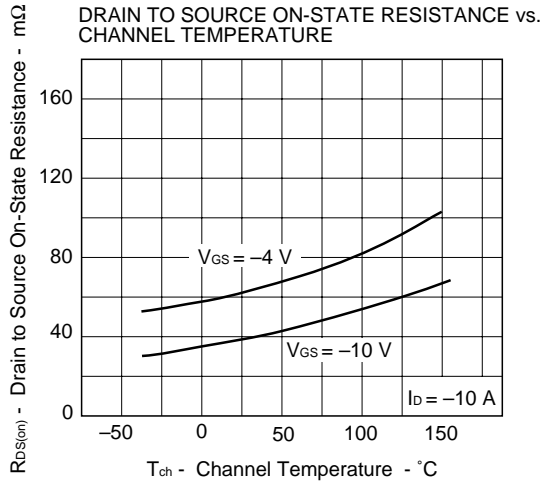


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE





Document Name	Document No.
NEC semiconductor device reliability/quality control system	C11745E
Power MOS FET features and application to switching power supply	D12971E
Application circuits using Power MOS FET	TEA-1035
Safe operating area of Power MOS FET	TEA-1037
Guide to prevent damage for semiconductor devices by electrostatic discharge (EDS)	C11892E

**EOL announced Product**



[MEMO]

**EOL announced Product**

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