REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Corrections to table I.	98-03-23	K. A. Cottongim
B	Add device type 02.	99-10-08	Ray Monnin
C	Editorial corrections to tables I, III, and figures 1, 2, 3, 4. Update drawing boilerplate.	03-03-31	Raymond Monnin

REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C			
SHEET	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51			
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Gary Zahn

STANDARD MICROCIRCUIT DRAWING

CHECKED BY
Michael C. Jones

DEFENSE SUPPLY CENTER COLUMBUS
POST OFFICE BOX 3990
COLUMBUS, OHIO 43216-5000
http://www.dscc.dla.mil

APPROVED BY
Kendall A. Cottongim

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

MICROCIRCUIT, HYBRID, DIGITAL, QUAD, (4 X 32-BIT) MICROCONTROLLER, +5 VOLT SUPPLY

DRAWING APPROVAL DATE
97-09-19

AMSC N/A

REVISION LEVEL	SIZE	CAGE CODE	
C	A	**67268**	**5962-97506**

SHEET 1 OF 51

DSCC FORM 2233
APR 97

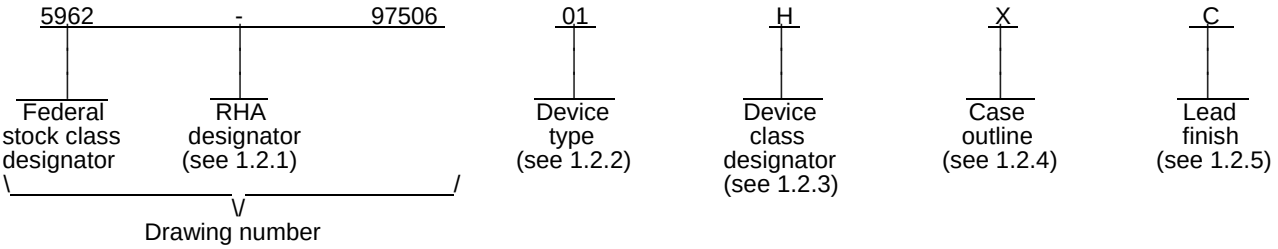
5962-E206-03

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents five product assurance classes as defined in paragraph 1.2.3 and MIL-PRF-38534. A choice of case outlines and lead finishes which are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	AD14060BF/QML-4	Quad digital signal processor, +5 V supply, 40 MHz, Twelve, 40 megabyte/s link ports (3 from each processor), Four, 40 megabit/s independent serial ports (1 from each processor)
02	AD14060TF/QML-4	Quad digital signal processor, +5 V supply, 40 MHz, Twelve, 40 megabyte/s link ports (3 from each processor), Four, 40 megabit/s independent serial ports (1 from each processor)

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level. All levels are defined by the requirements of MIL-PRF-38534 and require QML Certification as well as qualification (Class H, K, and E) or QML Listing (Class G and D). The product assurance levels are as follows:

Device class	Device performance documentation
K	Highest reliability class available. This level is intended for use in space applications.
H	Standard military quality class level. This level is intended for use in applications where non-space high reliability devices are required.
G	Reduced testing version of the standard military quality class. This level uses the Class H screening and In-Process Inspections with a possible limited temperature range, manufacturer specified incoming flow, and the manufacturer guarantees (but may not test) periodic and conformance inspections (Group A, B, C, and D).
E	Designates devices which are based upon one of the other classes (K, H, or G) with exception(s) taken to the requirements of that class. These exception(s) must be specified in the device acquisition document; therefore the acquisition document should be reviewed to ensure that the exception(s) taken will not adversely affect system performance.
D	Manufacturer specified quality class. Quality level is defined by the manufacturers internal, QML certified flow. This product may have a limited temperature range.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	308	Quad ceramic flat pack

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{DD})	-0.3 V dc to +7.0 V dc
Input voltage (V_{IN})	-0.5 V dc to V_{DD} + 0.5 V dc
Output voltage swing (V_{OUT})	-0.3 V dc to V_{DD} + 0.5 V dc
Load capacitance	200 pF
Junction temperature under bias (T_J)	+130°C
Junction-to-case temperature (θ_{JC})	0.36°C/W
Lead temperature soldering (5 seconds)	+280°C
Storage temperature	-65°C to +150°C

1.4 Recommended operating conditions.

Supply voltage (V_{DD})	+4.75 V dc to +5.25 V dc
Case operating temperature range (T_C):	
Device type 01	-40°C to +100°C
Device type 02	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum ratings may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device classes D, E, G, H, and K shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 may include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. Therefore, the tests and inspections herein may not be performed for the applicable device class (see MIL-PRF-38534). Furthermore, the manufacturer may take exceptions or use alternate methods to the tests and inspections herein and not perform them. However, the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram(s). The block diagram(s) shall be as specified on figure 3.

3.2.4 Timing waveform(s). The timing waveform(s) shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking of device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_C as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

(1) Static supply current (I_{DDq}).
Checks that current draw is not grossly excessive. Current exceeding 1.3 amperes on the module indicates failure. Normal measured current is about 0.5 amperes.

(2) Interconnects.
Checks for electrical continuity through the package leads and wire bonds, along with continuity of internal wiring within the module.

(3) Single processor functional.
A collection of test routines perform a rudimentary check of the basic functionally of each individual processor. The following individual processor units are tested: DAGs 1 and 2, timer, program sequencer, PX register, multiplier, data register file, shifter, ALU, link ports, serial ports, DMA, IOP registers, and memory.

(a) Serial port test.
This routine uses internal loopback to test basic operation of serial port 0 and serial port 1, by transmitting and receiving 16-bit words. In addition, the COMPare operation of the ALU and BitSET operation of the shifter are tested. Serial ports are tested at a clock rate of 10 MHz.

(b) Computation routine.
The routine tests basic operation of the ALU through ADD, SUBTRACT, and COMPare functions. In addition, the multiplier and DAGs are tested using floating point multiply and load/write functions, while the shifter is tested with a BitSET function. All operations use 32-bit words.

(c) Link routine.
Using 32-bit data and internal memory to memory receive, basic operation of Link buffers 0 - 5 is tested. In addition, the ALU, COMPare, and shifter BitSET functions are tested.

(d) PX routine.
This routine tests basic operation of the PX register and short word addressing. The PX register is loaded with a 48-bit word, then the PX is read into memory. Short word addressing is used to read back, in 16-bit word segments, the 48-bit word from memory. In addition, the ALU, COMPare, and shifter BitSET functions are tested.

(e) Timer routine.
This routine will count down the timer until $t_{count} = 0$, at which time an interrupt will occur, followed by a return to the code. This test will verify operation of the program sequencer, timer, ALU, COMPare function, and shifter BitSET function.

(4) Multiprocessor functional.

(a) Interprocessor links: all tested using 2 times the clock rate (80 MHz).

(b) Multiprocessor memory space: each processor accesses and checks memory of the other three processors.

c. Final electrical test parameters shall be as specified in table II herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level input voltage 2/	V_{IH1}	V_{DD} = +5.25 V dc	1,2,3	01,02	2.0		V
High level input voltage 3/	V_{IH2}	V_{DD} = +5.25 V dc	1,2,3	01,02	2.2		V
Low level input voltage 2/ 3/	V_{IL}	V_{DD} = +4.75 V dc	1,2,3	01,02		0.8	V
High level output voltage 4/	V_{OH}	V_{DD} = +4.75 V dc, 5/ I_{OH} = -2.0 mA	1,2,3	01,02	4.1		V
Low level output voltage 4/	V_{OL}	V_{DD} = +4.75 V dc, 5/ I_{OL} = 4.0 mA	1,2,3	01,02		0.4	V
High level input current 6/ 7/ 8/	I_{IH}	V_{DD} = +5.25 V dc, V_{IN} = V_{DD}MAX	1,2,3	01,02		10	∝A
High level input current 8/ 9/ 10/	I_{IHx4}	V_{DD} = +5.25 V dc, V_{IN} = V_{DD}MAX	1,2,3	01,02		40	∝A
Low level input current 6/	I_{IL}	V_{DD} = +5.25 V dc, V_{IN} = 0 V	1,2,3	01,02		10	∝A
Low level input current 9/	I_{ILx4}	V_{DD} = +5.25 V dc, V_{IN} = 0 V	1,2,3	01,02		40	∝A
Low level input current 7/	I_{ILP}	V_{DD} = +5.25 V dc, V_{IN} = 0 V	1,2,3	01,02		150	∝A
Low level input current 8/ 10/	I_{ILPx4}	V_{DD} = +5.25 V dc, V_{IN} = 0 V	1,2,3	01,02		600	∝A
Three state leakage current 11/ 12/ 13/ 14/	I_{OZH}	V_{DD} = +5.25 V dc, V_{IN} = V_{DD}MAX	1,2,3	01,02		10	∝A
Three state leakage current 15/ 16/	I_{OZHx4}	V_{DD} = +5.25 V dc, V_{IN} = V_{DD}MAX	1,2,3	01,02		40	∝A
Three state leakage current 11/ 17/	I_{OZL}	V_{DD} = +5.25 V dc, V_{IN} = 0 V	1,2,3	01,02		10	∝A
Three state leakage current 15/	I_{OZLx4}	V_{DD} = +5.25 V dc, V_{IN} = 0 V	1,2,3	01,02		40	∝A
Three state leakage current 17/	I_{OZHP}	V_{DD} = +5.25 V dc, V_{IN} = V_{DD}MAX	1,2,3	01,02		350	∝A
Three state leakage current 14/	I_{OZLC}	V_{DD} = +5.25 V dc, V_{IN} = 0 V	1,2,3	01,02		1.5	mA
Three state leakage current 18/	I_{OZLA}	V_{DD} = +5.25 V dc, V_{IN} = 2 V	1,2,3	01,02		350	∝A

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Three state leakage current 13/	I_{OZLAR}	V_{DD} = +5.25 V dc, V_{IN} = 0 V	1,2,3	01,02		4.2	mA
Three state leakage current 12/	I_{OZLS}	V_{DD} = +5.25 V dc, V_{IN} = 0 V	1,2,3	01,02		150	∝A
Three state leakage current 16/	I_{OZLSx4}	V_{DD} = +5.25 V dc, V_{IN} = 0 V	1,2,3	01,02		600	∝A
Supply current (internal) 19/	I_{DDIN}	t_{CK} = 25 ns, V_{DD} = MAX	1,2,3	01,02		2.92	A
Supply current (idle) 20/	I_{DDIDLE}	V_{DD} = max	1,2,3	01		800	mA
				02		1200	
Input capacitance	C_{IN}	f = 1 MHz, T_C = +25°C, V_{IN} = 2.5 V dc	---	01,02	21/		
Functional tests		See 4.3.1.c	7,8	01,02			
Clock Input Timing Requirements							
CLKIN period	t_{CK}	See figure 4.	9,10,11	01,02	25	100	ns
CLKIN width low	t_{CKL}				7		
CLKIN width high	t_{CKH}				5		
CLKIN rise/fall (0.4 V - 2.0 V)	t_{CKRF}					3	
Reset Timing Requirements							
$\overline{\text{RESET}}$ pulse width low 23/	t_{WRST}	See figure 4. 22/	9,10,11	01,02	$4t_{CK}$		ns
$\overline{\text{RESET}}$ setup before CLKIN high 24/	t_{SRST}				14+DT/2	t_{CK}	
Interrupts Timing Requirements							
$\overline{\text{IRQ}}$2-0 setup before CLKIN high 25/	t_{SIR}	See figure 4. 22/	9,10,11	01,02	18+3DT/4		ns
$\overline{\text{IRQ}}$2-0 hold before CLKIN high 25/	t_{HIR}					11.5+3DT/4	
$\overline{\text{IRQ}}$2-0 width pulse 26/	t_{IPW}				2+t_{CK}		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Timer Switching Characteristics							
CLKIN high to TIMEXP	t_{DTEX}	See figure 4. 22/	9,10,11	01,02		16	ns
FLAGS Timing and Switching Characteristics							
FLAG2-0$_{IN}$ setup before CLKIN high 27/	t_{SFI}	See figure 4. 22/	9,10,11	01,02	8+5DT/16		ns
FLAG2-0$_{IN}$ hold after CLKIN high 27/	t_{HFI}				0.5 - 5DT/16		
FLAG2-0$_{IN}$ delay after RD/WR low 27/	t_{DWRFI}					4.5+7DT/16	
FLAG2-0$_{IN}$ hold after $\overline{RD}$/$\overline{WR}$ deasserted 27/	t_{HFIWR}				0.5		
FLAG2-0$_{OUT}$ delay after CLKIN high	t_{DFO}					17	
FLAG2-0$_{OUT}$ hold after CLKIN high	t_{HFO}				4		
CLKIN high to FLAG2-0$_{OUT}$ enable	t_{DFOE}				3		
CLKIN high to FLAG2-0$_{OUT}$ disable	t_{DFOD}					15	
Memory Read - Bus Master Timing and Switching Requirements							
Address delay to data valid 29/ 30/	t_{DAD}	See figure 4. 22/ 28/	9,10,11	01,02		17.5+DT+W	ns
$\overline{RD}$ low to data valid 29/	t_{DRLD}					11.5+5DT /D+W	
Data hold from address 31/	t_{HDA}				1		
Data hold from $\overline{RD}$ high 31/	t_{HDRH}				2.5		
ACK delay from address 30/ 32/	t_{DAAK}					13.5+7DT /8+W	
ACK delay from $\overline{RD}$ low 31/	t_{DSAK}					7.5+DT /2+W	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Memory Read - Bus Master Timing and Switching Requirements - Continued.							
Address hold after $\overline{RD}$ high	t_{DRHA}	See figure 4. 22/ 28/	9,10,11	01,02	-0.5+H		ns
Address to $\overline{RD}$ low 30/	t_{DARL}				1.5+3DT /8		
$\overline{RD}$ pulse width	t_{RW}				12.5+5DT /8+W		
$\overline{RD}$ high to $\overline{WR}$, $\overline{RD}$, DMAGx low	t_{RWR}				8+3DT /8+HI		
Address setup before ADRCLK high 30/	t_{SADADC}				-0.5+DT/4		
Memory Write - Bus Master Timing and Switching Requirements							
ACK delay from address selects 30/ 32/	t_{DAAK}	See figure 4. 22/ 28/	9,10,11	01,02		13.5+7DT /8+W	ns
ACK delay from $\overline{WR}$ low 32/	t_{DSAK}					8+DT /2+W	
Address, selects to $\overline{WR}$ deasserted 30/	t_{DAWH}				16.5+15DT /16+W		
Address, selects to $\overline{WR}$ low 30/	t_{DAWL}				2.5+3DT/8		
$\overline{WR}$ pulse width	t_{WW}				12+9DT /16+W		
Data setup before $\overline{WR}$ high	t_{DDWH}				6.5+DT /2+W		
Address hold after $\overline{WR}$ deasserted	t_{DWHA}				0+DT /16+H		
Data disabled after $\overline{WR}$ deasserted 33/	t_{DATRWH}				0.5+DT /16+H	6.5+DT /16+H	
$\overline{WR}$ high to $\overline{WR}$, $\overline{RD}$, DMAGx low	t_{WWR}				8+7DT /16+H		
Data disable before $\overline{WR}$ or $\overline{RD}$ low	t_{DDWR}				4.5+3DT /8+I		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Memory Write - Bus Master Timing and Switching Requirements - Continued.							
$\overline{WR}$ low to data enabled	t_{WDE}	See figure 4. 22/ 28/	9,10,11	01,02	-1.5+DT/16		ns
Address, selects to ADRCLK high 30/	t_{SADADC}				0.5+DT/4		
Synchronous Read/Write - Bus Master Timing and Switching Requirements							
Data setup before CLKIN	t_{SSDATI}	See figure 4. 22/ 28/	9,10,11	01,02	3+DT/8		ns
Data hold after CLKIN	t_{HSDATI}				4-DT/8		
ACK delay after address, MSx, SW, BMS 30/ 32/	t_{DAAK}					13.5+7DT /8+W	
ACK setup before CLKIN 32/	t_{SACKC}				6.5+DT/4		
ACK hold after CLKIN	t_{HACKC}				-0.5-DT/4		
Address, $\overline{MSx}$, $\overline{BMS}$, $\overline{SW}$, delay after CLKIN 30/	t_{DADRO}					8-DT/8	
Address, $\overline{MSx}$, $\overline{BMS}$, $\overline{SW}$, hold after CLKIN 30/	t_{HADRO}				-1-DT/8		
PAGE delay after CLKIN	t_{DPGC}				9+DT/8	17+DT/8	
$\overline{RD}$ high delay after CLKIN	t_{DRDO}				-2-DT/8	5-DT/8	
$\overline{WR}$ high delay after CLKIN	t_{DWRO}				-3-3DT /16	5-3DT /16	
$\overline{RD}$/$\overline{WR}$ low delay after CLKIN	t_{DRWL}				8+DT/4	13.5+DT/4	
Data delay after CLKIN	t_{SDDATO}			01		20+5DT /16	
				02		20.5+5DT /16	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Synchronous Read/Write - Bus Master Timing and Switching Requirements - Continued.							
Data disable after CLKIN 33/	t_{DATTR}	See figure 4. 22/ 28/	9,10,11	01,02	0-DT/8	8-DT/8	ns
ADRCLK delay after CLKIN	t_{DADCCK}				4+DT/8	11+DT/8	
ADRCLK period	t_{ADRCK}				t_{CK}		
ADRCLK width high	t_{ADRCKH}				(t_{CK}/2-2)		
ADRCLK width low	t_{ADRCKL}				(t_{CK}/2-2)		
Synchronous Read/Write - Bus Slave Timing and Switching Requirements							
Address, $\overline{SW}$ setup before CLKIN	t_{SADRI}	See figure 4. 22/ 28/	9,10,11	01,02	15.5+DT /2		ns
Address, $\overline{SW}$ hold before CLKIN	t_{HADRI}					4.5+DT/2	
$\overline{RD}$/$\overline{WR}$ low setup before CLKIN 34/	t_{SRWLI}				9.5+5DT /16		
$\overline{RD}$/$\overline{WR}$ low hold after CLKIN	t_{HRWLI}			01	-3.5-5DT /16	8+7DT /16	
				02	-3-5DT /16	8+7DT /16	
$\overline{RD}$/$\overline{WR}$ pulse high	t_{RWHPI}			01,02	3		
Data setup before $\overline{WR}$ high	t_{SDATWH}				5.5		
Data hold after $\overline{WR}$ high	t_{HDATWH}				1.5		
Data delay after CLKIN	t_{SDDATO}			01		20+5DT /16	
				02		20.5+5DT /16	
Data disable after CLKIN 33/	t_{DATTR}			01,02	0-DT/8	8-DT/8	
ACK delay after address $\overline{SW}$ 35/	t_{DACKAD}					10	
ACK disable after CLKIN 35/	t_{ACKTR}				-1-DT/8	7-DT/8	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Multiprocessor Bus Request and Host Request Timing and Switching Requirements							
$\overline{HBG}$ low to $\overline{RD}$/$\overline{WR}$/$\overline{CS}$, valid	$t_{HBGRCSV}$	See figure 4. 22/ 28/	9,10,11	01,02		19.5+5DT /4	ns
$\overline{HBR}$ setup before CLKIN 37/	t_{SHBRI}				20+3DT/4		
$\overline{HBR}$ hold before CLKIN 37/	t_{HHBRI}					13.5+3DT /4	
$\overline{HBG}$ setup before CLKIN	t_{SHBGI}				13+DT/2		
$\overline{HBG}$ hold before CLKIN high	t_{HHBGI}			01		5.5+DT/2	
				02		5.25+DT/2	
$\overline{BR}$x, $\overline{CPA}$ setup before CLKIN high 38/	t_{SBRI}			01,02	13+DT/2		
$\overline{BR}$x, $\overline{CPA}$ hold before CLKIN high	t_{HBRI}					5.5+DT/2	
RPBA setup before CLKIN	t_{SRPBAI}				21+3DT/4		
RPBA hold before CLKIN	t_{HRPBAI}					11.5+3DT/4	
$\overline{HBG}$ delay after CLKIN	t_{DHBGO}					8-DT/8	
$\overline{HBG}$ hold after CLKIN	t_{HHBGO}				-2-DT/8		
$\overline{BR}$x delay after CLKIN	t_{DBRO}					8-DT/8	
$\overline{BR}$x hold after CLKIN	t_{HBRO}				-2-DT/8		
$\overline{CPA}$ low delay after CLKIN	t_{DCPAO}					9-DT/8	
$\overline{CPA}$ disable after CLKIN	t_{TRCPA}				-2-DT/8	5.5-DT/8	
REDY (O/D) or (A/D) low from CS and HBR low 39/	t_{DRDYCS}					9.5	
REDY (O/D) disable or 39/ REDY (A/D) high from HBG	t_{TRDYHG}				40+27DT /16		
REDY (A/D) disable from $\overline{CS}$ or HBR high 39/	t_{ARDYTR}					11	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Asynchronous Read Cycle Timing and Switching Requirements							
Address setup/$\overline{CS}$ low before $\overline{RD}$ low 40/	t_{SADRDL}	See figure 4. 22/ 28/	9,10,11	01,02	0.5		ns
Address hold/$\overline{CS}$ hold low after $\overline{RD}$	t_{HADRDH}				0.5		
$\overline{RD}$/$\overline{WR}$ high width	t_{WRWH}				6		
$\overline{RD}$ high delay after REDY (O/D) disable	$t_{DRDHRDY}$				0		
$\overline{RD}$ high delay after REDY (A/D) disable	$t_{DRDHRDY}$				0		
Data valid before REDY disable from low	$t_{SDATRDY}$				1.5		
REDY (O/D) or (A/D) low delay after RD low	$t_{DRDYRDL}$					11	
REDY (O/D) or (A/D) low pulse width for read	t_{RDYPRD}				45+DT		
Data disable after $\overline{RD}$ high	t_{HDARWH}				1.5	9	
Asynchronous Write Cycle Timing and Switching Requirements							
$\overline{CS}$ low setup before $\overline{WR}$ low	t_{SCSWRL}	See figure 4. 22/ 28/	9,10,11	01,02	0.5		ns
$\overline{CS}$ low hold after $\overline{WR}$ high	t_{HCSWRH}				0.5		
Address setup before $\overline{WR}$ high	t_{SADWRH}				5.5		
Address hold after $\overline{WR}$ high	t_{HADWRH}				2.5		
$\overline{WR}$ low width	t_{WWRL}				7		
$\overline{RD}$/$\overline{WR}$ high width	t_{WRWH}				6		
$\overline{WR}$ high delay after REDY (O/D) or (A/D) disable	$t_{DWRHRDY}$				0.5		
Data setup before $\overline{WR}$ high	t_{SDATWH}				5.5		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Asynchronous Write Cycle Timing and Switching Requirements - Continued.							
Data hold after $\overline{WR}$ high	t_{HDATWH}	See figure 4. 22/ 28/	9,10,11	01,02	1.5		ns
REDY (O/D) or (A/D) low delay after WR/CS low	$t_{DRDYWRL}$					11	
REDY (O/D) or (A/D) low pulse width for write	t_{RDYPWR}				15		
REDY (O/D) or (A/D) disable to CLKIN	t_{SRDYCK}				0+7DT /16	8+7DT /16	
Three State Timing - (Bus Master, Bus Slave, HBR, SBTS) Timing and Switching Requirements							
$\overline{SBTS}$ setup before CLKIN	t_{STSCK}	See figure 4. 22/ 28/	9,10,11	01,02	12.5+DT/2		ns
$\overline{SBTS}$ hold before CLKIN	t_{HTSCK}					5.5+DT/2	
Address/select enable after CLKIN	t_{MIENA}				-1.5-DT/8		
Strobes enable after CLKIN 41/	t_{MIENS}				-1.5-DT/8		
$\overline{HBG}$ enable after CLKIN	t_{MIENHG}				-1.5-DT/8		
Address select/disable after CLKIN	t_{MITRA}			01		1-DT/4	
				02		1.15-DT/4	
Strobes disable after CLKIN 41/	t_{MITRS}			01,02		2.5-DT/4	
$\overline{HBG}$ disable after CLKIN	t_{MITRHG}					3.0-DT/4	
Data enable after CLKIN 42/	t_{DATEN}				9+5DT/16		
Data disable after CLKIN 42/	t_{DATTR}				0-DT/8	8-DT/8	
ACK enable after CLKIN 42/	t_{ACKEN}				7.5+DT/4		
ACK disable after CLKIN 42/	t_{ACKTR}				-1-DT/8	7-DT/8	
ADRCLK enable after CLKIN 42/	t_{ADCEN}				-2-DT/8		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Three State Timing - (Bus Master, Bus Slave, HBR, SBTS) Timing and Switching Requirements - Continued.							
ADRCLK disable after CLKIN 42/	t_{ADCTR}	See figure 4. 22/ 28/	9,10,11	01,02		9-DT/4	ns
Memory interface disable before HBG low 43/	t_{MTRHBG}				-1+DT/8		
Memory interface enable after HBG low 43/	t_{MENHBG}				18.5+DT		
DMA Handshake Timing and Switching Requirements							
$\overline{\text{DMARx}}$ low setup before CLKIN 44/	t_{SDRLC}	See figure 4. 22/ 28/	9,10,11	01,02	5		ns
$\overline{\text{DMARx}}$ high setup before CLKIN 44/	t_{SDRHC}				5		
$\overline{\text{DMARx}}$ width low (nonsynchronous)	t_{WDR}				6		
Data setup after $\overline{\text{DMAGx}}$ low 45/	$t_{SDATDGL}$					9+5DT/8	
Data hold after $\overline{\text{DMAGx}}$ high	$t_{HDATIDG}$				2		
Data valid after $\overline{\text{DMARx}}$ high 45/	t_{DATDRH}					15.5+7DT /8	
$\overline{\text{DMAGx}}$ low edge to low edge	t_{DMARLL}				23+7DT/8		
$\overline{\text{DMAGx}}$ width high	t_{DMARH}				6		
$\overline{\text{DMAGx}}$ low delay after CLKIN	t_{DDGL}				9+DT/4	16+DT/4	
$\overline{\text{DMAGx}}$ high width	t_{WDGH}				6+3DT/8		
$\overline{\text{DMAGx}}$ low width	t_{WDGL}				12+5DT/8		
$\overline{\text{DMAGx}}$ high delay after CLKIN	t_{HDGC}				-2-DT/8	7-DT/8	
Data valid before $\overline{\text{DMAGx}}$ high 46/	$t_{VDATDGH}$				7.5+9DT/16		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DMA Handshake Timing and Switching Requirements - Continued.							
Data disable after $\overline{\text{DMAGx}}$ high 33/	$t_{DATRDGH}$	See figure 4. 22/ 28/	9,10,11	01,02	-1	7.5	ns
$\overline{\text{WR}}$ low before $\overline{\text{DMAGx}}$ low	t_{DGWRL}				-0.5	2.5	
$\overline{\text{DMAGx}}$ low before $\overline{\text{WR}}$ high	t_{DGWRH}				9.5+5DT /8+W		
$\overline{\text{WR}}$ high before $\overline{\text{DMAGx}}$ high	t_{DGWRR}				0.5+DT/16	3.5+DT/16	
$\overline{\text{RD}}$ low before $\overline{\text{DMAGx}}$ low	t_{DGRDL}			01	-0.25	2.5	
				02	-0.5	2.5	
$\overline{\text{RD}}$ low before $\overline{\text{DMAGx}}$ high	t_{DRDGH}			01,02	11+9DT /16+W		
$\overline{\text{RD}}$ high before $\overline{\text{DMAGx}}$ high	t_{DGRDR}				0	3.5	
$\overline{\text{DMAGx}}$ high to $\overline{\text{WR}}$, $\overline{\text{RD}}$, DMAGx low	t_{DGWR}				4.5+3DT /8+HI		
Address/select valid to DMAGx high	t_{DADGH}				16+DT		
Address/select hold after DMAGx high	t_{DDGHA}				-1.5		
Link Ports: 1 times Clock Speed Operation, Receive Timing and Switching Requirements							
Data setup before LCLK low	t_{SLDCL}	See figure 4. 22/ 28/	9,10,11	01,02	3.5		ns
Data hold after LCLK low	t_{HLDCL}				3		
LCLK period (1 x operation)	t_{LCLKIW}				t_{CK}		
LCLK width low	$t_{LCLKRWL}$				6		
LCLK width high	$t_{LCLKRWH}$				5		
LACK high delay after CLKIN high	t_{DLAHC}				18+DT/2	29.5+DT/2	
LACK low delay after CLKIN high 47/	t_{DLALC}				-3	13.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Link Ports: 1 times Clock Speed Operation, Receive Timing and Switching Requirements - Continued.							
LACK enable from CLKIN	t_{ENDLK}	See figure 4. 22/ 28/	9,10,11	01,02	5+DT/2		ns
LACK disable from CLKIN	t_{TDLK}					21+DT/2	
Link Ports: 1 times Clock Speed Operation, Transmit Timing and Switching Requirements							
LACK setup before LCLK high	t_{SLACH}	See figure 4. 22/ 28/	9,10,11	01	18		ns
				02	19.25		
LACK hold after LCLK high	t_{HLACH}			01,02	-7		
LCLK delay after CLKIN (1 x operation)	t_{DLCLK}			01		16.5	
				02		17	
Data delay after LCLK high	t_{DLDCH}			01,02		3.5	
Data hold after LCLK high	t_{HLDCH}				-3		
LCLK width low	$t_{LCLKTWL}$			01	$(t_{CK}/2)-2$	$(t_{CK}/2)+2$	
				02	$(t_{CK}/2)-2$	$(t_{CK}/2)+2.25$	
LCLK width high	$t_{LCLKTWH}$			01	$(t_{CK}/2)-2$	$(t_{CK}/2)+2$	
				02	$(t_{CK}/2)-2.25$	$(t_{CK}/2)+2$	
LCLK low delay after LACK high	t_{DLACLK}			01	$(t_{CK}/2)$ +8.5	$(3*t_{CK}/2)$ +17.5	
				02	$(t_{CK}/2)$ +8.5	$(3*t_{CK}/2)$ +18.5	
LDAT, LCLK enable after CLKIN	t_{ENDLK}			01,02	5+DT/2		
LDAT, LCLK disable after CLKIN	t_{TDLK}					21+DT/2	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Link Port Service Request Interrupts: 1 times and 2 times Speed Operation Timing Requirements							
LACK/LCLK setup before CLKIN low 48/	t_{SLCK}	See figure 4. 22/ 28/	9,10,11	01,02	10		ns
LACK/LCLK hold after CLKIN low 48/	t_{HLCK}				2.5		
Link Ports: 2 times Clock Speed Operation, Receive Timing and Switching Requirements							
Data setup before LCLK low	t_{SLDCL}	See figure 4. 22/ 28/	9,10,11	01,02	2.75		ns
Data hold after LCLK low	t_{HLDCL}				2.25		
LCLK period (2 x operation)	t_{LCLKIW}				$t_{CK}/2$		
LCLK width low	$t_{LCLKRWL}$			01	4.6		
				02	4.7		
LCLK width high	$t_{LCLKRWH}$			01,02	4.25		
LACK high delay after CLKIN high	t_{DLAHC}				18+DT/2	31.5+DT/2	
LACK low delay after CLKIN high 47/	t_{DLALC}				6	17.8	
Link Ports: 2 times Clock Speed Operation, Transmit Timing and Switching Requirements							
LACK setup before LCLK high	t_{SLACH}	See figure 4. 22/ 28/	9,10,11	01	20.25		ns
				02	19.25		
LACK hold after LCLK high	t_{HLACH}			01,02	-6.5		
LCLK delay after CLKIN (2 x operation	t_{DLCLK}					9	
Data delay after LCLK high	t_{DLDCH}			01		3.25	
				02		3.35	
Data hold after LCLK high	t_{HLDCH}			01,02	-2		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Link Ports: 2 times Clock Speed Operation, Transmit Timing and Switching Requirements - Continued.							
LCLK width low	$t_{LCLKTWL}$	See figure 4. 22/ 28/	9,10,11	01,02	$(t_{CK}/4)-1$	$(t_{CK}/4)+1.5$	ns
LCLK width high	$t_{LCLKTWH}$				$(t_{CK}/4)-1.5$	$(t_{CK}/4)+1$	
LCLK low delay after LACK high	t_{DLACLK}				$(t_{CK}/4)+9$	$(3*t_{CK}/4)+17$	
Link data setup skew 49/	t_{SLSK}					0.45 50/	
Link data hold skew 51/	t_{HLSK}					3.35	
Serial Ports: External Clock Timing Requirements							
TFS/RFS setup before TCLK/RCLK 52/	t_{SFSE}	See figure 4. 22/ 28/	9,10,11	01,02	4		ns
TFS/RFS hold after TCLK/RCLK 52/ 53/	t_{HFSE}				4.5		
Receive data setup before RCLK 52/	t_{SDRE}				1.5		
Receive data hold after RCLK 52/	t_{HDRE}				4.5		
TCLK/RCLK width	t_{SCLKW}				9.5		
TCLK/RCLK period	t_{SCLK}				t_{CK}		
Serial Ports: Internal Clock Timing Requirements							
TFS setup before TCLK: RFS setup before RCLK 52/	t_{SFSI}	See figure 4. 22/ 28/	9,10,11	01,02	9.5		ns
TFS/RFS hold after TCLK/RCLK 52/ 53/	t_{HFSI}				1		
Receive data setup before RCLK 52/	t_{SDRI}				4.5		
Receive data hold after RCLK 52/	t_{HDRI}				3		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Serial Ports: External or Internal Clock Switching Requirements							
RFS delay after RCLK 54/ (internally generated RFS)	t_{DFSE}	See figure 4. 22/ 28/	9,10,11	01,02		14.5	ns
RFS hold after RCLK 54/ (internally generated RFS)	t_{HOFSE}				2.5		
Serial Ports: External Clock Switching Requirements							
TFS delay after TCLK 54/ (internally generated TFS)	t_{DFSE}	See figure 4. 22/ 28/	9,10,11	01,02		14.5	ns
TFS hold after TCLK 54/ (internally generated TFS)	t_{HOFSE}				3		
Transmit data delay after TCLK 54/	t_{DDTE}					17.5	
Transmit data hold after TCLK 54/	t_{HDTE}				5		
Serial Ports: Internal Clock Switching Requirements							
TFS delay after TCLK 54/ (internally generated TFS)	t_{DFSI}	See figure 4. 22/ 28/	9,10,11	01,02		5	ns
TFS hold after TCLK 54/ (internally generated TFS)	t_{HOFSI}				-1.5		
Transmit data delay after TCLK 54/	t_{DDTI}					7.5	
Transmit data hold after TCLK 54/	t_{HDTI}				-0.5		
TCLK/RCLK width	t_{SCLKIW}				(SCLK/2)-2	(SCLK/2)+2	
Serial Ports: Enable and Three State Switching Requirements							
Data enable from external TCLK 54/	t_{DDTEN}	See figure 4. 22/ 28/	9,10,11	01,02	3.5		ns
Data disable from external TCLK 54/	t_{DDTTE}					12	
Data enable from internal TCLK 54/	t_{DDTIN}				-0.5		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Serial Ports: Enable and Three State Switching Requirements - Continued.							
Data disable from internal TCLK 54/	t_{DDTTI}	See figure 4. 22/ 28/	9,10,11	01,02		3	ns
TCLK/RCLK delay from CLKIN	t_{DCLK}					23.5+3DT/8	
SPORT disable after CLKIN	t_{DPTR}					18.5	
Serial Ports: Gated SCLK with External TFS (Mesh Multiprocessing)							
TFS setup before CLKIN 55/	t_{STFSCK}	See figure 4. 22/ 28/	9,10,11	01	5.5		ns
				02	5.6		
TFS hold after CLKIN 55/	t_{HTFSCK}			01,02	$(t_{CK}/2)+0.5$		
Serial Ports: External Late Frame Sync Switching Requirements							
Data disable from late external TFS or RFS with MCE = 1, MFD = 0 56/	$t_{DDTLFSE}$	See figure 4. 22/ 28/	9,10,11	01,02		14.1	ns
Data enable from late FS or MCE = 1, MFD = 0 56/	$t_{DDTENFS}$				3		
JTAG Test Access Port Emulation Timing and Switching Requirements							
TCLK period	t_{TCK}	See figure 4. 22/ 28/	9,10,11	01,02	t_{CK}		ns
TDI, TMS, setup before TCK high	T_{STAP}				5		
TDI, TMS, hold after TCK high	T_{HTAP}				6		
Systems inputs setup before TCK low 57/	t_{SSYS}			01	7		
				02	8		
Systems inputs hold after TCK low 57/	t_{HSYS}			01,02	18.5		
$\overline{\text{TRST}}$ pulse width	t_{TRSTW}				$4t_{CK}$		
TDO delay from TCK low before TCK low	t_{DTDO}					13.5	
Systems outputs delay after TCK low 58/	t_{DSYS}					20	

See footnotes on next sheet.

TABLE I. Electrical performance characteristics - Continued.

1/ Device type 01, -40°C ≤ T_C ≤ +100°C and +4.75 V dc ≤ V_{DD} ≤ +5.25 V dc, unless otherwise specified.
Device type 02, -55°C ≤ T_C ≤ +125°C and +4.75 V dc ≤ V_{DD} ≤ +5.25 V dc, unless otherwise specified.

2/ Applies to input and bi-directional pins: DATA47-0, ADDR31-0, RD, WR, SW, ACK, SBTS, IRQy2-0, FLAGy0, FLAG1, FLAGy2, HBG, CSy, DMAR1, DMAR2, BR6-1, RPBA, CPAy, TFS0, TFSy1, RFS0, RFSy1, LyxDAT3-0, LyxCLK, LyxACK, EBOOTA, LBOOTA, EBOOTBCD, LBOOTBCD, BMSA, BMSBCD, TMS, TDI, TCK, HBR, DR0, DRy1, TCLK0, TCLKy1, RCLK0, RCLKy1. For the group of signals LyxDAT3-0, LyxCLK, and LyxACK, only Link Port 4 signals (Ly4DT3-0, Ly4CLK, and Ly4ACK) from each of the processors are tested at the module level. Link Ports 1, 2, and 3 are not DC tested at the module level, but are tested at the die level prior to assembly.

3/ Applies to input pins: CLKIN, RESET,TRST.

4/ Applies to output and bi-directional pins: DATA47-0, ADDR31-0, $\overline{MS3-0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, FLAGy0, FLAG1, FLAGy2, TIMEXPy, HBG, REDY, DMAG1, DMAG2, BR6-1, CPAy, DTO, DTy1, TCLK0, TCLKy1, RCLK0, RCLKy1, TFS0, TFSy1, RFS0, RFSy1, LyxDAT3-0, LyxCLK, LyxACK, BMSA, BMSBCD, TDO, EMU. For the group of signals LyxDAT3-0, LyxCLK, and LyxACK, only Link Port 4 signals (Ly4DAT3-0, Ly4CLK, and Ly4ACK) from each of the processors are tested at the module level. Link Ports 1, 2, and 3 are not DC tested at the module level, but are tested at the die level prior to assembly.

5/ See "output drive currents" for typical drive current capabilities.

6/ Applies to input pins: IRQy2-0, CSy, EBOOTA, LBOOTA.

7/ Applies to input pins with internal pull-ups: DRy1, TDI.

8/ Individual signals tested to limits of I_{IH} = 10 ∝A and I_{ILP} = 150 ∝A at die level prior to assembly. At the module level, all eight DR0 and DRy1 inputs connected together are tested to limits of I_{IH} = 80 ∝A and I_{ILP} = 1200 ∝A.

9/ Applies to bussed input pins: SBTS, HBR, DMAR1, DMAR2, RPBA, EBOOTBCD, LBOOTBCD, CLKIN, $\overline{RESET}$, TCK.

10/ Applies to bussed input pins with internal pull-ups: DR0, TRST, TMS.

11/ Applies to three statable pins and bi-directional pins; FLAGy0, FLAGy2, $\overline{BMSA}$, TDO, TFSy1, RFSy1. TFSy1 and RFSy1 are tested individually to the limits of I_{OZH} = 10 ∝A and I_{OZL} = 10 ∝A at die level. At the module level, eight pins connected together are tested to limits of I_{OZH} = 80 ∝A and I_{OZL} = 80 ∝A.

12/ Applies to three statable pins with internal pull-ups: DTy1, TCLKy1, RCLKy1. Individual signals tested to limit of I_{OZH} = 10 ∝A and I_{OZLS} = 150 ∝A at die level. At the module level, eight serial port pins connected together are tested to limits of I_{OZH} = 80 ∝A and I_{OZLS} = 1200 ∝A.

13/ Applies to ACK pin when pulled up. (Note that ACK is pulled up internally with a 2 kΩ resistor during reset in a multiprocessor system, when ID2-0 = 001 and another single processor is not requesting bus mastership.)

14/ Applies to CPAy pin.

15/ Applies to bussed three statable pins and bi-directional pins: DATA47-0, ADDR31-0, $\overline{MS3-0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, SW, ACK, FLAG1, HBG, REDY, DMAG1, DMAG2, BMSBCD, TFS0, RFS0, BR5, BR6, EMU. (Note that ACK is pulled up internally with a 2 kΩ resistor during reset in a multiprocessor system, when ID2-0 = 001 and another single processor is not requesting bus mastership.) HBG and EMU are not tested for leakage current. At the die level, component pins that make up TFS0 and RFS0 are tested to limits of I_{OZH} = 10 ∝A and I_{OZL} = 10 ∝A . At the module level, eight pins connected together are tested to limits of I_{OZL} = 80 ∝A and I_{OZL} = 80 ∝A.

16/ Applies to bussed three statable pins with internal pull-ups: DT0, TCLK0, RCLK0. At the module level, all eight DR0 and DRy1 inputs connected together are tested to limits of I_{OZH} = 80 ∝A and I_{OZLS} = 1200 ∝A.

17/ Applies to three statable pins with internal pull-downs: LyxDAT3-0, LyxCLK, LyxACK. Only Link Port 4 signals (Ly4DAT3-0, Ly4CLK, and Ly4ACK) from each of the processors are tested at the module level. Link Ports 1, 2, and 3 are not DC tested at the module level, but are tested at the die level prior to assembly.

18/ Applies to ACK pin when keeper latch enabled.

19/ Applies to V_{DD} pins. Conditions of operation: each processor executing radix-2 FFT butterfly with instruction in cache, one data operand fetched from cache each internal memory block, and one DMA transfer occurring from/to internal memory at t_{CK} = 25 ns. Total power dissipation has two components, one due to internal circuitry and one due to the switching of external output drivers: $P_{TOTAL} = P_{INT} + P_{EXT}$. Internal power dissipation is $P_{INT} = I_{DDIN} \times V_{DD}$. The external component of total power dissipation is caused by the switching of output pins, and depends on: the number of pins that switch each cycle (O), the maximum frequency at which they can switch (f), the load capacitance per pin (C), the output voltage swing (V_{DD}): $P_{EXT} = O \times C \times V_{DD}^2 \times f$. Address and data pins can switch at f = 1/ ($2t_{CK}$). WR can switch at 1/ t_{CK}. MSx pins switch at 1/ ($2t_{CK}$).

20/ Applies to V_{DD} pins. Idle denotes like device type state during execution of IDLE instruction.

21/ Not tested. Nominal value of 15 pF derived through RC measurement at design characterization.

22/ Timing test limits are target limits for the module, based on calculated predictions only. The module is 100% production tested, and the test limits are guaranteed by design/analysis, and characterization testing (at T_A = 25°C) of the individual discrete microcontrollers. The limits shown are based on a CLKIN frequency of 40 MHz. DT is the difference between the actual CLKIN period and a CLKIN period of 25 ns: DT = t_{CK} - 25 ns. Link and serial ports: all are 100% tested at die level, serial ports are 100% AC tested at module level, only Link Port 4 from each processor is AC tested at module level, then link and serial ports are DC tested at module level.

23/ Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 2000 CLKIN cycles while RESET is low, assuming stable V_{DD} and CLKIN (not including start-up time of external oscillator).

24/ Only required if multiple microcontrollers must come out of reset synchronous to CLKIN with program counters (PC) equal (i. e. for a SIMD system). Not required for multiple microcontrollers communicating over the shared bus (through the external port), because the bus arbitration logic synchronizes it self automatically after reset.

25/ Only required for IRQx recognition in the following cycle.

26/ Applies only if t_{SIR} and t_{HIR} requirements are not met.

27/ Flag inputs meeting these setup and hold times will affect conditional instructions in the following instruction cycle.

28/ W = (number of wait states specified in WAIT register) times t_{CK}. HI = t_{CK} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0). H = t_{CK} (if an address hold cycle occurs as specified in WAIT register; otherwise H = 0). I = t_{CK} (if bus idle cycle occurs, as specified in WAIT register; otherwise I = 0).

29/ Data delay/setup: User must meet t_{DAD} or t_{DRLD} or synchronous specification t_{SSDATI}.

30/ For MSx, SW, and BMS, the falling edge is referenced.

31/ Data hold: User must meet t_{HDA} or t_{HDRH} or synchronous specification t_{HDATI}. To determine system hold time, the data output hold time in a particular system, first calculate $t_{DECAY} = C_L \Delta V / I_L$. Choose ΔV to be the difference between the microcontroller's output voltage and the input threshold for the device requiring the hold. Typical ΔV is 0.4 volt. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (i. e. t_{HDWD} for the write cycle).

32/ ACK delay/setup: User must meet t_{DSAK} or t_{DAAK} or synchronous specification t_{SACKC}.

33/ To determine system hold time, the data output hold time in a particular system, first calculate $t_{DECAY} = C_L \Delta V / I_L$. Choose ΔV to be the difference between the microcontroller's output voltage and the input threshold for the device requiring the hold. Typical ΔV is 0.4 volt. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (i. e. t_{HDWD} for the write cycle).

34/ t_{SRWLI} (min) = 9.5 + 5DT/16, when multiprocessor memory space wait state (MMSWS bit in WAIT register) is disabled; when MMSWS is enabled, t_{SRWLI} (min) = 4 + DT/8.

35/ t_{DACKAD} is true only if the address and SW inputs have setup times (before CLKIN) greater than 10.5 + DT/8 and less than 18.5 + 3DT/4. If the address and SW inputs have setup times greater than 19 + 3DT/4, then ACK is valid 15 + DT/4 (max) after CLKIN. A slave that sees an address with a M field match will respond with ACK regardless of the state of MMSWS or strobes. A slave will three state ACK every cycle with t_{ACKTR}.

36/ For first asynchronous access after HBR and CS asserted, ADDR31-0 must be a non-MMS value 1/2t_{CK} before $\overline{RD}$ or WR goes low or by $t_{HBGRCSV}$ after HBG goes low. This is easily accomplished by driving an upper address signal high when HBG is asserted.

37/ Only required for recognition in the current cycle.

38/ CPA assertion must meet the setup to CLKIN; deassertion does not need to meet the setup to CLKIN.

39/ (O/D) = open drain, (A/D) = active drain.

40/ Not required if RD and address are valid $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. For first access after $\overline{HBR}$ asserted, ADDR31-0 must be a non-MMS value 1/2t_{CK} before RD or WR goes low or by $t_{HBGRCSV}$ after HBG goes low. This is easily accomplished by driving an upper address signal high when HBG is asserted. For address bits to be driven during asynchronous host accesses, see QML manufacturer.

41/ Strobes = RD, WR, SW, PAGE, and DMAG.

42/ In addition to bus master transition cycles, these specifications also apply to bus master and bus slave synchronous read/write.

43/ Memory interface = Address, $\overline{RD}$, $\overline{WR}$, $\overline{MSx}$, $\overline{SW}$, $\overline{HBG}$, PAGE, $\overline{DMAGx}$, and $\overline{BMS}$ (in EPROM boot mode).

44/ Only required for recognition in the current cycle.
45/ $t_{SDATDGL}$ is the data setup requirement if DMARx is not being used to hold off completion of a write. Otherwise, if $\overline{DMARx}$ low holds off completion of the write, the data can be driven t_{DATDRH} after $\overline{DMARx}$ is brought high.
46/ $t_{VDATDGH}$ is valid if DMARx is not being used to hold off completion of a read. If DMARx is used to prolong the read, then $t_{VDATDGH} = 7.5 + 9DT/16 + (n * t_{ck})$ where "n" equals the number of extra cycles that the access is prolonged.
47/ LACK will go low with t_{DLALC} relative to rising edge of LCLK after first nibble is received. LACK will not go low if the receivers link buffer is not about to fill.
48/ Only required for interrupt recognition in the current cycle.
49/ t_{SLSK} is the maximum delay that can be introduced in the transmission path of LDATA relative LCLK:
$t_{SLSK} = (t_{LCLKTWH} - t_{DLDCH})min - t_{SLDCL}$ max.
50/ If link port 2 is transmitter, $t_{SLSK} = 0.28$ ns. Because of this small margin, extreme care must be taken in system design. If adequate setup time cannot be assured, link port operation should be limited to 1X, or system CLKIN frequency should be reduced to increase the setup margin at 2X.
51/ t_{HLSK} is the maximum delay that can be introduced in the transmission path of LCLK relative to LDATA:
$t_{HLSK} = (t_{LCLKTWL} - t_{HLDCH})min - t_{HLDCL}$ max.
52/ Reference to sample edge.
53/ RFS hold after RCK when MCE = 1, MFD = 0 is 0.5 ns minimum from drive edge. TFS hold after TCK for late external TFS is 0.5 ns minimum from drive edge.
54/ Reference to drive edge.
55/ Applies only to gated serial clock mode used for serial port system I/O in mesh multiprocessing systems.
56/ MCE = 1, TFS enable and TFS valid follow $t_{DDTLFSE}$ and $t_{DDTENFS}$.
57/ System inputs = DATA47-0, ADDR31-0, RD, WR, ACK, SBTS, SW, HBR, HBG, CS, DMAR1, DMAR2, BR6-1, RPBA, IRQ2-0, FLAG2,0, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, LxDAT3-0, LxCLK, LxACK, EBOOT, LBOOT, BMS, CLKIN, RESET.
58/ System outputs = DATA47-0, ADDR31-0, MS3-0, RD, WR, ACK, PAGE, ADRCLK, SW, HBG, REDY, DMAG1, DMAG2, BR6-1, CPA, FLAG2,0, TIMEXP, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, LxDAT3-0, LxCLK, LxACK, BMS.

Case outline X.

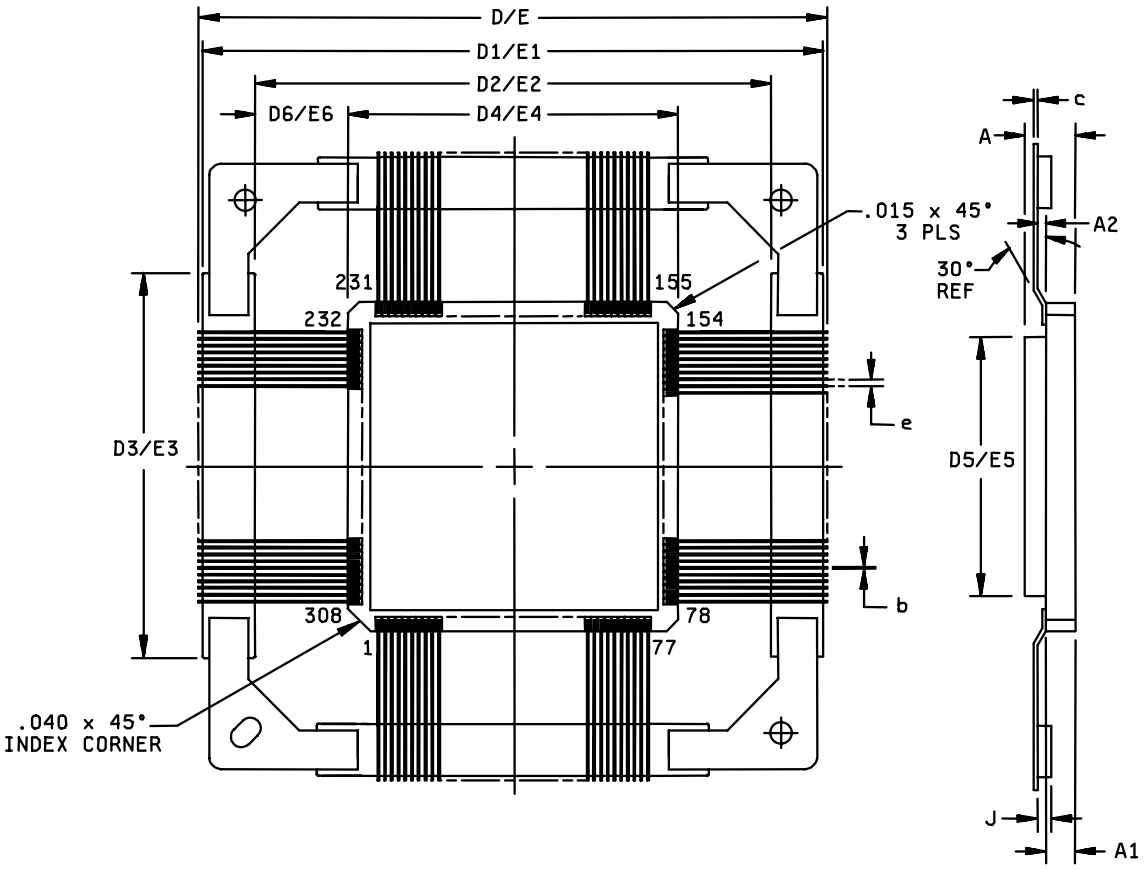


FIGURE 1. Case outline(s).

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-97506
DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000		REVISION LEVEL C	SHEET 25

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		4.06		.160
A1	2.11	2.57	.083	.101
A2	0.08	0.33	.003	.013
b	0.15	0.25	.006	.010
c	0.10	0.17	.004	.0065
D/E		77.47		3.050
D1/E1	75.95	76.45	2.990	3.010
D2/E2	68.96	69.72	2.715	2.745
D3/E3	57.66	59.18	2.270	2.330
D4/E4	51.77	52.37	2.038	2.062
D5/E5	47.88	48.13	1.885	1.895
D6/E6	8.38	8.89	.330	.350
e	0.64 BSC		.025 BSC	
J		0.89		.035

NOTES:

1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.

FIGURE 1. Case outline(s) - Continued.

Device types	01 and 02						
Case outline	X						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$\overline{WR}$	45	GND	89	ADDR13	133	$\overline{IRQ}$B0
2	$\overline{RD}$	46	RFSD1	90	ADDR12	134	$\overline{IRQ}$B1
3	GND	47	RCLKD1	91	ADDR11	135	$\overline{IRQ}$B2
4	$\overline{CSA}$	48	DRD1	92	GND	136	GND
5	$\overline{CSB}$	49	TFSD1	93	ADDR10	137	$\overline{IRQ}$C0
6	$\overline{CSC}$	50	TCLKD1	94	ADDR9	138	$\overline{IRQ}$C1
7	$\overline{CSD}$	51	DTD1	95	ADDR8	139	$\overline{IRQ}$C2
8	GND	52	V_{DD}	96	V_{DD}	140	$\overline{IRQ}$D0
9	HBG	53	$\overline{HBR}$	97	ADDR7	141	$\overline{IRQ}$D1
10	REDY	54	$\overline{DMAR}$1	98	ADDR6	142	$\overline{IRQ}$D2
11	ADRCLK	55	$\overline{DMAR}$2	99	ADDR5	143	V_{DD}
12	V_{DD}	56	$\overline{SBTS}$	100	GND	144	EBOOTA
13	RFS0	57	$\overline{BMSA}$	101	ADDR4	145	LBOOTA
14	RCLK0	58	BM$\overline{SB}$CD	102	ADDR3	146	EBOOTBCD
15	DR0	59	$\overline{SW}$	103	ADDR2	147	LBOOTBCD
16	TFS0	60	GND	104	V_{DD}	148	GND
17	TCLK0	61	$\overline{MS}$0	105	ADDR1	149	$\overline{RESET}$
18	DT0	62	$\overline{MS}$1	106	ADDR0	150	RPBA
19	GND	63	$\overline{MS}$2	107	FLAGA0	151	GND
20	CPAA	64	$\overline{MS}$3	108	GND	152	LD4ACK
21	CPAB	65	V_{DD}	109	FLAGA2	153	LD4CLK
22	CPAC	66	ADDR31	110	FLAGB0	154	LD4DAT0
23	CPAD	67	ADDR30	111	FLAGB2	155	LD4DAT1
24	V_{DD}	68	ADDR29	112	FLAGC0	156	LD4DAT2
25	RFSA1	69	GND	113	FLAGC2	157	LD4DAT3
26	RCLKA1	70	ADDR28	114	FLAGD0	158	V_{DD}
27	DRA1	71	ADDR27	115	FLAGD2	159	LD3ACK
28	TFSA1	72	ADDR26	116	V_{DD}	160	LD3CLK
29	TCLKA1	73	V_{DD}	117	F$\overline{LAG}$1	161	LD3DAT0
30	DTA1	74	ADDR25	118	$\overline{EMU}$	162	LD3DAT1
31	GND	75	ADDR24	119	TIMEXPA	163	LD3DAT2
32	RFSB1	76	ADDR23	120	TIMEXPB	164	LD3DAT3
33	RCLKB1	77	ADDR22	121	TIMEXPC	165	GND
34	DRB1	78	ADDR21	122	TIMEXPD	166	LD1ACK
35	TFSB1	79	ADDR20	123	GND	167	LD1CLK
36	TCLKB1	80	V_{DD}	124	$\overline{TDO}$	168	LD1DAT0
37	DTB1	81	ADDR19	125	$\overline{TRST}$	169	LD1DAT1
38	V_{DD}	82	ADDR18	126	TDI	170	LD1DAT2
39	RFSC1	83	ADDR17	127	TMS	171	LD1DAT3
40	RCLKC1	84	GND	128	TCK	172	V_{DD}
41	DRC1	85	ADDR16	129	$\overline{V_{DD}}$	173	LC4ACK
42	TFSC1	86	ADDR15	130	$\overline{IRQ}$A0	174	LC4CLK
43	TCLKC1	87	ADDR14	131	$\overline{IRQ}$A1	175	LC4DAT0
44	DTC1	88	V_{DD}	132	IRQA2	176	LC4DAT1

FIGURE 2. Terminal connections.

Device types	01 and 02				
Case outline	X				
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
177	LC4DAT2	221	GND	265	GND
178	LC4DAT3	222	LA3ACK	266	DATA24
179	GND	223	LA3CLK	267	DATA25
180	LC3ACK	224	LA3DAT0	268	DATA26
181	LC3CLK	225	LA3DAT1	269	DATA27
182	LC3DAT0	226	LA3DAT2	270	V_{DD}
183	LC3DAT1	227	LA3DAT3	271	DATA28
184	LC3DAT2	228	V_{DD}	272	DATA29
185	LC3DAT3	229	LA1ACK	273	DATA30
186	V_{DD}	230	LA1CLK	274	DATA31
187	LC1ACK	231	LA1DAT0	275	GND
188	LC1CLK	232	LA1DAT1	276	DATA32
189	LC1DAT0	233	LA1DAT2	277	DATA33
190	LC1DAT1	234	LA1DAT3	278	DATA34
191	LC1DAT2	235	GND	279	DATA35
192	LC1DAT3	236	DATA0	280	V_{DD}
193	GND	237	DATA1	281	DATA36
194	LB4ACK	238	DATA2	282	DATA37
195	LB4CLK	239	DATA3	283	DATA38
196	LB4DAT0	240	V_{DD}	284	DATA39
197	LB4DAT1	241	DATA4	285	GND
198	LB4DAT2	242	DATA5	286	DATA40
199	LB4DAT3	243	DATA6	287	DATA41
200	V_{DD}	244	DATA7	288	CLKIN
201	LB3ACK	245	GND	289	GND
202	LB3CLK	246	DATA8	290	DATA42
203	LB3DAT0	247	DATA9	291	DATA43
204	LB3DAT1	248	DATA10	292	V_{DD}
205	LB3DAT2	249	DATA11	293	DATA44
206	LB3DAT3	250	V_{DD}	294	DATA45
207	GND	251	DATA12	295	DATA46
208	LB1ACK	252	DATA13	296	DATA47
209	LB1CLK	253	DATA14	297	$\overline{\text{GND}}$
210	LB1DAT0	254	DATA15	298	$\overline{\text{BR1}}$
211	LB1DAT1	255	GND	299	$\overline{\text{BR2}}$
212	LB1DAT2	256	DATA16	300	$\overline{\text{BR3}}$
213	LB1DAT3	257	DATA17	301	$\overline{\text{BR4}}$
214	V_{DD}	258	DATA18	302	$\overline{\text{BR5}}$
215	LA4ACK	259	DATA19	303	BR6
216	LA4CLK	260	V_{DD}	304	PAGE
217	LA4DAT0	261	DATA20	305	$\overline{V_{DD}}$
218	LA4DAT1	262	DATA21	306	$\overline{\text{DMAG1}}$
219	LA4DAT2	263	DATA22	307	DMAG2
220	LA4DAT3	264	DATA23	308	ACK

FIGURE 2. Terminal connections - Continued.

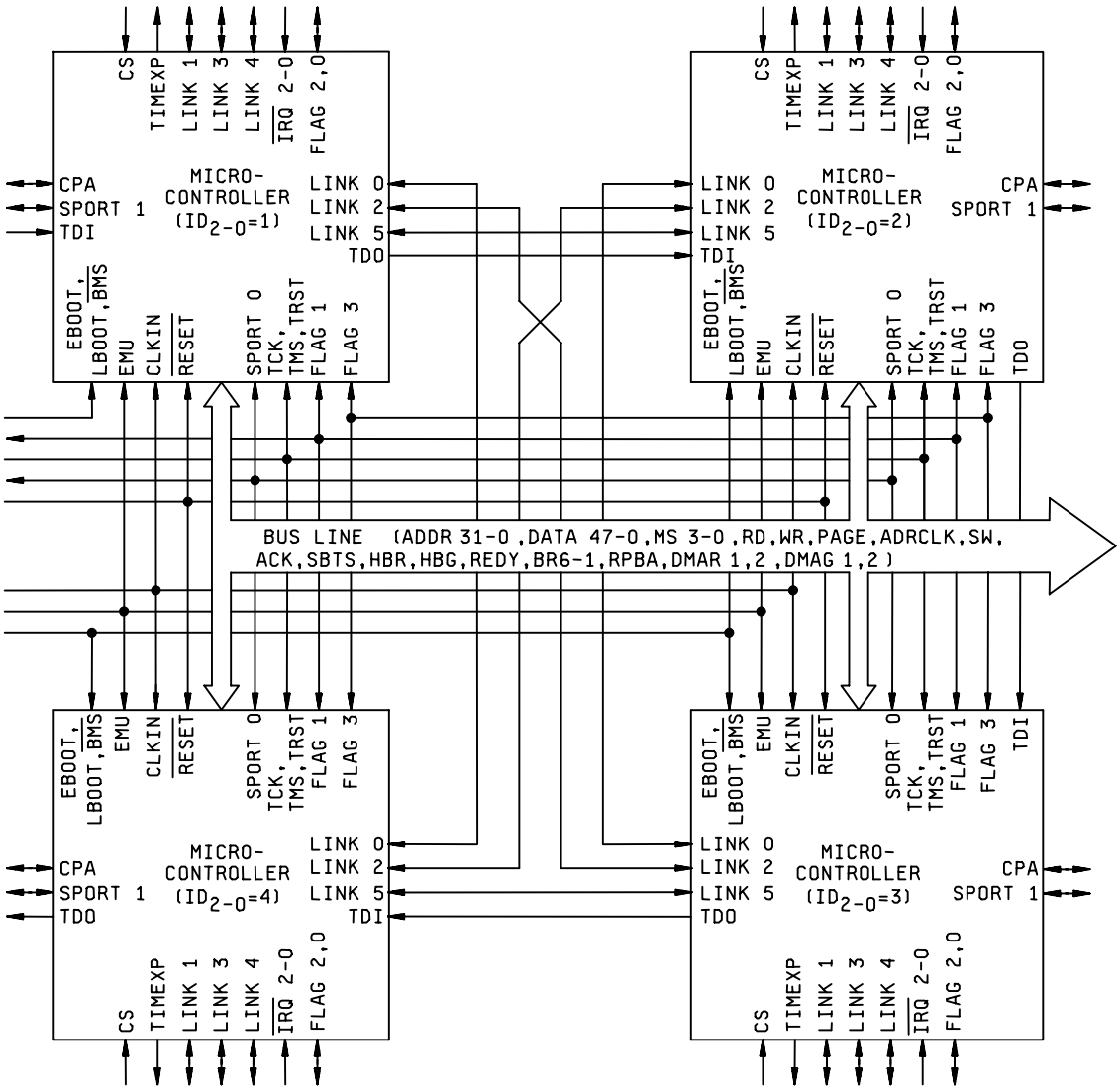


FIGURE 3. Block diagram.

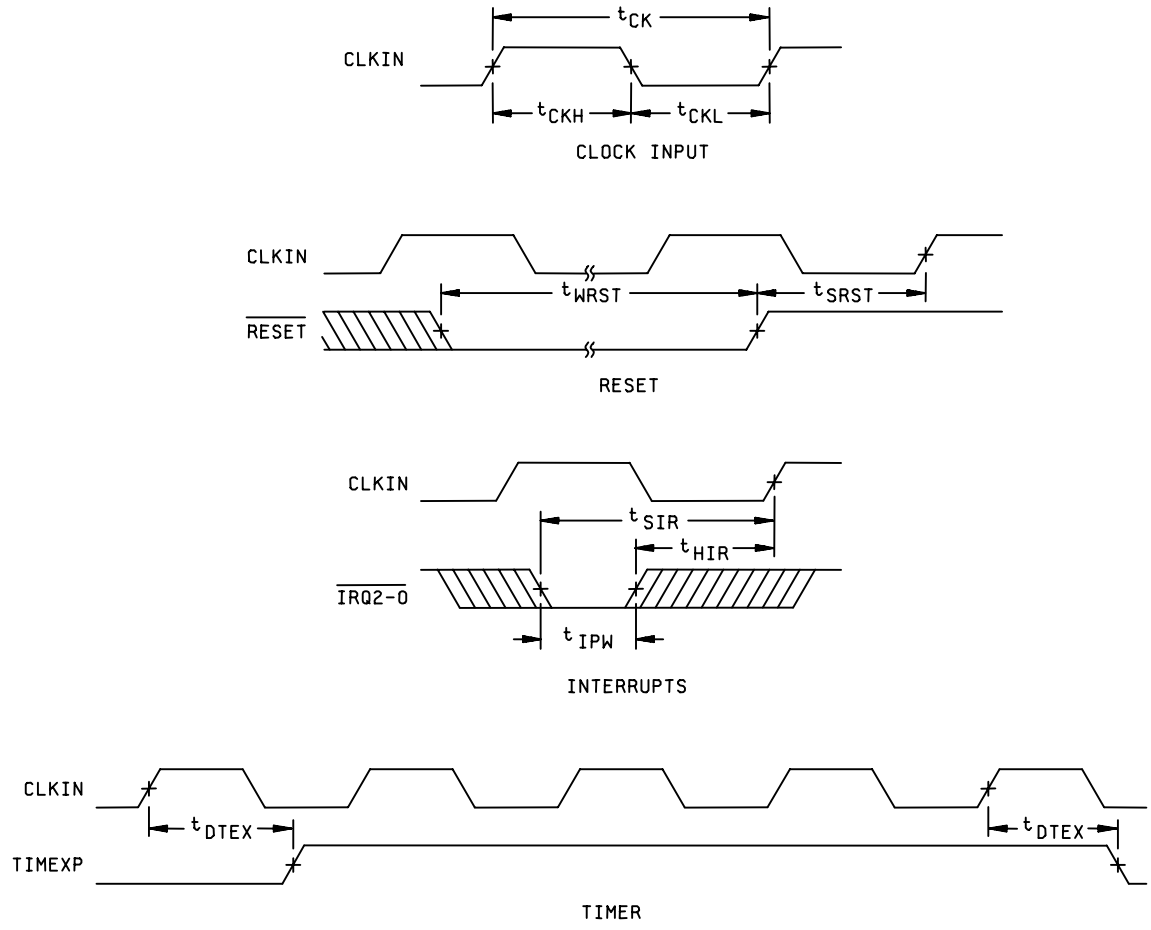
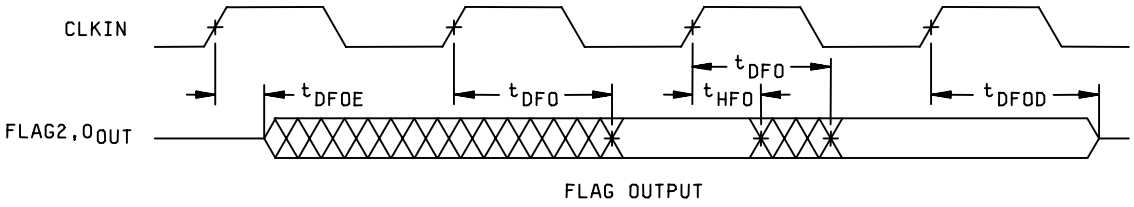
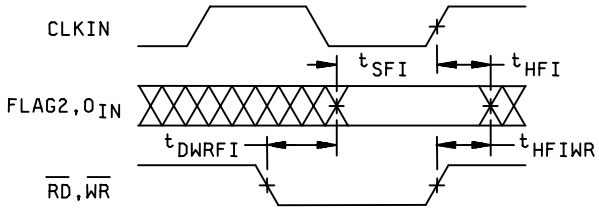


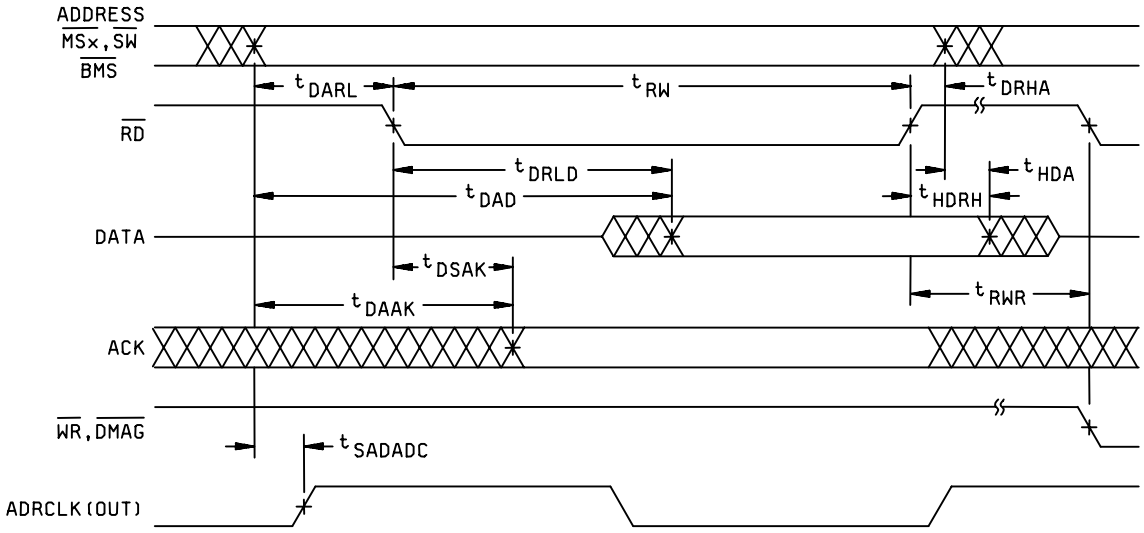
FIGURE 4. Timing waveforms.



FLAG OUTPUT

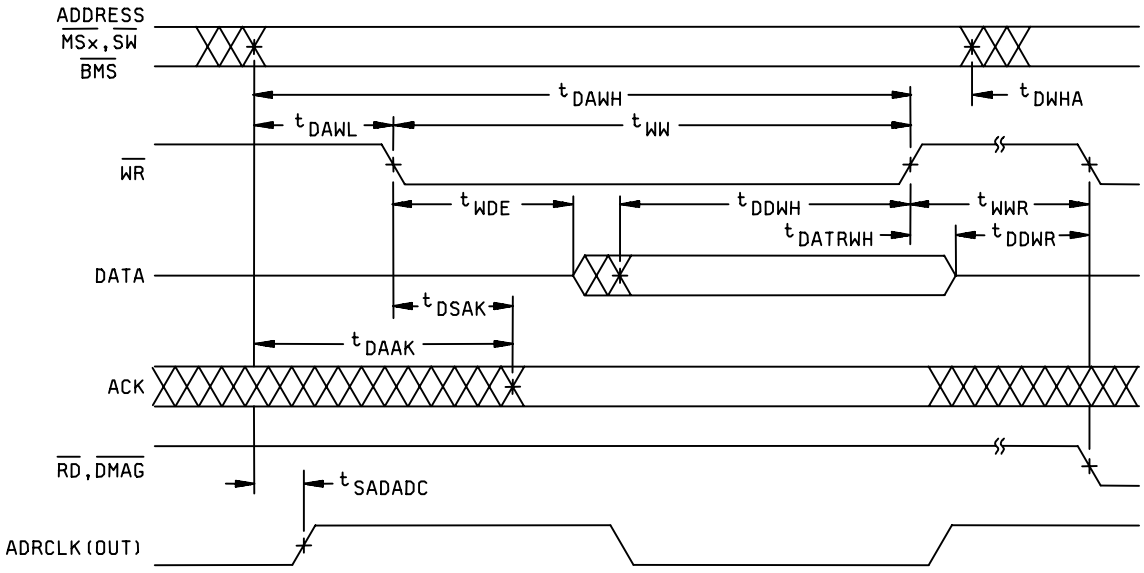


FLAG INPUT



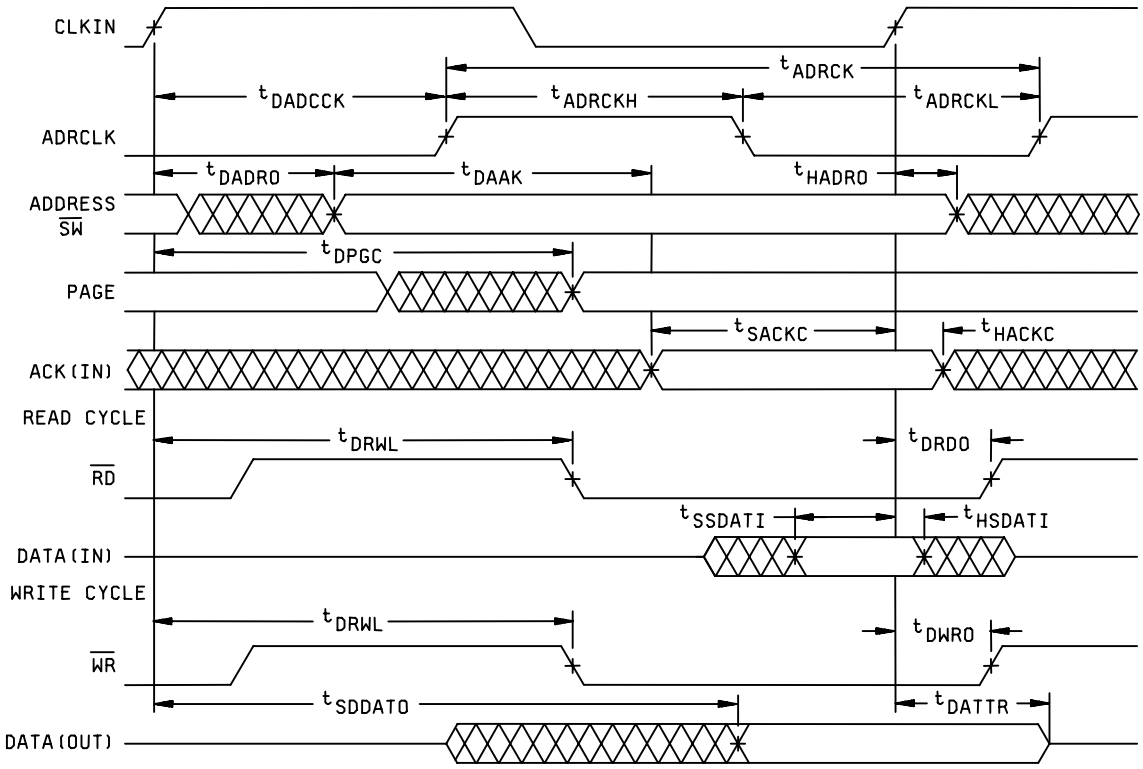
MEMORY READ - BUS MASTER

FIGURE 4. Timing waveforms - Continued.



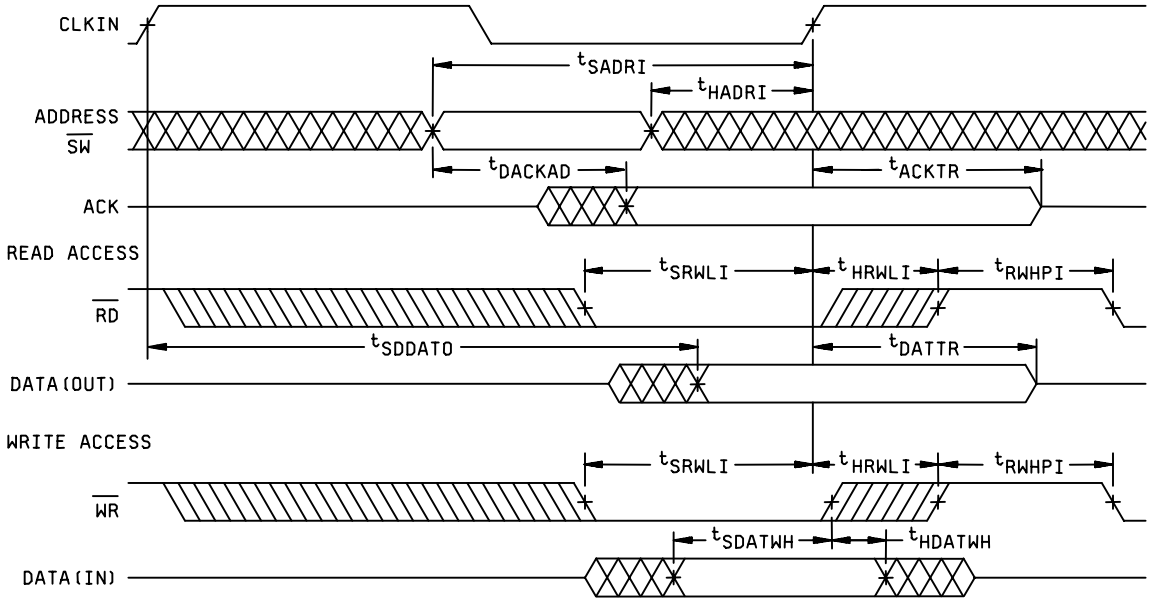
MEMORY WRITE - BUS MASTER

FIGURE 4. Timing waveforms - Continued.



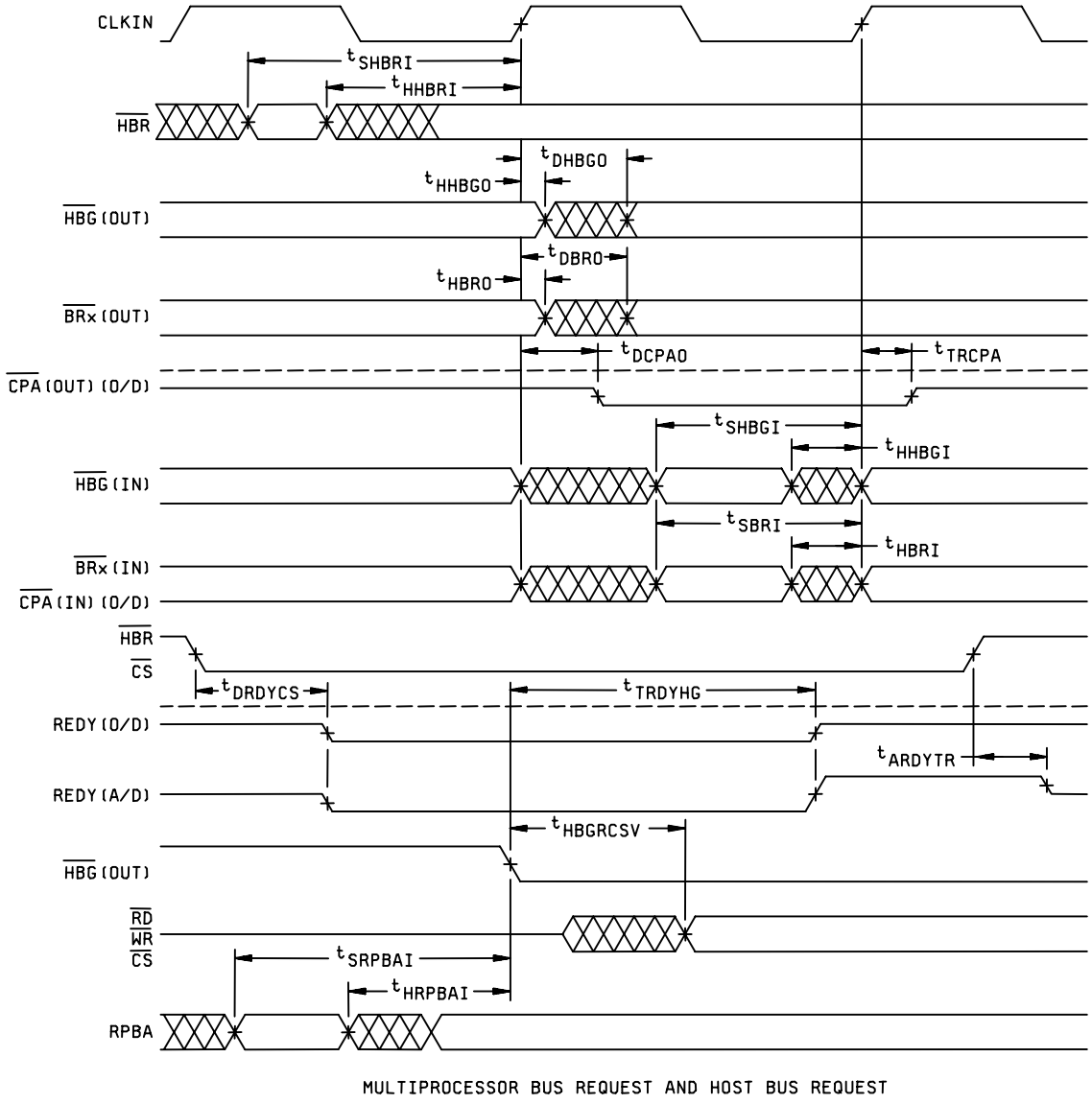
SYNCHRONOUS READ/WRITE - BUS MASTER

FIGURE 4. Timing waveforms - Continued.



SYNCHRONOUS READ/WRITE - BUS SLAVE

FIGURE 4. Timing waveforms - Continued.



MULTIPROCESSOR BUS REQUEST AND HOST BUS REQUEST

FIGURE 4. Timing waveforms - Continued.

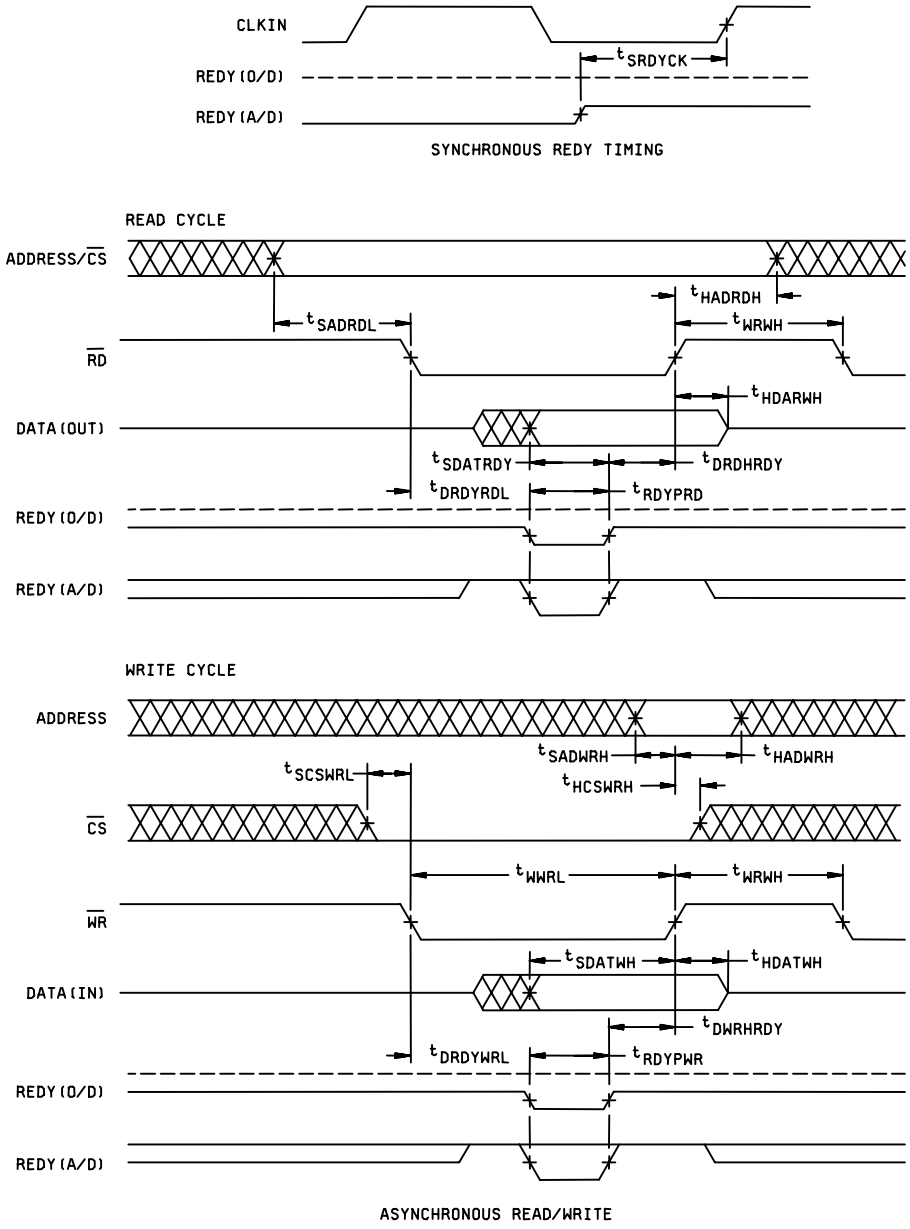


FIGURE 4. Timing waveforms - Continued.

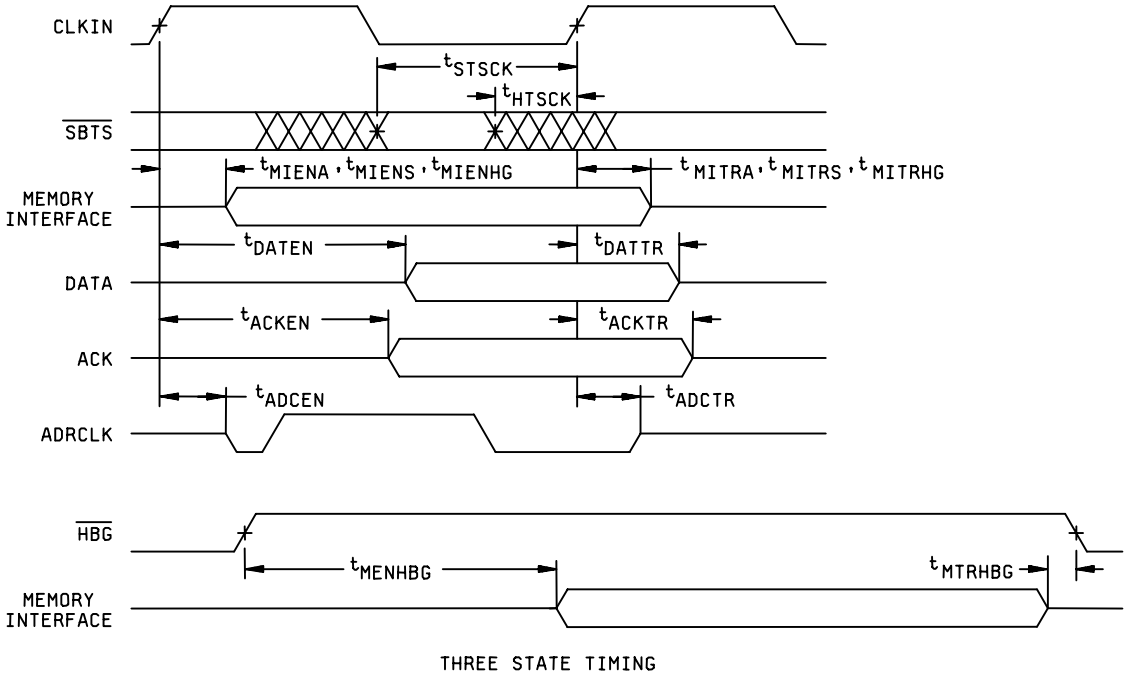
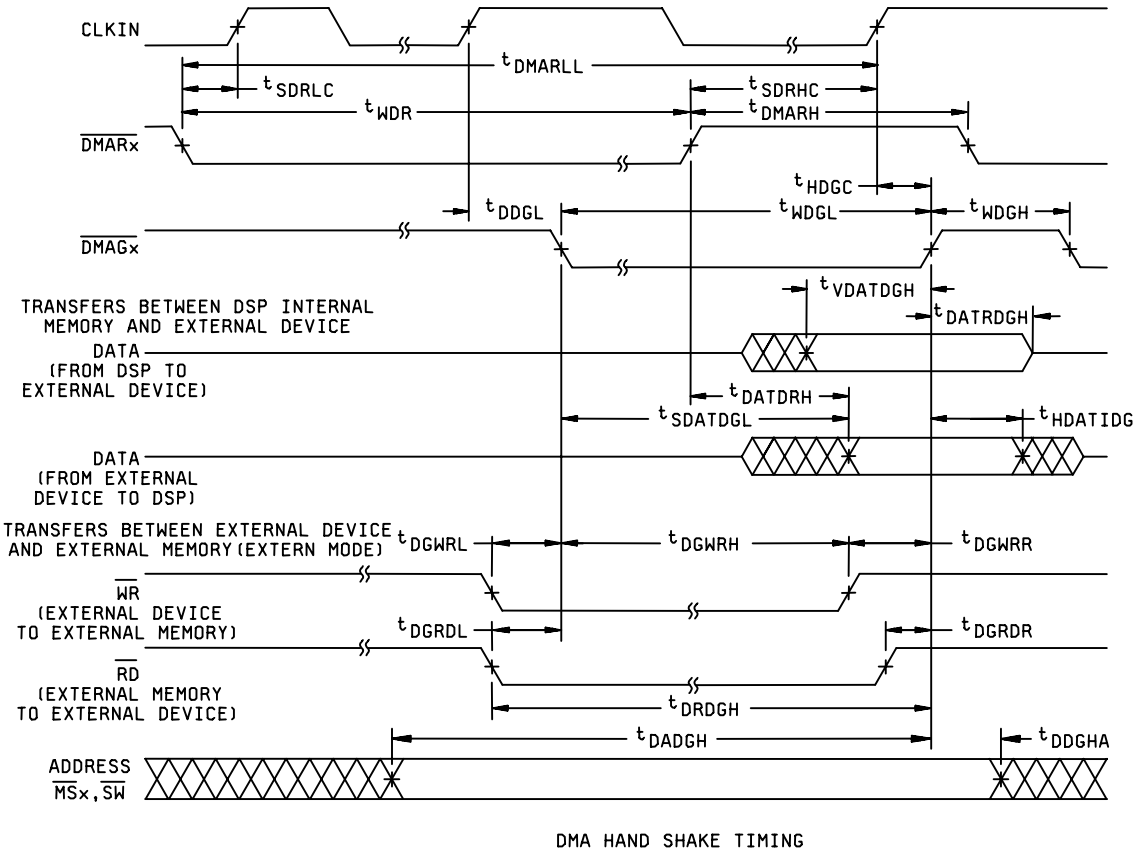


FIGURE 4. Timing waveforms - Continued.



DMA HAND SHAKE TIMING

FIGURE 4. Timing waveforms - Continued.

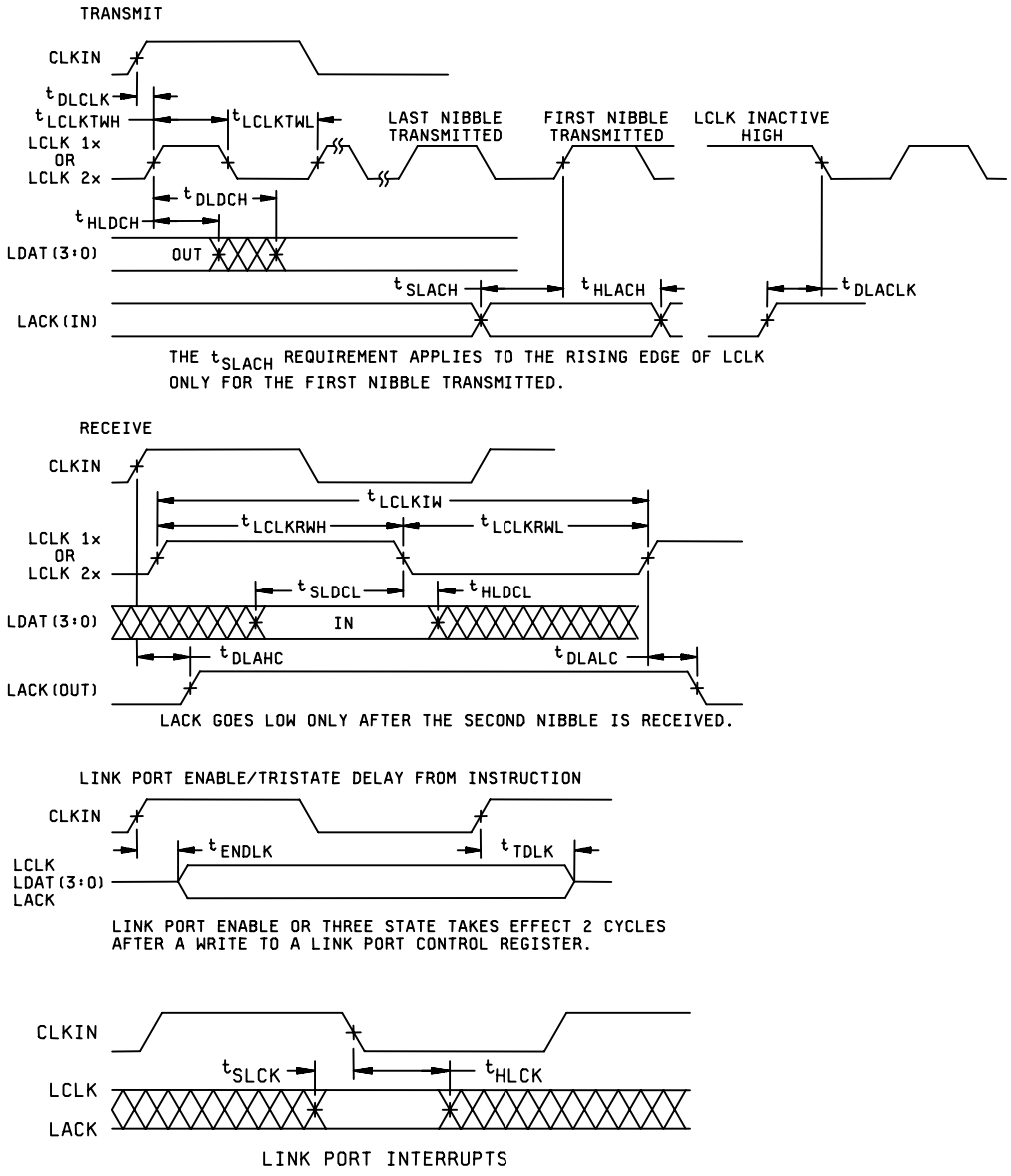
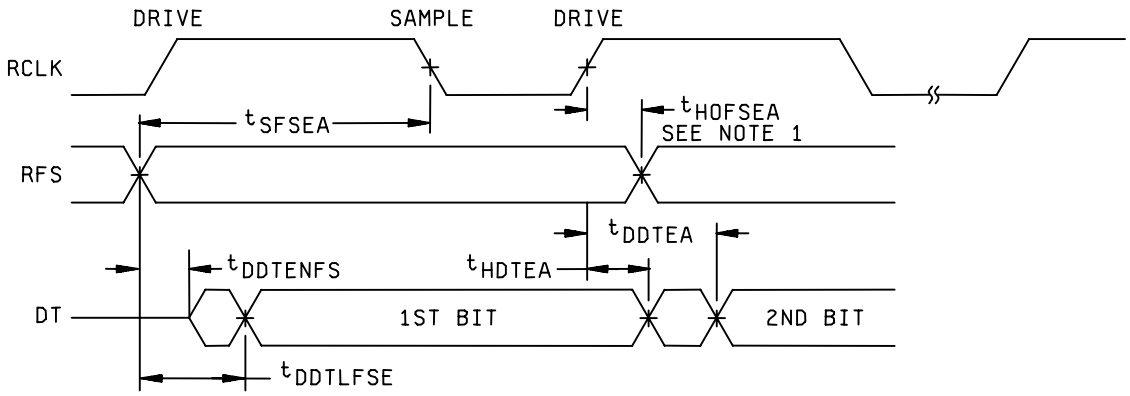
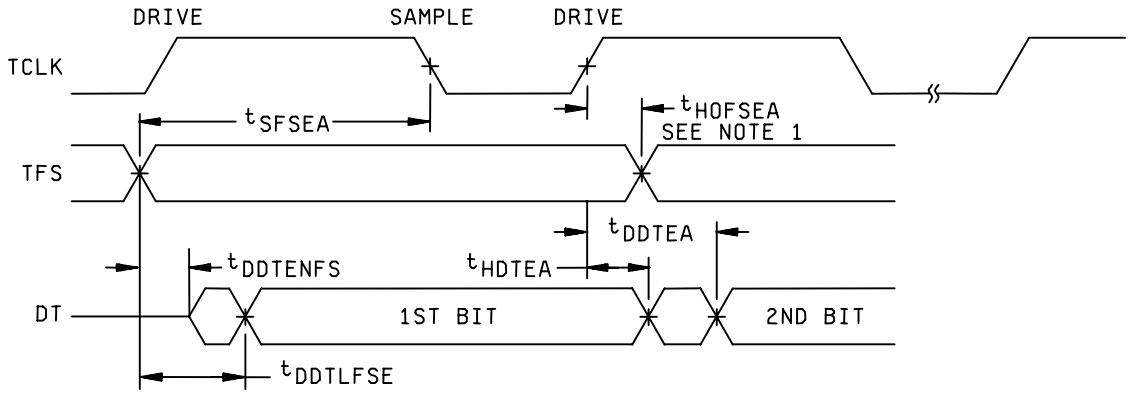


FIGURE 4. Timing waveforms - Continued.

EXTERNAL RFS WITH MCE = 1, MFD = 0



LATE EXTERNAL TFS



EXTERNAL LATE FRAME SYNC

NOTE:
1. RFS hold after RCLK when MCS = 1, MFD = 0 is 0.5 ns minimum from drive edge. TFS hold after TCLK for late external TFS is 0.5 ns minimum from drive edge.

FIGURE 4. Timing waveforms - Continued.

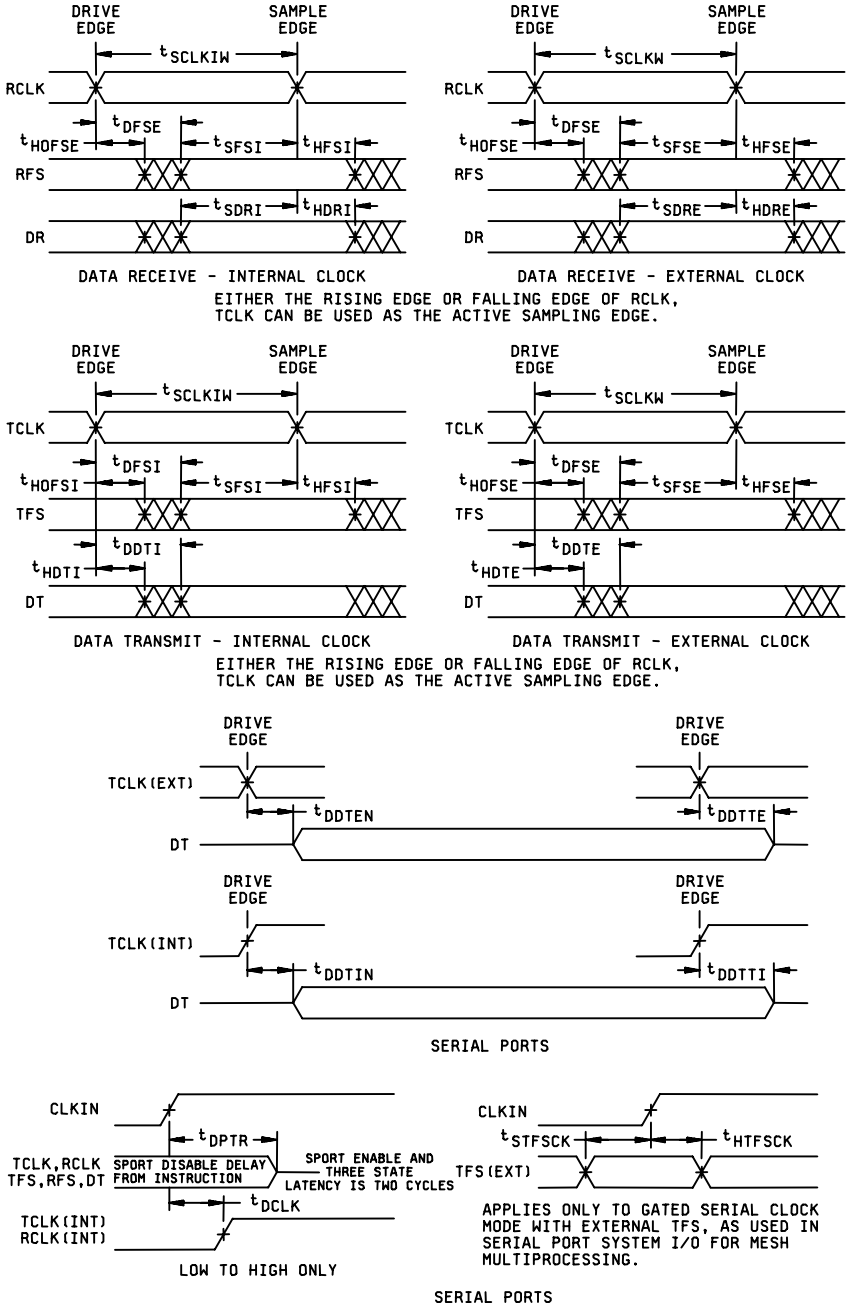


FIGURE 4. Timing waveforms - Continued.

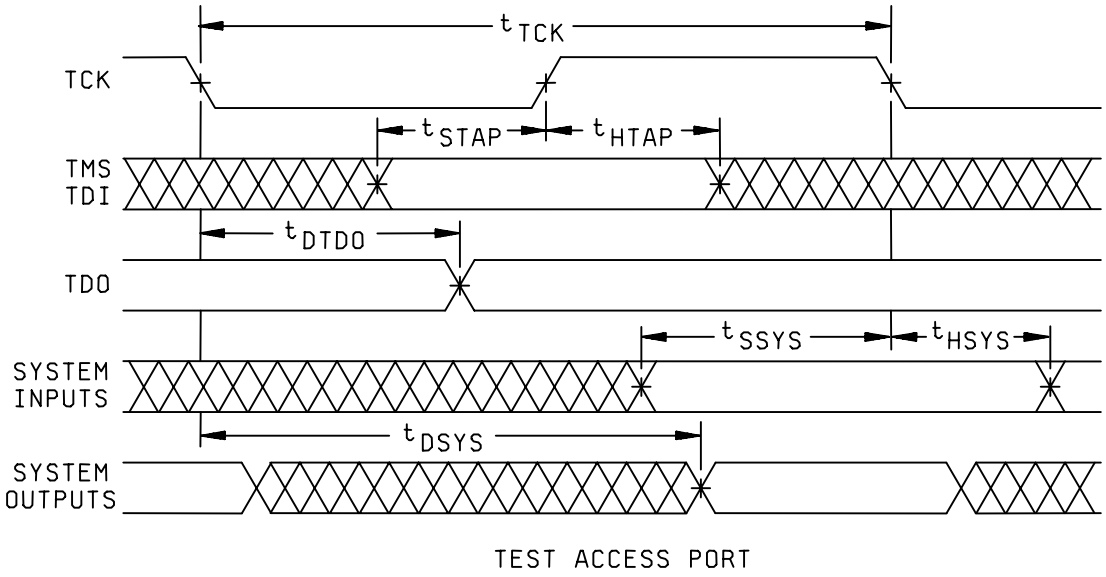
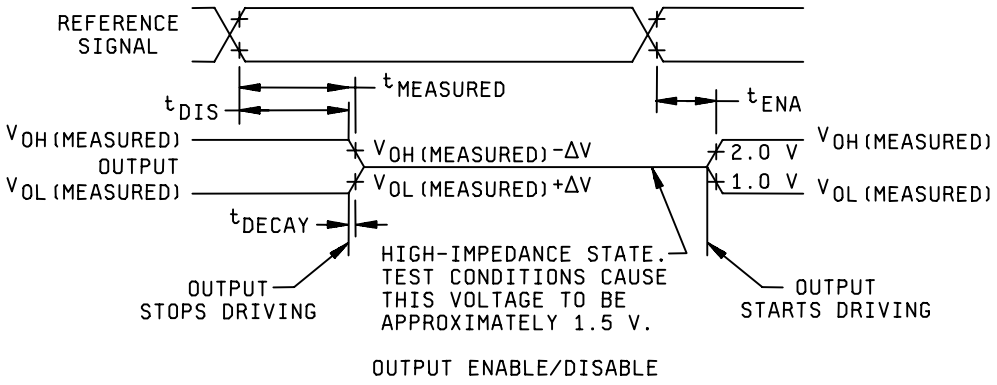
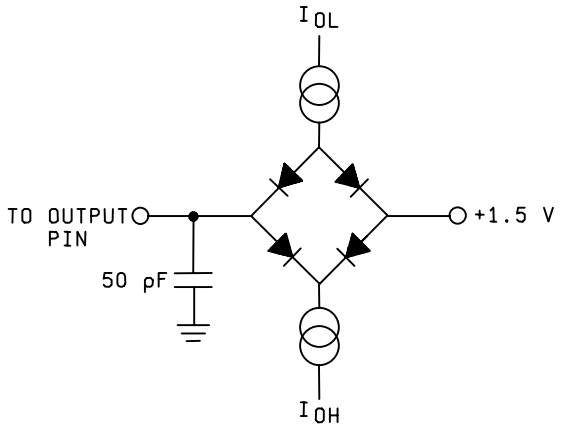


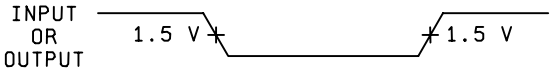
FIGURE 4. Timing waveforms - Continued.



OUTPUT ENABLE/DISABLE



EQUIVALENT DEVICE LOADING
FOR AC MEASUREMENTS
(INCLUDES ALL FIXTURES)



VOLTAGE REFERENCE LEVELS
FOR AC MEASUREMENTS
(EXCEPT OUTPUT ENABLE/DISABLE)

FIGURE 4. Timing waveforms - Continued.

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	Paragraph 4.2.b
Final electrical parameters	Paragraph 4.2.b*, 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements	1, 2, 3, 7, 8, 9, 10, 11
Group C end-point electrical parameters	1, 7, 9
End-point electrical parameters for radiation hardness assurance (RHA) devices	Not applicable

* PDA applies to subgroup 1.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the functionality of the device.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_C as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Radiation Hardness Assurance (RHA) inspection. RHA inspection is not currently applicable to this drawing.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-PRF-38534.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Post Office Box 3990, Columbus, Ohio 43216-5000, or telephone (614) 692-0536.

6.6 Sources of supply. Sources of supply are listed in MIL-HDBK-103 and QML-38534. The vendors listed in MIL-HDBK-103 and QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

TABLE III. Pin functions.

Terminal symbol	Type 1/	Function
ADDR31-0	I/O/T	External Bus Address. (Common to all processors). The module outputs addresses for external memory and peripherals on these pins. In a multiprocessor system, the bus master outputs addresses for read/writes on the internal memory or IOP registers of slave processors. The module inputs addresses when a host processor or multiprocessing bus master is reading or writing the internal memory or IOP registers of internal processors.
DATA47-0	I/O/T	External Bus DATA. (Common to all processors). The module inputs and outputs data and instructions on these pins. 32-bit single-precision floating-point data and 32-bit fixed-point data is transferred over bits 47 - 16 of the bus. 40-bit extended-precision floating-point data is transferred over bits 47 - 8 of the bus. 16-bit short word data is transferred over bits 31 - 16 of the bus. In PROM boot mode, 8-bit data is transferred over bits 23 - 16. Pull-up resistors on unused DATA pins are not necessary.
$\overline{\text{MS3-0}}$	O/T	Memory Select Lines. (Common to all processors). These lines are asserted (low) as chip selects for the corresponding banks of external memory. Memory bank size must be defined in the individual processors system control registers (SYSCON). The MS3-0 lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the MS3-0 lines are inactive; they are active, however, when a conditional memory access instruction is executed, whether or not the condition is true. MS0 can be used with the PAGE signal to implement a bank of DRAM memory (Bank 0). In multiprocessing system, the MS3-0 lines are output by the bus master.
$\overline{\text{RD}}$	I/O/T	Memory Read Strobe. (Common to all processors). This pin is asserted (low) when the processor reads from external devices or when the internal memory of internal processors is being accessed. External devices (including other processors) must assert RD to read from the processors internal memory. In a multiprocessing system, RD is output by the bus master and is input by all other processors.
$\overline{\text{WR}}$	I/O/T	Memory Write Strobe. (Common to all processors). This pin is asserted (low) when the processor writes from external devices or when the internal memory of internal processors is being accessed. External devices (including other processors) must assert WR to write from the processors internal memory. In a multiprocessing system, WR is output by the bus master and is input by all other processors.
PAGE	O/T	DRAM Page Boundary. (Common to all processors). The module asserts this pin to signal that an external DRAM page boundary has been crossed. DRAM page size must be defined in the individual processor's memory control register (WAIT). DRAM can only be implemented in external memory Bank 0; the PAGE signal can only be activated for Bank 0 accesses. In a multiprocessing system, PAGE is output by the bus master.
ADRCLK	O/T	Clock Output Reference. (Common to all processors). In a multiprocessing system, ADRCLK is output by the bus master.
$\overline{\text{SW}}$	I/O/T	Synchronous Write Select. (Common to all processors). This signal is used to interface the processor to synchronous memory devices (including other processors). The module asserts SW (low) to provide an early indication of an impending write cycle, which can be aborted if WR is not later asserted (e.g. in a conditional write instruction). In a multiprocessing system, SW is output by the bus master and is input by all other processors to determine if the multiprocessor memory access is a read or write. SW is asserted at the same time as the address output. A host processor using synchronous writes must assert this pin when writing to module.

See footnotes at end of table.

TABLE III. Pin functions - Continued.

Terminal symbol	Type 1/	Function
ACK	I/O/S	Memory Acknowledge. (Common to all processors). External devices can deassert ACK (low) to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access. The module deasserts ACK, as an output, to add wait states to a synchronous access of its internal memory. In a multiprocessing system, a slave processor deasserts the bus master's ACK input to add wait state(s) to an access of its internal memory. The bus master has a keeper latch on its ACK pin that maintains the input at the level it was last driven to.
$\overline{\text{SBTS}}$	I/S	Suspend Bus Three State. (Common to all processors). External devices can assert SBTS (low) to place the external bus address, data, selects, and strobes in a high impedance state for the following cycle. If the module attempts to access external memory while SBTS is asserted, the processor will halt and the memory access will not be completed until SBTS is deasserted. SBTS should only be used to recover from the host processor/ the module deadlock, or used with a DRAM controller.
$\overline{\text{HBR}}$	I/A	Host Bus Request. (Common to all processors). Must be asserted by a host processor to request control of the module's external bus. When HBR is asserted in a multiprocessor system, the processor that is bus master will relinquish the bus and assert HBG. To relinquish the bus, the processor places the address, data, select, and strobe lines in a high impedance state. HBR has priority over all processor bus requests (BR 6-1) in a multiprocessing system.
$\overline{\text{HBG}}$	I/O	Host Bus Grant. (Common to all processors). Acknowledges an $\overline{\text{HBR}}$ bus request, indicating that the host processor may take control of the external bus. HBG is asserted (held low) by the module until $\overline{\text{HBR}}$ is released. In a multiprocessing system, HBG is output by the processor bus master and is monitored by all others.
$\overline{\text{CSA}}$	I/A	Chip Select. Asserted by host processor to select processor-A.
$\overline{\text{CSB}}$	I/A	Chip Select. Asserted by host processor to select processor-B.
$\overline{\text{CSC}}$	I/A	Chip Select. Asserted by host processor to select processor-C.
$\overline{\text{CSD}}$	I/A	Chip Select. Asserted by host processor to select processor-D.
REDY (O/D)	O	Host Bus Acknowledge. (Common to all processors). The module deasserts REDY (low) to add wait states to an asynchronous access of its internal memory or IOP registers by a host. Open drain output (O/D) by default; can be programmed in ADREDY bit of SYSON register of individual processors to be active drive (A/D). REDY will only be output if the $\overline{\text{CS}}$ and $\overline{\text{HBR}}$ inputs are asserted.
$\overline{\text{BR6-1}}$	I/O/S	Multiprocessing Bus Requests. (Common to all processor). Used by multiprocessing processors to arbitrate for bus mastership. A processor only drives its own BRx line (corresponding to the value of its ID2-0 inputs) and monitors all others. In a multiprocessing system with less than six processors the unused BRx pins should be pulled high; BR4-1 must not be pulled high or low because they are outputs.

See footnotes at end of table.

TABLE III. Pin functions - Continued.

Terminal symbol	Type 1/	Function
RPBA	I/S	Rotating Priority Bus Arbitration Select. (Common to all processors). When RPBA is high, rotating priority for multiprocessor bus arbitration is selected. When RPBA is low, fixed priority is selected. This signal is a system configuration selection that must be set to the same value on every processor. If the value of RPBA is changed during system operation, it must be changed in the same CLKIN cycle on every processor.
$\overline{\text{CPA}}$y (O/D)	I/O	Core Priority Access (y=processor-A, -B, -C, -D). Asserting its $\overline{\text{CPA}}$ pin allows the core processor of a bus slave to interrupt background DMA transfers and gain access to the external bus. CPA is an open drain output that is connected to all processors in the system, if this function is required. The $\overline{\text{CPA}}$ pin of each internal processor is brought out individually. The CPA pin has an internal 5 kohm pull-up resistor. If core access priority is not required in a system, the CPA pin should be left unconnected.
DT0	O/T	Data Transmit (Common serial ports 0 to all processors, TDM). DT pin has four parallel 50 kohm internal pull-up resistors.
DR0	I	Data Receive (Common serial ports 0 to all processors, TDM). DR pin has four parallel 50 kohm internal pull-up resistors.
TCLK0	I/O	Transmit Clock (Common serial ports 0 to all processors, TDM). TCLK pin has four parallel 50 kohm internal pull-up resistors.
RCLK0	I/O	Receiver Clock (Common serial ports 0 to all processors, TDM). RCLK pin has four parallel 50 kohm internal pull-up resistors.
TFS0	I/O	Transmit Frame Sync (Common serial ports 0 to all processors, TDM).
RFS0	I/O	Receiver Frame Sync (Common serial ports 0 to all processors, TDM).
DTy1	O/T	Data Transmit (Serial port 1 individual from processor-A, -B, -C, -D). Each DT pin has a 50 kohm internal pull-up resistor.
DRy1	I	Data Receive (Serial port 1 individual from processor-A, -B, -C, -D). Each DR pin has a 50 kohm internal pull-up resistor.
TCLKy1	I/O	Transmit Clock (Serial port 1 individual from processor-A, -B, -C, -D). Each TCLK pin has a 50 kohm internal pull-up resistor.
RCLKy1	I/O	Receive Clock (Serial port 1 individual from processor-A, -B, -C, -D). Each RCLK pin has a 50 kohm internal pull-up resistor.
TFSy1	I/O	Transmit Frame Sync (Serial port 1 individual from processor-A, -B, -C, -D).
RFSy1	I/O	Receive Frame Sync (Serial port 1 individual from processor-A, -B, -C, -D).
FLAGy0	I/O/A	Flag Pins, 2/. (FLAG0 individual from processor-A, -B, -C, -D). Each is configured via control bits as either an input or output. As an input, it can be tested as a condition. As an output, it can be used to signal external peripherals.

See footnotes at end of table.

TABLE III. Pin functions - Continued.

Terminal symbol	Type 1/	Function
FLAG1	I/O/A	Flag Pins, 2/. (FLAG1 common to all processors). Configured by control bits internal to individual processors as either an input or output. As an input it can be tested as a condition. As an output, it can be used to signal external peripherals.
FLAGy2	I/O/A	FLAG Pins, 2/. (FLAG2 individual from processor-A, -B, -C, and -D). Each is configured by control bits as either an input or output. As an input, it can be tested as a condition. As an output, it can be used to signal external peripherals.
$\overline{\text{IRQy2-0}}$	I/A	Interrupt Request Lines. (Individual $\overline{\text{IRQ}}$2-0 from y = processor-A, -B, -C, -D). May be either edge-triggered or level-sensitive.
$\overline{\text{DMAR1}}$	I/A	DMA Request 1 (DMA Channel 7). Common to processor-A, -B, -C, -D.
$\overline{\text{DMAR2}}$	I/A	DMA Request 1 (DMA Channel 8). Common to processor-A, -B, -C, -D.
$\overline{\text{DMAG1}}$	O/T	DMA Grant 1 (DMA Channel 7). Common to processor-A, -B, -C, -D.
$\overline{\text{DMAG2}}$	O/T	DMA Grant 2 (DMA Channel 8). Common to processor-A, -B, -C, -D.
LyxCLK	I/O	Link Port Clock (y = processor-A, -B, -C, -D; x = Link Ports 1, 3, 4), 3/. Each LyxCLK pin has a 50 kohm internal pull-up resistor which is enabled or disabled by the LPDRD bit of the LCOM register, of the processor.
LyxDAT3-0	I/O	Link Port Data (y = processor-A, -B, -C, -D; x = Link Ports 1, 3, 4), 3/. Each LyxDAT pin has a 50 kohm internal pull-up resistor which is enabled or disabled by the LPDRD bit of the LCOM register, of the processor.
LyxACK	I/O	Link Port Acknowledge (y = processor-A, -B, -C, -D; x = Link Ports 1, 3, 4), 3/. Each LyxACK pin has a 50 kohm internal pull-up resistor which is enabled or disabled by the LPDRD bit of the LCOM register, of the processor.
$\overline{\text{BMSA}}$	I/O/T 4/	Boot Memory Select. Output: Used as chip select for boot EPROM devices (when EBOOTA = 1, LBOOTA = 0). In a multiprocessor system, BMS is output by the bus master. Input: When low, indicates that no booting will occur and that processor-A will begin executing instructions from external memory. See table in note 4. This input is a system configuration selection which should be hardwired.
EBOOTA	I	EPROM Boot Select. (processor-A) When EBOOTA is high, processor-A is configured for booting from an 8-bit EPROM. When EBOOTA is low, the LBOOTA and BMSA inputs determine booting mode for processor-A. See table in note 4. This signal is a configuration selection which should be hardwired.
LBOOTA	I	Link Boot. When LBOOTA is high, processor-A is configured for link port booting. When LBOOTA is low, processor-A is configured for host processor booting or no booting. See table in note 4. This signal is a system configuration selection which should be hardwired.

See footnotes at end of table.

TABLE III. Pin functions - Continued.

Terminal symbol	Type 1/	Function
EBOOTBCD	I	EPROM Boot Select. (Common to processor-B, -C, -D). When EBOOTBCD is high, processor-B, -C, -D are configured for booting from an 8-bit EPROM. When EBOOTBCD is low, the LBOOTBCD and BMSBCD inputs determine booting mode for processor-B, -C, and -D. See table in note 4. This signal is a system configuration selection which should be hardwired.
LBOOTBCD	I	LINK Boot. (Common to processor-B, -C, -D). When LBOOTBCD is high, processor-B, -C, -D are configured for link port booting. When LBOOTBCD is low, multiprocessor-B, -C, -D are configured for host processor booting or no booting. See table in note 4. This signal is a system configuration selection which should be hardwired.
$\overline{\text{BMSBCD}}$	I/O/T 4/	Boot Memory Select. Output: Used as chip select for boot EPROM devices (when EBOOTBCD = 1, LBOOTBCD = 0). In a multiprocessor system, BMS is output by the bus master. Input: When low, indicates that no booting will occur and that processor-B, -C, -D will begin executing instructions from external memory. See table in note 4. This input is a system configuration selection which should be hardwired.
TIMEXPy	O	Timer Expired. (Individual TIMEXP from y = processor-A, -B, -C, -D). Asserted for four cycles when the timer is enabled and t_{count} decrements to zero.
CLKIN	I	Clock In. (Common to all processors). External clock input to the module. The instruction cycle rate is equal to CLKIN. CLKIN may not be halted, changed, or operated below the minimum specified frequency.
$\overline{\text{RESET}}$	I/A	Module Reset. (Common to all processors). Resets the module to a known state. This input must be asserted (low) at power-up.
TCK	I	Test Clock (JTAG). (Common to all processors). Provides an asynchronous clock for JTAG boundary scan.
TMS	I/S	Test Mode Select (JTAG). (Common to all processors). Used to control the test state machine. TMS has four parallel 20 kohm internal pull-up resistors.
TDI	I/S	Test Data Input (JTAG). Provides serial data for the boundary scan logic chain starting at processor-A. TDI has a 20 kohm pull-up resistor.
TDO	O	Test Data Output (JTAG). Serial scan output of the boundary scan chain path, from processor-D.
$\overline{\text{TRST}}$	I/A	Test Reset (JTAG). Common to all processors). Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the module. TRST has four parallel 20 kohm internal pull-up resistors.
$\overline{\text{EMU}}$(O/D)	O	Emulation Status. (Common to all processors). Pin 118 must be connected to the module's target board test connector only.
V_{DD}	P	Power Supply. Nominally +5.0 V dc (26 pins).
GND	G	Power supply returns. The lid to the module is electrically connected to GND.

See footnotes on the following sheet.

TABLE III. Pin functions - Continued.

NOTES:

1/ Type: A = asynchronous, A/D = active drive, G = ground, I = input, O = output, O/D= open drain, P = power supply, S = synchronous, T = three state (when $\overline{\text{SBTS}}$ is asserted, or when the module is a bus slave).

Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN(or to TCK forTRST).

Unused inputs should be tied or pulled to VDD or GND, except for ADDR31-0, DATA47-0, FLAG2,0, $\overline{\text{SW}}$, and inputs that have internal pull-up or pull-down resistors (CPA, ACK, DTx, DTy, TCLKx, RCLKx, LxDAT3-0, LxCLK, LxACK, TMS, and TDI) - these pins can be left floating. These pins have a logic-level hold circuit that prevents the input from floating internally.

ID pins are hardwired internally.

2/ FLAG3 is connected internally, common to processor-A, -B, -C, and -D.

3/ LINK PORTS 0, 2, and 5 are connected internally between processors -A, -B, -C, and -D.

4/ Three statable only in EPROM boot mode (when $\overline{\text{BMS}}$ is an output).

EBOOT	LBOOT	$\overline{\text{BMS}}$	Booting Mode
1	0	output	EPROM (connect $\overline{\text{BMS}}$ to EPROM chip select)
0	0	1 (input)	Host processor
0	1	1 (input)	Link port
0	0	0 (input)	No booting. Processor executes from external memory.
0	1	0 (input)	Reserved
1	1	x (input)	Reserved

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 03-03-31

Approved sources of supply for SMD 5962-97506 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38534 during the next revisions. MIL-HDBK-103 and QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38534.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9750601HXC	34031	AD14060BF/QML-4
5962-9750602HXC	34031	AD14060TF/QML-4

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34031	Analog Devices, Incorporated 7910 Triad Center Drive Greensboro, NC 27409-9605 Point of contact: Assembled Products Division