MIC44F18/19/20

6A, 12.6V High Speed MOSFET Drivers with Enable Input

Features

- 4.5V to 12.6V Input Operating Range
- 6A Peak Output Current
- High Accuracy ±5% Enable Input Threshold
- High Speed Switching Capability
  - 10 ns Rise Time in 1000 pF Load
  - <15 ns Propagation Delay Time
- Flexible UVLO Function
  - 4.2V Internally Set UVLO
  - Programmable with External Resistors
- Latch-Up Protection to >500 mA Reverse Current on the Output Pin
- Enable Function
- Thermally Enhanced ePAD MSOP-8 Package Option
- Miniature 2 mm x 2 mm DFN-8 Package Option
- Pb-Free Packaging

Applications

- Synchronous Switch-Mode Power Supplies
- Secondary Side Synchronous Rectification

General Description

The MIC44F18, MIC44F19, and MIC44F20 are high-speed single MOSFET drivers capable of sinking and sourcing 6A for driving capacitive loads. With delay times of less than 15 ns and rise times into a 1000 pF load of 10 ns, these MOSFET drivers are ideal for driving large gate charge MOSFETs in power supply applications. The MIC44F18 is a non-inverting driver, the MIC44F19 is an inverting driver suited for driving P-Channel MOSFETs, and the MIC44F20 is an inverting driver for N-Channel MOSFETs.

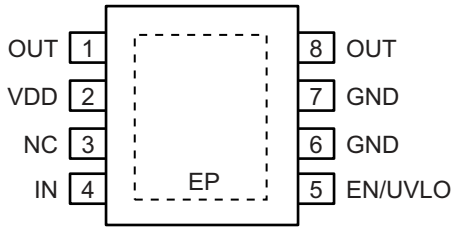
Fabricated using proprietary BiCMOS/DMOS process for low power consumption and high efficiency, the MIC44F18/19/20 translates TTL or CMOS input logic levels to output voltage levels that swing within 25 mV of the positive supply or ground. Comparable bipolar devices are capable of swinging only to within 1V of the supply.

The input supply voltage range of the MIC44F18/19/20 is 4.5V to 12.6V, making the devices suitable for driving MOSFETs in a wide range of power applications. Other features include an enable function, latch-up protection, and a programmable UVLO function.

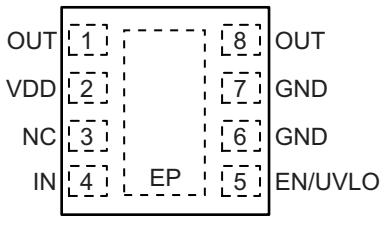
The MIC44F18/19/20 has a junction temperature range of –40°C to +125°C with exposed pad ePAD MSOP-8 and 2 mm x 2 mm DFN-8 package options.

Package Types

8-Pin ePAD MSOP (MME)



8-Pin 2 mm x 2 mm DFN (ML)



Please see pin descriptions in Table 3-1.

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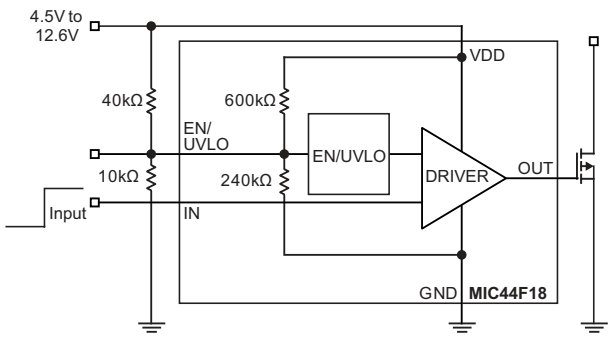
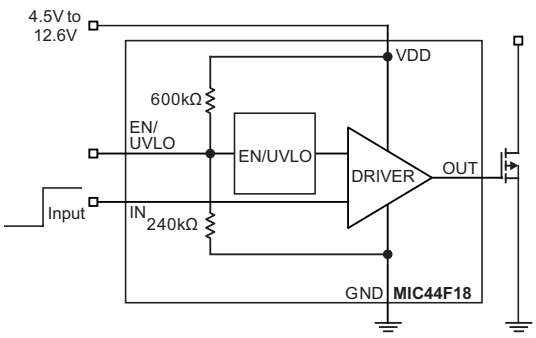
Typical Application Circuits

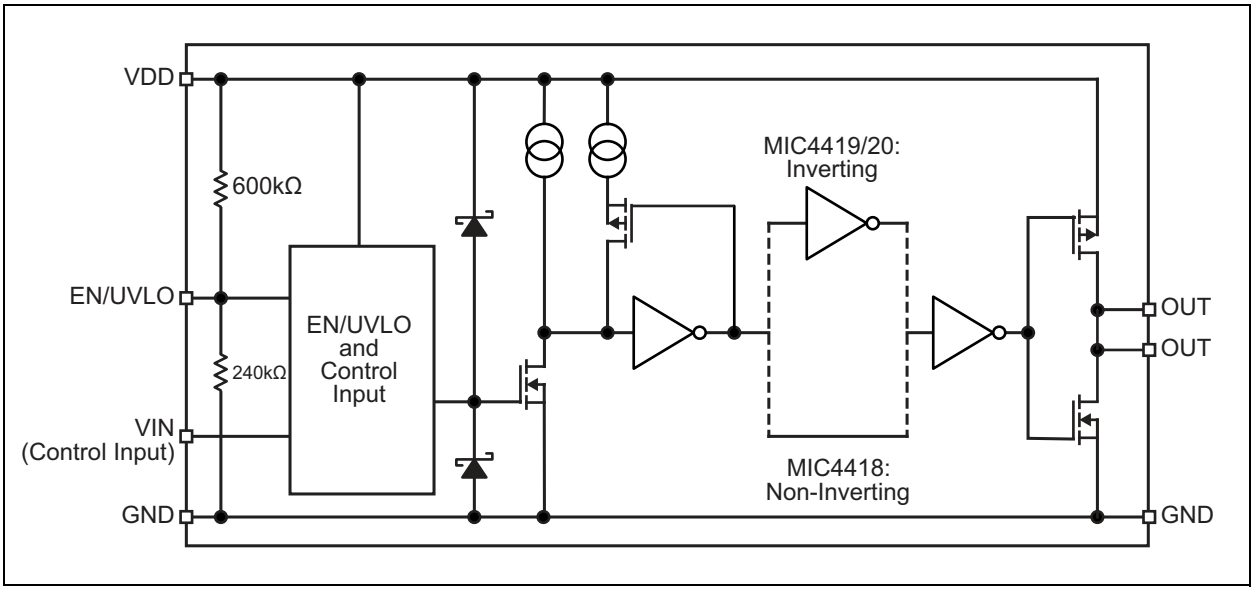
MOSFET Driver with 6.2V UVLO Externally Set



MOSFET Driver with 4.2V UVLO Internally Set



Functional Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{DD}) ..... +13V
UVLO/Enable Voltage ($V_{UVLO/EN}$) ..... +13V
Input Voltage (V_{IN}) ..... (V_S + 0.1V) to (GND – 5V)
Output Voltage (V_{OUT}) ..... +13V
ESD Rating (Note 1)
Pins 1, 2, 3, 5, 6, 7, 8 ..... 2 kV
Pin 4 ..... 500V

Operating Ratings ‡

Supply Voltage (V_{DD}) ..... +4.5V to +12.6V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5 kΩ in series with 100 pF.

TABLE 1-1: ELECTRICAL CHARACTERISTICS

Electrical Characteristics: 4.5V ≤ V_{DD} ≤ 12.6V, C_L = 1000 pF; T_A = +25°C.
Bold values indicate –40°C ≤ T_J ≤ +125°C. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply						
Supply Voltage Range	V_{DD}	**4.5**	—	**12.6**	V	—
High Output Quiescent Current	I_S	—	—	**2.5**	mA	V_{IN} = 5V (MIC44F18), V_{IN} = 0V (MIC44F19/20)
Low Output Quiescent Current		—	—	**2.5**		V_{IN} = 0V (MIC44F18), V_{IN} = 5V (MIC44F19/20)
Shutdown Current	I_{SD}	—	—	**200**	µA	V_{EN} = 0V
EN/UVLO						
Enable Threshold	V_{EN}	**1.3**	**1.4**	**1.5**	V	—
Enable Hysteresis	V_{EN_HYS}	—	120	—	mV	—
Undervoltage Lockout Threshold (Internally Set)	V_{UVLO}	3.6	4.2	4.4	V	V_{EN} = open, V_{DD} rising.
UVLO Hysteresis	—	—	370	—	mV	—
Undervoltage Lockout Threshold (Externally Set)	V_{UVLO}	$V_{EN(MAX)}$	—	V_{DD}	V	V_{DD} rising
Input						
Input Voltage Range	V_{IN}	**0**	—	**V_{DD}**	V	Steady State Voltage, Note 2
Logic 1 Input Voltage	V_{IH}	1.615	1.7	1.785	V	T_A = +25°C (±5%)
		1.53	**1.7**	**1.87**		Over temperature range (±10%)
Logic 0 Input Voltage	V_{IL}	1.45	1.53	1.607	V	T_A = +25°C (±5%)
		1.377	**1.53**	**1.683**		Over temperature range (±10%)
Input Current	I_{IN}	—	—	**5**	µA	4.5V ≤ V_{IN} ≤ 10V
Output						
Output High Voltage	V_{OH}	**V_S – 0.025**	—	—	V	See Functional Block Diagram
Output Low Voltage	V_{OL}	—	—	**0.025**	V	See Functional Block Diagram
Output Resistance, Output High	R_O	—	—	**2**	Ω	I_{OUT} = 100 mA, V_{DD} = 12V
		—	—	**3**		I_{OUT} = 100 mA, V_{DD} = 5V
Output Resistance, Output Low		—	—	**2**	Ω	I_{OUT} = 100 mA, V_{DD} = 12V
		—	—	**3**		I_{OUT} = 100 mA, V_{DD} = 5V
Peak Output Sink Current	I_{PEAK}	**6**	—	—	A	V_{DD} = 12V
Peak Output Source Current		**6**	—	—	A	V_S = 12V
Latch-Up Protection Withstand Reverse Current	I_R	**>500**	—	—	mA	—

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TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: 4.5V ≤ V_{DD} ≤ 12.6V, C_L = 1000 pF; T_A = +25°C.
Bold values indicate –40°C ≤ T_J ≤ +125°C. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Switching Time						
Rise Time	t_R	—	10	**20**	ns	V_S = 12V, C_L = 1000 pF See Timing Diagram
Fall Time	t_F	—	10	**20**	ns	V_S = 12V, C_L = 1000 pF See Timing Diagram
Delay Time	t_{D1}	—	15	**35**	ns	V_S = 12V, C_L = 1000 pF See Timing Diagram
Delay Time	t_{D2}	—	13	**35**	ns	V_S = 12V, C_L = 1000 pF See Timing Diagram
Pulse Width	t_{PW}	**50**	—	—	ns	V_S = 12V, See Timing Diagram
Maximum Input Frequency	f_{MAX}	—	Note 3	—	MHz	V_S = 12V, See Timing Diagram 2

Note 1: Specification for packaged product only

2: The device is protected from damage when –5V< V_{IN}< 0V. However, 0V is the recommended minimum continuous V_{IL} voltage. See the Application Information section for additional information.

3: See Application Information section for information on the maximum operating frequency.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Junction Temperature	T_J	—	—	+125	°C	—
Maximum Junction Temperature	—	—	—	+150	°C	—
Storage Temperature Range	T_{DD}	–65	—	+150	°C	—
Lead Temperature	—	—	—	+300	°C	Soldering, 10s
Package Thermal Resistances						
Thermal Resistance ePAD MSOP-8	θ_{JA}	—	78	—	°C/W	—
Thermal Resistance 3x3 DFN-8Ld	θ_{JA}	—	93	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

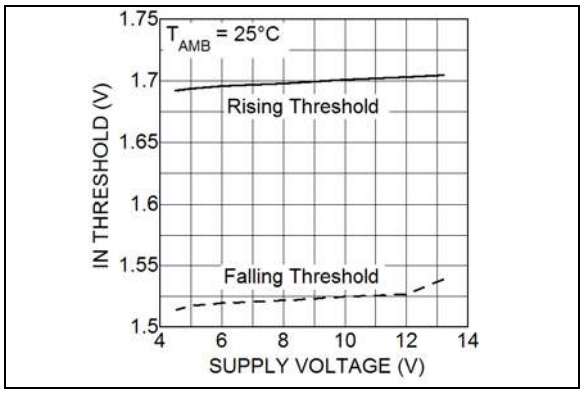

FIGURE 2-1: *IN Threshold vs. Supply Voltage.*

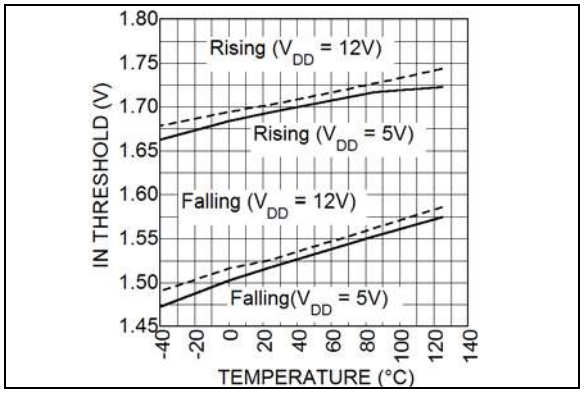

FIGURE 2-2: *IN Threshold vs. Temperature.*

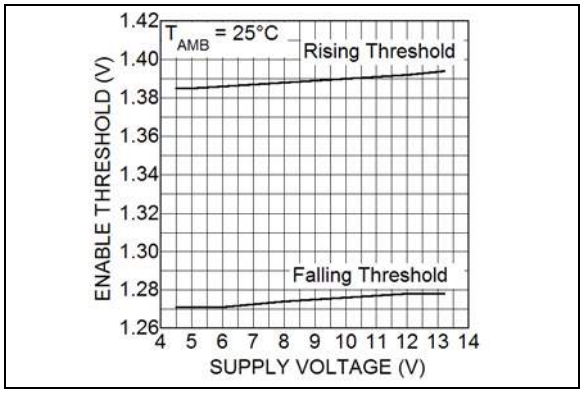

FIGURE 2-3: *Enable Threshold vs. Supply Voltage.*

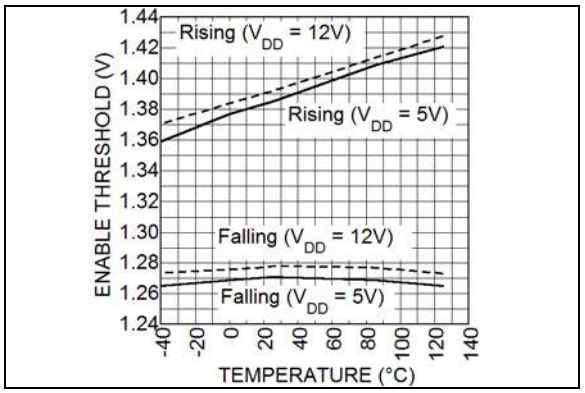

FIGURE 2-4: *Enable Threshold vs. Temperature.*

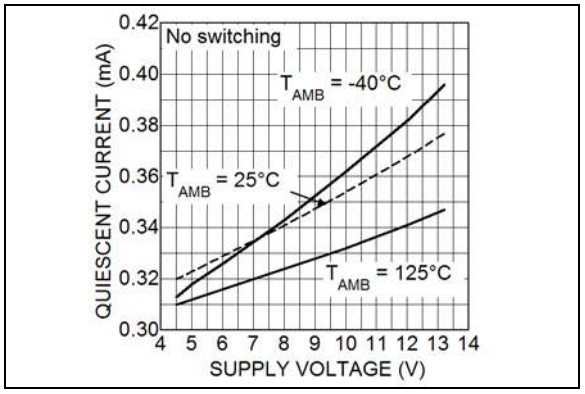

FIGURE 2-5: *Quiescent Current vs. Supply Voltage.*

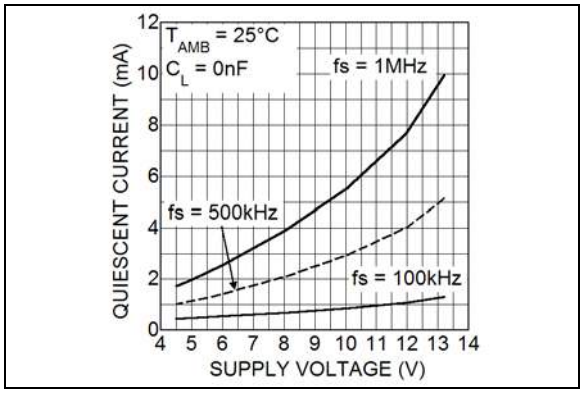

FIGURE 2-6: *Quiescent Current vs. Supply Voltage.*

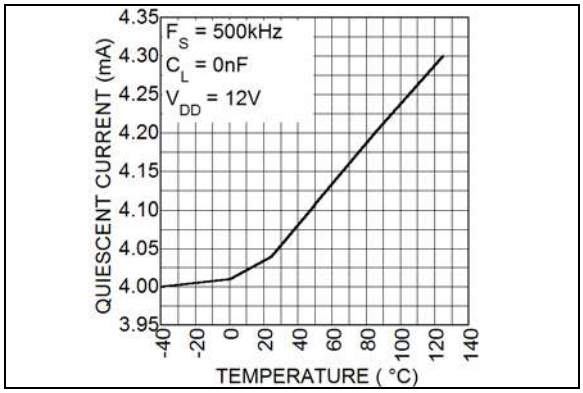

FIGURE 2-7: *Quiescent Current vs. Temperature.*

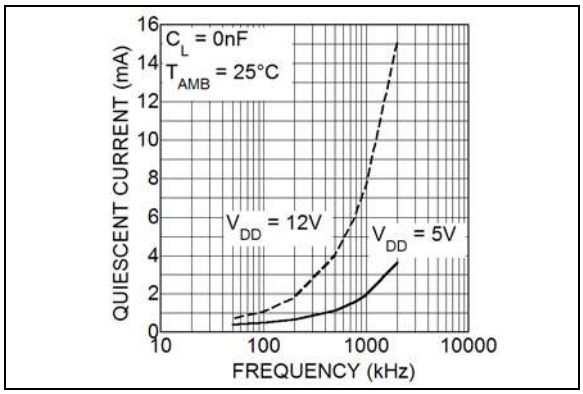

FIGURE 2-8: *Quiescent Current vs. Frequency.*

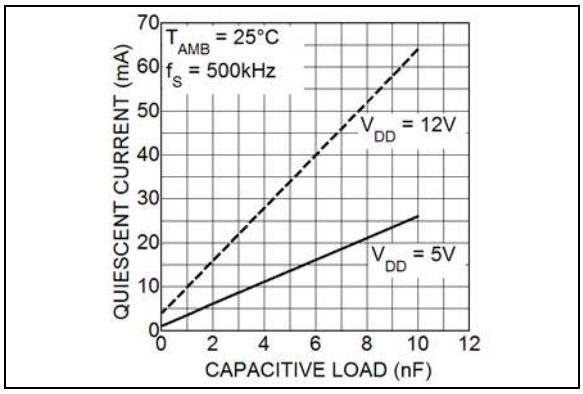

FIGURE 2-9: *Quiescent Current vs. Capacitive Load.*

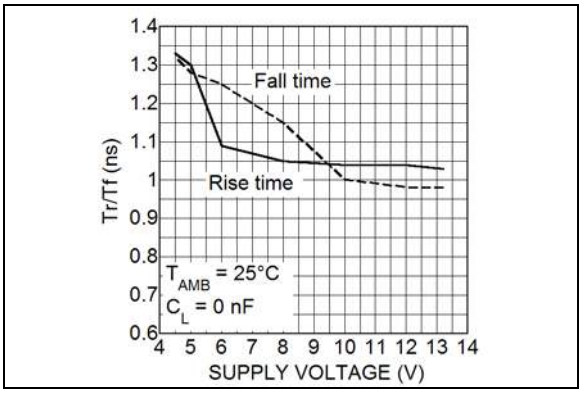

FIGURE 2-10: *Rise and Fall Time vs. Supply Voltage.*

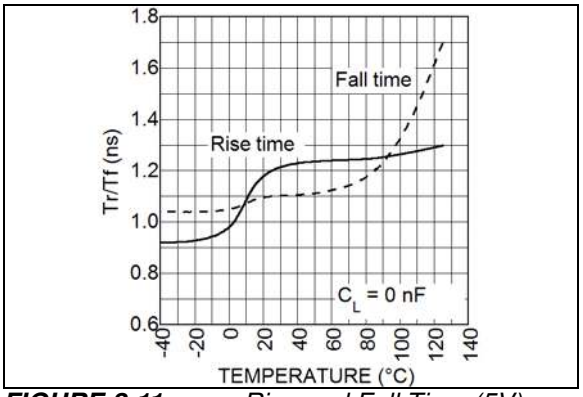

FIGURE 2-11: *Rise and Fall Time (5V) vs. Temperature.*

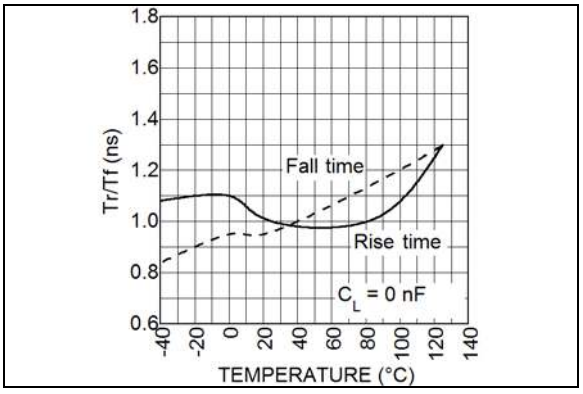

FIGURE 2-12: *Rise and Fall Time (12V) vs. Temperature.*

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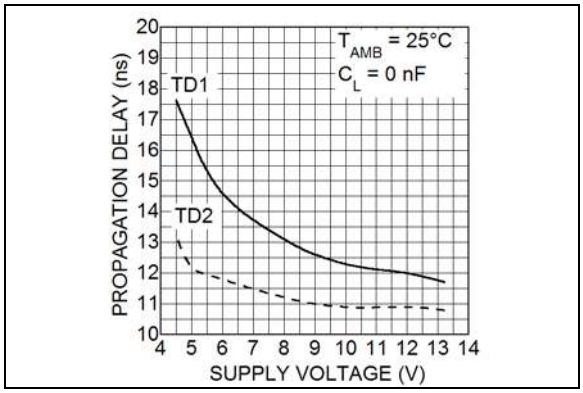


FIGURE 2-13: *Propagation Delay vs. Supply Voltage.*

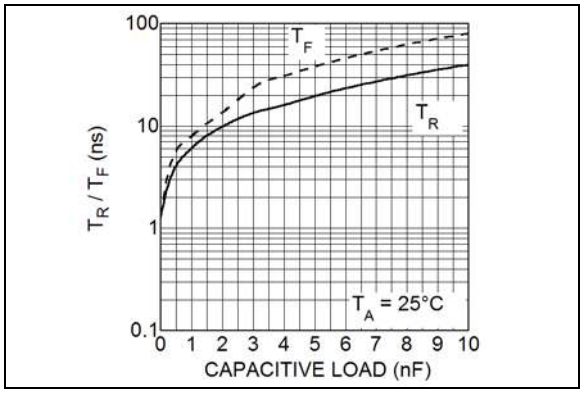


FIGURE 2-16: *Rise and Fall Time (5V) vs. Capacitive Load.*

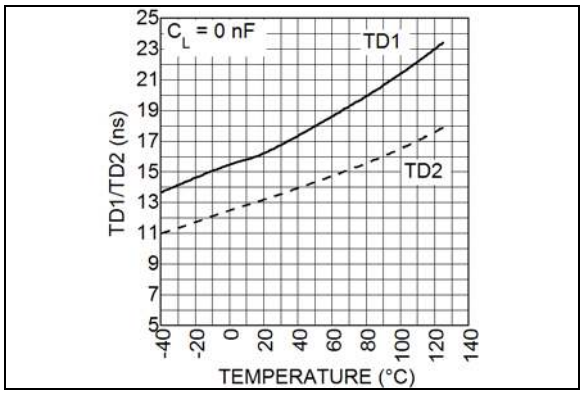


FIGURE 2-14: *Propagation Delay (5V) vs. Temperature.*

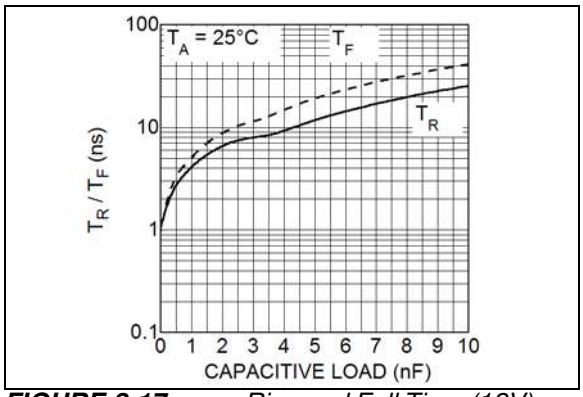


FIGURE 2-17: *Rise and Fall Time (12V) vs. Capacitive Load.*

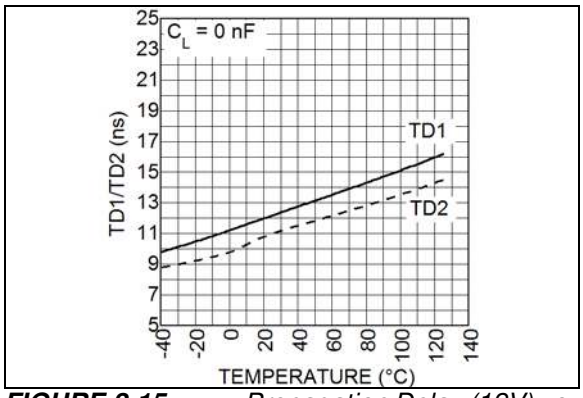


FIGURE 2-15: *Propagation Delay (12V) vs. Temperature.*

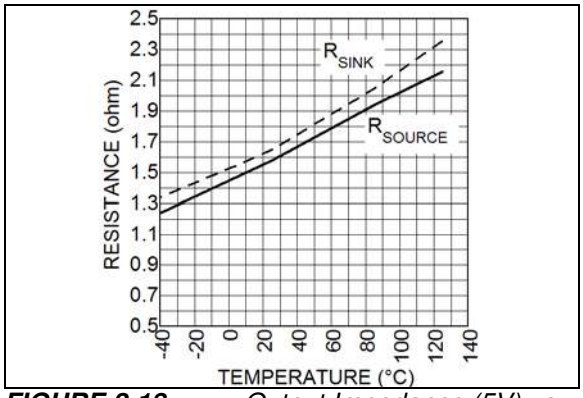


FIGURE 2-18: *Output Impedance (5V) vs. Temperature.*

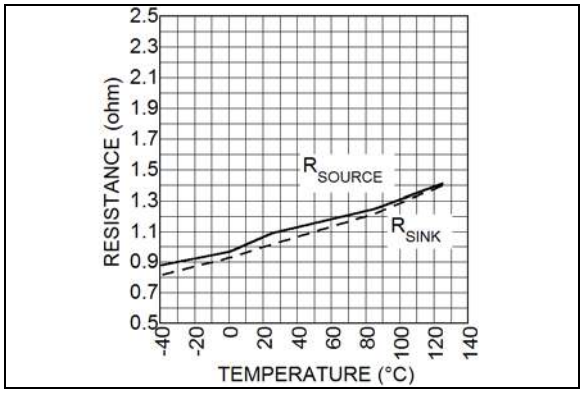
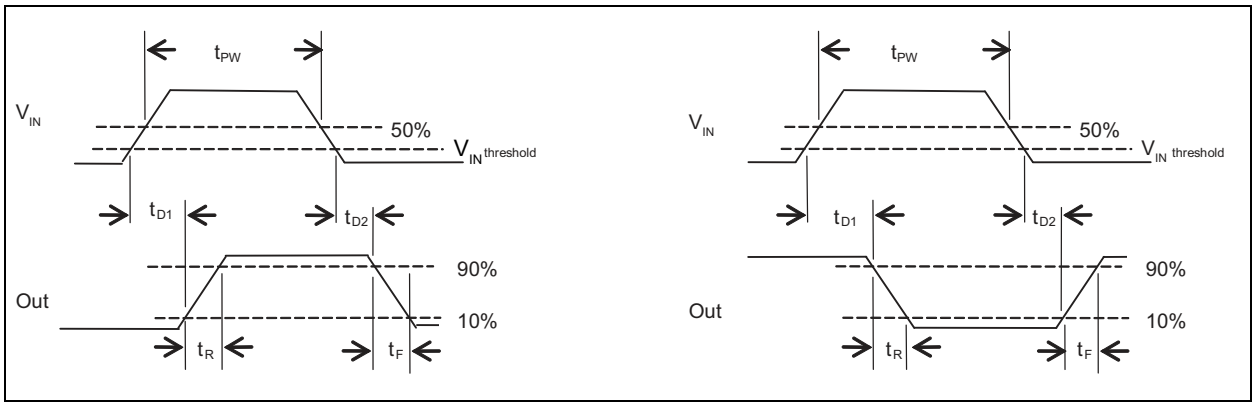


FIGURE 2-19: *Output Impedance (12V) vs. Temperature.*

Timing Diagram



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3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1, 8	OUT	Driver Output.
2	VDD	Supply Input.
3	NC	No Connect.
4	IN	Input (Input): Logic-high produces a high output voltage for the MIC44F18 and a low output voltage for the MIC44F19/20. Logic-low produces a low output voltage for the MIC44F18 and a high output voltage for the MIC44F19/20.
5	EN/UVLO	EN/Undervoltage Lockout (Input): Pulling this pin below low disables the driver. When disabled, the output is in the off state (low for the MIC44F18/20 and high for the MIC44F19). Floating this pin enables the driver and the UVLO circuitry when V_{DD} reaches the UVLO threshold. A resistor divider can set a different UVLO threshold voltage as shown on page 2 (See the Application Information section for more details).
6, 7	GND	Ground.
EP	ePAD	Ground. Exposed backside pad.

TABLE 3-2: LOGIC TABLE

EN/UVLO	IN	MIC44F18 OUTPUT	MIC44F19 OUTPUT	MIC44F20 OUTPUT
0	0	LOW	HIGH	LOW
0	1	LOW	HIGH	LOW
1	0	LOW	HIGH	HIGH
1	1	HIGH	LOW	LOW

4.0 FUNCTIONAL DESCRIPTION

The MIC44F18/19/20 family of drivers are high speed, high current drivers that are designed to drive P-channel and N-channel MOSFETs. The drivers come in both inverting and non-inverting versions. The block diagram of the MIC44Fxx driver is shown in the Functional Block Diagram.

The MIC44F18 is a non-inverting driver. When disabled, the VOUT pin is pulled low. The MIC44F19 is an inverting driver that is optimized to drive P-channel MOSFETs. When disabled, the VOUT pin is pulled high, which turns off the P-channel MOSFET. The MIC44F20 is an inverting driver, whose VOUT pin is pulled low when disabled. This allows it to drive an N-channel MOSFETs and turn it off when the driver is disabled. Table 3-2 summarizes the driver operation.

4.1 Start-Up and UVLO

The UVLO circuit disables the output until the V_{DD} supply voltage exceeds the UVLO threshold. Hysteresis in the UVLO circuit prevents noise and finite circuit impedance from causing chatter during turn-on and turn-off.

As shown in Figure 4-1, with the EN/UVLO pin open, an internal resistor divider senses the V_{DD} voltage and the UVLO threshold is set at the minimum operating voltage of the driver. The driver can be set to turn on at a higher voltage by adding an external resistor to the UVLO pin.

With an external divider, the V_{DD} turn on (rising V_{DD}) threshold is calculated as:

EQUATION 4-1:

$$V_{DD(ENABLE)} = V_{TH} \times \left(1 + \frac{R1}{R2}\right)$$

$$V_{DD(HYSTERESIS)} = V_{HYST} \times \left(1 + \frac{R1}{R2}\right)$$

Where:

V_{TH} = Enable threshold voltage.
$V_{DD(HYSTERESIS)}$ = Hysteresis voltage at the V_{DD} pin.
V_{HYST} = Enable hysteresis voltage.

Because the external resistors are parallel with the internal resistors, it is important to keep the value of the external resistors at least 10 times lower than the typical values of the internal resistors. This prevents the internal resistors from affecting the accuracy of the enable calculation as well as preventing the large tolerance of the internal resistors from affecting the tolerance of the enable voltage setting.

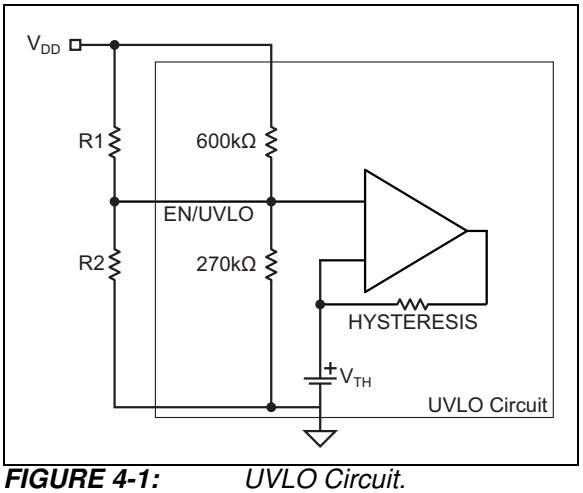

FIGURE 4-1: *UVLO Circuit.*

4.2 Input Stage

The MIC44Fxx family of drivers have a high-impedance, TTL-compatible input stage. The tight tolerance of the input threshold makes it compatible with CMOS devices powered from any supply voltage between 3V and V_{DD}. Hysteresis on the input pin improves noise immunity and prevents input signals with slow rise times from falsely triggering the output. The amplitude of the input voltage has no effect on the supply current draw of the driver.

The input voltage signal may go up to –5V below ground without damaging the driver or causing a latch up condition. Negative input voltages 0.7V below ground or greater will cause an increase in propagation delay.

4.3 Output Driver

A block diagram of the low-side driver is shown in Figure 4-2. Low driver impedances allow the external MOSFET to be turned on and off quickly. The rail-to-rail drive capability of the output ensures a low $R_{DS(ON)}$ from the external MOSFET.

Redundant VOUT pins lower the driver circuit impedance, which helps increase the drive current and minimize LC circuit ringing between the MOSFET gate and driver output.

The slew rate of the output is non-adjustable and depends only on the V_{DD} voltage and how much capacitance is present at the VOUT pin. The slew rate at the MOSFET gate can be adjusted by adding a resistor between the MOSFET gate and the driver output.

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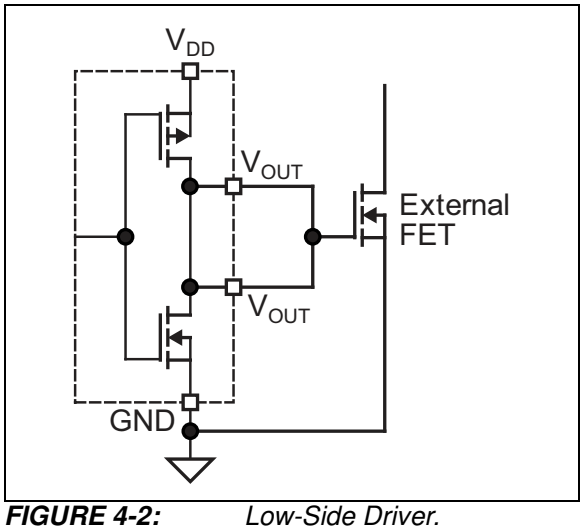

FIGURE 4-2: *Low-Side Driver.*

5.0 APPLICATION INFORMATION

5.1 Power Dissipation Considerations

Power dissipation in the driver can be separated into two areas:

- Output driver stage dissipation.
- Quiescent current dissipation used to supply the internal logic and control functions.

5.2 Output Driver Stage Power Dissipation

Power dissipation in the output driver stage is mainly caused by charging and discharging the gate to source and gate to drain capacitance of the external MOSFET. Figure 5-1 shows a simplified equivalent circuit of the MIC44F18 driving an external MOSFET.

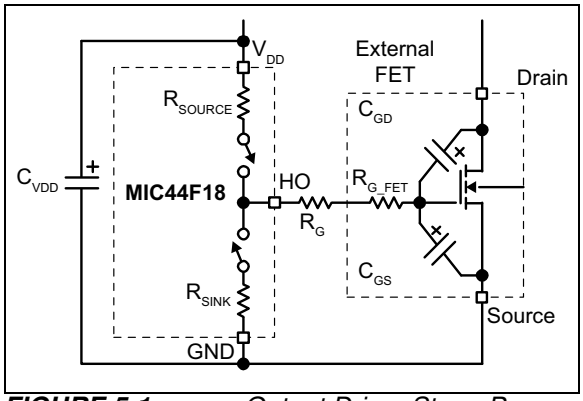

FIGURE 5-1: *Output Driver Stage Power Dissipation.*

5.2.1 DISSIPATION DURING THE EXTERNAL MOSFET TURN-ON

Energy from capacitor C_{VDD} is used to charge up the input capacitance of the MOSFET (C_{GD} and C_{GS}). The energy delivered to the MOSFET is dissipated in the three resistive components, R_{ON}, R_G, and R_{G_FET}. R_{ON} is the on resistance of the upper driver MOSFET in the MIC44F18. R_G is the series resistor (if any) between the driver IC and the MOSFET. R_{G_FET} is the gate resistance of the MOSFET. R_{G_FET} is usually listed in the power MOSFET's specifications. The ESR of capacitor C_B and the resistance of the connecting etch can be ignored since they are much less than R_{ON} and R_{G_FET}.

The effective capacitance of C_{GD} and C_{GS} is difficult to calculate since they vary non-linearly with I_D, V_{GS}, and V_{DS}. Fortunately, most power MOSFET specifications include a typical graph of total gate charge vs. V_{GS}. Figure 5-2 shows a typical gate charge curve for an arbitrary power MOSFET. This illustrates that for a gate voltage of 10V, the MOSFET requires about 23.5 nC of charge.

The energy dissipated by the resistive components of the gate drive circuit during turn-on is calculated as:

EQUATION 5-1:

$$E = \frac{1}{2} \times C_{ISS} \times V_{GS}^{2}$$

but

$$Q = C \times V$$

so

$$E = \frac{1}{2} \times Q_G \times V_{GS}$$

Where:

C_{ISS} = Total gate capacitance of the MOSFET.

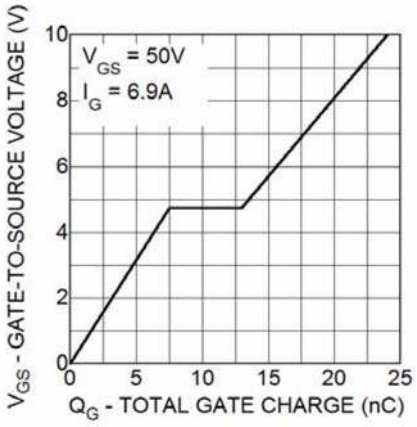

FIGURE 5-2: *Gate Charge.*

The same energy is dissipated by R_{OFF}, R_G, and R_{G_FET} when the driver IC turns the MOSFET off. Assuming R_{ON} is approximately equal to R_{OFF}, the total energy and power dissipated by the resistive drive elements is calculated in Equation 5-2.

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EQUATION 5-2:

$$E_{DRIVER} = Q_G \times V_{GS}$$

and

$$P_{DRIVER} = Q_G \times V_{GS} \times f_S$$

Where:

E_{DRIVER} = The energy dissipated per switching power.
P_{DRIVER} = The power dissipated by switching the MOSFET on and off.
Q_G = The total gate charge at V_{GS}.
V_{GS} = The gate-to-source voltage on the MOSFET.
f_S = The switching frequency of the gate drive circuit.

The power dissipated inside the MIC44F18/19/20 is equal to the ratio of R_{ON} and R_{OFF} to the external resistive losses in R_G and R_{G_FET}. Letting R_{ON} equal R_{OFF}, the power dissipated in the MIC44F18 due to driving the external MOSFET is:

EQUATION 5-3:

$$P_{DISSDRIVE} = P_{DRIVER} \times \frac{R_{ON}}{R_{ON} + R_G + R_{G_FET}}$$

5.3 Supply Current Power Dissipation

Power is dissipated in the MIC44F18 even if is there is nothing being driven. The supply current is drawn by the bias for the internal circuitry, the level shifting circuitry and shoot-through current in the output drivers. The supply current is proportional to operating frequency and the V_{DD} voltage. The typical characteristic graphs show how supply current varies with switching frequency and supply voltage.

The power dissipated by the MIC44F18 due to supply current is:

EQUATION 5-4:

$$P_{DISSSUPPLY} = V_{DD} \times I_{DD}$$

5.4 Total Power Dissipation and Thermal Considerations

Total power dissipation in the driver equals the power dissipation caused by driving the external MOSFETs plus the supply current:

EQUATION 5-5:

$$P_{DISSTOTAL} = P_{DISSSUPPLY} + P_{DISSDRIVE}$$

The die temperature may be calculated once the total power dissipation is known:

EQUATION 5-6:

$$T_J = T_A + P_{DISSTOTAL} \times \theta_{JA}$$

Where:

T_J = The junction temperature in °C.
T_A = The maximum ambient temperature.
$P_{DISSTOTAL}$ = The power dissipation of the driver.
θ_{JA} = The thermal resistance from junction-to-ambient air in °C/W.

The following graphs help determine the maximum gate charge that can be driven with respect to switching frequency, supply voltage and ambient temperature.

Figure 5-3 shows the power dissipation in the driver for different values of gate charge with V_{DD} = 5V. Figure 5-4 shows the power dissipation at V_{DD} = 12V. Figure 5-5 shows the maximum power dissipation for a given ambient temperature for the DFN and ePad packages.

The maximum operating frequency of the driver may be limited by the maximum power dissipation of the driver package.

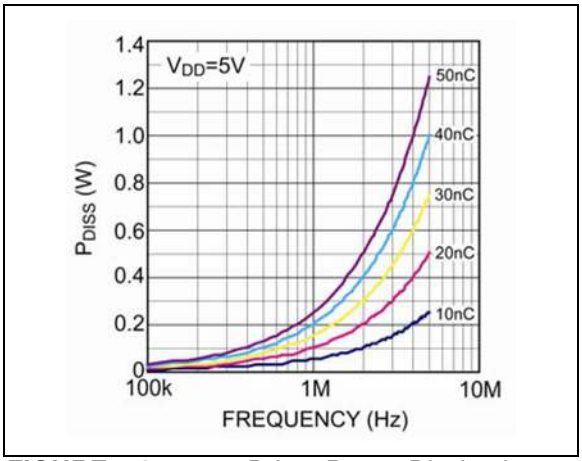

FIGURE 5-3: *Driver Power Dissipation.*

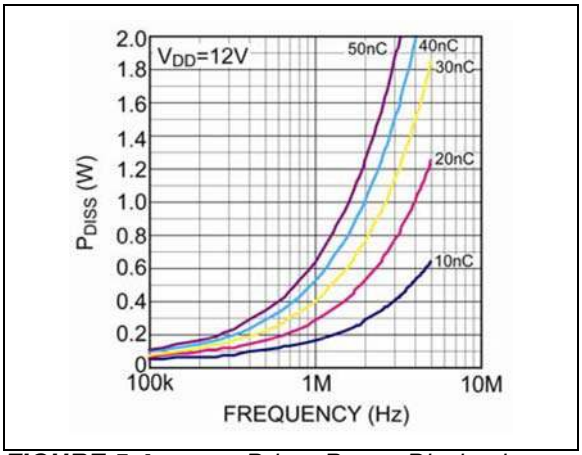

FIGURE 5-4: *Driver Power Dissipation.*

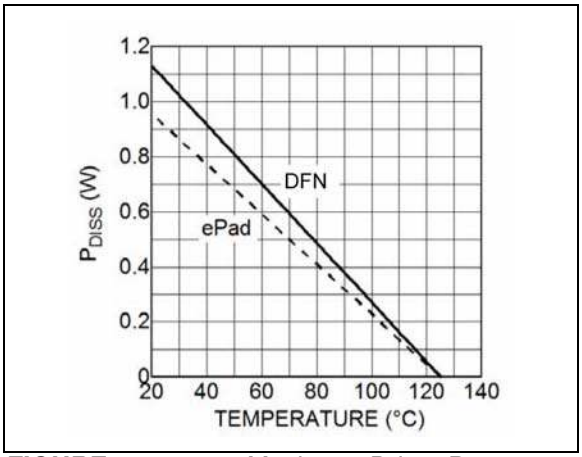

FIGURE 5-5: *Maximum Driver Power Dissipation.*

5.5 Propagation Delay, Delay Matching, and Other Timing Considerations

Fast propagation delay between the input and output drive waveform is desirable. It improves overcurrent protection by decreasing the response time between the control signal and the MOSFET gate drive. Minimizing propagation delay also minimizes phase shift errors in power supplies with wide bandwidth control loops.

Care must be taken to ensure the input signal pulse width is greater than the minimum specified pulse width. An input signal that is less than the minimum pulse width may result in no output pulse or an output pulse whose width is significantly less than the input.

5.6 Decoupling and Bootstrap Capacitor Selection

Decoupling capacitors are required for proper operation by supplying the charge necessary to drive the external MOSFETs as well as minimizing the voltage ripple on the supply pins.

Ceramic capacitors are recommended because of their low impedance and small size. Z5U type ceramic capacitor dielectrics are not recommended due to the large change in capacitance over temperature and voltage. A minimum value of 0.1 µF is required for each of the capacitors, regardless of the MOSFETs being driven. Larger MOSFETs may require larger capacitance values for proper operation. The voltage rating of the capacitors depends upon the supply voltage, ambient temperature and the voltage derating used for reliability.

Placement of the decoupling capacitors is critical. The bypass capacitor for V_{DD} should be placed as close as possible between the V_{DD} and V_{SS} pins. The etch connections must be short, wide and direct. The use of a ground plane to minimize connection impedance is recommended. Refer to the next section for more information.

5.7 Grounding, Component Placement and Circuit Layout

Nanosecond switching speeds and ampere peak currents in and around the MOSFET driver requires proper placement and trace routing of all components. Improper placement may cause degraded noise immunity, false switching and excessive ringing.

Figure 5-6 shows the critical current paths when the driver outputs go high and turn on the external MOSFETs. It also helps demonstrate the need for a low impedance ground plane. Charge needed to turn-on the MOSFET gates comes from the decoupling capacitors C_{VDD}. Current in the gate driver flows from C_{VDD} through the internal driver, into the MOSFET gate

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and out the source. The return connection back to the decoupling capacitor is made through the ground plane. Any inductance or resistance in the ground return path causes a voltage spike or ringing to appear on the source of the MOSFET. This voltage works against the gate drive voltage and can either slow down or turn off the MOSFET during the period when it should be turned on.

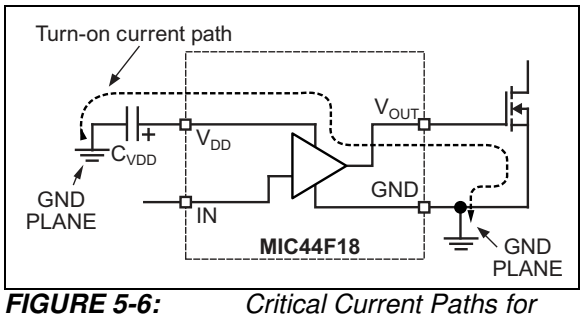


FIGURE 5-6: *Critical Current Paths for High Driver Outputs.*

Figure 5-7 shows the critical current paths when the driver outputs go low and turn off the external MOSFETs. Short, low impedance connections are important during turn-off for the same reasons given in the turn-on explanation. Current from the V_{DD} supply replenishes charge in the decoupling capacitor, C_{VDD}.

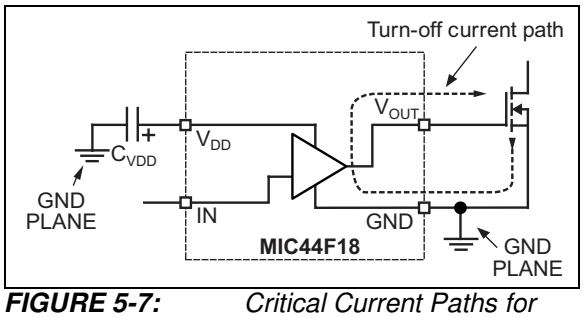


FIGURE 5-7: *Critical Current Paths for High Driver Outputs.*

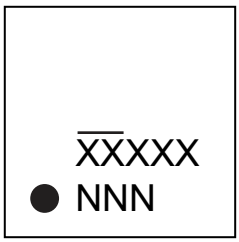
The following circuit guidelines should be adhered to for optimum circuit performance:

1. The V_{CC} bypass capacitor must be placed close to the V_{DD} and ground pins. It is critical that the etch length between the decoupling capacitor and the V_{DD} and GND pins be minimized to reduce pin inductance.
2. A ground plane is recommended to minimize parasitic inductance and impedance of the return paths. The MIC44F18 family of drivers is capable of high peak currents and very fast transition times. Any impedance between the driver, the decoupling capacitors and the external MOSFET will degrade the performance of the circuit.
3. Trace out the high di/dt and dv/dt paths, as shown in Figure 5-6 and Figure 5-7 and minimize etch length and loop area for these connections. Minimizing these parameters decreases the parasitic inductance and the radiated EMI generated by fast rise and fall times.

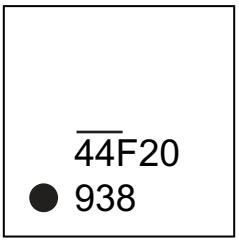
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

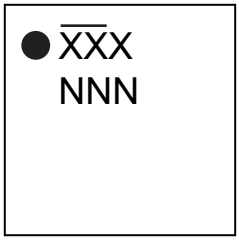
8-Pin ePAD MSOP*



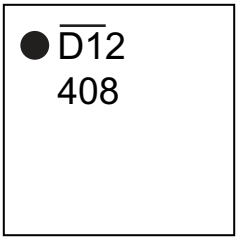
Example



8-Pin DFN*



Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

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8-Lead MSOP ePAD Package Outline and Recommended Land Pattern

TITLE
8 LEAD MSOP EPAD PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

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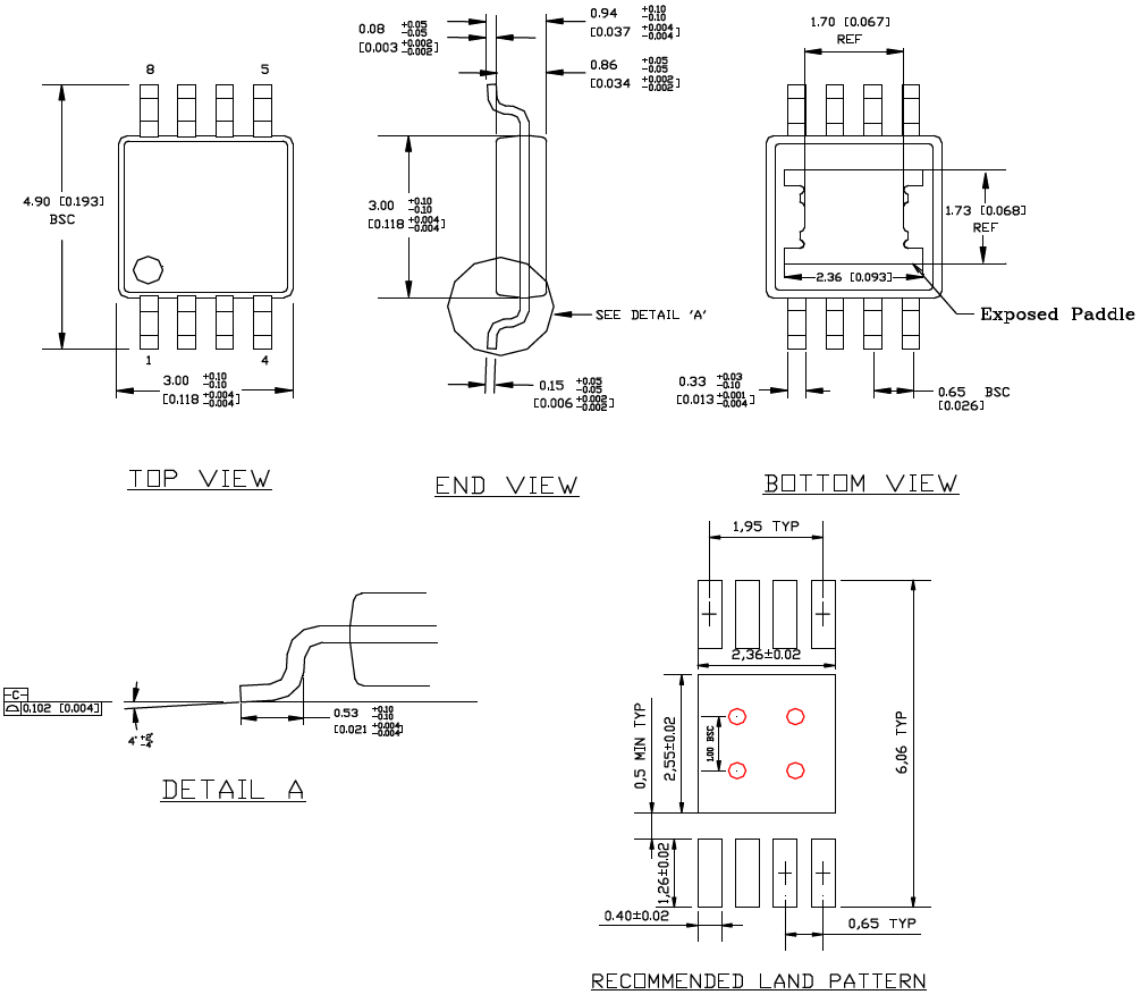


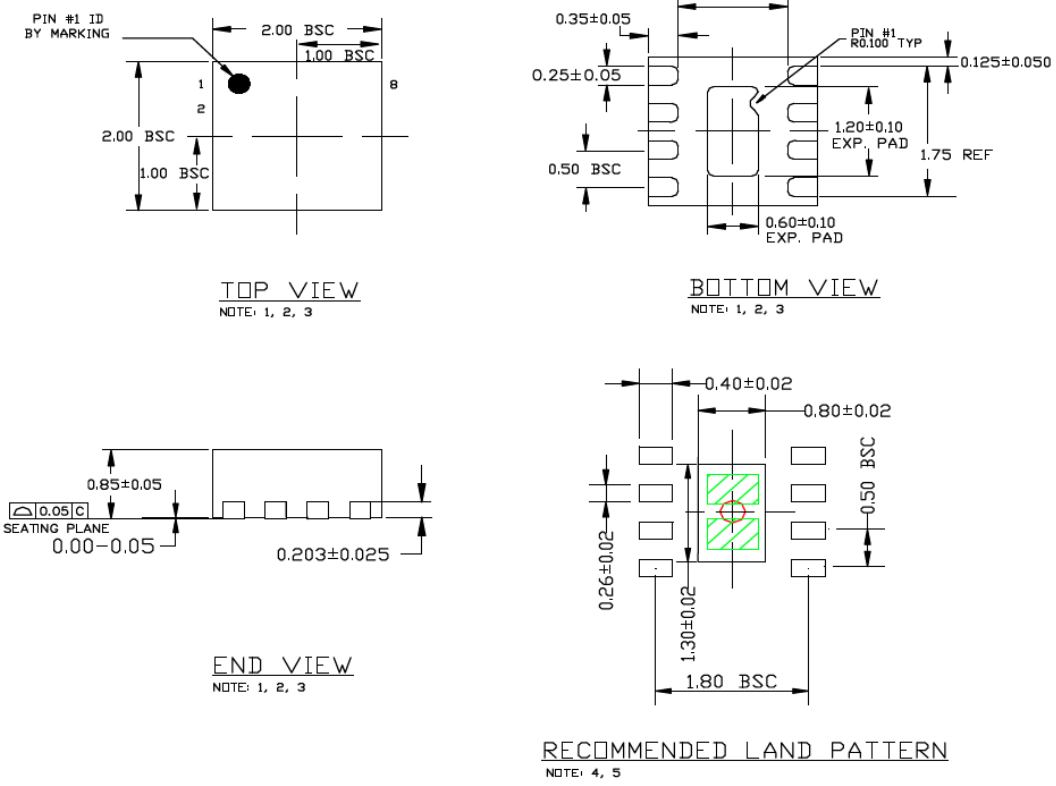
NOTE:
1. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.20 [0.008] PER SIDE
2. RED CIRCLES IN LAND PATTERN REPRESENT THERMAL VIAS. RECOMMENDED SIZE IS 0.30-0.35MM IN DIAMETER, 1.00 PITCH AND SHOULD BE CONNECTED TO GND FOR MAXIMUM PERFORMANCE

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

8-Lead 2 mm x 2 mm DFN Package Outline and Recommended Land Pattern

TITLE
8 LEAD DFN 2x2mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	DFN22-8LD-PL-1	**UNIT**	MM



NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.35MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) INDICATE SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.60x0.40 MM IN SIZE, 0.20 MM SPACING.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

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APPENDIX A: REVISION HISTORY

Revision A (November 2017)

- Converted Micrel document MIC44F18/19/20 to Microchip data sheet DS20005900A.
- Minor text changes throughout.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

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Device	Configuration	Junction Temp. Range	Package	Media Type

Device:	MIC44F__:	6A, 12.6V High Speed MOSFET Drivers with Enable Input
Configuration:	18 =	Non-Inverting
	19 =	Inverting Output high when disabled
	20 =	Inverting Output low when disabled
Junction Temperature Range:	Y =	–40°C to +125°C, RoHS-Compliant
Package:	MME=	8-Lead ePAD MSOP
	ML =	8-Lead 2 mm x 2 mm DFN
Media Type:	<blank>=	100/Tube (MME Package Only)
	TR =	2,500/Reel (MME Package)
	TR =	5,000/Reel (ML Package)

Examples:

a) MIC44F18YMME: 6A, 12.6V High Speed MOSFET Driver with Enable Input, Non-Inverting, –40°C to +125°C Temp. Range, 8-Lead ePAD MSOP, 100/Tube

b) MIC44F19YML-TR: 6A, 12.6V High Speed MOSFET Driver with Enable Input, Inverting Output High When Disabled, –40°C to +125°C Temp. Range, 8-Lead 2x2 DFN, 5,000/Reel

c) MIC44F20YMME-TR: 6A, 12.6V High Speed MOSFET Driver with Enable Input, Inverting Output Low When Disabled, –40°C to +125°C Temp. Range, 8-Lead ePAD MSOP, 2,500/Reel

d) MIC44F19YMME: 6A, 12.6V High Speed MOSFET Driver with Enable Input, Inverting Output High When Disabled, –40°C to +125°C Temp. Range, 8-Lead ePAD MSOP, 100/Tube

e) MIC44F18YML-TR: 6A, 12.6V High Speed MOSFET Driver with Enable Input, Non-Inverting, –40°C to +125°C Temp. Range, 8-Lead 2x2 DFN, 5,000/Reel

f) MIC44F20YML-TR: 6A, 12.6V High Speed MOSFET Driver with Enable Input, Inverting Output Low When Disabled, –40°C to +125°C Temp. Range, 8-Lead 2x2 DFN, 5,000/Reel

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