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XRT86VL38

OCTAL T1/E1/J1 FRAMER/LIU COMBO - T1 REGISTER DESCRIPTION

GENERAL DESCRIPTION

The XRT86VL38 is an eight-channel 1.544 Mbit/s or 2.048 Mbit/s DS1/E1/J1 framer and LIU integrated solution featuring R^3 technology (Relayless, Reconfigurable, Redundancy). The physical interface is optimized with internal impedance, and with the patented pad structure, the XRT86VL38 provides protection from power failures and hot swapping.

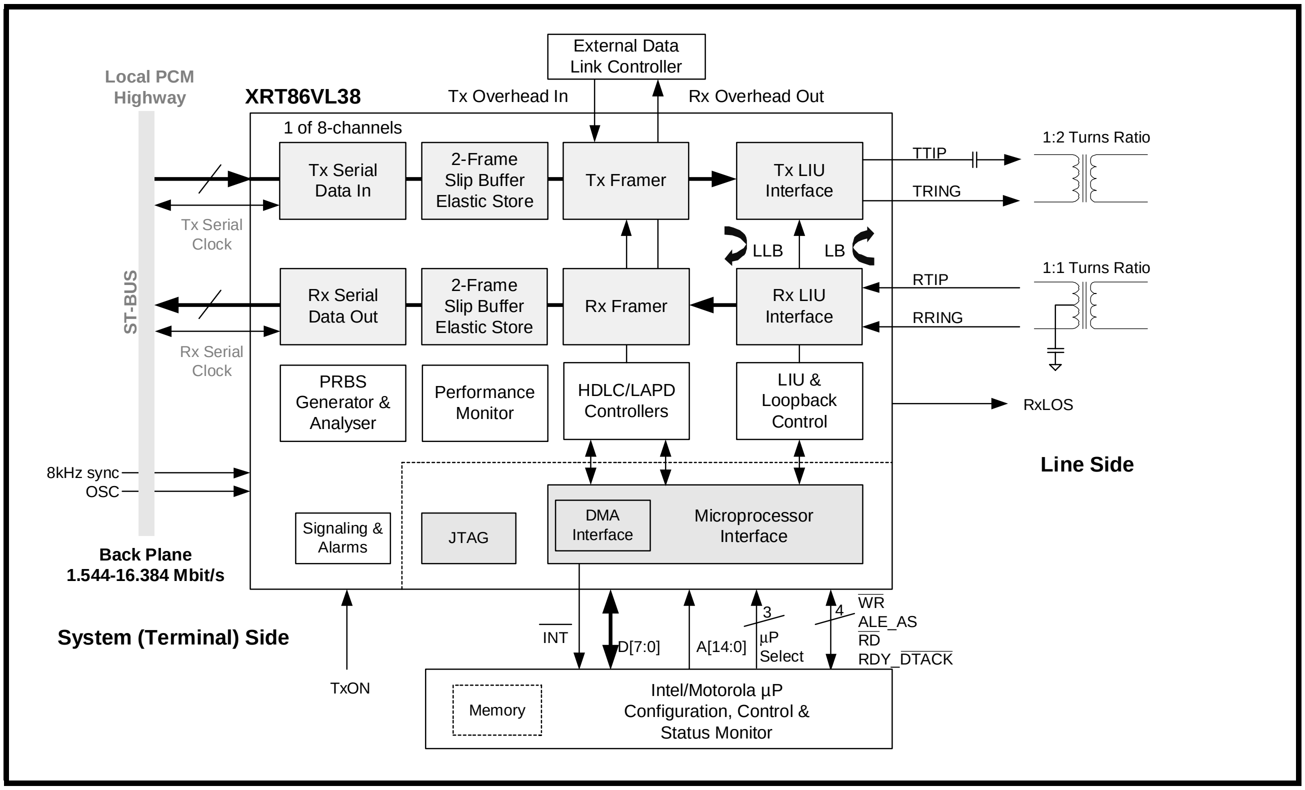
The XRT86VL38 contains an integrated DS1/E1/J1 framer and LIU which provide DS1/E1/J1 framing and error accumulation in accordance with ANSI/ITU_T specifications. Each framer has its own framing synchronizer and transmit-receive slip buffers. The slip buffers can be independently enabled or disabled as required and can be configured to frame to the common DS1/E1/J1 signal formats.

Each Framer block contains its own Transmit and Receive E1/J1 Framing function. There are 3 Transmit HDLC controllers per channel which encapsulate contents of the Transmit HDLC buffers into LAPD Message frames. There are 3 Receive HDLC controllers per channel which extract the payload content of Receive LAPD Message frames from the incoming E1/J1 data stream and write the contents into the Receive HDLC buffers. Each framer also contains a Transmit and Overhead Data Input port, which permits Data Link Terminal Equipment direct access to the outbound E1/J1 frames. Likewise, a Receive Overhead output data port permits Data Link Terminal Equipment direct access to the Data Link bits of the inbound E1/J1 frames.

The XRT86VL38 fully meets all of the latest E1/J1 specifications: ANSI E1.107-1988, ANSI E1.403-1995, ANSI E1.231-1993, ANSI E1.408-1990, AT&T TR 62411 (12-90) TR54016, and ITU G-703, G.704, G706 and G.733, AT&T Pub. 43801, and ETS 300 011, 300 233, JT G.703, JT G.704, JT G706, I.431. Extensive test and diagnostic functions include Loop-backs, Boundary scan, Pseudo Random bit sequence (PRBS) test pattern generation, Performance Monitor, Bit Error Rate (BER) meter, forced error insertion, and LAPD unchannelized data payload processing according to ITU-T standard Q.921.

Applications and Features (next page)

FIGURE 1. XRT86VL38 8-CHANNEL DS1 (E1/J1) FRAMER/LIU COMBO



APPLICATIONS

- High-Density E1/J1 interfaces for Multiplexers, Switches, LAN Routers and Digital Modems
- SONET/SDH terminal or Add/Drop multiplexers (ADMs)
- E1/J1 add/drop multiplexers (MUX)
- Channel Service Units (CSUs): E1/J1 and Fractional E1/J1
- Digital Access Cross-connect System (DACs)
- Digital Cross-connect Systems (DCS)
- Frame Relay Switches and Access Devices (FRADS)
- ISDN Primary Rate Interfaces (PRA)
- PBXs and PCM channel bank
- T3 channelized access concentrators and M13 MUX
- Wireless base stations
- ATM equipment with integrated DS1 interfaces
- Multichannel DS1 Test Equipment
- E1/J1 Performance Monitoring
- Voice over packet gateways
- Routers

FEATURES

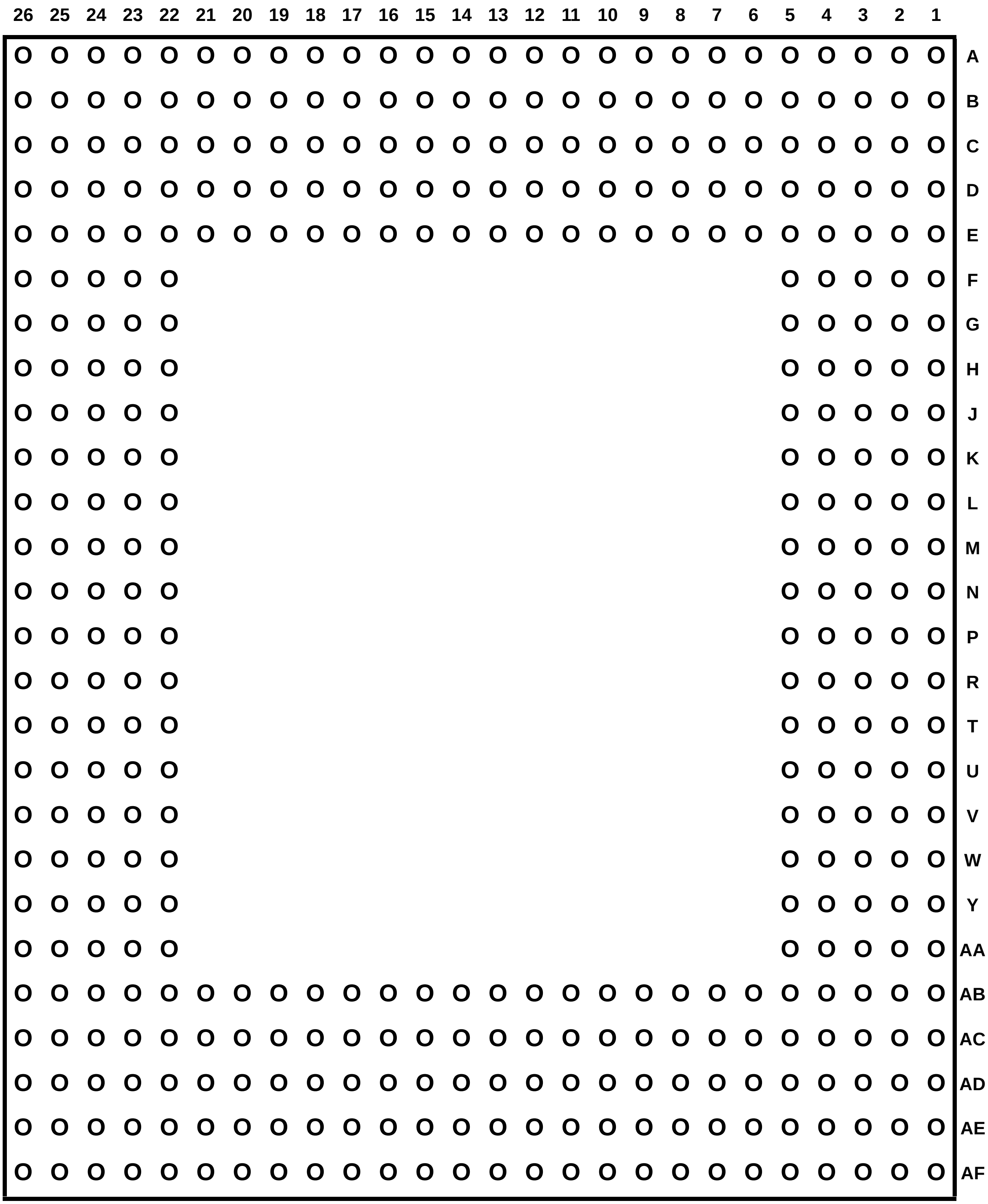
- Eight independent, full duplex DS1 Tx and Rx Framer/LIUs
- Two 512-bit (two-frame) elastic store, PCM frame slip buffers (FIFO) on TX and Rx provide up to 8.192 MHz asynchronous back plane connections with jitter and wander attenuation
- Supports input PCM and signaling data at 1.544, 2.048, 4.096 and 8.192 Mbits. Also supports 4-channel multiplexed 12.352/16.384 (HMVIP/H.100) Mbit/s on the back plane bus
- Programmable output clocks for Fractional E1/J1
- Supports Channel Associated Signaling (CAS)
- Supports Common Channel Signalling (CCS)
- Supports ISDN Primary Rate Interface (ISDN PRI) signaling
- Extracts and inserts robbed bit signaling (RBS)
- 3 Integrated HDLC controllers per channel for transmit and receive, each controller having two 96-byte buffers (buffer 0 / buffer 1)
- HDLC Controllers Support SS7
- Timeslot assignable HDLC
- V5.1 or V5.2 Interface
- Automatic Performance Report Generation (PMON Status) can be inserted into the transmit LAPD interface every 1 second or for a single transmission
- Alarm Indication Signal with Customer Installation signature (AIS-CI)
- Remote Alarm Indication with Customer Installation (RAI-CI)
- Gapped Clock interface mode for Transmit and Receive.

- Intel/Motorola and Power PC interfaces for configuration, control and status monitoring
- Parallel search algorithm for fast frame synchronization
- Wide choice of T1 framing structures: SF/D4, ESF, SLC®96, T1DM and N-Frame (non-signaling)
- Direct access to D and E channels for fast transmission of data link information
- PRBS, QRSS, and Network Loop Code generation and detection
- Programmable Interrupt output pin
- Supports programmed I/O and DMA modes of Read-Write access
- Each framer block encodes and decodes the E1/J1 Frame serial data
- Detects and forces Red (SAI), Yellow (RAI) and Blue (AIS) Alarms
- Detects OOF, LOF, LOS errors and COFA conditions
- Loopbacks: Local (LLB) and Line remote (LB)
- Facilitates Inverse Multiplexing for ATM
- Performance monitor with one second polling
- Boundary scan (IEEE 1149.1) JTAG test port
- Accepts external 8kHz Sync reference
- 1.8V Inner Core Voltage
- 3.3V I/O operation with 5V tolerant inputs
- 420-pin PBGA package or 484-pin STBGA package with -40°C to +85°C operation

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT86VL38IB	420 Plastic Ball Grid Array	-40°C to +85°C
XRT86VL38IB484	484 Shrink Thin Ball Grid Array	-40°C to +85°C

420 BALL - PLASTIC BALL GRID ARRAY (BOTTOM VIEW, SEE PIN LIST FOR DESCRIPTION)



484 BALL - SHRINK THIN BALL GRID ARRAY (BOTTOM VIEW - SEE PIN LIST FOR DESCRIPTION)

22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	A
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	B
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	C
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	D
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	E
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	F
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	G
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	H
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	J
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	K
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	L
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	M
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	N
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	P
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	R
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	T
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	U
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	V
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	W
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	Y
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	AA
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	AB

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DESCRIPTION OF THE CONTROL REGISTERS - T1 MODE

TABLE 1: REGISTER SUMMARY

FUNCTION	SYMBOL	HEX
Control Registers (0xn100 - 0xn1FF)		
Clock and Select Register	CSR	0xn100
Line Interface Control Register	LICR	0xn101
General Purpose Input/Output Control 0	GPIOCR0	0x0102
General Purpose Input/Output Control 1	GPIOCR1	0x4102
Reserved	-	0xn103 - 0xn106
Framing Select Register	FSR	0xn107
Alarm Generation Register	AGR	0xn108
Synchronization MUX Register	SMR	0xn109
Transmit Signaling and Data Link Select Register	TSDLSR	0xn10A
Framing Control Register	FCR	0xn10B
Receive Signaling & Data Link Select Register	RSDLSR	0xn10C
Receive Signaling Change Register 0	RSCR0	0xn10D
Receive Signaling Change Register 1	RSCR1	0xn10E
Receive Signaling Change Register 2	RSCR2	0xn10F
Reserved - E1 mode only	-	0xn110 - 0xn111
Receive In-Frame Register	RIFR	0xn112
Data Link Control Register 1	DLCR1	0xn113
Transmit Data Link Byte Count Register 1	TDLBCR1	0xn114
Receive Data Link Byte Count Register 1	RDLBCR1	0xn115
Slip Buffer Control Register	SBCR	0xn116
FIFO Latency Register	FIFOLR	0xn117
DMA 0 (Write) Configuration Register	D0WCR	0xn118
DMA 1 (Read) Configuration Register	D1RCR	0xn119
Interrupt Control Register	ICR	0xn11A
LAPD Select Register	LAPDSR	0xn11B
Customer Installation Alarm Generation Register	CIAGR	0xn11C
Performance Report Control Register	PRCR	0xn11D
Gapped Clock Control Register	GCCR	0xn11E
Transmit Interface Control Register	TICR	0xn120
PRBS Control & Status - Register 0	PRBSCSR0	0xn121

TABLE 1: REGISTER SUMMARY

FUNCTION	SYMBOL	HEX
Receive Interface Control Register	RICR	0xn122
PRBS Control & Status - Register 1	PRBSCSR1	0xn123
Loopback Code Control Register	LCCR	0xn124
Transmit Loopback Code Register	TLCR	0xn125
Receive Loopback Activation Code Register	RLACR	0xn126
Receive Loopback Deactivation Code Register	RLDCR	0xn127
Defect Detection Enable Register	DDER	0xn129
Reserved - E1 mode only	-	0xn130 - 0xn13F
Transmit SPRM Control Register	TSPRMCR	0xn142
Data Link Control Register 2	DLCR2	0xn143
Transmit Data Link Byte Count Register 2	TDLBCR2	0xn144
Receive Data Link Byte Count Register 2	RDLBCR2	0xn145
Data Link Control Register 3	DLCR3	0xn153
Transmit Data Link Byte Count Register 3	TDLBCR3	0xn154
Receive Data Link Byte Count Register 3	RDLBCR3	0xn155
Device ID Register	DEVID	0xn1FE
Revision Number Register	REVID	0xn1FF
Time Slot (payload) Control (0xn300 - 0xn3FF)		
Transmit Channel Control Register 0-23	TCCR 0-23	0xn300 - 0xn317
Transmit User Code Register 0-23	TUCR 0-23	0xn320 - 0xn337
Transmit Signaling Control Register 0-23	TSCR 0-23	0xn340 - 0xn357
Receive Channel Control Register 0-23	RCCR 0-23	0xn360 - 0xn377
Receive User Code Register 0-23	RUCR 0-23	0xn380 - 0xn397
Receive Signaling Control Register 0-23	RSCR 0-23	0xn3A0 - 0xn3B7
Receive Substitution Signaling Register 0-23	RSSR 0-23	0xn3C0 - 0xn3D7
Receive Signaling Array (0xn500 - 0xn51F)		
Receive Signaling Array Register 0	RSAR0-23	0xn500 - 0xn517
LAPDn Buffer 0		
LAPD Buffer 0 Control Register	LAPDBCR0	0xn600 - 0xn660
LAPDn Buffer 1		
LAPD Buffer 1 Control Register	LAPDBCR1	0xn700 - 0xn760

TABLE 1: REGISTER SUMMARY

FUNCTION	SYMBOL	HEX
Performance Monitor		
Receive Line Code Violation Counter: MSB	RLCVCU	0xn900
Receive Line Code Violation Counter: LSB	RLCVCL	0xn901
Receive Frame Alignment Error Counter: MSB	RFAECU	0xn902
Receive Frame Alignment Error Counter: LSB	RFAECL	0xn903
Receive Severely Errored Frame Counter	RSEFC	0xn904
Receive Synchronization Bit (CRC-6) Error Counter: MSB	RSBBECU	0xn905
Receive Synchronization Bit (CRC-6) Error Counter: LSB	RSBBECL	0xn906
Reserved - E1 Mode Only		0xn907 - 0xn908
Receive Slip Counter	RSC	0xn909
Receive Loss of Frame Counter	RLFC	0xn90A
Receive Change of Frame Alignment Counter	RCOAC	0xn90B
LAPD Frame Check Sequence Error counter 1	LFCSEC1	0xn90C
PRBS bit Error Counter: MSB	PBECU	0xn90D
PRBS bit Error Counter: LSB	PBECL	0xn90E
Transmit Slip Counter	TSC	0xn90F
Excessive Zero Violation Counter: MSB	EZVCU	0xn910
Excessive Zero Violation Counter: LSB	EZVCL	0xn911
LAPD Frame Check Sequence Error counter 2	LFCSEC2	0xn91C
LAPD Frame Check Sequence Error counter 3	LFCSEC3	0xn92C
Interrupt Generation/Enable Register Address Map (0xnB00 - 0xnB41)		
Block Interrupt Status Register	BISR	0xnB00
Block Interrupt Enable Register	BIER	0xnB01
Alarm & Error Interrupt Status Register	AEISR	0xnB02
Alarm & Error Interrupt Enable Register	AEIER	0xnB03
Framer Interrupt Status Register	FISR	0xnB04
Framer Interrupt Enable Register	FIER	0xnB05
Data Link Status Register 1	DLSR1	0xnB06
Data Link Interrupt Enable Register 1	DLIER1	0xnB07
Slip Buffer Interrupt Status Register	SBISR	0xnB08
Slip Buffer Interrupt Enable Register	SBIER	0xnB09
Receive Loopback code Interrupt and Status Register	RLCISR	0xnB0A
Receive Loopback code Interrupt Enable Register	RLCIER	0xnB0B

TABLE 1: REGISTER SUMMARY

FUNCTION	SYMBOL	HEX
Reserved - E1 Mode Only	-	0xnB0C - 0xnB0D
Excessive Zero Status Register	EXZSR	0xnB0E
Excessive Zero Enable Register	EXZER	0xnB0F
SS7 Status Register for LAPD 1	SS7SR1	0xnB10
SS7 Enable Register for LAPD 1	SS7ER1	0xnB11
RxLOS/CRC Interrupt Status Register	RLCISR	0xnB12
RxLOS/CRC Interrupt Enable Register	RLCIER	0xnB13
Data Link Status Register 2	DLSR2	0xnB16
Data Link Interrupt Enable Register 2	DLIER2	0xnB17
SS7 Status Register for LAPD 2	SS7SR2	0xnB18
SS7 Enable Register for LAPD 2	SS7ER2	0xnB19
Data Link Status Register 3	DLSR3	0xnB26
Data Link Interrupt Enable Register 3	DLIER3	0xnB27
SS7 Status Register for LAPD 3	SS7SR3	0xnB28
SS7 Enable Register for LAPD 3	SS7ER3	0xnB29
Customer Installation Alarm Status Register	CIASR	0xnB40
Customer Installation Alarm Interrupt Enable Register	CIAIER	0xnB41
LIU Register Summary - Channel Control Registers		
LIU Channel Control Register 0	LIUCCR0	0x0Fn0
LIU Channel Control Register 1	LIUCCR1	0x0Fn1
LIU Channel Control Register 2	LIUCCR2	0x0Fn2
LIU Channel Control Register 3	LIUCCR3	0x0Fn3
LIU Channel Control Interrupt Enable Register	LIUCCIER	0x0Fn4
LIU Channel Control Status Register	LIUCCSR	0x0Fn5
LIU Channel Control Interrupt Status Register	LIUCCISR	0x0Fn6
LIU Channel Control Cable Loss Register	LIUCCCCR	0x0Fn7
LIU Channel Control Arbitrary Register 1	LIUCCAR1	0x0Fn8
LIU Channel Control Arbitrary Register 2	LIUCCAR2	0x0Fn9
LIU Channel Control Arbitrary Register 3	LIUCCAR3	0x0FnA
LIU Channel Control Arbitrary Register 4	LIUCCAR4	0x0FnB
LIU Channel Control Arbitrary Register 5	LIUCCAR5	0x0FnC
LIU Channel Control Arbitrary Register 6	LIUCCAR6	0x0FnD
LIU Channel Control Arbitrary Register 7	LIUCCAR7	0x0FnE

TABLE 1: REGISTER SUMMARY

FUNCTION	SYMBOL	HEX
LIU Channel Control Arbitrary Register 8	LIUCCAR8	0x0FnF
Reserved	-	0x0F80 - 0x0FDF
LIU Register Summary - Global Control Registers		
LIU Global Control Register 0	LIUGCR0	0x0FE0
LIU Global Control Register 1	LIUGCR1	0x0FE1
LIU Global Control Register 2	LIUGCR2	0x0FE2
LIU Global Control Register 3	LIUGCR3	0x0FE4
LIU Global Control Register 4	LIUGCR4	0x0FE9
LIU Global Control Register 5	LIUGCR5	0x0FEA
Reserved	-	0x0FEB - 0x0FFF

1.0 REGISTER DESCRIPTIONS - T1 MODE

TABLE 2: CLOCK SELECT REGISTER(CSR) **HEX ADDRESS: 0xn100**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	LCV Insert	R/W	0	**Line Code Violation Insertion** This bit is used to force a Line Code Violation (LCV) on the transmit output of TTIP/TRING. A “0” to “1” transition on this bit will cause a single LCV to be inserted on the transmit output of TTIP/TRING.
6	Set T1 Mode	R/W	0	**T1 Mode select** This bit is used to program the individual channel to operate in either T1 or E1 mode. 0 = Configures the selected channel to operate in E1 mode. 1 = Configures the selected channel to operate in T1 mode.
5	Sync All Transmitters to 8kHz	R/W	0	**Sync All Transmit Framers to 8kHz** This bit permits the user to configure each of the eight (8) Transmit T1 Framer blocks to synchronize their “transmit output” frame alignment with the 8kHz signal that is derived from the MCLK PLL, as described below. 0 - Disables the “Sync all Transmit Framers to 8kHz” feature for all 8 channels. 1 - Enables the “Sync all Transmit Framers to 8kHz” feature for all 8 channels. **NOTE:** *Writing to this bit in register 0x0100 will enable this feature for all 8 channels.* **NOTE:** *This bit is only active if the MCLK PLL is used as the “Timing Source” for the Transmit T1 Framer” blocks. CSS[1:0] of this register allows users to select the transmit source of the framer.*
4	Clock Loss Detect	R/W	1	**Clock Loss Detect Enable/Disable Select** This bit enables a clock loss protection feature for the Framer whenever the recovered line clock is used as the timing source for the transmit section. If the LIU loses clock recovery, the Clock Distribution Block will detect this occurrence and automatically begin to use the internal clock derived from MCLK PLL as the Transmit source, until the LIU is able to regain clock recovery. 0 = Disables the clock loss protection feature. 1 = Enables the clock loss protection feature. **NOTE:** *This bit needs to be enabled in order to detect the clock closs detection interrupt status (address: 0xnB00, bit 5)*
3:2	Reserved	R/W	00	**Reserved**

TABLE 2: CLOCK SELECT REGISTER(CSR) HEX ADDRESS: 0xn100

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>1:0</td><td>CSS[1:0]</td><td>R/W</td><td>01</td><td>
Clock Source Select
These bits select the timing source for the Transmit T1 Framer block. These bits can also determine the direction of TxSERCLK, TxSYNC, and TxMSYNC in base rate operation mode (1.544MHz Clock mode).
In Base Rate (1.544MHz Clock Mode):
<table>
<tr><th>CSS[1:0]</th><th>TRANSMIT SOURCE FOR THE TRANSMIT T1 FRAMER BLOCK</th><th>DIRECTION OF TXSERCLK</th></tr>
<tr><td>00/11</td><td>Loop Timing Mode
The recovered line clock is chosen as the timing source.</td><td>Output</td></tr>
<tr><td>01</td><td>External Timing Mode
The Transmit Serial Input Clock from the TxSERCLK_n input pin is chosen as the timing source.</td><td>Input</td></tr>
<tr><td>10</td><td>Internal Timing Mode
The MCLK PLL is chosen as the timing source.</td><td>Output</td></tr>
</table>
<i>NOTE: TxSYNC/TxMSYNC can be programmed as input or output depending on the setting of SYNC INV bit in Register Address 0xn109, bit 4. Please see Register Description for the Synchronization Mux Register (SMR - 0xn109) Table 10.</i>
<i>NOTES: In High-Speed or multiplexed modes, TxSERCLK, TxSYNC, and TxMSYNC are all configured as INPUTS only.</i>
</td></tr>
</table>

TABLE 3: LINE INTERFACE CONTROL REGISTER (LICR) **HEX ADDRESS: 0XN101**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>7</td><td>FORCE_LOS</td><td>R/W</td><td>0</td><td>Force Transmit LOS (To the Line Side)
This bit permits the user to configure the transmit direction circuitry (within the channel) to transmit the LOS pattern to the remote terminal equipment, as described below.
0 - Configures the transmit direction circuitry to transmit “normal” traffic.
1 - Configures the transmit direction circuitry to transmit the LOS Pattern.</td></tr>
<tr><td>6</td><td>SR</td><td>R/W</td><td>0</td><td>Single Rail Mode
This bit can only be set if the LIU Block is also set to single rail mode. See Register 0x0FE0, bit 7.
0 - Dual Rail
1 - Single Rail</td></tr>
<tr><td>5:4</td><td>LB[1:0]</td><td>R/W</td><td>00</td><td>Framer Loopback Selection
These bits are used to select any of the following loop-back modes for the framer section. For LIU loopback modes, see the LIU configuration registers.
<table>
<tr><th>LB[1:0]</th><th>TYPES OF LOOPBACK SELECTED</th></tr>
<tr><td>00</td><td>Normal Mode (No LoopBack)</td></tr>
<tr><td>01</td><td>Framer Local LoopBack:
When framer local loopback is enabled, the transmit PCM input data is looped back to the receive PCM output data. The receive input data at RTIP/RRING is ignored while an All Ones Signal is transmitted out to the line interface.</td></tr>
<tr><td>10</td><td>Framer Far-End (Remote) Line LoopBack:
When framer remote loopback is enabled, the digital data enters the framer interface, however does not enter the framing blocks. The receive digital data from the LIU is allowed to pass through the LIU Decoder/ Encoder circuitry before returning to the line interface.</td></tr>
<tr><td>11</td><td>Framer Payload LoopBack:
When framer payload loopback is enabled, the raw data within the receive time slots are looped back to the transmit framer block where the data is re-framed according to the transmit timing.</td></tr>
</table>
</td></tr>
<tr><td>3:2</td><td>Reserved</td><td>R/W</td><td>0</td><td>Reserved</td></tr>
</table>

TABLE 3: LINE INTERFACE CONTROL REGISTER (LICR) **HEX ADDRESS: 0XN101**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	Encode B8ZS	R/W	0	**Encode AMI or B8ZS/HDB3 Line Code Select** This bit enables or disables the B8ZS/HDB3 encoder on the transmit path. 0 = Enables the B8ZS encoder. 1 = Disables the B8ZS encoder. ***NOTE:*** *When B8ZS encoder is disabled, AMI line code is used.*
0	Decode AMI/B8ZS	R/W	0	**Decode AMI or B8ZS/HDB3 Line Code Select** This bit enables or disables the B8ZS/HDB3 decoder on the receive path. 0 = Enables the B8ZS decoder. 1 = Disables the B8ZS decoder. ***NOTE:*** *When B8ZS decoder is disabled, AMI line code is received.*

TABLE 4: GENERAL PURPOSE INPUT/OUTPUT 0 CONTROL REGISTER(GPIOCR0) HEX ADDRESS: 0X0102

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-4	GPIO0_3DIR GPIO0_2DIR GPIO0_1DIR GPIO0_0DIR	R/W	1111	**GPIO0_3/GPIO0_2/GPIO0_1/GPIO0_0 Direction** These bits permit the user to define the General Purpose I/O Pins, GPIO0_3/GPIO0_2/GPIO0_1/GPIO0_0 as either Input pins or Output pins, as described below. 0 – Configures GPIO0_3/GPIO0_2/GPIO0_1/GPIO0_0 to function as input pins. 1 – Configures GPIO0_3/GPIO0_2/GPIO0_1/GPIO0_0 to function as output pins. **1.** If GPIO0_3/GPIO0_2/GPIO0_1/GPIO0_0 are configured to function as input pins, then the user can monitor the state of these input pins by reading out the state of Bit 3-0 (GPIO0_3/GPIO0_2/GPIO0_1/GPIO0_0) within this register. **2.** If GPIO0_3/GPIO0_2/GPIO0_1/GPIO0_0 are configured to function as output pins, then the user can control the state of these output pins by writing the appropriate value into Bit 3-0 (GPIO0_3/GPIO0_2/GPIO0_1/GPIO0_0) within this register.
3-0	GPIO0_3 GPIO0_2 GPIO0_1 GPIO0_0	R/W	0000	**GPIO0_3/GPIO0_2/GPIO0_1/GPIO0_0 Control** The exact function of this bit depends upon whether General Purpose I/O Pins, GPIO0_3/GPIO0_2/GPIO0_1/GPIO0_0 have been configured to function as input or output pins, as described below. **If GPIO0_3/GPIO0_2/GPIO0_1/GPIO0_0 are configured to function as input pins:** If GPIO0_3/GPIO0_2/GPIO0_1/GPIO0_0 are configured to function as input pins, then the user can monitor the state of the corresponding input pin by reading out the state of these bits. ***NOTE:*** *If GPIO0_3/GPIO0_2/GPIO0_1/GPIO0_0 are configured to function as input pins, then writing to this particular register will have no effect on the state of this pin.* **If GPIO0_3/GPIO0_2/GPIO0_1/GPIO0_0 are configured to function as output pins:** If GPIO0_3/GPIO0_2/GPIO0_1/GPIO0_0 are configured to function as output pins, then the user can control the state of the corresponding output pin by writing the appropriate value to these bits. ***NOTE:*** GPIO0_3/GPIO0_2/GPIO0_1/GPIO0_0 *can be configured to function as input or output pins, by writing the appropriate value to Bit 7-4 (GPIO0_3DIR/GPIO0_2DIR/GPIO0_1DIR/GPIO0_0DIR) within this register.*

TABLE 5: GENERAL PURPOSE INPUT/OUTPUT 1 CONTROL REGISTER(GPIOCR1) HEX ADDRESS: 0X4102

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-4	GPIO1_3DIR GPIO1_2DIR GPIO1_1DIR GPIO1_0DIR	R/W	0000	**GPIO1_3/GPIO1_2/GPIO1_1/GPIO1_0 Direction** These bits permit the user to define the General Purpose I/O Pins, GPIO1_3/GPIO1_2/GPIO1_1/GPIO1_0 as either Input pins or Output pins, as described below. 0 – Configures GPIO1_3/GPIO1_2/GPIO1_1/GPIO1_0 to function as input pins. 1 – Configures GPIO1_3/GPIO1_2/GPIO1_1/GPIO1_0 to function as output pins. **1.** If GPIO1_3/GPIO1_2/GPIO1_1/GPIO1_0 are configured to function as input pins, then the user can monitor the state of these input pins by reading out the state of Bit 3-0 (GPIO1_3/GPIO1_2/GPIO1_1/GPIO1_0) within this register. **2.** If GPIO1_3/GPIO1_2/GPIO1_1/GPIO1_0 are configured to function as output pins, then the user can control the state of these output pins by writing the appropriate value into Bit 3-0 (GPIO1_3/GPIO1_2/GPIO1_1/GPIO1_0) within this register.
3-0	GPIO1_3 GPIO1_2 GPIO1_1 GPIO1_0	R/W	0000	**GPIO1_3/GPIO1_2/GPIO1_1/GPIO1_0 Control** The exact function of this bit depends upon whether General Purpose I/O Pins, GPIO1_3/GPIO1_2/GPIO1_1/GPIO1_0 have been configured to function as input or output pins, as described below. **If GPIO1_3/GPIO1_2/GPIO1_1/GPIO1_0 are configured to function as input pins:** If GPIO1_3/GPIO1_2/GPIO1_1/GPIO1_0 are configured to function as input pins, then the user can monitor the state of the corresponding input pin by reading out the state of these bits. ***NOTE:*** *If* GPIO1_3/GPIO1_2/GPIO1_1/GPIO1_0 *are configured to function as input pins, then writing to this particular register will have no effect on the state of this pin.* **If GPIO1_3/GPIO1_2/GPIO1_1/GPIO1_0 are configured to function as output pins:** If GPIO1_3/GPIO1_2/GPIO1_1/GPIO1_0 are configured to function as output pins, then the user can control the state of the corresponding output pin by writing the appropriate value to these bits. ***NOTE:*** *GPIO1_3/GPIO1_2/GPIO1_1/GPIO1_0 can be configured to function as input or output pins, by writing the appropriate value to Bit 7-4 (GPIO1_3DIR/GPIO1_2DIR/GPIO1_1DIR/GPIO1_0DIR) within this register.*

TABLE 6: FRAMING SELECT REGISTER (FSR) **HEX ADDRESS: 0xn107**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Signaling update on Superframe Boundaries	R/W	0	**Enable Robbed-Bit Signaling Update on Superframe Boundary on Both Transmit and Receive Direction** This bit enables or disables robbed-bit signaling update on the superframe boundary for both the transmit and receive side of the framer. **On the Receive Side:** If signaling update is enabled, signaling data on the receive side (RxSIG pin and Signaling Array Register - RSAR) will be updated on the superframe boundary, otherwise, signaling data will be updated as soon as it is received. **On the Transmit Side:** If signaling update is enabled, any signaling data changes on the transmit side will be transmitted on the superframe boundary, otherwise, signaling data will be transmitted as soon as it is changed. 0 - Disables the signaling update feature for both transmit and receive. 1 - Enables the signaling update feature for both transmit and receive.
6	Force CRC Errors	R/W	0	**Force CRC Errors (To the Line Side)** This bit permits the user to force the Transmit T1 Framer block to transmit CRC errors within the outbound T1 data-stream, as depicted below. 0 - Disables CRC error transmission on the outbound T1 stream. 1 - Enables CRC error transmission on the outbound T1 stream.
5	J1_MODE	R/W	0	**J1 Mode** This bit is used to configure the device in J1 mode. Once the device is configured in J1 mode, the following two changes will happen: **1.** CRC calculation is done in J1 format. The J1 CRC6 calculation is based on the actual values of all 4632 bits in a T1 multiframe including Fe bits instead of assuming all Fe bits to be a one in T1 format. **2.** Receive and Transmit Yellow Alarm signal format is interpreted per the J1 standard. (J1-SF or J1-ESF) 0 - Configures the device in T1 mode. (Default) 1 - Configures the device in J1 mode. ***NOTE:*** *Users can select between J1-SF or J1-ESF by setting this bit and the T1 Framing Mode Select Bits[2:0] (Bits 2-0 within this register).*
4	ONEONLY	R/W	0	**Allow Only One Sync Candidate** This bit is used to specify one of the synchronization criteria that the Receive T1 Framer block employs. 0 - Allows the Receive T1 Framer to select any one of the winners in the matching process when there are two or more valid synchronization patterns appear in the required time frame. 1 - Allows the Receive T1 Framer to declare success of match when there is only one candidate left in the required time frame.

TABLE 6: FRAMING SELECT REGISTER (FSR) HEX ADDRESS: 0xn107

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>3</td><td>FASTSYNC</td><td>R/W</td><td>0</td><td>Faster Sync Algorithm
This bit is used to specify one of the synchronization criteria that the Receive T1 Framer block employs. If this “Faster Sync Algorithm” is enabled, the Receive T1 Framer Block will declare synchronization earlier. The table below specifies the number of consecutive frames with correct F-bits that the T1 Receive framer must receive in order to declare “SYNC” when FASTSYNC is enabled or disabled.
<table>
<tr><th>Framing</th><th>FastSync = 0</th><th>FastSync = 1</th></tr>
<tr><td>ESF</td><td>96</td><td>48</td></tr>
<tr><td>SF</td><td>48</td><td>24</td></tr>
<tr><td>N</td><td>48</td><td>24</td></tr>
<tr><td>SLC ® 96</td><td>48</td><td>24</td></tr>
</table>
0 - Disables FASTSYNC feature.
1 - Enables FASTSYNC feature.</td></tr>
<tr><td>2-0</td><td>FSI[2:0]</td><td>R/W</td><td>000</td><td>T1 Framing Mode Select [2:0]
These three bits permit the user to select the exact T1 framing format that the channel is to operate in.
Bit 2 is MSB and Bit 0 is LSB. The following table shows the five different framing formats that can be selected by configuring these three bits accordingly.
NOTE: <i>Changing Framing formats 'on the fly' will cause the Receive T1 Framer block to undergo a “Reframe” event.</i>
<table>
<tr><th>Framing</th><th>FS[2]</th><th>FS[1]</th><th>FS[0]</th></tr>
<tr><td>ESF</td><td>0</td><td>X</td><td>X</td></tr>
<tr><td>SF</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>N</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>T1DM</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>SLC®96</td><td>1</td><td>0</td><td>0</td></tr>
</table></td></tr>
</table>

TABLE 7: ALARM GENERATION REGISTER (AGR) HEX ADDRESS: 0xn108

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Yellow Alarm - One Second Rule	R/W	0	**One-Second Yellow Alarm Rule Enforcement** This bit is used to enforce the one-second yellow alarm rule according to the yellow alarm (RAI) transmission duration per the ANSI standards. **If the one second alarm rule is enforced, the following will happen:** **1.** RAI will be transmitted for at least one second for both ESF and SF. **2.** There must be a minimum of one second delay between termination of the first RAI and the initiation of a subsequent RAI. **3.** ALARM_ENB bit (see description of bit 6 of this register) controls the duration of RAI. **4.** YEL[0] & YEL[1] (see description of bits 5-4 of this register) controls the format of RAI. **If the one second alarm rule is NOT enforced, the following will happen:** **1.** RAI will be transmitted for at least one second for ESF and SF. **2.** Minimum one second delay between termination of the first RAI and the initiation of the subsequent RAI is NOT enforced. **3.** YEL[0] and YEL[1] bits (see description of bits 5-4 of this register) are used to control the duration AND the format of RAI transmission. 0 - The one-second yellow alarm rule is NOT enforced. 1 - The one-second yellow alarm rule is enforced. **NOTE:** *When setting this bit to '0', yellow alarm transmission will be backward compatible with the XRT86L38 device. XRT86L38 does not support the one-second yellow alarm rule.*
6	ALARM_ENB	R/W	0	**Yellow Alarm Transmission Enable** This bit is used to control the duration of yellow alarm (RAI) when the one-second yellow alarm rule is enforced (bit 7 of this register set to'1'). When the one-second yellow alarm rule is not enforced (bit 7 of this register set to'0'), the duration of the RAI is controlled by the YEL[0] and YEL[1] bits (bits 5-4 of this register). **If the one-second alarm rule is enforced:** 0 - Stop the transmission of yellow alarm (see description of bits 5-4). 1 - Start the transmission of yellow alarm (see description of bits 5-4). **NOTE:** *This bit has no function if the one second alarm rule is not enforced.*

TABLE 7: ALARM GENERATION REGISTER (AGR) **HEX ADDRESS: 0xn108**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
5-4	YEL[1:0]	R/W	00	**Yellow Alarm (RAI) Duration and Format** The exact function of these bits depends on whether or not the one-second yellow alarm rule is enforced. (Bit 7 of this register). The decoding of these bits are explained in Table 8 and Table 9 below.

TABLE 8: YELLOW ALARM DURATION AND FORMAT WHEN ONE SECOND RULE IS NOT ENFORCED

YEL[1:0]	YELLOW ALARM DURATION AND FORMAT
00	Disable the transmission of yellow alarm
01	**SF or N mode:** RAI is transmitted as bit 2 = 0 (second MSB) in all DS0 data channel. **T1DM mode:** RAI is transmitted as Y-bit = 0 (6th bit in the SYNC byte). **ESF mode:** **1.** If YEL[0] bit is set 'high' for a duration shorter or equal to the time required to transmit 255 patterns of 1111_1111_0000_0000 on the 4-kbit/s data link bits (M1-M12), RAI is transmitted for 255 patterns.of 1111_1111_0000_0000 (approximately 1 second) **2.** If YEL[0] bit is set 'high' for a duration longer than the time required to transmit 255 patterns of 1111_1111_0000_0000 on the 4-kbit/s data link bits (M1-M12), RAI transmission continues until YEL[0] bit is set 'low'. **3.** If YEL[0] bit forms another pulse during the RAI transmission, it resets the pattern counter and extends the RAI duration for another 255 patterns of 1111_1111_0000_0000. (approximately 1 second)
10	**SF mode:** RAI is transmitted as a "1" in the Fs bit of frame 12 (This is RAI for J1 SF standard). **T1DM mode**: RAI is transmitted as Y-bit = 0 (6th bit in the SYNC byte). **ESF mode**: RAI is controlled by the duration of YEL[1] bit. This allows continuous RAI of any length.
11	**SF, N, and T1DM mode:** RAI format is the same as described above when YEL[1:0] is set to'01'. **ESF mode:** RAI duration is the same as described above when YEL[1:0] is set to'01', except that format of RAI is transmitted as 255 patterns of 1111_1111_1111_1111 (sixteen ones) on the 4kbits/s data link bits instead of 255 patterns of 1111_1111_0000_0000. **NOTE:** *255 patterns of 1111_1111_1111_111 is the J1 ESF RAI standard)*

TABLE 7: ALARM GENERATION REGISTER (AGR) HEX ADDRESS: 0xn108

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
5-4	YEL[1:0]	R/W	00	(**Continued**)

TABLE 9: YELLOW ALARM FORMAT WHEN ONE SECOND RULE IS ENFORCED

YEL[1:0]	YELLOW ALARM FORMAT
00	Disable the transmission of yellow alarm
01	**SF or N mode**: RAI is transmitted as bit 2 = 0 (second MSB) in all DS0 data channel. **T1DM mode:** RAI is transmitted as Y-bit = 0 (6th bit in the SYNC byte). **ESF mode:** YEL[1:0] controls the format of RAI. When YEL[1:0] is set to'01', RAI is transmitted as 255 patterns of 1111_1111_0000_0000 on the 4-kbit/s data link (M1-M12) (approximately 1 second). ALARM_ENB (Bit 6 of this register) controls the duration of RAI as described below: **1.** If ALARM_ENB bit is set 'high' for a duration shorter or equal to the time required to transmit 255 pattern of 1111_1111_0000_0000 on the 4-kbit/s data link (M1-M12), RAI is transmitted for 255 patterns. (approximately 1 second) **2.** If ALARM_ENB bit is set 'high' for a duration longer than the time required to transmit 255 patterns of 1111_1111_0000_0000 on the 4-kbit/s data link (M1-M12), RAI continues until ALARM_ENB bit is set 'low'. **3.** If ALARM_ENB forms another pulse during an alarm transmission, it resets the pattern counter and extends the RAI duration for another 255 patterns.(approximately 1 second) ***NOTE:*** *A minimum of one second delay between termination of the first RAI and the initiation of a subsequent RAI is enforced.*
10	**SF mode:** RAI is transmitted as a "1" in the Fs bit of frame 12 (This is RAI for J1 SF standard). **T1DM mode**: RAI is transmitted as Y-bit = 0 (6th bit in the SYNC byte). **ESF mode**: RAI is controlled by the duration of ALARM_ENB bit. This allows continuous RAI of any length.
11	**SF, N, and T1DM mode:** RAI format is the same as described above when YEL[1:0] is set to'01'. **ESF mode:** RAI duration is the same as described above when YEL[1:0] is set to'01', except that format of RAI is transmitted as 255 patterns of 1111_1111_1111_1111 on the 4kbits/s data link bits (J1 ESF standard) instead of 255 patterns of 1111_1111_0000_0000.

TABLE 7: ALARM GENERATION REGISTER (AGR) **HEX ADDRESS: 0xn108**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3-2	Transmit AIS Pattern Select[1:0]	R/W	00	**Transmit AIS Pattern Select[1:0]:** These two bits permit the user to do the following. 1. To select the appropriate AIS Pattern that the Transmit T1 Framer block will transmit to the remote terminal equipment, and 2. To command (via Software Control) the Transmit T1 Framer block to transmit that particular AIS Pattern to the remote terminal equipment, as depicted below.
1-0	AIS Defect Declaration Criteria [1:0]	R/W	00	**AIS Defect Declaration Criteria[1:0]:** These bits permit the user to specify the types of AIS Patterns that the Receive T1 Framer block must detect before it will declare the AIS defect condition.

AISG[1:0]	TYPES OF AIS PATTERNS TRANSMITTED
00/10	**Disable AIS Alarm Generation** The Transmit T1 Framer block will transmit “normal” T1 traffic to the remote terminal equipment.
01	**Enable Unframed AIS Alarm Generation** Transmit T1 Framer block will transmit an Unframed All Ones Pattern, as an AIS Pattern.
11	**Enable Framed AIS Alarm Generation** Transmit T1 Framer block will transmit a Framed, All Ones Pattern, as the AIS Pattern.

NOTE: *For normal operation (e.g., to configure the Transmit T1 Framer block to transmit normal T1 traffic) the user should set this bit to “[X, 0]”*

AISD[1:0]	AIS Defect Declaration Criteria
00/10	**AIS Detection Disabled** AIS Defect Condition will NOT be declared.
01	**Enable Unframed and Framed AIS Alarm Detection** ReceiveT1 Framer block will detect both Unframed and Framed AIS pattern
11	**Enable Framed AIS Alarm Detection** Receive T1 Framer block will detect only Framed AIS pattern

TABLE 10: SYNCHRONIZATION MUX REGISTER (SMR) **HEX ADDRESS: 0xn109**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	-	-	**Reserved**
6	MFRAMEALIGN	R/W	0	**Transmit Multiframe Sync Alignment** This bit forces Transmit T1 framer block to align with the backplane multiframe boundary (TxMSYNC_n). 0 = Do not force the transmit T1 framer block to align with the TxMSYNC signal. 1 = Force the transmit T1 framer block to align with the TxMSYNC signal. ***NOTE:*** *This bit is not used in base rate (1.544MHz Clock) mode.*
5	MSYNC	R/W	O	**Transmit Super Frame Boundary** This bit provides an option to use the transmit single frame boundary (TxSYNC) as the transmit multi-frame boundary (TxMSYNC) in high speed or multiplexed modes. In 1.544MHz clock mode (base rate), the TxMSYNC is used as the transmit superframe boundary, in other clock modes (i.e. high speed or multiplexed modes), TxMSYNC is used as an input transmit clock for the backplane interface. 0 = Configures the TxSYNC as a single frame boundary. 1 = Configures the TxSYNC as a superframe boundary (TxMSYNC) in high-speed or multiplexed mode. ***NOTE:*** *This bit is not used in base rate (1.544MHz Clock) mode.*

TABLE 10: SYNCHRONIZATION MUX REGISTER (SMR) **HEX ADDRESS: 0xn109**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
4	Transmit Frame Sync Select	R/W	0	**Transmit Frame Sync Select** This bit permits the user to configure the System-Side Terminal Equipment or the T1 Transmit Framer to dictate whenever the Transmit T1 Framer block will initiate its generation and transmission of the very next T1 frame. If the system side controls, then all of the following will be true. 1. The corresponding TxSync_n and TxMSync_n pins will function as input pins. 2. The Transmit T1 Framer block will initiate its generation of a new T1 frame whenever it samples the corresponding “TxSync_n” input pin “high” (via the TxSerClk_n input clock signal). 3. The Transmit T1 Framer block will initiate its generation of a new Multiframe whenever it samples the corresponding “TxMSync_n” input pin “high”. This bit can also be used to select the direction of the transmit single frame boundary (TxSYNC) and multi-frame boundary (TxMSYNC) depending on whether TxSERCLK is chosen as the timing source for the transmit section of the framer. (CSS[1:0] = 01 in register 0xn100) **If TxSERCLK is chosen as the timing source:** 0 = Configures TxSYNC and TxMSYNC as inputs. (System Side Controls) 1 = Configures TxSYNC and TxMSYNC as outputs. (Chip Controls) **If either Recovered Line Clock, MCLK PLL is chosen as the timing source:** 0 = Configures TxSYNC and TxMSYNC as outputs. (Chip Controls) 1 = Configures TxSYNC and TxMSYNC as inputs. (System Side Controls) ***NOTE:*** *TxSERCLK is chosen as the transmit clock if CSS[1:0] of the Clock Select Register (Register Address: 0xn100) is set to b01. Recovered Clock is chosen as the transmit clock if CSS[1:0] is set to b00 or b11; Internal Clock is chosen as the transmit clock if CSS[1:0] is set to b10.*
3 - 2	Reserved	-	-	**Reserved**

TABLE 10: SYNCHRONIZATION MUX REGISTER (SMR) HEX ADDRESS: 0xn109

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	CRC-6 Bits Source Select	R/W	0	**CRC-6 Bits Source Select** This bit permits the user to specify the source of the CRC-6 bits, within the outbound T1 data-stream, as depicted below. 0 - Configures the Transmit T1 Framer block to internally compute and insert the CRC-6 bits within the outbound T1 data-stream. 1 - Configures the Transmit T1 Framer block to externally accept data from the TxSer_n input pin, and to insert this data into the CRC-6 bits within the outbound T1 data-stream. *This bit is ignored if CRC Multiframe Alignment is disabled*
0	Framing Bits Source Select	R/W	0	**Framing Bits Source Select** This bit is used to specify the source for the Framing bits that will be inserted into the outbound T1 frames. The Framing bits can be generated internally or inserted from the transmit serial input pin. (TxSER_n input pin) 0 = Configures the Transmit T1 Framer block to internally generate and insert the Framing bits into the outbound T1 data stream. 1 = Configures the Transmit T1 Framer block to externally accept framing bits from the TxSer_n input pin, and to insert this data to the outbound T1 data-stream.

TABLE 11: TRANSMIT SIGNALING AND DATA LINK SELECT REGISTER (TSDLSR) **HEX ADDRESS:0xn10A**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>7</td><td>Reserved</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>6</td><td>Reserved</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>5-4</td><td>TxDLBW[1:0]</td><td>R/W</td><td>00</td><td>Transmit Data Link Bandwidth[1:0]
These two bits are used to select the bandwidth for data link message transmission. Data Link messages can be transmitted at a 4kHz rate or at a 2kHz rate on odd or even framing bits depending on the configuration of these three bits. The table below specifies the four different configurations.
<table>
<tr><th>TxDLBW[1:0]</th><th>TRANSMIT DATA LINK BANDWIDTH SELECTED</th></tr>
<tr><td>00</td><td>Data link bits are inserted in every frame. Facility Data Link Bits (FDL) is a 4kHz data link channel.</td></tr>
<tr><td>01</td><td>Data link bits are inserted in every other frame. Facility Data Link Bits (FDL) is a 2kHz data link channel carried by odd framing bits (Frames 1,5,9.....)</td></tr>
<tr><td>10</td><td>Data link bits are inserted in every other frame. Facility Data Link Bits (FDL) is a 2kHz data link channel carried by even framing bits (Frames 3,7,11.....)</td></tr>
<tr><td>11</td><td>Reserved</td></tr>
</table>
NOTE: <i>This bit only applies to T1 ESF framing format. For SLC96 and N framing formats, FDL is a 4kHz data link channel. For T1DM, FDL is a 8kHz data link channel.</i></td></tr>
<tr><td>3-2</td><td>TxDE[1:0]</td><td>R/W</td><td>00</td><td>Transmit D/E TimeSlot Source Select[1:0]:
These two bits specify the source for transmit D/E time slots. The table below shows the different sources from which D/E time slots can be inserted.
<table>
<tr><th>TxDE[1:0]</th><th>SOURCE FOR TRANSMIT D/E TIMESLOTS</th></tr>
<tr><td>00</td><td>TxSER_n input pin - The D/E time slots are inserted from the transmit serial data input pin (TxSER_n) pin.</td></tr>
<tr><td>01</td><td>Transmit LAPD Controller - The D/E time slots are inserted from LAPD Controller.</td></tr>
<tr><td>10</td><td>Reserved</td></tr>
<tr><td>11</td><td>TxFRTD_n - The D/E time slots are inserted from the transmit fractional input pin.</td></tr>
</table></td></tr>
</table>

TABLE 11: TRANSMIT SIGNALING AND DATA LINK SELECT REGISTER (TSDLSR) **HEX ADDRESS:0xn10A**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>1-0</td><td>TxDL[1:0]</td><td>R/W</td><td>00</td><td>Transmit Data Link Source Select [1:0]
These two bits specify the source for data link bits that will be inserted in the outbound T1 frames. The table below shows the three different sources from which data link bits can be inserted.
<table>
<tr><th>TxDL[1:0]</th><th>SOURCE FOR DATA LINK BITS</th></tr>
<tr><td>00</td><td>Transmit LAPD Controller #1 / SLC96 Buffer - The Data Link bits are inserted from the Transmit LAPD Controller #1 or SLC96 Buffer.
<i>NOTE:</i> <i>LAPD Controller #1 is the only LAPD controller that can be used to transport LAPD messages through the data link bits</i></td></tr>
<tr><td>01</td><td>TxSER_n input pin - The Data Link bits are inserted from the transmit serial data input pin (TxSER_n) pin.</td></tr>
<tr><td>10</td><td>TxOH_n input pin - The Data Link bits are inserted from the transmit overhead input pin. (TxOH_n)</td></tr>
<tr><td>11</td><td>Data Link bits are forced to 1.</td></tr>
</table>
</td></tr>
</table>

TABLE 12: FRAMING CONTROL REGISTER (FCR) **HEX ADDRESS: 0xn10B**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reframe	R/W	0	**Force Reframe** A '0' to '1' transition will force the Receive T1 Framer to restart the synchronization process. This bit field is automatically cleared (set to 0) after frame synchronization is reached.
6	Framing with CRC Checking	R/W	1	**Framing with CRC Checking in ESF** This bit permits the user to include CRC verification as a part of the "T1/ESF Framing Alignment" process. If the user enables this feature, then the Receive T1 Framer block will also check and verify that the incoming T1 data-stream contains correct CRC data, prior to declaring the "In-Frame" condition. 0 - CRC Verification is NOT included in the "Framing Alignment" process. 1 - Receive T1 Framer block will also check for correct CRC values prior to declaring the "In-Frame" condition.
5-3	LOF Tolerance[2:0]	R/W	000	**LOF Defect Declaration Tolerance[2:0]:** These bits along with the LOF_RANGE[2:0] bits are used to define the LOF Defect Declaration criteria. The Receive T1 Framer block will declare the LOF defect condition anytime it detects "LOF_Tolerance[2:0]" out of "LOF_Range[2:0] framing bit errors within the incoming T1 data-stream. The recommended LOF_TOLR value is 2. ***NOTE:*** *A "0" value for LOF_TOLR is internally blocked. A LOF_TOLR value must be specified.*
2-0	LOF_Range[2:0]	R/W	011	**LOF Defect Declaration Range[2:0]:** These bits along with the "LOF_Tolerance[2:0] bits are used to define the "LOF Defect Declaration" criteria. The Receive T1 Framer block will declare the LOF Defect condition anytime it has received "LOF_Tolerance[2:0] out of "LOF_Range[2:0] framing bit errors, within the incoming T1 data-stream. The recommended LOF_ANG value is 5. ***NOTE:*** *A "0" value for LOF_RANG is internally blocked. A LOF_RANG value must be specified.*

TABLE 13: RECEIVE SIGNALING & DATA LINK SELECT REGISTER (RSDLSR) HEX ADDRESS: 0xn10C

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>7</td><td>Reserved</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>6</td><td>Reserved</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>5-4</td><td>RxDLBW[1:0]</td><td>R/W</td><td>00</td><td>Receive Data Link Bandwidth[1:0]:
These two bits select the bandwidth for data link message reception. Data Link messages can be received at a 4kHz rate or at a 2kHz rate on odd or even framing bits depending on the configuration of these bits. The table below specifies the different configurations.
<table>
<tr><th>RxDLBW[1:0]</th><th>RECEIVE DATA LINK BANDWIDTH SELECTED</th></tr>
<tr><td>00</td><td>Received Data link bits are extracted in every frame. Facility Data Link Bits (FDL) is a 4kHz data link channel.</td></tr>
<tr><td>01</td><td>Received Data link bits are extracted in every other frame. Facility Data Link Bits (FDL) is a 2kHz data link channel carried by odd framing bits (Frames 1,5,9.....)</td></tr>
<tr><td>10</td><td>Received Data link bits are extracted in every other frame. Facility Data Link Bits (FDL) is a 2kHz data link channel carried by even framing bits (Frames 3,7,11.....)</td></tr>
<tr><td>11</td><td>Reserved</td></tr>
</table>
NOTE: <i>This bit only applies to T1 ESF framing format. For SLC96 and N framing formats, FDL is a 4kHz data link channel. For T1DM, FDL is a 8kHz data link channel.</i></td></tr>
<tr><td>3-2</td><td>RxDE[1:0]</td><td>R/W</td><td>00</td><td>Receive D/E Time-Slot Destination Select[1:0]:
These bits permit the user to specify the “destination” circuitry that will receive and process the D/E-Time-slot within the incoming T1 data-stream.
<table>
<tr><th>RxDE[1:0]</th><th>DESTINATION CIRCUITRY FOR RECEIVE D/E TIME-SLOT</th></tr>
<tr><td>00</td><td>RxSER_n output pin - The D/E time slots are output to the receive serial data output pin (RxSER_n) pin.</td></tr>
<tr><td>01</td><td>Receive LAPD Controller Block - The D/E time slots are output to Receive LAPD Controller Block.</td></tr>
<tr><td>10</td><td>Reserved</td></tr>
<tr><td>11</td><td>RxFRTD_n output pin- The D/E time slots are output to the receive fractional output pin.</td></tr>
</table></td></tr>
</table>

TABLE 13: RECEIVE SIGNALING & DATA LINK SELECT REGISTER (RSDLSR) **HEX ADDRESS: 0xn10C**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1-0	RxDL[1:0]	R/W	00	**Receive Data-Link Destination Select[1:0]:** These bits specify the destination circuitry, that is used to process the Data-Link data, within the incoming T1 data-stream.

RXDL[1:0]	DESTINATION CIRCUITRY FOR RECEIVE DATA-LINK
00	**Receive LAPD Controller Block # 1 and RxSER_n** - The Data Link bits are routed to the Receive LAPD Controller block #1 and the RxSER_n output pin ***NOTE:*** *LAPD Controller #1 is the only LAPD controller that can be used to extract LAPD messages through the data link bits*
01	**RxSER_n**- The Data Link bits are routed to the RxSER_n output pin.
10	**RxOH_n and RxSER_n** - The Data Link bits are routed to the RxOH_n and RxSER_n output pins.
11	**Data Link bits are forced to 1**.

TABLE 14: RECEIVE SIGNALING CHANGE REGISTER 0 (RSCR 0) **HEX ADDRESS: 0xn10D**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Ch. 0	RUR	0	These bits indicate whether the Channel Associated signaling data, associated with Time-Slots 0 through 7 within the incoming T1 data-stream, has changed since the last read of this register, as depicted below. 0 - CAS data (for Time-slots 0 through 7) has NOT changed since the last read of this register. 1 - CAS data (for Time-slots 0 through 7) HAS changed since the last read of this register. **NOTES:** *This register is only active if the incoming T1 data-stream is using Channel Associated Signaling.*
6	Ch. 1	RUR	0	
5	Ch.2	RUR	0	
4	Ch.3	RUR	0	
3	Ch.4	RUR	0	
2	Ch.5	RUR	0	
1	Ch.6	RUR	0	
0	Ch.7	RUR	0	

TABLE 15: RECEIVE SIGNALING CHANGE REGISTER 1(RSCR 1) **HEX ADDRESS: 0xn10E**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Ch.8	RUR	0	These bits indicate whether the Channel Associated signaling data, associated with Time-Slots 8 through 15 within the incoming T1 data-stream, has changed since the last read of this register, as depicted below. 0 - CAS data (for Time-slots 8 through 15) has NOT changed since the last read of this register. 1 - CAS data (for Time-slots 8 through 15) HAS changed since the last read of this register. *This register is only active if the incoming T1 data-stream is using Channel Associated Signaling.*
6	Ch.9	RUR	0	
5	Ch.10	RUR	0	
4	Ch.11	RUR	0	
3	Ch.12	RUR	0	
2	Ch.13	RUR	0	
1	Ch.14	RUR	0	
0	Ch.15	RUR	0	

TABLE 16: RECEIVE SIGNALING CHANGE REGISTER 2 (RSCR 2) **HEX ADDRESS: 0xn10F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Ch.16	RUR	0	These bits indicate whether the Channel Associated signaling data, associated with Time-Slots 16 through 23 within the incoming T1 data-stream, has changed since the last read of this register, as depicted below. 0 - CAS data (for Time-slots 16 through 23) has NOT changed since the last read of this register. 1 - CAS data (for Time-slots 16 through 23) HAS changed since the last read of this register. **NOTE:** *This register is only active if the incoming T1 data-stream is using Channel Associated Signaling.*
6	Ch.17	RUR	0	
5	Ch.18	RUR	0	
4	Ch.19	RUR	0	
3	Ch.20	RUR	0	
2	Ch.21	RUR	0	
1	Ch.22	RUR	0	
0	Ch.23	RUR	0	

TABLE 17: RECEIVE IN FRAME REGISTER (RIFR) HEX ADDRESS: 0xn112

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	In Frame	RO	0	**In Frame State** This READ-ONLY bit indicates whether the Receive T1 Framer block is currently declaring the "In-Frame" condition with the incoming T1 data-stream. 0 - Indicates that the Receive T1 Framer block is currently declaring the LOF (Loss of Frame) Defect condition. 1 - Indicates that the Receive T1 Framer block is currently declaring itself to be in the "In-Frame" condition.
6-0	Reserved	-	-	**Reserved (E1 Mode Only)**

TABLE 18: DATA LINK CONTROL REGISTER (DLCR1) HEX ADDRESS: 0xn113

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	SLC-96 Data Link Enable	R/W	0	**SLC®96 DataLink Enable** This bit permits the user to configure the channel to support the transmission and reception of the "SLC-96 type" of data-link message. 0 - Channel does not support the transmission and reception of "SLC-96" type of data-link messages. Regular SF framing bits will be transmitted. 1 - Channel supports the transmission and reception of the "SLC-96" type of data-link messages. *This bit is only active if the channel has been configured to operate in either the SLC-96 or the ESF Framing formats.*
6	MOS ABORT Disable	R/W	0	**MOS ABORT Disable:** This bit permits the user to either enable or disable the "Automatic MOS ABORT" feature within Transmit HDLC Controller # 1. If the user enables this feature, then Transmit HDLC Controller block # 1 will automatically transmit the ABORT Sequence (e.g., a zero followed by a string of 7 consecutive "1s") whenever it abruptly transitions from transmitting a MOS type of message, to transmitting a BOS type of message. If the user disables this feature, then the Transmit HDLC Controller Block # 1 will NOT transmit the ABORT sequence, whenever it abruptly transitions from transmitting a MOS-type of message to transmitting a BOS-type of message. 0 - Enables the "Automatic MOS Abort" feature 1 - Disables the "Automatic MOS Abort" feature
5	Rx_FCS_DIS	R/W	0	**Receive Frame Check Sequence (FCS) Verification Enable/Disable** This bit permits the user to configure the Receive HDLC Controller Block # 1 to compute and verify the FCS value within each incoming LAPD message frame. 0 - Enables FCS Verification 1 - Disables FCS Verification

TABLE 18: DATA LINK CONTROL REGISTER (DLCR1) HEX ADDRESS: 0xn113

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
4	AutoRx	R/W	0	**Auto Receive LAPD Message** This bit configures the Receive HDLC Controller Block #1 to discard any incoming BOS or LAPD Message frame that exactly match which is currently stored in the Receive HDLC1 buffer. 0 = Disables this “AUTO DISCARD” feature 1 = Enables this “AUTO DISCARD” feature.
3	Tx_ABORT	R/W	0	**Transmit ABORT** This bit configures the Transmit HDLC Controller Block #1 to transmit an ABORT sequence (string of 7 or more consecutive 1’s) to the Remote terminal. 0 - Configures the Transmit HDLC Controller Block # 1 to function normally (e.g., not transmit the ABORT sequence). 1 - Configures the Transmit HDLC Controller block # 1 to transmit the ABORT Sequence.
2	Tx_IDLE	R/W	0	**Transmit Idle (Flag Sequence Byte)** This bit configures the Transmit HDLC Controller Block #1 to unconditionally transmit a repeating string of Flag Sequence octets (0X7E) in the data link channel to the Remote terminal. In normal conditions, the Transmit HDLC Controller block will repeatedly transmit the Flag Sequence octet whenever there is no MOS message to transmit to the remote terminal equipment. However, if the user invokes this “Transmit Idle Sequence” feature, then the Transmit HDLC Controller block will UNCONDITIONALLY transmit a repeating stream of the Flag Sequence octet (thereby overwriting all outbound MOS data-link messages). 0 - Configures the Transmit HDLC Controller Block # 1 to transmit data-link information in a “normal” manner. 1 - Configures the Transmit HDLC Controller block # 1 to transmit a repeating string of Flag Sequence Octets (0x7E). **NOTE:** *This bit is ignored if the* Transmit *HDLC1 controller is operating in the BOS Mode - bit 0 (MOS/BOS) within this register is set to 0.*

TABLE 18: DATA LINK CONTROL REGISTER (DLCR1) **HEX ADDRESS: 0xn113**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	Tx_FCS_EN	R/W	0	**Transmit LAPD Message with Frame Check Sequence (FCS)** This bit permits the user to configure the Transmit HDLC Controller block # 1 to compute and append FCS octets to the "back-end" of each outbound MOS data-link message. 0 - Configures the Transmit HDLC Controller block # 1 to NOT compute and append the FCS octets to the back-end of each outbound MOS data-link message. 1 - Configures the Transmit HDLC Controller block # 1 TO COMPUTE and append the FCS octets to the back-end of each outbound MOS data-link message. ***NOTE:*** *This bit is ignored if the transmit HDLC1 controller has been configured to operate in the BOS mode - bit 0 (MOS/BOS) within this register is set to 0.*
0	MOS/$\overline{\text{BOS}}$	R/W	0	**Message Oriented Signaling/Bit Oriented Signaling Send** This bit permits the user to enable LAPD transmission through HDLC Controller Block # 1 using either BOS (Bit-Oriented Signaling) or MOS (Message-Oriented Signaling) frames. 0 - Transmit HDLC Controller block # 1 BOS message Send. 1 - Transmit HDLC Controller block # 1 MOS message Send. ***NOTE:*** *This is not an Enable bit. This bit must be set to "0" each time a BOS is to be sent.*

TABLE 19: TRANSMIT DATA LINK BYTE COUNT REGISTER (TDLBCR1) **HEX ADDRESS: 0xn114**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxHDLC1 BUFAvail/ BUFSel	R/W	0	**Transmit HDLC1 Buffer Available/Buffer Select** This bit has different functions, depending upon whether the user is writing to or reading from this register, as depicted below. **If the user is writing data into this register bit:** 0 - Configures the Transmit HDLC1 Controller to read out and transmit the data, residing within "Transmit HDLC1 Buffer # 0", via the Data Link channel to the remote terminal equipment. 1 - Configures the Transmit HDLC1 Controller to read out and transmit the data, residing within the "Transmit HDLC1 Buffer #1", via the Data Link channel to the remote terminal equipment. **If the user is reading data from this register bit:** 0 - Indicates that "Transmit HDLC1 Buffer # 0" is the next available buffer. In this case, if the user wishes to write in the contents of a new "outbound" Data Link Message into the Transmit HDLC1 Message Buffer, he/she should proceed to write this message into "Transmit HDLC1 Buffer # 0" - Address location: 0xn600. 1 - Indicates that "Transmit HDLC1 Buffer # 1" is the next available buffer. In this case, if the user wishes to write in the contents of a new "outbound" Data Link Message into the Transmit HDLC1 Message Buffer, he/she should proceed to write this message into "Transmit HDLC1 Buffer # 1" - Address location: 0xn700. **NOTE:** *If one of these Transmit HDLC1 buffers contain a message which has yet to be completely read-in and processed for transmission by the Transmit HDLC1 controller, then this bit will automatically reflect the value corresponding to the next available buffer when it is read. Changing this bit to the in-use buffer is not permitted.*
6-0	TDLBC[6:0]	R/W	0000000	**Transmit HDLC1 Message - Byte Count** The exact function of these bits depends on whether the Transmit HDLC 1 Controller is configured to transmit MOS or BOS messages to the Remote Terminal Equipment. **In BOS MODE:** These bit fields contain the number of repetitions the BOS message must be transmitted before the Transmit HDLC1 controller generates the Transmit End of Transfer (TxEOT) interrupt and halts transmission. If these fields are set to 00000000, then the BOS message will be transmitted for an indefinite number of times. **In MOS MODE:** These bit fields contain the length, in number of octets, of the message to be transmitted. The length of MOS message specified in these bits include header bytes such as the SAPI, TEI, Control field, however, it does not include the FCS bytes.

TABLE 20: RECEIVE DATA LINK BYTE COUNT REGISTER (RDLBCR1) **HEX ADDRESS: 0XN115**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RBUFPTR	R/W	0	**Receive HDLC1 Buffer-Pointer** This bit Identifies which Receive HDLC1 buffer contains the most recently received HDLC1 message. 0 - Indicates that Receive HDLC1 Buffer # 0 contains the contents of the most recently received HDLC message. 1 - Indicates that Receive HDLC1 Buffer # 1 contains the contents of the most recently received HDLC message.
6-0	RDLBC[6:0]	R/W	0000000	**Receive HDLC Message - byte count** The exact function of these bits depends on whether the Receive HDLC Controller Block #1 is configured to receive MOS or BOS messages. **In BOS Mode:** These seven bits contain the number of repetitions the BOS message must be received before the Receive HDLC1 controller generates the Receive End of Transfer (RxEOT) interrupt. If these bits are set to “0000000”, the message will be received indefinitely and no Receive End of Transfer (RxEOT) interrupt will be generated. **In MOS Mode:** These seven bits contain the size in bytes of the HDLC1 message that has been received and written into the Receive HDLC buffer. The length of MOS message shown in these bits include header bytes such as the SAPI, TEI, Control field, AND the FCS bytes.

TABLE 21: SLIP BUFFER CONTROL REGISTER (SBCR) **HEX ADDRESS: 0xn116**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxSB_ISFIFO	R/W	0	**Transmit Slip Buffer Mode** This bit permits the user to configure the Transmit Slip Buffer to function as either “Slip-Buffer” Mode, or as a “FIFO”, as depicted below. 0 - Configures the Transmit Slip Buffer to function as a “Slip-Buffer”. 1 - Configures the Transmit Slip Buffer to function as a “FIFO”. ***NOTE:*** *Transmit slip buffer is only used in high-speed or multiplexed mode where TxSERCLKn must be configured as inputs only. Users must make sure that the “Transmit Direction” timing (i.e. TxMSYNC) and the TxSerClk input clock signal are synchronous to prevent any transmit slips from occuring.* ***NOTE:*** *The data latency is dictated by FIFO Latency in the FIFO Latency Register (register 0xn117).*
6-5	Reserved	-	-	**Reserved**
4	SB_FORCESF	R/W	0	**Force Signaling Freeze** This bit permits the user to freeze any signaling update on the RxSIGn output pin as well as the Receive Signaling Array Register -RSAR (0xn500-0xn51F) until this bit is cleared. 0 = Signaling on RxSIG and RSAR is updated immediately. 1 = Signaling on RxSIG and RSAR is not updated until this bit is set to ‘0’.
3	SB_SFENB	R/W	0	**Signal Freeze Enable Upon Buffer Slips** This bit enables signaling freeze for one multiframe after the receive buffer slips. If signaling freeze is enabled, then the “Receive Channel” will freeze all signaling updates on RxSIG pin and RSAR (0xn500-0xn51F) for at least “one-multiframe” period, after a “slip-event” has been detected within the “Receive Slip Buffer”. 0 = Disables signaling freeze for one multi-frame after receive buffer slips. 1 = Enables signaling freeze for one multi-frame after receive buffer slips.
2	SB_SDIR	R/W	1	**Slip Buffer (RxSync) Direction Select** This bit permits user to select the direction of the receive frame boundary (RxSYNC) signal if the receive buffer is enabled. (i.e. SB_ENB[1:0] = 01 or 10). If slip buffer is bypassed, RxSYNC is always an output pin. 0 = Selects the RxSync signal as an output 1 = Selects the RxSync signal as an input

TABLE 21: SLIP BUFFER CONTROL REGISTER (SBCR) **HEX ADDRESS: 0xn116**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>1</td><td>SB_ENB(1)</td><td>R/w</td><td>0</td><td rowspan="2">Receive Slip Buffer Mode Select
These bits select modes of operation for the receive slip buffer. These two bits also select the direction of RxSERCLK and RxSYNC in base clock rate (2.048MHz). The following table shows the corresponding slip buffer modes as well as the direction of the RxSYNC/RxSERCLK according to the setting of these two bits.
<table>
<tr><th>SB_ENB [1:0]</th><th>RECEIVE SLIP BUFFER MODE SELECT</th><th>DIRECTION OF RXSERCLK</th><th>DIRECTION OF RXSYNC</th></tr>
<tr><td>00/11</td><td>Receive Slip Buffer is bypassed</td><td>Output</td><td>Output</td></tr>
<tr><td>01</td><td>Slip Buffer Mode</td><td>Input</td><td>Depends on the setting of SB_SDIR (bit 2 of this register)
If SB_SDIR = 0: RxSYNC = Output
If SB_SDIR = 1: RxSYNC = Input</td></tr>
<tr><td>10</td><td>FIFO Mode.
FIFO data latency can be programmed by the 'FIFO Latency Register' (Address = 0xn117).</td><td>Input</td><td>Depends on the setting of SB_SDIR (bit 2 of this register)
If SB_SDIR = 0: RxSYNC = Output
If SB_SDIR = 1: RxSYNC = Input</td></tr>
</table>
NOTE: <i>Users must make sure that the RxSerClk input pin is synchronized to the Recovered Clock signal for this particular channel to prevent any buffer slips from occurring.</i></td></tr>
<tr><td>0</td><td>SB_ENB(0)</td><td>R/W</td><td>1</td></tr>
</table>

TABLE 22: FIFO LATENCY REGISTER (FFOLR) **HEX ADDRESS: 0xn117**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-5	Reserved	-	-	**Reserved**
4-0	Rx Slip Buffer FIFO Latency[4:0]	R/W	00100	**Receive Slip Buffer FIFO Latency[4:0]:** These bits permit the user to specify the “Receive Data” Latency (in terms of RxSerClk_n clock periods), whenever the Receive Slip Buffer has been configured to operate in the “FIFO” Mode. **NOTE:** *These bits are only active if the Receive Slip Buffer has been configured to operate in the FIFO Mode.*

TABLE 23: DMA 0 (WRITE) CONFIGURATION REGISTER (D0WCR) HEX ADDRESS: 0xn118

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	DMA0 RST	R/W	0	**DMA_0 Reset** This bit resets the transmit DMA (Write) channel 0. 0 = Normal operation. 1 = A zero to one transition resets the transmit DMA (Write) channel 0.
6	DMA0 ENB	R/W	0	**DMA_0 Enable** This bit enables the transmit DMA_0 (Write) interface. After a transmit DMA is enabled, DMA transfers are only requested when the transmit buffer status bits indicate that there is space for a complete message or cell. The DMA write channel is used by the external DMA controller to transfer data from the external memory to the HDLC buffers within the T1 Framer. The DMA Write cycle starts by T1 Framer asserting the DMA Request (REQ0) 'low', then the external DMA controller should drive the DMA Acknowledge (ACK0) 'low' to indicate that it is ready to start the transfer. The external DMA controller should place new data on the Microprocessor data bus each time the Write Signal is Strobed low if the WR is configured as a Write Strobe. If WR is configured as a direction signal, then the external DMA controller would place new data on the Microprocessor data bus each time the Read Signal (RD) is Strobed low. 0 = Disables the transmit DMA_0 (Write) interface 1 = Enables the transmit DMA_0 (Write) interface
5	WR TYPE	R/W	0	**Write Type Select** This bit selects the function of the WR signal. 0 = WR functions as a direction signal (indicates whether the current bus cycle is a read or write operation) and RD functions as a data strobe signal. 1 =WR functions as a write strobe signal
4 - 3	Reserved	-	-	**Reserved**
2	DMA0_CHAN(2)	R/W	0	**Channel Select** These three bits select which T1 channel within the XRT86VL38 uses the Transmit DMA_0 (Write) interface. 000 = Channel 0 001 = Channel 1 001 = Channel 2 011 = Channel 3 100 = Channel 4 101 = Channel 5 110 = Channel 6 111 = Channel 7
1	DMA0_CHAN(1)	R/W	0	
0	DMA0_CHAN(0)	R/W	0	

TABLE 24: DMA 1 (READ) CONFIGURATION REGISTER (D1RCR) HEX ADDRESS: 0xn119

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-6	Reserved	-	-	**Reserved**
7	DMA1 RST	R/W	0	**DMA_1 Reset** This bit resets the Receive DMA (Read) Channel 1 0 = Normal operation. 1 = A zero to one transition resets the Receive DMA (Read) channel 1.
6	DMA1 ENB	R/W	0	**DMA1_ENB** This bit enables the Receive DMA_1 (Read) interface. After a receive DMA is enabled, DMA transfers are only requested when the receive cell buffer contains a complete message or cell. The DMA read channel is used by the T1 Framer to transfer data from the HDLC buffers within the T1 Framer to external memory. The DMA Read cycle starts by T1 Framer asserting the DMA Request (REQ1) 'low', then the external DMA controller should drive the DMA Acknowledge (ACK1) 'low' to indicate that it is ready to receive the data. The T1 Framer should place new data on the Microprocessor data bus each time the Read Signal is Strobed low if the RD is configured as a Read Strobe. If RD is configured as a direction signal, then the T1 Framer would place new data on the Microprocessor data bus each time the Write Signal (WR) is Strobed low. 0 = Disables the DMA_1 (Read) interface 1 = Enables the DMA_1 (Read) interface
5	RD TYPE	R/W	0	**READ Type Select** This bit selects the function of the RD signal. 0 = RD functions as a Read Strobe signal 1 = RD acts as a direction signal (indicates whether the current bus cycle is a read or write operation), and WR works as a data strobe.
4 - 3	Reserved	-	-	**Reserved**
2	DMA1_CHAN(2)	R/W	0	**Channel Select** These three bits select which T1 channel within the chip uses the Receive DMA_1 (Read) interface. 000 = Channel 0 001 = Channel 1 001 = Channel 2 011 = Channel 3 100 = Channel 4 101 = Channel 5 110 = Channel 6 111 = Channel 7
1	DMA1_CHAN(1)	R/W	0	
0	DMA1_CHAN(0)	R/W	0	

TABLE 25: INTERRUPT CONTROL REGISTER (ICR) **HEX ADDRESS: 0xn11A**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-3	Reserved	-	-	**Reserved**
2	INT_WC_RUR	R/W	0	**Interrupt Write-to-Clear or Reset-upon-Read Select** This bit configures all Interrupt Status bits to be either Reset Upon Read or Write-to-Clear 0= Configures all Interrupt Status bits to be Reset-Upon-Read (RUR). 1= Configures all Interrupt Status bits to be Write-to-Clear (WC).
1	ENBCLR	R/W	0	**Interrupt Enable Auto Clear** This bit configures all interrupt enable bits to clear or not clear after reading the interrupt status bit. 0= Configures all Interrupt Enable bits to not cleared after reading the interrupt status bit. The corresponding Interrupt Enable bit will stay ‘high’ after reading the interrupt status bit. 1= Configures all interrupt Enable bits to clear after reading the interrupt status bit. The corresponding interrupt enable bit will be set to ‘low’ after reading the interrupt status bit.
0	INTRUP_ENB	R/W	0	**Interrupt Enable for Framer_n** This bit enables or disables the entire T1 Framer Block for Interrupt Generation. 0 = Disables the T1 framer block for Interrupt Generation 1 = Enables the T1 framer block for Interrupt Generation

TABLE 26: LAPD SELECT REGISTER (LAPDSR) **HEX ADDRESS: 0xn11B**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
[7:2]	Reserved	-	-	**Reserved**
[1:0]	HDLC Controller Select[1:0]	R/W	0	**HDLC Controller Select[1:0]:** These bits permit the user to select any of the three (3) HDLC Controllers that he/she will use within this particular channel, as depicted below. 00 & 11 - Selects HDLC Controller # 1 01 - Selects HDLC Controller # 2 10 - Selects HDLC Controller # 3

TABLE 27: CUSTOMER INSTALLATION ALARM GENERATION REGISTER (CIAGR) HEX ADDRESS: 0xn11C

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
[7:4]	Reserved	-	-	**Reserved**
[3:2]	CIAG	R/W	00	**CI Alarm Transmit (Only in ESF)** These two bits are used to enable or disable AIS-CI or RAI-CI generation in T1 ESF mode only. Alarm Indication Signal-Customer Installation (AIS-CI) and Remote Alarm Indication-Customer Installation (RAI-CI) are intended for use in a network to differentiate between an issue within the network or the Customer Installation (CI). **AIS-CI** AIS-CI is an all ones signal with an embedded signature of 01111100 11111111 (right-to left) which recurs at 386 bit intervals in-the DS-1 signal. **RAI-CI** Remote Alarm Indication - Customer Installation (RAI-CI) is a repetitive pattern with a period of 1.08 seconds. It comprises 0.99 seconds of RAI message (00000000 11111111 Right-to-left) and a 90 ms of RAI-CI signature (00111110 11111111 Right to left) to form a RAI-CI signal. RAI-CI applies to T1 ESF framing mode only. 00/11 = Disables RAI-CI or AIS-CI alarms generation 01 = Enables unframed AIS-CI alarm generation 10 = Enables RAI-CI alarm generation
[1:0]	CIAD	R/W	00	**CI Alarm Detect (Only in ESF)** These two bits are used to enable or disable RAI-CI or AIS-CI alarm detection in T1 ESF mode only. 00/11 = Disables the RAI-CI or AIS-CI alarm detection 01 = Enables the unframed AIS-CI alarm detection 10 = Enables the RAI-CI alarm detection

TABLE 28: PERFORMANCE REPORT CONTROL REGISTER (PRCR) HEX ADDRESS: 0xn11D

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>7</td><td>LBO_ADJ_ENB</td><td>R/W</td><td>0</td><td>Transmit Line Build Out Auto Adjustment:
This bit is used to enable or disable the transmit line build out auto adjustment feature. When the transmitter of the device is sending AIS condition, the transmit line build out will automatically be adjust to one setting lower if this feature is enabled. (Please refer to the EQC[4:0] bits in register 0x0Fn0 for different settings of Transmit Line Build Out). This feature is designed to for power saving purposes when an AIS signal is being transmitted.
1 - Enables the transmit line build out auto adjustment feature.
0 - Disables the transmit line build out auto adjustment feature.
<i>NOTE:</i> <i>This feature is only available for T1 short haul applications.</i></td></tr>
<tr><td>6</td><td>RLOS_OUT_ENB</td><td>R/W</td><td>1</td><td>RLOS Output Enable:
This bit is used to enable or disable the Receive LOS (RLOS_n) output pins.
0 - Disables the RLOS output pin.
1 - Enables the RLOS output pin.</td></tr>
<tr><td>[5-3]</td><td>Reserved</td><td>-</td><td>-</td><td>Reserved.</td></tr>
<tr><td>2</td><td>C/R_BIt</td><td>R/W</td><td>0</td><td>C/R Bit Control
This bit allows user to control the value of C/R bit within an outgoing performance report.
0 - Outgoing C/R bit will be set to’0’
1 - Outgoing C/R bit will be set to’1’</td></tr>
<tr><td>[1:0]</td><td>APCR</td><td>R/W</td><td>00</td><td>Automatic Performance Control/Response Report
These bits automatically generates a summary report of the PMON status so that it can be inserted into an out going LAPD message. Automatic performance report can be generated every time these bits transition from ‘b00’ to ‘b01‘or automatically every one second. The table below describes the different APCR[1:0] bits settings.
<table>
<tr><th>APCR[1:0]</th><th>SOURCE FOR RECEIVE D/E TIMESLOTS</th></tr>
<tr><td>00/11</td><td>No performance report issued</td></tr>
<tr><td>01</td><td>Single performance report is issued when these bits transitions from ‘b00’ to b’01’.</td></tr>
<tr><td>10</td><td>Automatically issues a performance report every one second</td></tr>
</table></td></tr>
</table>

TABLE 29: GAPPED CLOCK CONTROL REGISTER (GCCR) **HEX ADDRESS: 0xn11E**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	FrOutclk	R/W	0	**Framer Output Clock Reference** This bit is used to enable or disable high-speed T1 rate on the T1OSCCLK and the E1OSCCLK output pins. By default, the output clock reference on T1OSCCLK and E1OSCCLK output pins are set to 1.544MHz/2.048MHz respectively. By setting this bit to a “1”, the output clock reference on the T1OSCLK and the E1OSCCLK are changed to 49.408MHz/ 65.536MHz respectively. 0 = Disables high-speed rate to be output on the T1OSCCLK and E1OSCCLK output pins. 1 = Enables high-speed rate to be output on the T1OSCCLK and E1OSCCLK output pins.
[6:2]	Reserved	-	-	**Reserved**
1	TxGCCR	R/W	0	**Transmit Gapped Clock Interface** This bit is used to enable or disable the transmit gapped clock interface operating at 2.048Mbit/s in DS-1 mode. In this application, 63 gaps (missing data) are inserted so that the overall bit rate is reduced to 1.544Mbit/s. **If the transmit Gapped Clock Interface is enabled:** TxMSYNC is used as the 2.048MHz Gapped Clock Input. TxSER is used as the 2.048MHz Gapped Data Input. TxSERCLK must be a 1.544MHz clock input. 0 = Disables the transmit gapped clock interface. 1 = Enables the transmit gapped clock interface.
0	RxGCCR	R/W	0	**Receive Gapped Clock Interface** This bit is used to enable or disable the receive gapped clock interface operating at 2.048Mbit/s in DS-1 mode. In this application, 63 gaps (missing data) are extracted so that the overall bit rate is reduced to 1.544Mbit/s. **If the Receive Gapped Clock Interface is enabled:** RxSERCLK should be configured as a Gapped clock input at 2.048MHz so that a 2.048MHz Gapped Clock can be applied to the Framer block. RxSER is used as the 2.048MHz Gapped Data Output. The position of the gaps will be determined by the gaps placed on RxSERCLK by the user. 0 = Disables the Receive Gapped Clock Interface 1 = Enables the Receive Gapped Clock Interface

TABLE 30: TRANSMIT INTERFACE CONTROL REGISTER (TICR) **HEX ADDRESS:0xn120**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxSyncFrD	R/W	0	**Tx Synchronous fraction data interface** This bit selects whether TxCHCLK or TxSERCLK will be used for fractional data input if fractional interface is enabled. If TxSERCLK is selected to clock in fractional data input, TxCHCLK will be used as an enable signal 0 = Fractional data Is clocked into the chip using TxChCLK if fractional data interface is enabled. 1 = Fractional data is clocked into the chip using TxSerClk. TxChClk is used as fractional data enable. ***NOTE:*** *The Time Slot Identifier Pins (TxChn[4:0]) still indicates the time slot number if fractional data interface is not enabled. Fractional Interface can be enabled by setting TxFr1544 to 1*
6	Reserved	-	-	**Reserved**
5	TxPLClkEnb/ TxSync Is Low	R/W	0	**Transmit payload clock enable/TxSYNC is Active Low** This exact function of this bit depends on whether the T1 framer is configured to operate in base rate or high speed modes of operation. **If the T1 framer is configured to operate in base rate - TxPayload Clock:** This bit configures the framer to output a regular clock or a payload clock on the transmit serial clock (TxSERCLK) pin when TxSERCLK is configured to be an output. 0 = Configures the framer to output a 1.544MHz clock on the TxSERCLK pin when TxSERCLK is configured as an output. 1 = Configures the framer to output a 1.544MHz clock on the TxSERCLK pin when transmitting payload bits. There will be gaps on the TxSERCLK output pin when transmitting overhead bits. **If the T1 framer is configured to operate in high-speed or multiplexed modes - TxSYNC is Active Low:** This bit is used to select whether the transmit frame boundary (TxSYNC) is active low or active high. 0 = Selects TxSync to be active “High” 1 = Selects TxSync to be active “Low”

TABLE 30: TRANSMIT INTERFACE CONTROL REGISTER (TICR) **HEX ADDRESS:0xn120**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
4	TxFr1544	R/W	0	**Fractional/Signaling Interface Enabled** This bit is used to enable or disable the transmit fractional data interface, signaling input, as well as the 32MHz transmit clock and the transmit overhead Signal output. 0 = Configures the 5 time slot identifier pins (TxChn[4:0]) to output the channel number as usual. 1 = Configures the 5 time slot identifier pins (TxChn[4:0]) to function as the following: TxChn[0] becomes the Transmit Serial SIgnaling pin (TxSIG_n) for signaling inputs. Signaling data can now be input from the TxSIG pin if configured appropriately. TxChn[1] becomes the Transmit Fractional Data Input pin (TxFrTD_n) for fractional data input. Fractional data can now be input from the TxFrTD pin if configured appropriately. TxChn[2] becomes the 32 MHz transmit clock output TxChn[3] becomes the Transmit Overhead Signal which pulses high on the first bit of each multi-frame. **NOTE:** *This bit has no effect in the high speed or multiplexed modes of operation. In high-speed or multiplexed modes, TxCHN[0] functions as TxSIGn for signaling input.*
3	TxICLKINV	R/W	0	**Transmit Clock Inversion (Backplane Interface)** This bit selects whether data transition will happen on the rising or falling edge of the transmit clock. 0 = Selects data transition to happen on the rising edge of the transmit clocks. 1 = Selects data transition to happen on the falling edge of the transmit clocks. **NOTE:** *This feature is only available for base rate configuration (i.e. non-highspeed, and non-multiplexed modes).*
2	TxMUXEN	R/W	0	**Multiplexed Mode Enable** This bit enables or disables the multiplexed mode. When multiplexed mode is enable, multiplexed data of four channels at 12.352 or 16.384MHz are demultiplexed inside the transmit framer and sent to 4 channels on the line side. The backplane speed will be running at either 12.352 or 16.384MHz depending on the multiplexed mode selected by TxIMODE[1:0] of this register. 0 = Disables the multiplexed mode. 1 = Enables the multiplexed mode.

TABLE 30: TRANSMIT INTERFACE CONTROL REGISTER (TICR) **HEX ADDRESS:0xn120**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1-0	TxIMODE[1:0]	R/W	00	**Transmit Interface Mode selection** This bit determines the transmit interface speed. The exact function of these two bits depends on whether Multiplexed mode is enabled or disabled. Table 31 and Table 32 shows the functions of these two bits for non-multiplexed and multiplexed modes.:

TABLE 31: TRANSMIT INTERFACE SPEED WHEN MULTIPLEXED MODE IS DISABLED (TXMUXEN = 0)

TXIMODE[1:0]	TRANSMIT INTERFACE SPEED
00	**1.544Mbit/s Base Rate Mode:** Transmit Backplane interface signals include: TxSERCLK is an input or output clock at 1.544MHz TxMSYNC is the superframe boundary at 3ms (ESF) or 1.5ms (SF) TxSYNC is the single frame boundary at 125 us TxSER is the base-rate data input
01	**2.048Mbit/s (High-Speed MVIP Mode):** Transmit backplane interface signals include: TxSERCLK is an input clock at 1.544MHz TxMSYNC is the high speed input clock at 2.048MHz to input high-speed data TxSYNC can be configured as a single frame or superframe boundary, depending on the setting of bit 5 of register 0xn109 TxSER is the high-speed data input
10	**4.096Mbit/s High-Speed Mode:** Transmit Backplane interface signals include: TxSERCLK is an input clock at 1.544MHz TxMSYNC will become the high speed input clock at 4.096MHz to input high-speed data TxSYNC can be configured as a single frame or superframe boundary, depending on the setting of bit 5 of register 0xn109 TxSER is the high-speed data input
11	**8.192Mbit/s High-Speed Mode:** Transmit Backplane interface signals include: TxSERCLK is an input clock at 1.544MHz TxMSYNC will become the high speed input clock at 8.192MHz to input high-speed data TxSYNC can be configured as a single frame or superframe boundary, depending on the setting of bit 5 of register 0xn109 TxSER is the high-speed data input

TABLE 30: TRANSMIT INTERFACE CONTROL REGISTER (TICR) **HEX ADDRESS:0xn120**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1-0	TxIMODE[1:0]	R/W	00	**(Continued)**

TABLE 32: TRANSMIT INTERFACE SPEED WHEN MULTIPLEXED MODE IS ENABLED (TxMUXEN = 1)

TxIMODE[1:0]	TRANSMIT INTERFACE SPEED
00	**Bit-Multiplexed Mode at 12.352MHz is Enabled:** Transmit backplane interface is taking four-channel multiplexed data at a rate of 12.352Mbit/s from channel 0 and bit-demultiplexing the serial data into 4 channels and output to the line on channels 0 through 3. The TxSYNC signal pulses “High” during the framing bit of each DS-1 frame.
01	**Bit-Multiplexed Mode at 16.384MHz is Enabled:** Transmit backplane interface is taking four-channel multiplexed data at a rate of 16.384Mbit/s from channel 0 and bit-demultiplexing the serial data into 4 channels and output to the line on channels 0 through 3. The TxSYNC signal pulses “High” during the framing bit of each DS-1 frame.
10	**HMVIP High-Speed Multiplexed Mode Enabled:** Transmit backplane interface is taking four-channel multiplexed data at a rate of 16.384Mbit/s from channel 0 and byte-demultiplexing the serial data into 4 channels and output on channels 0 through 3. The TxSYNC signal pulses “High” during the last two bits of the previous DS-1 frame and the first two bits of the current DS-1 frame.
11	**H.100 High-Speed Multiplexed Mode Enabled:** Transmit backplane interface is taking four-channel multiplexed data at a rate of 16.384Mbit/s from channel 0 and byte-demultiplexing the serial data into 4 channels and output to the line on channels 0 through 3. The TxSYNC signal pulses “High” during the last bit of the previous DS-1 frame and the first bit of the current DS-1 frame.

Transmit backplane interface signals include:

TxSERCLK is an input clock at 1.544MHz

TxMSYNC will become the highspeed input clock at 12.352 or 16.384MHz to input high-speed multiplexed data on the back-plane interface

TxSYNC can be configured as a single frame or super-frame boundary, depending on the setting of bit 5 of register 0xn109

TxSER is the high-speed data input

NOTE: *In high speed mode, transmit data is sampled on the rising edge of the 12Mhz or 16MHz clock edge.*

NOTE: *Multiplexed data on Channel 4 is de-multiplexed into the LIU outputs at channel 4 through 7.*

TABLE 33: PRBS CONTROL & STATUS REGISTER (PRBSCSR0) HEX ADDRESS: 0XN121

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>7-4</td><td>Reserved</td><td>-</td><td>-</td><td>These bits are not used</td></tr>
<tr><td>3</td><td>PRBS_Switch</td><td>R/W</td><td>0</td><td>PRBS Switch
This bit enables or disables the PRBS switch function within the XRT86VL38 device.
By enabling the PRBS switch function, PRBS functionality will be switched between the receive and transmit framer. T1 Receive framer will generate the PRBS pattern and insert it onto the receive backplane interface, and T1 Transmit Framer will be monitoring the transmit backplane interface for PRBS pattern and declare PRBS LOCK if PRBS has locked onto the input pattern.
If PRBS switch is disabled, T1 Transmit framer will generate the PRBS pattern to the line interface and the receive framer will be monitoring the line for PRBS/QRTS pattern and declare PRBS LOCK if PRBS has locked onto the input pattern.
0 = Disables the PRBS Switch Feature.
1 = Enables the PRBS Switch Feature.</td></tr>
<tr><td>2</td><td>BER[1]</td><td>R/W</td><td>0</td><td rowspan="2">Bit Error Rate
This bit is used to insert PRBS bit error at the rates presented at the table below. The exact function of this bit depends on whether PRBS switch function is enabled or not. (bit 3 within this register).
If the PRBS switch function is disabled, bit error will be inserted by the T1 transmit framer out to the line interface if this bit is enabled.
If the PRBS switch function is enabled, bit error will be inserted by the T1 receive framer out to the receive backplane interface if this bit is enabled.
<table>
<tr><th>BER[1:0]</th><th>BIT ERROR RATE</th></tr>
<tr><td>00/11</td><td>Disable Bit Error insertion to the transmit output or receive backplane interface</td></tr>
<tr><td>01</td><td>Bit Error is inserted to the transmit output or receive backplane interface at a rate of 1/1000 (one out of one Thousand)</td></tr>
<tr><td>10</td><td>Bit Error is inserted to the transmit output or receive backplane interface at a rate of 1/ 1,000,000 (one out of one million)</td></tr>
</table></td></tr>
<tr><td>1</td><td>BER[0]</td><td>R/W</td><td>0</td></tr>
</table>

TABLE 33: PRBS CONTROL & STATUS REGISTER (PRBSCSR0) **HEX ADDRESS: 0XN121**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
0	UnFramedPRBS	R/W	0	**Unframed PRBS Pattern** This bit enables or disables unframed PRBS/QRTS pattern generation (i.e. All timeslots and framing bits are all PRBS/QRTS data). The exact function of this bit depends on whether PRBS switch function is enabled or not. (bit 3 within this register). If PRBS switch function is disabled, T1 Transmit Framer will generate an unframed PRBS 15 or QRTS pattern to the line side if this bit is enabled. If PRBS switch function is enabled, T1 Receive Framer will generate an unframed PRBS 15 or QRTS pattern to the receive backplane interface if this bit is enabled. 0 - Enables an unframed PRBS/QRTS pattern generation to the line interface or to the receive backplane interface 1 - Disables an unframed PRBS/QRTS pattern generation to the line interface or to the receive backplane interface

TABLE 34: RECEIVE INTERFACE CONTROL REGISTER (RICR) **HEX ADDRESS: 0XN122**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RxSyncFrD	R/W	0	**Receive Synchronous fraction data interface** This bit selects whether RxCHCLK or RxSERCLK will be used for fractional data output if receive fractional interface is enabled. If RxSERCLK is selected to clock out fractional data, RxCHCLK will be used as an enable signal 0 = Fractional data Is clocked out of the chip using RxChCLK if the receive fractional interface is enabled. 1 = Fractional data is clocked out of the chip using RxSerClk if the receive fractional interface is enabled. RxChClk is used as fractional data enable. ***NOTE:*** *The Time Slot Identifier Pins (RxChn[4:0]) still indicates the time slot number if the receive fractional data interface is not enabled. Fractional Interface can be enabled by setting RxFr1544 to 1*
6	Reserved	-	-	**Reserved**
5	RxPLClkEnb/ RxSync is low	R/W	0	**Receive payload clock enable/RxSYNC is Active Low** This exact function of this bit depends on whether the T1 framer is configured to operate in base rate or high speed modes of operation. **If the T1 framer is configured to operate in base rate - TxPayload Clock:** This bit configures the T1 framer to either output a regular clock or a payload clock on the receive serial clock (RxSERCLK) pin when RxSERCLK is configured to be an output. 0 = Configures the framer to output a 1.544MHz clock on the RxSERCLK pin when RxSERCLK is configured as an output. 1 = Configures the framer to output a 1.544MHz clock on the RxSERCLK pin when receiving payload bits. There will be gaps on the RxSERCLK output pin when receiving overhead bits. **If the T1 framer is configured to operate in high-speed or multiplexed modes - RxSYNC is Active Low:** This bit is used to select whether the receive frame boundary (RxSYNC) is active low or active high. 0 = Selects RxSync to be active “High” 1 = Selects RxSync to be active “Low”

TABLE 34: RECEIVE INTERFACE CONTROL REGISTER (RICR) **HEX ADDRESS: 0XN122**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
4	RxFr1544	R/W	0	**Receive Fractional/Signaling Interface Enabled** This bit is used to enable or disable the receive fractional output interface, receive signaling output, the serial channel number output, as well as the 8kHz and the received recovered clock output. This bit only functions when the device is configured in non-high speed or multiplexed modes of operations. If the device is configured in base rate: 0 = Configures the 5 time slot identifier pins (RxChn[4:0]) to output the channel number in parallel as usual. 1 = Configures the 5 time slot identifier pins (RxChn[4:0]) into the following different functions: RxChn[0] becomes the Receive Serial SIgnaling output pin (RxSIG_n) for signaling outputs. Signaling data can now be output to the RxSIG pin if configured appropriately. RxChn[1] becomes the Receive Fractional Data Output pin (RxFrTD_n) for fractional data output. Fractional data can now be output to the RxFrTD pin if configured appropriately. RxChn[2] outputs the serial channel number RxChn[3] outputs an 8kHz clock signal. RxCHN[4] outputs the received recovered clock signal (1.544MHz for T1) ***NOTE:*** *This bit has no effect in the high speed or multiplexed modes of operation. In high-speed or multiplexed modes, RxCHN[0] outputs the Signaling data and RxCHN[4] outputs the recovered clock.*
3	RxICLKINV	N/A	0	**Receive Clock Inversion (Backplane Interface)** This bit selects whether data transition will happen on the rising or falling edge of the receive clock. 0 = Selects data transition to happen on the rising edge of the receive clocks. 1 = Selects data transition to happen on the falling edge of the receive clocks. ***NOTE:*** *This feature is only available for base rate configuration (i.e. non-highspeed, or non-multiplexed modes).*
2	RxMUXEN	R/W	0	**Receive Multiplexed Mode Enable** This bit enables or disables the multiplexed mode on the receive side. When multiplexed mode is enable, data of four channels from the line side are multiplexed onto one serial stream inside the receive framer and output to the back-plane interface on RxSER. The backplane speed will become either 12.352MHz or 16.384MHz once multiplexed mode is enabled. 0 = Disables the multiplexed mode. 1 = Enables the multiplexed mode.

TABLE 34: RECEIVE INTERFACE CONTROL REGISTER (RICR) **HEX ADDRESS: 0XN122**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>1-0</td><td>RxIMODE[1:0]</td><td>R/W</td><td>00</td><td>Receive Interface Mode Selection[1:0]
This bit determines the receive backplane interface speed. The exact function of these two bits depends on whether Receive Multiplexed mode is enabled or disabled. Table 35 and Table 36 shows the functions of these two bits for non-multiplexed and multiplexed modes.:
TABLE 35: RECEIVE INTERFACE SPEED WHEN MULTIPLEXED MODE IS DISABLED (TXMUXEN = 0)
<table>
<tr><th>RXIMODE[1:0]</th><th>RECEIVE INTERFACE SPEED</th></tr>
<tr><td>00</td><td>1.544Mbit/s Base Rate Mode
Receive backplane interface signals include:
RxSERCLK is an input or output clock at 1.544MHz
RxSYNC is an input or output signal which indicates the receive singe frame boundary
RxSER is the base-rate data output</td></tr>
<tr><td>01</td><td>2.048Mbit/s High-Speed MVIP Mode:
Receive backplane interface signals include:
RxSERCLK is an input clock at 2.048MHz
RxSYNC is an input signal which indicates the receive singe frame boundary
RxSER is the high-speed data output</td></tr>
<tr><td>10</td><td>4.096Mbit/s High-Speed Mode:
Receive backplane interface signals include:
RxSERCLK is an input clock at 4.096MHz
RxSYNC is an input signal which indicates the receive singe frame boundary
RxSER is the high-speed data output</td></tr>
<tr><td>11</td><td>8.192Mbit/s High-Speed Mode:
Receive backplane interface signals include:
RxSERCLK is an input clock at 8.192MHz
RxSYNC is an input signal which indicates the receive singe frame boundary
RxSER is the high-speed data output</td></tr>
</table>
</td></tr>
</table>

TABLE 34: RECEIVE INTERFACE CONTROL REGISTER (RICR) HEX ADDRESS: 0XN122

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>1-0</td><td>RxIMODE[1:0]</td><td>R/W</td><td>00</td><td>
(Continued):(
TABLE 36: RECEIVE INTERFACE SPEED WHEN MULTIPLEXED MODE IS ENABLED (TXMUXEN = 1)
<table>
<tr><th>TXIMODE[1:0]</th><th>TRANSMIT INTERFACE SPEED</th></tr>
<tr><td>00</td><td>Bit-Multiplexed Mode at 12.352MHz is Enabled:
Receive backplane interface is taking data from the four LIU input channels 0 through 3 and bit-multiplexing the four-channel data into one 12.352MHz serial stream and output on channel 0 of the Receive Serial Output (RxSER). The RxSYNC signal pulses “High” during the framing bit of each DS-1 frame.</td></tr>
<tr><td>01</td><td>Bit-Multiplexed Mode at 16.384MHz is Enabled:
Receive backplane interface is taking data from the four LIU input channels 0 through 3 and bit-multiplexing the four-channel data into one 16.384MHz serial stream and output to channel 0 of the Receive Serial Output (RxSER). The RxSYNC signal pulses “High” during the framing bit of each T1 frame.</td></tr>
<tr><td>10</td><td>HMVIP High-Speed Multiplexed Mode Enabled:
Receive backplane interface is taking data from the four LIU input channels 0 through 3 and byte-multiplexing the four-channel data into one 16.384MHz serial stream and output to channel 0 of the Receive Serial Output (RxSER). The RxSYNC signal pulses “High” during the last two bits of the previous T1 frame and the first two bits of the current T1 frame.</td></tr>
<tr><td>11</td><td>H.100 High-Speed Multiplexed Mode Enabled:
Receive backplane interface is taking data from the four LIU input channels 0 through 3 and byte-multiplexing the four-channel data into one 16.384MHz serial stream and output to channel 0 of the Receive Serial Output (RxSER). The RxSYNC signal pulses “High” during the last bit of the previous T1 frame and the first bit of the current T1 frame.</td></tr>
</table>
Receive backplane interface signals include:
RxSERCLK is an input clock at either 12.352MHz or16.384MHz depending on the selected multiplexed mode.
RxSYNC is an input signal which indicates the multiplexed frame boundary. The length of RxSYNC depends on the multiplexed mode selected.
RxSER is the high-speed data output
<i>NOTE:</i> <i>In high speed mode, receive data is clocked out on the rising edge of the 12Mhz or 16MHz clock edge.</i>
<i>NOTE:</i> <i>Channels 4 through 7 data are multiplexed into the receive serial output (RxSER) at channel 4 in the same fashion.</i>
</td></tr>
</table>

TABLE 37: PRBS CONTROL & STATUS REGISTER (PRBSCSR1) **HEX ADDRESS: 0XN123**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	PRBSTyp	R/W	0	**PRBS Pattern Type** This bit selects the type of PRBS pattern that the T1 Transmit/ Receive framer will generate or detect. PRBS 15 ($X^{15} + X^{14} +1$) Polynomial or QRTS (Quasi-Random Test Signal) Pattern can be generated by the transmit or receive framer depending on whether PRBS switch function is enabled or not (bit 3 in register 0xn121). If the PRBS Switch function is disabled, T1 transmit framer will generate either PRBS 15 or QRTS pattern and output to the line interface. PRBS 15 or QRTS pattern depends on the setting of this bit. If the PRBS Switch function is enabled, T1 receive framer will generate either PRBS 15 or QRTS pattern and output to the receive back plane interface. PRBS 15 or QRTS pattern depends on the setting of this bit. 0 = Enables the PRBS 15 ($X^{15} + X^{14} +1$) Polynomial generation. 1 = Enables the QRTS (Quasi-Random Test Signal) pattern generation.
6	ERRORIns	R/W	0	**Error Insertion** This bit is used to insert a single PRBS/QRTS error to the transmit or receive output depending on whether PRBS switch function is enabled or not. (bit 3 in register 0xn121). If the PRBS Switch function is disabled, T1 transmit framer will insert a single PRBS/QRTS error and output to the line interface if this bit is enabled. If the PRBS Switch function is enabled, T1 receive framer will insert a single PRBS/QRTS error and output to the receive back plane interface if this bit is enabled. A ‘0’ to ‘1’ transition will cause one output bit inverted in the PRBS/ QRTS stream. ***NOTE:*** *This bit only works if PRBS/QRTS generation is enabled.*
5	DATAInv	R/W	0	**PRBS Data Invert:** This bit inverts the Transmit PRBS/QRTS output data and the Receive PRBS/QRTS input data. The exact function of this bit depends on whether PRBS switch function is enabled or not. (bit 3 in register 0xn121). If the PRBS Switch function is disabled and if this bit is enabled, T1 transmit framer will invert the PRBS/QRTS data before it outputs to the line interface, and the T1 receive framer will invert the incoming PRBS/QRTS data before it receives it. If the PRBS Switch function and this bit are both enabled, T1 receive framer will invert the PRBS/QRTS data before it outputs to the line interface, and the T1 transmit framer will invert the incoming PRBS/QRTS data before it receives it. 0 - Transmit and Receive Framer will NOT invert the Transmit and Receive PRBS/QRTS data. 1 - Transmit and Receive Framer will invert the Transmit and Receive PRBS/QRTS data.

TABLE 37: PRBS CONTROL & STATUS REGISTER (PRBSCSR1) **HEX ADDRESS: 0XN123**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
4	RxPRBSLock	RO	0	**Lock Status** This bit indicates whether or not the Receive or Transmit PRBS lock has obtained. The exact function of this bit depends on whether PRBS switch function is enabled or not. (bit 3 in register 0xn121). If the PRBS Switch function is disabled, T1 receive framer will declare LOCK if PRBS/QRTS has locked onto the input pattern. If the PRBS Switch function is disabled, T1 transmit framer will declare LOCK if PRBS/QRTS has locked onto the input pattern. 0 = Indicates the Receive PRBS/QRTS has not Locked onto the input patterns. 1 = Indicates the Receive PRBS/QRTS has locked onto the input patterns.
3	RxPRBSEnb	R/W	0	**Receive PRBS Detection/Generation Enable** This bit enables or disables the receive PRBS/QRTS pattern detection or generation. The exact function of this bit depends on whether PRBS switch function is enabled or not. (bit 3 in register 0xn121). If the PRBS switch function is disabled and if this bit is enabled, T1 Receive Framer will detect the incoming PRBS/QRTS pattern from the line side and declare PRBS/QRTS lock if incoming data locks onto the PRBS/QRTS pattern. If the PRBS switch function and this bit are both enabled, T1 Transmit Framer will detect the incoming PRBS/QRTS pattern from the transmit backplane interface and declare PRBS/QRTS lock if incoming data locks onto the PRBS/QRTS pattern. 0 = Disables the Receive PRBS/QRTS pattern detection. 1 = Enables the Receive PRBS/QRTS pattern detection.
2	TxPRBSEnb	R/W	0	**Transmit PRBS Generation Enable** This bit enables or disables the Transmit PRBS pattern generator. The exact function of this bit depends on whether PRBS switch function is enabled or not. (bit 3 in register 0xn121). If PRBS switch function is disabled, T1 Transmit Framer will generate the PRBS 15 or QRTS pattern to the line side if this bit is enabled. If PRBS switch function is enabled, T1 Receive Framer will generate the PRBS 15 or QRTS pattern to the receive backplane interface if this bit is enabled. 0 = Disables the Transmit PRBS/QRTS pattern generator. 1 = Enables the Transmit PRBS/QRTS pattern generator.
1	RxBypass	R/W	0	**Receive Framer Bypass** This bit enables or disables the Receive T1 Framer bypass. 0 = Disables the Receive T1 framer Bypass. 1 = Enables the Receive T1 Framer Bypass.
0	TxBypass	R/W	0	**Transmit Framer Bypass** This bit enables or disables the Transmit T1 Framer bypass. 0 = Disables the Transmit T1 framer Bypass. 1 = Enables the Transmit T1 Framer Bypass.

TABLE 38: LOOPBACK CODE CONTROL REGISTER (LCCR) **HEX ADDRESS: 0XN124**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>7-6</td><td>RXLBCALEN[1:0]</td><td>R/W</td><td>00</td><td>Receive Loopback Code Activation Length
This bit determines the receive loopback code activation length. There are four lengths supported by the XRT86VL38 as presented in the table below:
<table>
<tr><th>RXLBCALEN[1:0]</th><th>RECEIVE LOOPBACK CODE ACTIVATION LENGTH</th></tr>
<tr><td>00</td><td>Selects 4-bit receive loopback code activation Sequence</td></tr>
<tr><td>01</td><td>Selects 5-bit receive loopback code activation Sequence</td></tr>
<tr><td>10</td><td>Selects 6-bit receive loopback code activation Sequence</td></tr>
<tr><td>11</td><td>Selects 7-bit receive loopback code activation Sequence</td></tr>
</table></td></tr>
<tr><td>5-4</td><td>RXLBCDLEN[1:0]</td><td>R/W</td><td>00</td><td>Receive Loopback Code Deactivation Length
This bit determines the receive loopback code deactivation length. There are four lengths supported by the XRT86VL38 as presented in the table below
<table>
<tr><th>RXLBCDLEN[1:0]</th><th>RECEIVE LOOPBACK CODE DEACTIVATION LENGTH</th></tr>
<tr><td>00</td><td>Selects 4-bit receive loopback code deactivation Sequence</td></tr>
<tr><td>01</td><td>Selects 5-bit receive loopback code deactivation Sequence</td></tr>
<tr><td>10</td><td>Selects 6-bit receive loopback code deactivation Sequence</td></tr>
<tr><td>11</td><td>Selects 7-bit receive loopback code deactivation Sequence</td></tr>
</table></td></tr>
</table>

TABLE 38: LOOPBACK CODE CONTROL REGISTER (LCCR) HEX ADDRESS: 0XN124

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>3-2</td><td>TXLBCLEN[1:0]</td><td>R/W</td><td>00</td><td>Transmit Loopback Code Length
This bit determines transmit loopback code length. There are four lengths supported by the XRT86VL38 as presented in the table below
<table>
<tr><th>TXLBCLEN[1:0]</th><th>TRANSMIT LOOPBACK CODE ACTIVATION LENGTH</th></tr>
<tr><td>00</td><td>Selects 4-bit transmit loopback code Sequence</td></tr>
<tr><td>01</td><td>Selects 5-bit transmit loopback code Sequence</td></tr>
<tr><td>10</td><td>Selects 6-bit transmit loopback code Sequence</td></tr>
<tr><td>11</td><td>Selects 7-bit transmit loopback code Sequence</td></tr>
</table></td></tr>
<tr><td>1</td><td>FRAMED</td><td>R/W</td><td>0</td><td>Framed Loopback Code
This bit selects either framed or unframed loopback code generation in the transmit path.
0 = Selects an “Unframed” loopback code for transmission.
1 = Selects a “framed” loopback code for transmission.</td></tr>
<tr><td>0</td><td>AUTOENB</td><td>R/W</td><td>0</td><td>Remote Loopback Automatically
This bit configures the XRT86VL38 in remote loopback automatically upon detecting the loopback code activation code specified in the Receive Loopback Code Activation Register if Receive activation loopback code is enabled (Register address:0xn126).
The XRT86VL38 will cancel the remote loopback upon detecting the loopback code deactivation code specified in the Receive Loopback Code Deactivation register if the Receive deactivation loopback code is enabled. (Register address:0xn127)
0 = Disables automatic remote loopback upon detecting the receive activation code.
1 = Enables automatic remote loopback upon detecting the receive activation code.</td></tr>
</table>

TABLE 39: TRANSMIT LOOPBACK CODER REGISTER (TLCR) HEX ADDRESS: 0XN125

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-1	TXLBC[6:0]	R/W	1010101	**Transmit Loopback Code** These seven bits determine the transmit loopback code. The MSB of the transmit loopback code is loaded first for transmission.
0	TXLBCENB	R/W	0	**Transmit Loopback Code Enable** This bit enables loopback code generation in the transmit path. Transmit loopback code is generated by writing the transmit loopback code in this register and enabling it using this bit. The length and the format of the transmit loopback code is determined by the Loopback Code Control Register (Register address: 0xn124) 0 = Disables the transmit loopback code generation. 1 = Enables the transmit loopback code generation.

TABLE 40: RECEIVE LOOPBACK ACTIVATION CODE REGISTER (RLACR) HEX ADDRESS: 0XN126

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-1	RXLBAC[6:0]	R/W	1010101	**Receive activation loopback code** These seven bits determine the receive loopback activation code. The MSB of the receive activation loopback code is received first.
0	RXLBACENB	R/W	0	**Receive activation loopback code enable** This bit enables the receive loopback activation code detection. Receive loopback activation code is detected by writing the expected receive activation loopback code in this register and enabling it using this bit. The length and format of the Receive loopback activation code is determined by the Loopback Code Control Register (Register 0xn124). 0 = Disables the receive loopback code activation detection. 1 = Enables the receive loopback code activation detection.

TABLE 41: RECEIVE LOOPBACK DEACTIVATION CODE REGISTER (RLDCR) HEX ADDRESS: 0XN127

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-1	RXLBDC[6:0]	R/W	1010101	**Receive deactivation loopback code** These seven bits determine the receive loopback deactivation code. The MSB of the receive deactivation loopback code is received first.
0	RXLBDCENB	R/W	0	**Receive deactivation loopback code enable** This bit enables the receive loopback deactivation code detection. Receive loopback deactivation code is detected by writing the expected receive deactivation loopback code in this register and enabling it using this bit. The length and format of the Receive loopback deactivation code is determined by the Loopback Code Control Register (Register 0xn124). 0 = Disables the receive loopback code deactivation detection. 1 = Enables the receive loopback code deactivation detection.

TABLE 42: DEFECT DETECTION ENABLE REGISTER (DDER) **HEX ADDRESS: 0XN129**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	DEFDET	R/W	1	For defect detection per ANSI T1.231-1997 and T1.403-1999, user should leave this bit set to ‘1’.

TABLE 43: TRANSMIT SPRM CONTROL REGISTER (TSPRMCR) **HEX ADDRESS: 0XN142**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
5	U1_BIT	R/W	0	**U1 Bit** This bit provides the contents of the U1 bit within the outgoing SPRM message.
4	U2_BIT	R/W	0	**U2 Bit** This bit provides the contents of the U2 bit within the outgoing SPRM message.
3-0	R_BIT	R/W	0000	**R Bit** This bit provides the contents of the R bit within the outgoing SPRM message.

TABLE 44: DATA LINK CONTROL REGISTER (DLCR2) **HEX ADDRESS: 0xn143**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	SLC-96 Data Link Enable	R/W	0	**SLC®96 DataLink Enable** This bit permits the user to configure the channel to support the transmission and reception of the "SLC-96 type" of data-link message. 0 - Channel does not support the transmission and reception of "SLC-96" type of data-link messages. Regular SF framing bits will be transmitted. 1 - Channel supports the transmission and reception of the "SLC-96" type of data-link messages. ***NOTE:*** *This bit is only active if the channel has been configured to operate in either the SLC-96 or the ESF Framing formats.*
6	MOS ABORT Disable	R/W	0	**MOS ABORT Disable:** This bit permits the user to either enable or disable the "Automatic MOS ABORT" feature within Transmit HDLC Controller # 2. If the user enables this feature, then Transmit HDLC Controller block # 2 will automatically transmit the ABORT Sequence (e.g., a zero followed by a string of 7 consecutive "1s") whenever it abruptly transitions from transmitting a MOS type of message, to transmitting a BOS type of message. If the user disables this feature, then the Transmit HDLC Controller Block # 2 will NOT transmit the ABORT sequence, whenever it abruptly transitions from transmitting a MOS-type of message to transmitting a BOS-type of message. 0 - Enables the "Automatic MOS Abort" feature 1 - Disables the "Automatic MOS Abort" feature
5	Rx_FCS_DIS	R/W	0	**Receive Frame Check Sequence (FCS) Verification Enable/Disable** This bit permits the user to configure the Receive HDLC Controller Block # 2 to compute and verify the FCS value within each incoming LAPD message frame. 0 - Enables FCS Verification 1 - Disables FCS Verification
4	AutoRx	R/W	0	**Auto Receive LAPD Message** This bit configures the Receive HDLC Controller Block #2 to discard any incoming BOS or LAPD Message frame that exactly match which is currently stored in the Receive HDLC1 buffer. 0 = Disables this "AUTO DISCARD" feature 1 = Enables this "AUTO DISCARD" feature.
3	Tx_ABORT	R/W	0	**Transmit ABORT** This bit configures the Transmit HDLC Controller Block # 2 to transmit an ABORT sequence (string of 7 or more consecutive 1's) to the Remote terminal. 0 - Configures the Transmit HDLC Controller Block # 2 to function normally (e.g., not transmit the ABORT sequence). 1 - Configures the Transmit HDLC Controller block # 2 to transmit the ABORT Sequence.

TABLE 44: DATA LINK CONTROL REGISTER (DLCR2) **HEX ADDRESS: 0xn143**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2	Tx_IDLE	R/W	0	**Transmit Idle (Flag Sequence Byte)** This bit configures the Transmit HDLC Controller Block #2 to unconditionally transmit a repeating string of Flag Sequence octets (0X7E) in the data link channel to the Remote terminal. In normal conditions, the Transmit HDLC Controller block will repeatedly transmit the Flag Sequence octet whenever there is no MOS message to transmit to the remote terminal equipment. However, if the user invokes this “Transmit Idle Sequence” feature, then the Transmit HDLC Controller block will UNCONDITIONALLY transmit a repeating stream of the Flag Sequence octet (thereby overwriting all outbound MOS data-link messages). 0 - Configures the Transmit HDLC Controller Block # 2 to transmit data-link information in a “normal” manner. 1 - Configures the Transmit HDLC Controller block # 2 to transmit a repeating string of Flag Sequence Octets (0x7E). ***NOTE:*** *This bit is ignored if the* Transmit *HDLC2 controller is operating in the BOS Mode - bit 0 (MOS/BOS) within this register is set to 0.*
1	Tx_FCS_EN	R/W	0	**Transmit LAPD Message with Frame Check Sequence (FCS)** This bit permits the user to configure the Transmit HDLC Controller block # 2 to compute and append FCS octets to the “back-end” of each outbound MOS data-link message. 0 - Configures the Transmit HDLC Controller block # 2 to NOT compute and append the FCS octets to the back-end of each outbound MOS data-link message. 1 - Configures the Transmit HDLC Controller block # 2 TO COMPUTE and append the FCS octets to the back-end of each outbound MOS data-link message. ***NOTE:*** *This bit is ignored if the transmit HDLC2 controller has been configured to operate in the BOS mode - bit 0 (MOS/BOS) within this register is set to 0.*
0	MOS/$\overline{\text{BOS}}$	R/W	0	**Message Oriented Signaling/Bit Oriented Signaling Send** This bit permits the user to enable LAPD transmission through HDLC Controller Block # 2 using either BOS (Bit-Oriented Signaling) or MOS (Message-Oriented Signaling) frames. 0 - Transmit HDLC Controller block # 2 BOS message Send. 1 - Transmit HDLC Controller block # 2 MOS message Send. ***NOTE:*** *This is not an Enable bit. This bit must be set to "0" each time a BOS is to be sent.*

TABLE 45: TRANSMIT DATA LINK BYTE COUNT REGISTER (TDLBCR2) HEX ADDRESS: 0xn144

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxHDLC2 BUFAvail/ BUFSel	R/W	0	**Transmit HDLC2 Buffer Available/Buffer Select** This bit has different functions, depending upon whether the user is writing to or reading from this register, as depicted below. **If the user is writing data into this register bit:** 0 - Configures the Transmit HDLC2 Controller to read out and transmit the data, residing within “Transmit HDLC2 Buffer # 0", via the Data Link channel to the remote terminal equipment. 1 - Configures the Transmit HDLC2 Controller to read out and transmit the data, residing within the “Transmit HDLC2 Buffer #1”, via the Data Link channel to the remote terminal equipment. **If the user is reading data from this register bit:** 0 - Indicates that “Transmit HDLC2 Buffer # 0" is the next available buffer. In this case, if the user wishes to write in the contents of a new “outbound” Data Link Message into the Transmit HDLC2 Message Buffer, he/she should proceed to write this message into “Transmit HDLC2 Buffer # 0" - Address location: 0xn600. 1 - Indicates that “Transmit HDLC2 Buffer # 1" is the next available buffer. In this case, if the user wishes to write in the contents of a new “outbound” Data Link Message into the Transmit HDLC2 Message Buffer, he/she should proceed to write this message into “Transmit HDLC2 Buffer # 1" - Address location: 0xn700. **NOTE:** *If one of these Transmit HDLC2 buffers contain a message which has yet to be completely read-in and processed for transmission by the Transmit HDLC2 controller, then this bit will automatically reflect the value corresponding to the next available buffer when it is read. Changing this bit to the in-use buffer is not permitted.*
6-0	TDLBC[6:0]	R/W	0000000	**Transmit HDLC2 Message - Byte Count** The exact function of these bits depends on whether the Transmit HDLC 2 Controller is configured to transmit MOS or BOS messages to the Remote Terminal Equipment. **In BOS MODE:** These bit fields contain the number of repetitions the BOS message must be transmitted before the Transmit HDLC2 controller generates the Transmit End of Transfer (TxEOT) interrupt and halts transmission. If these fields are set to 00000000, then the BOS message will be transmitted for an indefinite number of times. **In MOS MODE:** These bit fields contain the length, in number of octets, of the message to be transmitted. The length of MOS message specified in these bits include header bytes such as the SAPI, TEI, Control field, however, it does not include the FCS bytes.

TABLE 46: RECEIVE DATA LINK BYTE COUNT REGISTER (RDLBCR2) **HEX ADDRESS: 0xn145**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RBUFPTR	R/W	0	**Receive HDLC2 Buffer-Pointer** This bit Identifies which Receive HDLC2 buffer contains the most recently received HDLC2 message. 0 - Indicates that Receive HDLC2 Buffer # 0 contains the contents of the most recently received HDLC message. 1 - Indicates that Receive HDLC2 Buffer # 1 contains the contents of the most recently received HDLC message.
6-0	RDLBC[6:0]	R/W	0000000	**Receive HDLC Message - byte count** The exact function of these bits depends on whether the Receive HDLC Controller Block #2 is configured to receive MOS or BOS messages. **In BOS Mode:** These seven bits contain the number of repetitions the BOS message must be received before the Receive HDLC2 controller generates the Receive End of Transfer (RxEOT) interrupt. If these bits are set to “0000000”, the message will be received indefinitely and no Receive End of Transfer (RxEOT) interrupt will be generated. **In MOS Mode:** These seven bits contain the size in bytes of the HDLC2 message that has been received and written into the Receive HDLC buffer. The length of MOS message shown in these bits include header bytes such as the SAPI, TEI, Control field, AND the FCS bytes.

TABLE 47: DATA LINK CONTROL REGISTER (DLCR3) **HEX ADDRESS: 0xn153**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	SLC-96 Data Link Enable	R/W	0	**SLC®96 DataLink Enable** This bit permits the user to configure the channel to support the transmission and reception of the “SLC-96 type” of data-link message. 0 - Channel does not support the transmission and reception of “SLC-96” type of data-link messages. Regular SF framing bits will be transmitted. 1 - Channel supports the transmission and reception of the “SLC-96” type of data-link messages. ***NOTE:*** *This bit is only active if the channel has been configured to operate in either the SLC-96 or the ESF Framing formats.*
6	MOS ABORT Disable	R/W	0	**MOS ABORT Disable:** This bit permits the user to either enable or disable the “Automatic MOS ABORT” feature within Transmit HDLC Controller # 3. If the user enables this feature, then Transmit HDLC Controller block # 3 will automatically transmit the ABORT Sequence (e.g., a zero followed by a string of 7 consecutive “1s”) whenever it abruptly transitions from transmitting a MOS type of message, to transmitting a BOS type of message. If the user disables this feature, then the Transmit HDLC Controller Block # 3 will NOT transmit the ABORT sequence, whenever it abruptly transitions from transmitting a MOS-type of message to transmitting a BOS-type of message. 0 - Enables the “Automatic MOS Abort” feature 1 - Disables the “Automatic MOS Abort” feature
5	Rx_FCS_DIS	R/W	0	**Receive Frame Check Sequence (FCS) Verification Enable/Disable** This bit permits the user to configure the Receive HDLC Controller Block # 3 to compute and verify the FCS value within each incoming LAPD message frame. 0 - Enables FCS Verification 1 - Disables FCS Verification
4	AutoRx	R/W	0	**Auto Receive LAPD Message** This bit configures the Receive HDLC Controller Block #3 to discard any incoming BOS or LAPD Message frame that exactly match which is currently stored in the Receive HDLC3 buffer. 0 = Disables this “AUTO DISCARD” feature 1 = Enables this “AUTO DISCARD” feature.
3	Tx_ABORT	R/W	0	**Transmit ABORT** This bit configures the Transmit HDLC Controller Block #3 to transmit an ABORT sequence (string of 7 or more consecutive 1’s) to the Remote terminal. 0 - Configures the Transmit HDLC Controller Block # 3 to function normally (e.g., not transmit the ABORT sequence). 1 - Configures the Transmit HDLC Controller block # 3 to transmit the ABORT Sequence.

TABLE 47: DATA LINK CONTROL REGISTER (DLCR3) **HEX ADDRESS: 0xn153**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2	Tx_IDLE	R/W	0	**Transmit Idle (Flag Sequence Byte)** This bit configures the Transmit HDLC Controller Block #3 to unconditionally transmit a repeating string of Flag Sequence octets (0X7E) in the data link channel to the Remote terminal. In normal conditions, the Transmit HDLC Controller block will repeatedly transmit the Flag Sequence octet whenever there is no MOS message to transmit to the remote terminal equipment. However, if the user invokes this “Transmit Idle Sequence” feature, then the Transmit HDLC Controller block will UNCONDITIONALLY transmit a repeating stream of the Flag Sequence octet (thereby overwriting all outbound MOS data-link messages). 0 - Configures the Transmit HDLC Controller Block # 3 to transmit data-link information in a “normal” manner. 1 - Configures the Transmit HDLC Controller block # 3 to transmit a repeating string of Flag Sequence Octets (0x7E). ***NOTE:*** *This bit is ignored if the* Transmit *HDLC3 controller is operating in the BOS Mode - bit 0 (MOS/BOS) within this register is set to 0.*
1	Tx_FCS_EN	R/W	0	**Transmit LAPD Message with Frame Check Sequence (FCS)** This bit permits the user to configure the Transmit HDLC Controller block # 3 to compute and append FCS octets to the “back-end” of each outbound MOS data-link message. 0 - Configures the Transmit HDLC Controller block # 3 to NOT compute and append the FCS octets to the back-end of each outbound MOS data-link message. 1 - Configures the Transmit HDLC Controller block # 3 TO COMPUTE and append the FCS octets to the back-end of each outbound MOS data-link message. ***NOTE:*** *This bit is ignored if the transmit HDLC3 controller has been configured to operate in the BOS mode - bit 0 (MOS/BOS) within this register is set to 0.*
0	MOS/$\overline{\text{BOS}}$	R/W	0	**Message Oriented Signaling/Bit Oriented Signaling Send** This bit permits the user to enable LAPD transmission through HDLC Controller Block # 3 using either BOS (Bit-Oriented Signaling) or MOS (Message-Oriented Signaling) frames. 0 - Transmit HDLC Controller block # 3 BOS message Send. 1 - Transmit HDLC Controller block # 3 MOS message Send. ***NOTE:*** *This is not an Enable bit. This bit must be set to "0" each time a BOS is to be sent.*

TABLE 48: TRANSMIT DATA LINK BYTE COUNT REGISTER (TDLBCR3) HEX ADDRESS: 0xn154

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxHDLC3 BUFAvail/ BUFSel	R/W	0	**Transmit HDLC3 Buffer Available/Buffer Select** This bit has different functions, depending upon whether the user is writing to or reading from this register, as depicted below. **If the user is writing data into this register bit:** 0 - Configures the Transmit HDLC3 Controller to read out and transmit the data, residing within “Transmit HDLC3 Buffer # 0", via the Data Link channel to the remote terminal equipment. 1 - Configures the Transmit HDLC3 Controller to read out and transmit the data, residing within the “Transmit HDLC3 Buffer #1”, via the Data Link channel to the remote terminal equipment. **If the user is reading data from this register bit:** 0 - Indicates that “Transmit HDLC3 Buffer # 0" is the next available buffer. In this case, if the user wishes to write in the contents of a new “outbound” Data Link Message into the Transmit HDLC3 Message Buffer, he/she should proceed to write this message into “Transmit HDLC3 Buffer # 0" - Address location: 0xn600. 1 - Indicates that “Transmit HDLC3 Buffer # 1" is the next available buffer. In this case, if the user wishes to write in the contents of a new “outbound” Data Link Message into the Transmit HDLC3 Message Buffer, he/she should proceed to write this message into “Transmit HDLC3 Buffer # 1" - Address location: 0xn700. ***NOTE:*** *If one of these Transmit HDLC3 buffers contain a message which has yet to be completely read-in and processed for transmission by the Transmit HDLC3 controller, then this bit will automatically reflect the value corresponding to the next available buffer when it is read. Changing this bit to the in-use buffer is not permitted.*
6-0	TDLBC[6:0]	R/W	0000000	**Transmit HDLC3 Message - Byte Count** The exact function of these bits depends on whether the Transmit HDLC 3 Controller is configured to transmit MOS or BOS messages to the Remote Terminal Equipment. **In BOS MODE:** These bit fields contain the number of repetitions the BOS message must be transmitted before the Transmit HDLC3 controller generates the Transmit End of Transfer (TxEOT) interrupt and halts transmission. If these fields are set to 00000000, then the BOS message will be transmitted for an indefinite number of times. **In MOS MODE:** These bit fields contain the length, in number of octets, of the message to be transmitted. The length of MOS message specified in these bits include header bytes such as the SAPI, TEI, Control field, however, it does not include the FCS bytes.

TABLE 49: RECEIVE DATA LINK BYTE COUNT REGISTER (RDLBCR3) **HEX ADDRESS: 0xn155**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RBUFPTR	R/W	0	**Receive HDLC2 Buffer-Pointer** This bit Identifies which Receive HDLC3 buffer contains the most recently received HDLC3 message. 0 - Indicates that Receive HDLC3 Buffer # 0 contains the contents of the most recently received HDLC message. 1 - Indicates that Receive HDLC3 Buffer # 1 contains the contents of the most recently received HDLC message.
6-0	RDLBC[6:0]	R/W	0000000	**Receive HDLC Message - byte count** The exact function of these bits depends on whether the Receive HDLC Controller Block #3 is configured to receive MOS or BOS messages. **In BOS Mode:** These seven bits contain the number of repetitions the BOS message must be received before the Receive HDLC3 controller generates the Receive End of Transfer (RxEOT) interrupt. If these bits are set to “0000000”, the message will be received indefinitely and no Receive End of Transfer (RxEOT) interrupt will be generated. **In MOS Mode:** These seven bits contain the size in bytes of the HDLC3 message that has been received and written into the Receive HDLC buffer. The length of MOS message shown in these bits include header bytes such as the SAPI, TEI, Control field, AND the FCS bytes.

TABLE 50: DEVICE ID REGISTER (DEVID) HEX ADDRESS: 0XN1FE

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	DEVID[7:0]	RO	0x3B	**DEVID** This register is used to identify the XRT86VL38 Framer/LIU. The value of this register is 0x3Bh.

TABLE 51: REVISION ID REGISTER (REVID) HEX ADDRESS: 0XN1FF

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	REVID[7:0]	RO	00000010	**REVID** This register is used to identify the revision number of the XRT86VL38. The value of this register for the current revision is B - 0x02h. ***NOTE:*** *The content of this register is subject to change when a newer revision of the device is issued.*

TABLE 52: TRANSMIT CHANNEL CONTROL REGISTER 0-23 (TCCR 0-23) HEX ADDRESS: 0xn300 TO 0xn317

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>7</td><td>LAPDcntl[1]</td><td>R/W</td><td>1</td><td rowspan="2">Transmit LAPD Control
These bits select which one of the three Transmit LAPD controller is configured to use D/E time slot (Octets 0-23) for transmitting LAPD messages. The following table presents the different settings of these two bits.
<table>
<tr><th>LAPDCNTL[1:0]</th><th>LAPD CONTROLLER SELECTED</th></tr>
<tr><td>00</td><td>Transmit LAPD Controller 1</td></tr>
<tr><td>01</td><td>Transmit LAPD Controller 2</td></tr>
<tr><td>10</td><td>The TxDE[1:0] bits in the Transmit Signaling and Data Link Select Register (TSDLSR - Register Address - 0xn10A, bit 3-2) determine the data source for D/E time slots.</td></tr>
<tr><td>11</td><td>Transmit LAPD Controller 3</td></tr>
</table>
NOTE: <i>All three Transmit LAPD Controllers can use D/E timeslots for transmission. However, only Transmit LAPD Controller 1 can use datalink for transmission. Register 0xn300 represents D/E time slot 0, and 0xn317 represents D/E time slot 23.</i></td></tr>
<tr><td>6</td><td>LAPDcntl[0]</td><td>R/W</td><td>0</td></tr>
<tr><td>5 - 4</td><td>TxZERO[1:0]</td><td>R/W</td><td>00</td><td>Selects Type of Zero Suppression
These bits select the type of zero code suppression used by the XRT86VL38 device
.
<table>
<tr><th>TXZERO[1:0]</th><th>TYPE OF ZERO CODE SUPPRESSION SELECTED</th></tr>
<tr><td>00</td><td>No zero code suppression is used</td></tr>
<tr><td>01</td><td>AT&T bit 7 stuffing is used</td></tr>
<tr><td>10</td><td>GTE zero code suppression is used. If GTE zero code suppression is used, bit 8 is stuffed in non-signaling frame. Otherwise, bit 7 is stuffed in signaling frame if signaling bit is zero.</td></tr>
<tr><td>11</td><td>DDS zero code suppression is used. The value 0x98 replaces the input data</td></tr>
</table></td></tr>
</table>

TABLE 52: TRANSMIT CHANNEL CONTROL REGISTER 0-23 (TCCR 0-23) HEX ADDRESS: 0xn300 TO 0xn317

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3-0	TxCond(3:0)	R/W	0000	**Transmit Channel Conditioning for Timeslot 0 to 23** These bits allow the user to substitute the input PCM data (Octets 0-23) with internally generated Conditioning Codes prior to transmission to the remote terminal equipment on a per-channel basis. The table below presents the different conditioning codes based on the setting of these bits. *Register address 0xn300 represents time slot 0, and address 0xn317 represents time slot 23.*

TXCOND[1:0]	CONDITIONING CODES
0x0 / 0xE	Contents of timeslot octet are unchanged.
0x1	All 8 bits of the selected timeslot octet are inverted (1's complement) OUTPUT = (TIME_SLOT_OCTET) XOR 0xFF
0x2	Even bits of the selected timeslot octet are inverted OUTPUT = (TIME_SLOT_OCTET) XOR 0xAA
0x3	Odd bits of the selected time slot octet are inverted OUTPUT = (TIME_SLOT_OCTET) XOR 0x55
0x4	Contents of the selected timeslot octet will be substituted with the 8 -bit value in the Transmit Programmable User Code Register (0xn320-0xn337),
0x5	Contents of the timeslot octet will be substituted with the value 0x7F (BUSY Code)
0x6	Contents of the timeslot octet will be substituted with the value 0xFF (VACANT Code)
0x7	Contents of the timeslot octet will be substituted with the BUSY time slot code (111#_####), where ##### is the Timeslot number
0x8	Contents of the timeslot octet will be substituted with the MOOF code (0x1A)
0x9	Contents of the timeslot octet will be substituted with the A-Law Digital Milliwatt pattern
0xA	Contents of the timeslot octet will be substituted with the μ-Law Digital Milliwatt pattern
0xB	The MSB (bit 1) of input data is inverted
0xC	All input data except MSB is inverted
0xD	Contents of the timeslot octet will be substituted with the PRBS $X^{15} + X^{14} + 1$/QRTS pattern **NOTE:** *PRBS $X^{15} + X^{14} + 1$ or QRTS pattern depends on PRBSType selected in the register 0xn123 - bit 7*
0xF	D/E time slot - The TxDE[2:0] bits in the Transmit Signaling and Data Link Select Register (0xn10A) will determine the data source for D/E time slots.

TABLE 53: TRANSMIT USER CODE REGISTER 0-23 (TUCR 0-23) **HEX ADDRESS: 0xn320 TO 0xn337**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	TUCR[7:0]	R/W	b00010111	**Transmit Programmable User code.** These eight bits allow users to program any code in this register to replace the input PCM data when the Transmit Channel Control Register (TCCR) is configured to replace timeslot octet with programmable user code. (i.e. if TCCR is set to ‘0x4’) The default value of this register is an IDLE Code (b00010111).

TABLE 54: TRANSMIT SIGNALING CONTROL REGISTER 0-23 (TSCR 0-23) HEX ADDRESS: 0xn340 TO 0XN357

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	A (x)	R/W	See Note	**Transmit Signaling bit A** This bit allows user to provide signaling Bit A (Octets 0-23) if Robbed-bit signaling is enabled (Rob_Enb bit of this register set to 1) and if signalling data is inserted from TSCR (TxSIGSRC[1:0] = 01 in this register). ***NOTE:*** *Register 0xn340 represents signaling data for Time Slot 0, and 0xn357 represents signaling data for Time Slot 23.*
6	B (y)	R/W	See Note	**Transmit Signaling bit B** This bit allows user to provide signaling Bit B (Octets 0-23) if Robbed-bit signaling is enabled (Rob_Enb bit of this register set to 1) and if signalling data is inserted from TSCR (TxSIGSRC[1:0] = 01 in this register). ***NOTE:*** *Register 0xn340 represents signaling data for Time Slot 0, and 0xn357 represents signaling data for Time Slot 23.*
5	C (x)	R/W	See Note	**Transmit Signaling bit C** This bit allows user to provide signaling Bit C (Octets 0-23) if Robbed-bit signaling is enabled (Rob_Enb bit of this register set to 1) and if signalling data is inserted from TSCR (TxSIGSRC[1:0] = 01 in this register). ***NOTE:*** *Register 0xn340 represents signaling data for Time Slot 0, and 0xn357 represents signaling data for Time Slot 23.*
4	D (x)	R/W	See Note	**Transmit Signaling bit D** This bit allows user to provide signaling Bit D (Octets 0-23) if Robbed-bit signaling is enabled (Rob_Enb bit of this register set to 1) and if signalling data is inserted from TSCR (TxSIGSRC[1:0] = 01 in this register). ***NOTE:*** *Register 0xn340 represents signaling data for Time Slot 0, and 0xn357 represents signaling data for Time Slot 23.*
3	Reserved	-	See Note	**Reserved**
2	Rob_Enb	R/W	See Note	**Robbed-bit signaling enable** This bit enables or disables Robbed-bit signaling transmission. If robbed-bit signaling is enabled, signaling data is conveyed in the 8th position of each signaling channel by replacing the original LSB of the voice channel with signaling data. 0 = Disables Robbed-bit signaling. 1 = Enables Robbed-bit signaling.

TABLE 54: TRANSMIT SIGNALING CONTROL REGISTER 0-23 (TSCR 0-23) HEX ADDRESS: 0XN340 TO 0XN357

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	TxSIGSRC[1]	R/W	See Note	**Channel signaling control** These bits determine the source for signaling information, see table below.
0	TxSIGSRC[0]	R/W	See Note	

TXSIGSRC[1:0]	SIGNALING SOURCE SELECTED
00/11	Signaling data is inserted from input PCM data (TxSERn pin)
01	Signaling data is inserted from this register (TSCRs).
10	Signaling data is inserted from the Transmit Signaling input pin (TxSIG_n) if the Transmit Signaling Interface bit is enabled (i.e. TxFr1544 bit = 1 in the Transmit Interface Control Register (TICR) Register 0xn120),

NOTE: *The default value for register address 0xn340 = 0x01, 0xn341-0xn34F = 0xD0, 0xn350 = 0xB3, 0xn351-0xn35F = 0xD0*

TABLE 55: RECEIVE CHANNEL CONTROL REGISTER 0-23 (RCCR 0-23) HEX ADDRESS: 0xn360 TO 0xn377

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>7</td><td>LAPDcntl[1]</td><td>R/W</td><td>1</td><td rowspan="2">Receive LAPD Control
These bits select which one of the three Receive LAPD controller will be configured to use D/E time slot (Octets 0-23) for receiving LAPD messages.
<table>
<tr><th>LAPDCNTL[1:0]</th><th>RECEIVE LAPD CONTROLLER SELECTED</th></tr>
<tr><td>00</td><td>Receive LAPD Controller 1</td></tr>
<tr><td>01</td><td>Receive LAPD Controller 2</td></tr>
<tr><td>10</td><td>The RxDE[1:0] bits in the Receive Signaling and Data Link Select Register (RSDLSR - Address - 0xn10C) determine the data source for Receive D/E time slots.</td></tr>
<tr><td>11</td><td>Receive LAPD Controller 3</td></tr>
</table>
NOTE: <i>All three LAPD Controller can use D/E timeslots for receiving LAPD messages. However, only LAPD Controller 1 can use datalink for reception.</i>
NOTE: <i>Register 0xn360 represents D/E time slot 0, and 0xn377 represents D/E time slot 23.</i></td></tr>
<tr><td>6</td><td>LAPDcntl[0]</td><td>R/W</td><td>0</td></tr>
<tr><td>5-4</td><td>RxZERO[1:0]</td><td>R/W</td><td>00</td><td>Type of Zero Suppression
These bits select the type of zero code suppression used by the XRT86VL38 device.
<table>
<tr><th>RxZERO[1:0]</th><th>TYPE OF ZERO CODE SUPPRESSION SELECTED</th></tr>
<tr><td>00</td><td>No zero code suppression is used</td></tr>
<tr><td>01</td><td>AT&T bit 7 stuffing is used</td></tr>
<tr><td>10</td><td>GTE zero code suppression is used. If GTE zero code suppression is used, bit 8 is stuffed in non-signaling frame. Otherwise, bit 7 is stuffed in signaling frame if signaling bit is zero.</td></tr>
<tr><td>11</td><td>DDS zero code suppression is used. The value 0x98 replaces the input data</td></tr>
</table></td></tr>
</table>

Table 55: Receive Channel Control Register 0-23 (RCCR 0-23) **Hex Address: 0xn360 to 0xn377**

Bit	Function	Type	Default	Description-Operation
3-0	RxCOND[3:0]	R/W	0000	**Receive Channel Conditioning for Timeslot 0 to 23** These bits allow the user to substitute the input line data (Octets 0-23) with internally generated Conditioning Codes prior to transmission to the backplane interface on a per-channel basis. The table below presents the different conditioning codes based on the setting of these bits. ***Note:*** *Register address 0xn300 represents time slot 0, and address 0xn317 represents time slot 23.*

RxCond[1:0]	Conditioning Codes
0x0 / 0xE	Contents of timeslot octet are unchanged.
0x1	All 8 bits of the selected timeslot octet are inverted (1's complement) OUTPUT = (TIME_SLOT_OCTET) XOR 0xFF
0x2	Even bits of the selected timeslot octet are inverted OUTPUT = (TIME_SLOT_OCTET) XOR 0xAA
0x3	Odd bits of the selected time slot octet are inverted OUTPUT = (TIME_SLOT_OCTET) XOR 0x55
0x4	Contents of the selected timeslot octet will be substituted with the 8 -bit value in the Receive Programmable User Code Register (0xn380-0xn397),
0x5	Contents of the timeslot octet will be substituted with the value 0x7F (BUSY Code)
0x6	Contents of the timeslot octet will be substituted with the value 0xFF (VACANT Code)
0x7	Contents of the timeslot octet will be substituted with the BUSY time slot code (111#_####), where ##### is the Timeslot number
0x8	Contents of the timeslot octet will be substituted with the MOOF code (0x1A)
0x9	Contents of the timeslot octet will be substituted with the A-Law Digital Milliwatt pattern
0xA	Contents of the timeslot octet will be substituted with the µ-Law Digital Milliwatt pattern
0xB	The MSB (bit 1) of input data is inverted
0xC	All input data except MSB is inverted
0xD	Contents of the timeslot octet will be substituted with the PRBS $X^{15} + X^{14} + 1$/QRTS pattern ***Note:*** *PRBS $X^{15} + X^{14} + 1$ or QRTS pattern depends on PRBSType selected in the register 0xn123 - bit 7*
0xF	D/E time slot - The RxDE[2:0] bits in the Transmit Signaling and Data Link Select Register (0xn10C) will determine the data source for Receive D/E time slots.

TABLE 56: RECEIVE USER CODE REGISTER 0-23 (RUCR 0-23) **HEX ADDRESS: 0XN380 TO 0XN397**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	RxUSER[7:0]	R/W	11111111	**Receive Programmable User code.** These eight bits allow users to program any code in this register to replace the received data when the Receive Channel Control Register (RCCR) is configured to replace timeslot octet with the receive programmable user code. (i.e. if RCCR is set to ‘0x4’)

TABLE 57: RECEIVE SIGNALING CONTROL REGISTER 0-23 (RSCR 0-23) HEX ADDRESS: 0xn3A0 TO 0xn3B7

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
6	SIGC_ENB	R/W	0	**Signaling substitution enable** This bit enables or disables signaling substitution on the receive side on a per channel basis. Once signaling substitution is enabled, received signaling bits ABCD will be substituted with the ABCD values in the Receive Substitution Signaling Register (RSSR). Signaling substitution only occurs in the output PCM data (RxSERn). Receive Signaling Array Register (RSAR - Address 0xn500-0xn51F) and the external Signaling bus (RxSIG_n) output pin will not be affected. 0 = Disables signaling substitution on the receive side. 1 = Enables signaling substitution on the receive side.
5	OH_ENB	R/W	0	**Signaling OH interface output enable** This bit enables or disables signaling information to output via the Receive Overhead pin (RxOH_n) on a per channel basis. The signaling information in the receive signaling array registers (RSAR - Address 0xn500-0xn51F) is output to the receive overhead output pin (RxOH_n) if this bit is enabled. 0 = Disables signaling information to output via RxOH_n. 1 = Enables signaling information to output via RxOH_n.
4	DEB_ENB	R/W	0	**Per-channel debounce enable** This bit enables or disables the signaling debounce feature on a per channel basis. When this feature is enabled, the per-channel signaling state must be in the same state for 2 superframes before the Receive Framer updates signaling information on the Receive Signaling Array Register (RSAR) and the Signaling Pin (RxSIGn). If the signaling bits for two consecutive superframes are not the same, the current state of RSAR and RxSIG will not change. When this feature is disabled, RSAR and RxSIG will be updated as soon as the receive signaling bits have changed. 0 = Disables the Signaling Debounce feature. 1 = Enables the Signaling Debounce feature.

TABLE 57: RECEIVE SIGNALING CONTROL REGISTER 0-23 (RSCR 0-23) HEX ADDRESS: 0xn3A0 TO 0xn3B7

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>3-2</td><td>RxSIGC[1:0]]</td><td>R/W</td><td>00</td><td>Signaling conditioning [1:0]
These bits allow user to select the format of signaling substitution on a per-channel basis, as presented in the table below.
<table>
<tr><th>RxSIGC[1:0]</th><th>SIGNALING SUBSTITUTION SCHEMES</th></tr>
<tr><td>00</td><td>Substitutes all signaling bits with one.</td></tr>
<tr><td>01</td><td>Enables 16-code (A,B,C,D) signaling substitution.
Users must write to bits 3-0 in the Receive Signaling Substitution Register (RSSR) to provide the 16-code (A,B,C,D) signaling substitution values.</td></tr>
<tr><td>10</td><td>Enables 4-code (A,B) signaling substitution.
Users must write to bits 4-5 in the Receive Signaling Substitution Register (RSSR) to provide the 4-code (A,B) signaling substitution values.</td></tr>
<tr><td>11</td><td>Enables 2-code (A) signaling substitution.
Users must write to bit 6 in the Receive Signaling Substitution Register (RSSR) to provide the 2-code (A) signaling substitution values.</td></tr>
</table></td></tr>
<tr><td>1-0</td><td>RxSIGE[1:0]</td><td>R/W</td><td>00</td><td>Receive Signaling Extraction [1:0]
These bits control per-channel signaling extraction as presented in the table below. Signaling information can be extracted to the Receive Signaling Array Register (RSAR), the Receive Signaling Output pin (RxSIG_n) if the Receive SIgnaling Interface is enable, or the Receive Overhead Interface output (RxOH_n) if OH_ENB bit is enabled. (bit 5 of this register).
<table>
<tr><th>RxSIGE[1:0]</th><th>SIGNALING EXTRACTION SCHEMES</th></tr>
<tr><td>00</td><td>No signaling information is extracted.</td></tr>
<tr><td>01</td><td>Enables 16-code (A,B,C,D) signaling extraction.
All signaling bits A,B,C,D will be extracted.</td></tr>
<tr><td>10</td><td>Enables 4-code (A,B) signaling extraction
Only signaling bits A,B will be extracted.</td></tr>
<tr><td>11</td><td>Enables 2-code (A) signaling extraction
Only signaling bit A will be extracted.</td></tr>
</table></td></tr>
</table>

TABLE 58: RECEIVE SUBSTITUTION SIGNALING REGISTER 0-23 (RSSR 0-23) HEX ADDRESS: 0xn3C0 TO 0xn3D7

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-4	Reserved	-	-	**Reserved**
3	SIG16-A, 4-A, 2-A	R/W	0	**16-code/4-code/2-code Signaling Bit A** This bit provides the value of signaling bit A to substitute the receive signaling bit A on a per channel basis when 16-code or 4-code or 2-code signaling substitution is enabled.
2	SIG16-B, 4-B, 2-A	R/W	0	**16-code/4-code Signaling Bit B** This bit provides the value of signaling bit B to substitute the receive signaling bit B on a per channel basis when 16-code or 4-code signaling substitution is enabled.
1	SIG16-C, 4-A, 2-A	R/W	0	**16-code Signaling Bit C** This bit provides the value of signaling bit C to substitute the receive signaling bit C on a per channel basis when 16-code signaling substitution is enabled.
0	SIG16-D, 4-B, 2-A	R/W	0	**16-code Signaling Bit D** This bit provides the value of signaling bit D to substitute the receive signaling bit D on a per channel basis when 16-code signaling substitution is enabled.

TABLE 59: RECEIVE SIGNALING ARRAY REGISTER 0 TO 23 (RSAR 0-23) HEX ADDRESS: 0Xn500 TO 0XN517

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-4	Reserved	-	-	**Reserved**
3	A	RO	0	These READ ONLY registers reflect the most recently received signaling value (A,B,C,D) associated with timeslot 0 to 31. If signaling debounce feature is enabled, the received signaling state must be the same for 2 superframes before this register is updated. If the signaling bits for two consecutive superframes are not the same, the current value of this register will not be changed. When Bit 7 within register 0xn107 is set to ’1’, signaling bits in this register are updated on superframe boundary If the signaling debounce feature is disabled or if Bit 7 within register 0xn107 is set to ’0’, this register is updated as soon as the received signaling bits have changed. ***NOTE:*** *The content of this register only has meaning when robbed-bit signaling is enabled.*
2	B	RO	0	
1	C	RO	0	
0	D	RO	0	

TABLE 60: LAPD BUFFER 0 CONTROL REGISTER (LAPDBCR0) HEX ADDRESS: 0xn600

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	LAPD Buffer 0	R/W	0	**LAPD Buffer 0 (96-Bytes) Auto Incrementing** This register is used to transmit and receive LAPD messages within buffer 0 of the HDLC controller. Any one of the three HDLC controller can be chosen in the LAPD Select Register (0xn11B). Users should determine the next available buffer by reading the BUFAVAL bit (bit 7 of the Transmit Data Link Byte Count Register 1 (address 0xn114), Register 2 (0xn144) and Register 3 (0xn154) depending on which HDLC controller is selected. If buffer 0 is available, writing to buffer 0 will insert the message into the outgoing LAPD frame after the LAPD message is sent and the data from the transmit buffer cannot be retrieved. After detecting the Receive end of transfer interrupt (RxEOT), users should read the RBUFPTR bit (bit 7 of the Receive Data Link Byte Count Register 1 (address 0xn115), Register 2 (0xn145), or Register 3 (0xn155) depending on which HDLC controller is selected) to determine which buffer contains the received LAPD message ready to be read. If RBUFPTR bit indicates that buffer 0 is available to be read, reading buffer 0 (Register 0xn600) continuously will retrieve the entire received LAPD message. **NOTE:** *When writing to or reading from Buffer 0, the register is automatically incremented such that the entire 96 Byte LAPD message can be written into or read from buffer 0 (Register 0xn600) continuously.*

TABLE 61: LAPD BUFFER 1 CONTROL REGISTER (LAPDBCR1) HEX ADDRESS: 0xn700

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	LAPD Buffer 1	R/W	0	**LAPD Buffer 1 (96-Bytes) Auto Incrementing** This register is used to transmit and receive LAPD messages within buffer 1 of the HDLC controller. Any one of the three HDLC controller can be is chosen in the LAPD Select Register (0xn11B). Users should determine the next available buffer by reading the BUFAVAL bit (bit 7 of the Transmit Data Link Byte Count Register 1 (address 0xn114), Register 2 (0xn144) and Register 3 (0xn154) depending on which HDLC controller is selected. If buffer 1 is available, writing to buffer 1 will insert the message into the outgoing LAPD frame after the LAPD message is sent and the data from the transmit buffer 1 cannot be retrieved. After detecting the Receive end of transfer interrupt (RxEOT), users should read the RBUFPTR bit (bit 7 of the Receive Data Link Byte Count Register 1 (address 0xn115), Register 2 (0xn145), or Register 3 (0xn155) depending on which HDLC controller is selected) to determine which buffer contains the received LAPD message ready to be read. If RBUFPTR bit indicates that buffer 1 is available to be read, reading buffer 1 (Register 0xn700) continuously will retrieve the entire received LAPD message. **NOTE:** *When writing to or reading from Buffer 0, the register is automatically incremented such that the entire 96 Byte LAPD message can be written into or read from buffer 0 (Register 0xn600) continuously.*

TABLE 62: PMON RECEIVE LINE CODE VIOLATION COUNTER MSB (RLCVCU) HEX ADDRESS: 0xn900

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RLCVC[15]	RUR	0	**Performance Monitor "Receive Line Code Violation" 16-bit Counter - Upper Byte:** These RESET-upon-READ bits, along with that within the PMON Receive Line Code Violation Counter Register LSB combine to reflect the cumulative number of instances that Line Code Violation has been detected by the Receive T1 Framer block since the last read of this register. This register contains the Most Significant byte of this 16-bit of the Line Code Violation counter. **NOTE:** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	RLCVC[14]	RUR	0	
5	RLCVC[13]	RUR	0	
4	RLCVC[12]	RUR	0	
3	RLCVC[11]	RUR	0	
2	RLCVC[10]	RUR	0	
1	RLCVC[9]	RUR	0	
0	RLCVC[8]	RUR	0	

TABLE 63: PMON RECEIVE LINE CODE VIOLATION COUNTER LSB (RLCVCL) HEX ADDRESS: 0xn901

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RLCVC[7]	RUR	0	**Performance Monitor "Receive Line Code Violation" 16-bit Counter - Lower Byte:** These RESET-upon-READ bits, along with that within the PMON Receive Line Code Violation Counter Register MSB combine to reflect the cumulative number of instances that Line Code Violation has been detected by the Receive T1 Framer block since the last read of this register. This register contains the Least Significant byte of this 16-bit of the Line Code Violation counter. **NOTE:** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	RLCVC[6]	RUR	0	
5	RLCVC[5]	RUR	0	
4	RLCVC[4]	RUR	0	
3	RLCVC[3]	RUR	0	
2	RLCVC[2]	RUR	0	
1	RLCVC[1]	RUR	0	
0	RLCVC[0]	RUR	0	

TABLE 64: PMON RECEIVE FRAMING ALIGNMENT BIT ERROR COUNTER MSB (RFAECU) HEX ADDRESS: 0xn902

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RFAEC[15]	RUR	0	**Performance Monitor "Receive Framing Alignment Error 16-Bit counter" - Upper Byte:** These RESET-upon-READ bits, along with that within the "PMON Receive Framing Alignment Error Counter Register LSB" combine to reflect the cumulative number of instances that the Receive Framing Alignment errors has been detected by the Receive T1 Framer block since the last read of this register. This register contains the Most Significant byte of this 16-bit of the Receive Framing Alignment Error counter. **NOTE:** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	RFAEC[14]	RUR	0	
5	RFAEC[13]	RUR	0	
4	RFAEC[12]	RUR	0	
3	RFAEC[11]	RUR	0	
2	RFAEC[10]	RUR	0	
1	RFAEC[9]	RUR	0	
0	RFAEC[8]	RUR	0	

TABLE 65: PMON RECEIVE FRAMING ALIGNMENT BIT ERROR COUNTER LSB (RFAECL) HEX ADDRESS: 0xn903

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RFAEC[7]	RUR	0	**Performance Monitor "Receive Framing Alignment Error 16-Bit Counter" - Lower Byte:** These RESET-upon-READ bits, along with that within the "PMON Receive Framing Alignment Error Counter Register MSB" combine to reflect the cumulative number of instances that the Receive Framing Alignment errors has been detected by the Receive T1 Framer block since the last read of this register. This register contains the Least Significant byte of this 16-bit of the Receive Framing Alignment Error counter. **NOTE:** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	RFAEC[6]	RUR	0	
5	RFAEC[5]	RUR	0	
4	RFAEC[4]	RUR	0	
3	RFAEC[3]	RUR	0	
2	RFAEC[2]	RUR	0	
1	RFAEC[1]	RUR	0	
0	RFAEC[0]	RUR	0	

TABLE 66: PMON RECEIVE SEVERELY ERRORED FRAME COUNTER (RSEFC) HEX ADDRESS: 0xn904

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RSEFC[7]	RUR	0	**Performance Monitor - Receive Severely Errored frame Counter (8-bit Counter)** These Reset-Upon-Read bit fields reflect the cumulative number of instances that Receive Severely Errored Frames have been detected by the T1 Framer since the last read of this register. in T1 mode, Severely Errored Frame is defined as having framing bit errors in contiguous windows. In T1 SF mode, SEF is defined if Ft bits have been received consecutively in errors for 0.75ms or 6 SF frames. In T1 ESF mode, SEF is defined if FPS bit have been received consecutively in errors for 3 ms or 24 ESF frames.
6	RSEFC[6]	RUR	0	
5	RSEFC[5]	RUR	0	
4	RSEFC[4]	RUR	0	
3	RSEFC[3]	RUR	0	
2	RSEFC[2]	RUR	0	
1	RSEFC[1]	RUR	0	
0	RSEFC[0]	RUR	0	

TABLE 67: PMON RECEIVE CRC-6 BIT ERROR COUNTER - MSB (RSBBECU) HEX ADDRESS: 0xn905

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RSBBEC[15]	RUR	0	**Performance Monitor "Receive Synchronization Bit Error 16-Bit Counter" - Upper Byte:** These RESET-upon-READ bits, along with that within the "PMON Receive Synchronization Bit Error Counter Register LSB" combine to reflect the cumulative number of instances that the Receive Synchronization Bit errors has been detected by the Receive T1 Framer block since the last read of this register. This register contains the Most Significant byte of this 16-bit of the Receive Synchronization Bit Error counter. **NOTE:** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	RSBBEC[14]	RUR	0	
5	RSBBEC[13]	RUR	0	
4	RSBBEC[12]	RUR	0	
3	RSBBEC[11]	RUR	0	
2	RSBBEC[10]	RUR	0	
1	RSBBEC[9]	RUR	0	
0	RSBBEC[8]	RUR	0	

TABLE 68: PMON RECEIVE CRC-6 BIT ERROR COUNTER - LSB (RSBBECL) HEX ADDRESS: 0xn906

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RSBBEC[7]	RUR	0	**Performance Monitor "Receive Synchronization Bit Error 16-Bit Counter" - Lower Byte:** These RESET-upon-READ bits, along with that within the "PMON Receive Synchronization Bit Error Counter Register MSB" combine to reflect the cumulative number of instances that the Receive Synchronization Bit errors has been detected by the Receive T1 Framer block since the last read of this register. This register contains the Least Significant byte of this 16-bit of the Receive Synchronization Bit Error counter. **NOTE:** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	RSBBEC[6]	RUR	0	
5	RSBBEC[5]	RUR	0	
4	RSBBEC[4]	RUR	0	
3	RSBBEC[3]	RUR	0	
2	RSBBEC[2]	RUR	0	
1	RSBBEC[1]	RUR	0	
0	RSBBEC[0]	RUR	0	

TABLE 69: PMON RECEIVE SLIP COUNTER (RSC) HEX ADDRESS: 0xn909

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RSC[7]	RUR	0	**Performance Monitor - Receive Slip Counter (8-bit Counter)** These Reset-Upon-Read bit fields reflect the cumulative number of instances that Receive Slip events have been detected by the T1 Framer since the last read of this register. **NOTE:** *A slip event is defined as a replication or deletion of a T1 frame by the receive slip buffer.*
6	RSC[6]	RUR	0	
5	RSC[5]	RUR	0	
4	RSC[4]	RUR	0	
3	RSC[3]	RUR	0	
2	RSC[2]	RUR	0	
1	RSC[1]	RUR	0	
0	RSC[0]	RUR	0	

TABLE 70: PMON RECEIVE LOSS OF FRAME COUNTER (RLFC) HEX ADDRESS: 0xn90A

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RLFC[7]	RUR	0	**Performance Monitor - Receive Loss of Frame Counter (8-bit Counter)** These Reset-Upon-Read bit fields reflect the cumulative number of instances that Receive Loss of Frame condition have been detected by the T1 Framer since the last read of this register. **NOTE:** *This counter counts once every time the Loss of Frame condition is declared. This counter provides the capability to measure an accumulation of short failure events.*
6	RLFC[6]	RUR	0	
5	RLFC[5]	RUR	0	
4	RLFC[4]	RUR	0	
3	RLFC[3]	RUR	0	
2	RLFC[2]	RUR	0	
1	RLFC[1]	RUR	0	
0	RLFC[0]	RUR	0	

TABLE 71: PMON RECEIVE CHANGE OF FRAME ALIGNMENT COUNTER (RCFAC) HEX ADDRESS: 0xn90B

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RCFAC[7]	RUR	0	**Performance Monitor - Receive Change of Frame Alignment Counter (8-bit Counter)** These Reset-Upon-Read bit fields reflect the cumulative number of instances that Receive Change of Framing Alignment have been detected by the T1 Framer since the last read of this register. **NOTE:** *Change of Framing Alignment (COFA) is declared when the newly-locked framing pattern is different from the one offered by off-line framer.*
6	RCFAC[6]	RUR	0	
5	RCFAC[5]	RUR	0	
4	RCFAC[4]	RUR	0	
3	RCFAC[3]	RUR	0	
2	RCFAC[2]	RUR	0	
1	RCFAC[1]	RUR	0	
0	RCFAC[0]	RUR	0	

TABLE 72: PMON LAPD1 FRAME CHECK SEQUENCE ERROR COUNTER 1 (LFCSEC1) HEX ADDRESS: 0xn90C

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	FCSEC1[7]	RUR	0	**Performance Monitor - LAPD 1 Frame Check Sequence Error Counter (8-bit Counter)** These Reset-Upon-Read bit fields reflect the cumulative number of instances that Frame Check Sequence Error have been detected by the LAPD Controller 1 since the last read of this register.
6	FCSEC1[6]	RUR	0	
5	FCSEC1[5]	RUR	0	
4	FCSEC1[4]	RUR	0	
3	FCSEC1[3]	RUR	0	
2	FCSEC1[2]	RUR	0	
1	FCSEC1[1]	RUR	0	
0	FCSEC1[0]	RUR	0	

TABLE 73: PRBS BIT ERROR COUNTER MSB (PBECU) HEX ADDRESS: 0xn90D

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	PRBSE[15]	RUR	0	**Performance Monitor - T1 PRBS Bit Error 16-Bit Counter - Upper Byte:** These RESET-upon-READ bits, along with that within the “PMON T1 PRBS Bit Error Counter Register LSB” combine to reflect the cumulative number of instances that the ReceiveT1 PRBS Bit errors has been detected by the Receive T1 Framer block since the last read of this register. This register contains the Most Significant byte of this 16-bit of the Receive T1 PRBS Bit Error counter. **NOTE:** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	PRBSE[14]	RUR	0	
5	PRBSE[13]	RUR	0	
4	PRBSE[12]	RUR	0	
3	PRBSE[11]	RUR	0	
2	PRBSE[10]	RUR	0	
1	PRBSE[9]	RUR	0	
0	PRBSE[8]	RUR	0	

TABLE 74: PRBS BIT ERROR COUNTER LSB (PBECL) HEX ADDRESS: 0xn90E

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	PRBSE[7]	RUR	0	**Performance Monitor - T1 PRBS Bit Error 16-Bit Counter - Lower Byte:** These RESET-upon-READ bits, along with that within the “PMON T1 PRBS Bit Error Counter Register MSB” combine to reflect the cumulative number of instances that the ReceiveT1 PRBS Bit errors has been detected by the Receive T1 Framer block since the last read of this register. This register contains the Least Significant byte of this 16-bit of the Receive T1 PRBS Bit Error counter. **NOTE:** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	PRBSE[6]	RUR	0	
5	PRBSE[5]	RUR	0	
4	PRBSE[4]	RUR	0	
3	PRBSE[3]	RUR	0	
2	PRBSE[2]	RUR	0	
1	PRBSE[1]	RUR	0	
0	PRBSE[0]	RUR	0	

TABLE 75: TRANSMIT SLIP COUNTER (TSC) HEX ADDRESS: 0xn90F

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxSLIP[7]	RUR	0	**Performance Monitor - Transmit Slip Counter (8-bit Counter)** These Reset-Upon-Read bit fields reflect the cumulative number of instances that Transmit Slip events have been detected by the T1 Framer since the last read of this register. **NOTE:** *A slip event is defined as a replication or deletion of a T1 frame by the transmit slip buffer.*
6	TxSLIP[6]	RUR	0	
5	TxSLIP[5]	RUR	0	
4	TxSLIP[4]	RUR	0	
3	TxSLIP[3]	RUR	0	
2	TxSLIP[2]	RUR	0	
1	TxSLIP[1]	RUR	0	
0	TxSLIP[0]	RUR	0	

TABLE 76: EXCESSIVE ZERO VIOLATION COUNTER MSB (EZVCU) HEX ADDRESS: 0xn910

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	EZVC[15]	RUR	0	**Performance Monitor - T1 Excessive Zero Violation 16-Bit Counter - Upper Byte:** These RESET-upon-READ bits, along with that within the “PMON T1 Excessive Zero Violation Counter Register LSB” combine to reflect the cumulative number of instances that the ReceiveT1 Excessive Zero Violation has been detected by the Receive T1 Framer block since the last read of this register. This register contains the Most Significant byte of this 16-bit of the Receive T1 Excessive Zero Violation counter. **NOTE:** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	EZVC[14]	RUR	0	
5	EZVC[13]	RUR	0	
4	EZVC[12]	RUR	0	
3	EZVC[11]	RUR	0	
2	EZVC[10]	RUR	0	
1	EZVC[9]	RUR	0	
0	EZVC[8]	RUR	0	

TABLE 77: EXCESSIVE ZERO VIOLATION COUNTER LSB (EZVCL) HEX ADDRESS: 0xn911

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	EZVC[7]	RUR	0	**Performance Monitor - T1 Excessive Zero Violation 16-Bit Counter - Lower Byte:** These RESET-upon-READ bits, along with that within the “PMON T1 Excessive Zero Violation Counter Register MSB” combine to reflect the cumulative number of instances that the ReceiveT1 Excessive Zero Violation has been detected by the Receive T1 Framer block since the last read of this register. This register contains the Least Significant byte of this 16-bit of the Receive T1 Excessive Zero Violation counter. **NOTE:** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	EZVC[6]	RUR	0	
5	EZVC[5]	RUR	0	
4	EZVC[4]	RUR	0	
3	EZVC[3]	RUR	0	
2	EZVC[2]	RUR	0	
1	EZVC[1]	RUR	0	
0	EZVC[0]	RUR	0	

TABLE 78: PMON LAPD2 FRAME CHECK SEQUENCE ERROR COUNTER 2 (LFCSEC2) HEX ADDRESS: 0xn91C

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	FCSEC2[7]	RUR	0	**Performance Monitor - LAPD 2 Frame Check Sequence Error Counter (8-bit Counter)** These Reset-Upon-Read bit fields reflect the cumulative number of instances that Frame Check Sequence Error have been detected by the LAPD Controller 2 since the last read of this register.
6	FCSEC2[6]	RUR	0	
5	FCSEC2[5]	RUR	0	
4	FCSEC2[4]	RUR	0	
3	FCSEC2[3]	RUR	0	
2	FCSEC2[2]	RUR	0	
1	FCSEC2[1]	RUR	0	
0	FCSEC2[0]	RUR	0	

TABLE 79: PMON LAPD2 FRAME CHECK SEQUENCE ERROR COUNTER 3 (LFCSEC3) HEX ADDRESS: 0xn92C

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	FCSEC3[7]	RUR	0	**Performance Monitor - LAPD 3 Frame Check Sequence Error Counter (8-bit Counter)** These Reset-Upon-Read bit fields reflect the cumulative number of instances that Frame Check Sequence Error have been detected by the LAPD Controller 3 since the last read of this register.
6	FCSEC3[6]	RUR	0	
5	FCSEC3[5]	RUR	0	
4	FCSEC3[4]	RUR	0	
3	FCSEC3[3]	RUR	0	
2	FCSEC3[2]	RUR	0	
1	FCSEC3[1]	RUR	0	
0	FCSEC3[0]	RUR	0	

TABLE 80: BLOCK INTERRUPT STATUS REGISTER (BISR) HEX ADDRESS: 0xnB00

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved			For E1 mode only
6	LBCODE	RO	0	**Loopback Code Block Interrupt Status** This bit indicates whether or not the Loopback Code block has an interrupt request awaiting service. 0 - Indicates no outstanding Loopback Code Block interrupt request is awaiting service 1 - Indicates the Loopback Code block has an interrupt request awaiting service. Interrupt Service routine should branch to the interrupt source and read the Loopback Code Interrupt Status register (address 0xnB0A) to clear the interrupt **NOTE:** *This bit will be reset to 0 after the microprocessor has performed a read to the Loopback Code Interrupt Status Register.*
5	RxClkLOS	RO	0	**Loss of Recovered Clock Interrupt Status** This bit indicates whether or not the framer has experienced a Loss of Recovered Clock interrupt since last read of this register. 0 = Indicates Loss of Recovered Clock interrupt has not occurred since last read of this register 1 = Indicates Loss of Recovered Clock interrupt has occurred since last read of this register. **NOTE:** *This bit is only active if the clock loss detection feature is enabled (Register - 0xn100)*
4	ONESEC	RO	0	**One Second Interrupt Status** This bit indicates whether or not the framer has experienced a One Second interrupt since the last read of this register. 0 = Indicates One Second interrupt has not occurred since the last read of this register 1 = Indicates One Second interrupt has occurred since the last read of this register
3	HDLC	RO	0	**HDLC Block Interrupt Status** This bit indicates whether or not the HDLC block has any interrupt request awaiting service. 0 = Indicates no outstanding HDLC block interrupt request is awaiting service 1 = Indicates HDLC Block has an interrupt request awaiting service. Interrupt Service routine should branch to the interrupt source and read the corresponding Data LInk Status Registers (address 0xnB06, 0xnB16, 0xnB26, 0xnB10, 0xnB18, 0xnB28) to clear the interrupt. **NOTE:** *This bit will be reset to 0 after the microprocessor has performed a read to the corresponding Data Link Status Registers that generated the interrupt.*

TABLE 80: BLOCK INTERRUPT STATUS REGISTER (BISR) **HEX ADDRESS: 0xnB00**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2	SLIP	RO	0	**Slip Buffer Block Interrupt Status** This bit indicates whether or not the Slip Buffer block has any outstanding interrupt request awaiting service. 0 = Indicates no outstanding Slip Buffer Block interrupt request is awaiting service 1 = Indicates Slip Buffer block has an interrupt request awaiting service. Interrupt Service routine should branch to the interrupt source and read the Slip Buffer Interrupt Status register (address 0xnB08) to clear the interrupt **NOTE:** *This bit will be reset to 0 after the microprocessor has performed a read to the Slip Buffer Interrupt Status Register.*
1	ALARM	RO	0	**Alarm & Error Block Interrupt Status** This bit indicates whether or not the Alarm & Error Block has any outstanding interrupt request awaiting service. 0 = Indicates no outstanding interrupt request is awaiting service 1 = Indicates the Alarm & Error Block has an interrupt request awaiting service. Interrupt service routine should branch to the interrupt source and read the corresponding alarm and error status registers (address 0xnB02, 0xnB0E, 0xnB40) to clear the interrupt. **NOTE:** *This bit will be reset to 0 after the microprocessor has performed a read to the corresponding Alarm & Error Interrupt Status register that generated the interrupt.*
0	T1 FRAME	RO	0	**T1 Framer Block Interrupt Status** This bit indicates whether or not the T1 Framer block has any outstanding interrupt request awaiting service. 0 = Indicates no outstanding interrupt request is awaiting service. 1 = Indicates the T1 Framer Block has an interrupt request awaiting service. Interrupt service routine should branch to the interrupt source and read the T1 Framer status register (address 0xnB04) to clear the interrupt **NOTE:** *This bit will be reset to 0 after the microprocessor has performed a read to the T1 Framer Interrupt Status register.*

TABLE 81: BLOCK INTERRUPT ENABLE REGISTER (BIER) **HEX ADDRESS: 0xnB01**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved			**For E1 mode only**
6	LBCODE_ENB	R/W	0	**Loopback Code Block interrupt enable** This bit permits the user to either enable or disable the Loopback Code Interrupt Block for interrupt generation. Writing a “0” to this register bit will disable the Loopback Code Block for interrupt generation, all Loopback Code interrupts will be disabled for interrupt generation. If the user writes a “1” to this register bit, the Loopback Code Interrupts at the “Block Level” will be enabled. However, the individual Loopback Code interrupts at the “Source Level” still need to be enabled to in order to generate that particular interrupt to the interrupt pin. 0 - Disables all Loopback Code Interrupt Block interrupt within the device. 1 - Enables the Loopback Code interrupt at the “Block-Level”.
5	RXCLKLOSS	R/W	0	**Loss of Recovered Clock Interrupt Enable** This bit permits the user to either enable or disable the Loss of Recovered Clock Interrupt for interrupt generation. 0 - Disables the Loss of Recovered Clock Interrupt within the device. 1 - Enables the Loss of Recovered Clock interrupt at the “Source-Level”.
4	ONESEC_ENB	R/W	0	**One Second Interrupt Enable** This bit permits the user to either enable or disable the One Second Interrupt for interrupt generation. 0 - Disables the One Second Interrupt within the device. 1 - Enables the One Second interrupt at the “Source-Level”.
3	HDLC_ENB	R/W	0	**HDLC Block Interrupt Enable** This bit permits the user to either enable or disable the HDLC Block for interrupt generation. Writing a “0” to this register bit will disable the HDLC Block for interrupt generation, all HDLC interrupts will be disabled for interrupt generation. If the user writes a “1” to this register bit, the HDLC Block interrupt at the “Block Level” will be enabled. However, the individual HDLC interrupts at the “Source Level” still need to be enabled in order to generate that particular interrupt to the interrupt pin. 0 - Disables all SA6 Block interrupt within the device. 1 - Enables the SA6 interrupt at the “Block-Level”.

TABLE 81: BLOCK INTERRUPT ENABLE REGISTER (BIER) **HEX ADDRESS: 0xnB01**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2	SLIP_ENB	R/W	0	**Slip Buffer Block Interrupt Enable** This bit permits the user to either enable or disable the Slip Buffer Block for interrupt generation. Writing a “0” to this register bit will disable the Slip Buffer Block for interrupt generation, then all Slip Buffer interrupts will be disabled for interrupt generation. If the user writes a “1” to this register bit, the Slip Buffer Block interrupt at the “Block Level” will be enabled. However, the individual Slip Buffer interrupts at the “Source Level” still need to be enabled in order to generate that particular interrupt to the interrupt pin. 0 - Disables all Slip Buffer Block interrupt within the device. 1 - Enables the Slip Buffer interrupt at the “Block-Level”.
1	ALARM_ENB	R/W	0	**Alarm & Error Block Interrupt Enable** This bit permits the user to either enable or disable the Alarm & Error Block for interrupt generation. Writing a “0” to this register bit will disable the Alarm & Error Block for interrupt generation, then all Alarm & Error interrupts will be disabled for interrupt generation. If the user writes a “1” to this register bit, the Alarm & Error Block interrupt at the “Block Level” will be enabled. However, the individual Alarm & Error interrupts at the “Source Level” still need to be enabled in order to generate that particular interrupt to the interrupt pin. 0 - Disables all Alarm & Error Block interrupt within the device. 1 - Enables the Alarm & Error interrupt at the “Block-Level”.
0	T1FRAME_ENB	R/W	0	**T1 Framer Block Enable** This bit permits the user to either enable or disable the T1 Framer Block for interrupt generation. Writing a “0” to this register bit will disable the T1 Framer Block for interrupt generation, then all T1 Framer interrupts will be disabled for interrupt generation. If the user writes a “1” to this register bit, the T1 Framer Block interrupt at the “Block Level” will be enabled. However, the individual T1 Framer interrupts at the “Source Level” still need to be enabled in order to generate that particular interrupt to the interrupt pin. 0 - Disables all T1 Framer Block interrupt within the device. 1 - Enables the T1 Framer interrupt at the “Block-Level”.

TABLE 82: ALARM & ERROR INTERRUPT STATUS REGISTER (AEISR) **HEX ADDRESS: 0xnB02**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Rx LOF State	RO	0	**Receive Loss of Frame State** This READ-ONLY bit indicates whether or not the Receive T1 Framer block is currently declaring the “Loss of Frame” condition within the incoming T1 data-stream, as described below. Loss of Frame is declared when “TOLR” out of “RANG” errors in the framing bit pattern is detected. (Register 0xn10B) 0 – The Receive T1 Framer block is NOT currently declaring the “Loss of Frame” condition. 1 – The Receive T1 Framer block is currently declaring the “Loss of Frame” condition.
6	RxAIS State	RO	0	**Receive Alarm Indication Status Defect State** This READ-ONLY bit indicates whether or not the Receive T1 Framer block is currently declaring the AIS defect condition within the incoming T1 data-stream, as described below. AIS defect is declared when AIS condition persists for 42 milliseconds. AIS defect is cleared when AIS condition is absent for 42 milliseconds. 0 – The Receive T1 Framer block is NOT currently declaring the AIS defect condition. 1 – The Receive T1 Framer block is currently declaring the AIS defect condition.
5	RxYEL_State	RO	0	**Receive Yellow Alarm State** This READ-ONLY bit indicates whether or not the Receive T1 Framer block is currently declaring the Yellow Alarm condition within the incoming T1 data-stream, as described below. Yellow alarm or Remote Alarm Indication (RAI) is declared when RAI condition persists for 900 milliseconds. Yellow alarm or RAI is cleared immediately when RAI condition is absent even if the T1 Framer is receiving T1 Idle or RAI-CI signatures in ESF mode. 0 – The Receive T1 Framer block is NOT currently declaring the Yellow Alarm condition. 1 – The Receive T1 Framer block is currently declaring the Yellow Alarm condition.
4	LOS_State	RO	0	**Framer Receive Loss of Signal (LOS) State** This READ-ONLY bit indicates whether or not the Receive T1 framer is currently declaring the Loss of Signal (LOS) condition within the incoming T1 data-stream, as described below LOS defect is declared when LOS condition persists for 175 consecutive bits. LOS defect is cleared when LOS condition is absent or when the received signal reaches a 12.5% ones density for 175 consecutive bits. 0 = The Receive T1 Framer block is NOT currently declaring the Loss of Signal (LOS) condition. 1 = The Receive T1 Framer block is currently declaring the Loss of Signal (LOS) condition.

TABLE 82: ALARM & ERROR INTERRUPT STATUS REGISTER (AEISR) **HEX ADDRESS: 0xnB02**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	LCV Int Status	RUR/ WC	0	**Line Code Violation Interrupt Status**. This Reset-Upon-Read bit field indicates whether or not the Receive T1 LIU block has detected a Line Code Violation interrupt since the last read of this register. 0 = Indicates no Line Code Violation have occurred since the last read of this register. 1 = Indicates one or more Line Code Violation interrupt has occurred since the last read of this register.
2	Rx LOF State Change	RUR/ WC	0	**Change in Receive Loss of Frame Condition Interrupt Status**. This Reset-Upon-Read bit field indicates whether or not the "Change in Receive Loss of Frame Condition" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block declares the Loss of Frame condition. **2.** Whenever the Receive T1 Framer block clears the Loss of Frame condition 0 = Indicates that the "Change in Receive Loss of Frame condition" interrupt has not occurred since the last read of this register 1 = Indicates that the "Change in Receive Loss of Frame condition" interrupt has occurred since the last read of this register
1	RxAIS State Change	RUR/ WC	0	**Change in Receive AIS Condition Interrupt Status**. This Reset-Upon-Read bit field indicates whether or not the "Change in Receive AIS Condition" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block declares the AIS condition. **2.** Whenever the Receive T1 Framer block clears the AIS condition 0 = Indicates that the "Change in Receive AIS condition" interrupt has not occurred since the last read of this register 1 = Indicates that the "Change in Receive AIS condition" interrupt has occurred since the last read of this register
0	RxYEL State Change	RUR/ WC	0	**Change in Receive Yellow Alarm Interrupt Status.** This Reset-Upon-Read bit field indicates whether or not the "Change in Receive Yellow Alarm Condition" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block declares the Yellow Alarm condition. **2.** Whenever the Receive T1 Framer block clears the Yellow Alarm condition 0 = Indicates that the "Change in Receive Yellow Alarm condition" interrupt has not occurred since the last read of this register 1 = Indicates that the "Change in Receive Yellow Alarm condition" interrupt has occurred since the last read of this register

TABLE 83: ALARM & ERROR INTERRUPT ENABLE REGISTER (AEIER) **HEX ADDRESS: 0xnB03**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-5	Reserved	-	-	**Reserved (E1 mode only)**
4	-	-	-	**This bit should be set to'0' for proper operation.**
3	LCV ENB	R/W	0	**Line Code violation interrupt enable** This bit permits the user to either enable or disable the "Line Code Violation" interrupt within the XRT86VL38 device. If the user enables this interrupt, then the Receive T1 Framer block will generate an interrupt when Line Code Violation is detected. 0 = Disables the interrupt generation when Line Code Violation is detected. 1 = Enables the interrupt generation when Line Code Violation is detected.
2	RxLOF ENB	R/W	0	**Change in Loss of Frame Condition interrupt enable** This bit permits the user to either enable or disable the "Change in Loss of Frame Condition" Interrupt, within the XRT86VL38 device. If the user enables this interrupt, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** The instant that the Receive T1 Framer block declares the Loss of Frame condition. **2.** The instant that the Receive T1 Framer block clears the Loss of Frame condition. 0 – Disables the "Change in Loss of Frame Condition" Interrupt. 1 – Enables the "Change in Loss of Frame Condition" Interrupt.
1	RxAIS ENB	R/W	0	**Change in AIS Condition interrupt enable** This bit permits the user to either enable or disable the "Change in AIS Condition" Interrupt, within the XRT86VL38 device. If the user enables this interrupt, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** The instant that the Receive T1 Framer block declares the AIS condition. **2.** The instant that the Receive T1 Framer block clears the AIS condition. 0 – Disables the "Change in AIS Condition" Interrupt. 1 – Enables the "Change in AIS Condition" Interrupt.
0	RxYEL ENB	R/W	0	**Change in Yellow alarm Condition interrupt enable** This bit permits the user to either enable or disable the "Change in Yellow Alarm Condition" Interrupt, within the XRT86VL38 device. If the user enables this interrupt, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** The instant that the Receive T1 Framer block declares the Yellow Alarm condition. **2.** The instant that the Receive T1 Framer block clears the Yellow Alarm condition. 0 – Disables the "Change in Yellow Alarm Condition" Interrupt. 1 – Enables the "Change in Yellow Alarm Condition" Interrupt.

TABLE 84: FRAMER INTERRUPT STATUS REGISTER (FISR) **HEX ADDRESS: 0xnB04**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-6	-	-	-	**Reserved (For E1 mode only)**
5	SIG	RUR/ WC	0	**Change in Signaling Bits Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the “Change in Signaling Bits” interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt whenever any one of the four signaling bits values (A,B,C,D) has changed in any one of the 24 channels within the incoming T1 frames. Users can read the signaling change registers (address 0xn10D-0xn10F) to determine which signalling channel has changed. 0 = Indicates that the “Change in Signaling Bits” interrupt has not occurred since the last read of this register. 1 = Indicates that the “Change in Signaling Bits” interrupt has occurred since the last read of this register. ***NOTE:*** *This bit only has meaning when Robbed-Bit Signaling is enabled.*
4	COFA	RUR/ WC	0	**Change of Frame Alignment (COFA) Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the “Change of Framing Alignment (COFA)” interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt whenever the Receive T1 Framer block detects a Change of Framing Alignment Signal (e.g., the Framing bits have appeared to move to a different location within the incoming T1 data stream). 0 = Indicates that the “Change of Framing Alignment (COFA)” interrupt has not occurred since the last read of this register. 1 = Indicates that the “Change of Framing Alignment (COFA)” interrupt has occurred since the last read of this register.
3	LOF_Status	RUR/ WC	0	**Change in Receive Loss of Frame Condition Interrupt Status**. This Reset-Upon-Read bit field indicates whether or not the “Change in Receive Loss of Frame Condition” interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block declares the Loss of Frame condition. **2.** Whenever the Receive T1 Framer block clears the Loss of Frame condition 0 = Indicates that the “Change in Receive Loss of Frame condition” interrupt has not occurred since the last read of this register 1 = Indicates that the “Change in Receive Loss of Frame condition” interrupt has occurred since the last read of this register

TABLE 84: FRAMER INTERRUPT STATUS REGISTER (FISR) **HEX ADDRESS: 0xnB04**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2	FMD	RUR/ WC	0	**Frame Mimic Detection Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Frame Mimic Detection" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt whenever the Receive T1 Framer block detects the presence of Frame Mimic bits (i.e., the Payload bits have appeared to mimic the Framing Bit pattern within the incoming T1 data stream). 0 = Indicates that the "Frame Mimic Detection" interrupt has not occurred since the last read of this register. 1 = Indicates that the "Frame Mimic Detection" interrupt has occurred since the last read of this register.
1	SE	RUR/ WC	0	**Synchronization Bit Error (CRC-6) Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "CRC-6 Error" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt whenever the Receive T1 Framer block detects a CRC-6 Error within the incoming T1 multiframe. 0 = Indicates that the "CRC-6 Error" interrupt has not occurred since the last read of this register. 1 = Indicates that the "CRC-6 Error" interrupt has occurred since the last read of this register.
0	FE	RUR/ WC	0	**Framing Error Interrupt Status** This Reset-Upon-Read bit field indicates whether or not a "Framing Error" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt whenever the Receive T1 Framer block detects one or more Framing Alignment Bit Error within the incoming T1 data stream. 0 = Indicates that the "Framing Error" interrupt has not occurred since the last read of this register. 1 = Indicates that the "Framing Error" interrupt has occurred since the last read of this register. **NOTE:** *This bit doesn't not necessarily indicate that synchronization has been lost.*

TABLE 85: FRAMER INTERRUPT ENABLE REGISTER (FIER) **HEX ADDRESS: 0xnB05**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
5	SIG_ENB	R/W	0	**Change in Signaling Bits Interrupt Enable** This bit permits the user to either enable or disable the “Change in Signaling Bits” Interrupt, within the XRT86VL38 device. If the user enables this interrupt, then the Receive T1 Framer block will generate an interrupt when it detects a change in the any four signaling bits (A,B,C,D) in any one of the 24 signaling channels. Users can read the signaling change registers (address 0xn10D-0xn10F) to determine which signalling channel has changed state. 0 - Disables the Change in Signaling Bits Interrupt 1 - Enables the Change in Signaling Bits Interrupt ***NOTE:*** *This bit has no meaning when Robbed-Bit Signaling is disabled.*
4	COFA_ENB	R/W	0	**Change of Framing Alignment (COFA) Interrupt Enable** This bit permits the user to either enable or disable the “Change in FAS Framing Alignment (COFA)” Interrupt, within the XRT86VL38 device. If the user enables this interrupt, then the Receive T1 Framer block will generate an interrupt when it detects a Change of Framing Alignment Signal (e.g., the Framing bits have appeared to move to a different location within the incoming T1 data stream). 0 - Disables the “Change of Framing Alignment (COFA)” Interrupt. 1 - Enables the “Change of Framing Alignment (COFA)” Interrupt.
3	LOF_ENB	R/W	0	**Change in Loss of Frame Condition interrupt enable** This bit permits the user to either enable or disable the “Change in Loss of Frame Condition” Interrupt, within the XRT86VL38 device. If the user enables this interrupt, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** The instant that the Receive T1 Framer block declares the Loss of Frame condition. **2.** The instant that the Receive T1 Framer block clears the Loss of Frame condition. 0 – Disables the “Change in Loss of Frame Condition” Interrupt. 1 – Enables the “Change in Loss of Frame Condition” Interrupt.
2	FMD_ENB	R/W	0	**Frame Mimic Detection Interrupt Enable** This bit permits the user to either enable or disable the “Frame Mimic Detection” Interrupt, within the XRT86VL38 device. If the user enables this interrupt, then the Receive T1 Framer block will generate an interrupt when it detects the presence of Frame mimic bits (i.e., the payload bits have appeared to mimic the framing bit pattern within the incoming T1 data stream). 0 - Disables the “Frame Mimic Detection” Interrupt. 1 - Enables the “Frame Mimic Detection” Interrupt.

TABLE 85: FRAMER INTERRUPT ENABLE REGISTER (FIER) **HEX ADDRESS: 0xnB05**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	SE_ENB	R/W	0	**Synchronization Bit (CRC-6) Error Interrupt Enable** This bit permits the user to either enable or disable the “CRC-6 Error Detection” Interrupt, within the XRT86VL38 device. If the user enables this interrupt, then the Receive T1 Framer block will generate an interrupt when it detects a CRC-6 error within the incoming T1 multiframe. 0 - Disables the “CRC-6 Error Detection” Interrupt. 1 - Enables the “CRC-6 Error Detection” Interrupt.
0	FE_ENB	R/W	0	**Framing Bit Error Interrupt Enable** This bit permits the user to either enable or disable the “Framing Alignment Bit Error Detection” Interrupt, within the XRT86VL38 device. If the user enables this interrupt, then the Receive T1 Framer block will generate an interrupt when it detects one or more Framing Alignment Bit error within the incoming T1 data stream. 0 - Disables the “Framing Alignment Bit Error Detection” Interrupt. 1 - Enables the “Framing Alignment Bit Error Detection” Interrupt. ***NOTE:*** *Detecting Framing Alignment Bit Error doesn't not necessarily indicate that synchronization has been lost.*

TABLE 86: DATA LINK STATUS REGISTER 1 (DLSR1) **HEX ADDRESS: 0xnB06**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	MSG TYPE	RO	0	**HDLC1 Message Type Identifier** This READ ONLY bit indicates the type of data link message received by Receive HDLC 1 Controller. Two types of data link messages are supported within the XRT86VL38 device: Message Oriented Signaling (MOS) or Bit-Oriented Signalling (BOS). 0 = Indicates Bit-Oriented Signaling (BOS) type data link message is received 1 = Indicates Message Oriented Signaling (MOS) type data link message is received
6	TxSOT	RUR/ WC	0	**Transmit HDLC1 Controller Start of Transmission (TxSOT) Interrupt Status** This Reset-Upon-Read bit indicates whether or not the "Transmit HDLC1 Controller Start of Transmission (TxSOT) "Interrupt has occurred since the last read of this register. Transmit HDLC1 Controller will declare this interrupt when it has started to transmit a data link message. For sending large HDLC messages, start loading the next available buffer once this interrupt is detected. 0 = Transmit HDLC1 Controller Start of Transmission (TxSOT) interrupt has not occurred since the last read of this register 1 = Transmit HDLC1 Controller Start of Transmission interrupt (TxSOT) has occurred since the last read of this register.
5	RxSOT	RUR/ WC	0	**Receive HDLC1 Controller Start of Reception (RxSOT) Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receive HDLC1 Controller Start of Reception (RxSOT) interrupt has occurred since the last read of this register. Receive HDLC1 Controller will declare this interrupt when it has started to receive a data link message. 0 = Receive HDLC1 Controller Start of Reception (RxSOT) interrupt has not occurred since the last read of this register 1 = Receive HDLC1 Controller Start of Reception (RxSOT) interrupt has occurred since the last read of this register
4	TxEOT	RUR/ WC	0	**Transmit HDLC1 Controller End of Transmission (TxEOT) Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Transmit HDLC1 Controller End of Transmission (TxEOT) Interrupt has occurred since the last read of this register. Transmit HDLC1 Controller will declare this interrupt when it has completed its transmission of a data link message. For sending large HDLC messages, it is critical to load the next available buffer before this interrupt occurs. 0 = Transmit HDLC1 Controller End of Transmission (TxEOT) interrupt has not occurred since the last read of this register 1 = Transmit HDLC1 Controller End of Transmission (TxEOT) interrupt has occurred since the last read of this register

TABLE 86: DATA LINK STATUS REGISTER 1 (DLSR1) HEX ADDRESS: 0xnB06

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	RxEOT	RUR/ WC	0	**Receive HDLC1 Controller End of Reception (RxEOT) Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receive HDLC1 Controller End of Reception (RxEOT) Interrupt has occurred since the last read of this register. Receive HDLC1 Controller will declare this interrupt once it has completely received a full data link message, or once the buffer is full. 0 = Receive HDLC1 Controller End of Reception (RxEOT) interrupt has not occurred since the last read of this register 1 = Receive HDLC1 Controller End of Reception (RxEOT) Interrupt has occurred since the last read of this register
2	FCS Error	RUR/ WC	0	**FCS Error Interrupt Status** This Reset-Upon-Read bit indicates whether or not the FCS Error Interrupt has occurred since the last read of this register. Receive HDLC1 Controller will declare this interrupt when it has detected the FCS error in the most recently received data link message. 0 = FCS Error interrupt has not occurred since the last read of this register 1 = FCS Error interrupt has occurred since the last read of this register
1	Rx ABORT	RUR/ WC	0	**Receipt of Abort Sequence Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receipt of Abort Sequence interrupt has occurred since last read of this register. Receive HDLC1 Controller will declare this interrupt if it detects the Abort Sequence (i.e. a string of seven (7) consecutive 1's) in the incoming data link channel. 0 = Receipt of Abort Sequence interrupt has not occurred since last read of this register 1 = Receipt of Abort Sequence interrupt has occurred since last read of this register
0	RxIDLE	RUR/ WC	0	**Receipt of Idle Sequence Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receipt of Idle Sequence interrupt has occurred since the last read of this register. The Receive HDLC1 Controller will declare this interrupt if it detects the flag sequence octet (0x7E) in the incoming data link channel. If RxIDLE "AND" RxEOT occur together, then the entire HDLC message has been received. 0 = Receipt of Idle Sequence interrupt has not occurred since last read of this register 1 = Receipt of Idle Sequence interrupt has occurred since last read of this register.

TABLE 87: DATA LINK INTERRUPT ENABLE REGISTER 1 (DLIER1) **HEX ADDRESS: 0xnB07**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	-	-	**Reserved**
6	TxSOT ENB	R/W	0	**Transmit HDLC1 Controller Start of Transmission (TxSOT) Interrupt Enable** This bit enables or disables the “Transmit HDLC1 Controller Start of Transmission (TxSOT) “Interrupt within the XRT86VL38 device. Once this interrupt is enabled, the Transmit HDLC1 Controller will generate an interrupt when it has started to transmit a data link message. 0 = Disables the Transmit HDLC1 Controller Start of Transmission (TxSOT) interrupt. 1 = Enables the Transmit HDLC1 Controller Start of Transmission (TxSOT) interrupt.
5	RxSOT ENB	R/W	0	**Receive HDLC1 Controller Start of Reception (RxSOT) Interrupt Enable** This bit enables or disables the “Receive HDLC1 Controller Start of Reception (RxSOT) “Interrupt within the XRT86VL38 device. Once this interrupt is enabled, the Receive HDLC1 Controller will generate an interrupt when it has started to receive a data link message. 0 = Disables the Receive HDLC1 Controller Start of Reception (RxSOT) interrupt. 1 = Enables the Receive HDLC1 Controller Start of Reception (RxSOT) interrupt.
4	TxEOT ENB	R/W	0	**Transmit HDLC1 Controller End of Transmission (TxEOT) Interrupt Enable** This bit enables or disables the “Transmit HDLC1 Controller End of Transmission (TxEOT) “Interrupt within the XRT86VL38 device. Once this interrupt is enabled, the Transmit HDLC1 Controller will generate an interrupt when it has finished transmitting a data link message. 0 = Disables the Transmit HDLC1 Controller End of Transmission (TxEOT) interrupt. 1 = Enables the Transmit HDLC1 Controller End of Transmission (TxEOT) interrupt.
3	RxEOT ENB	R/W	0	**Receive HDLC1 Controller End of Reception (RxEOT) Interrupt Enable** This bit enables or disables the “Receive HDLC1 Controller End of Reception (RxEOT) “Interrupt within the XRT86VL38 device. Once this interrupt is enabled, the Receive HDLC1 Controller will generate an interrupt when it has finished receiving a complete data link message. 0 = Disables the Receive HDLC1 Controller End of Reception (RxEOT) interrupt. 1 = Enables the Receive HDLC1 Controller End of Reception (RxEOT) interrupt.

TABLE 87: DATA LINK INTERRUPT ENABLE REGISTER 1 (DLIER1) HEX ADDRESS: 0xnB07

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2	FCS ERR ENB	R/W	0	**FCS Error Interrupt Enable** This bit enables or disables the “Received FCS Error “Interrupt within the XRT86VL38 device. Once this interrupt is enabled, the Receive HDLC1 Controller will generate an interrupt when it has detected the FCS error within the incoming data link message. 0 = Disables the “Receive FCS Error” interrupt. 1 = Enables the “Receive FCS Error” interrupt.
1	RxABORT ENB	R/W	0	**Receipt of Abort Sequence Interrupt Enable** This bit enables or disables the “Receipt of Abort Sequence“ Interrupt within the XRT86VL38 device. Once this interrupt is enabled, the Receive HDLC1 Controller will generate an interrupt when it has detected the Abort Sequence (i.e. a string of seven (7) consecutive 1’s) within the incoming data link channel. 0 = Disables the “Receipt of Abort Sequence” interrupt. 1 = Enables the “Receipt of Abort Sequence” interrupt.
0	RxIDLE ENB	R/W	0	**Receipt of Idle Sequence Interrupt Enable** This bit enables or disables the “Receipt of Idle Sequence“ Interrupt within the XRT86VL38 device. Once this interrupt is enabled, the Receive HDLC1 Controller will generate an interrupt when it has detected the Idle Sequence Octet (i.e. 0x7E) within the incoming data link channel. 0 = Disables the “Receipt of Idle Sequence” interrupt. 1 = Enables the “Receipt of Idle Sequence” interrupt.

TABLE 88: SLIP BUFFER INTERRUPT STATUS REGISTER (SBISR) **HEX ADDRESS: 0xnB08**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxSB_FULL	RUR/ WC	0	**Transmit Slip buffer Full Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Transmit Slip Buffer Full interrupt has occurred since the last read of this register. The transmit Slip Buffer Full interrupt is declared when the transmit slip buffer is filled. If the transmit slip buffer is full and a WRITE operation occurs, then a full frame of data will be deleted, and this interrupt bit will be set to ‘1’. 0 = Indicates that the Transmit Slip Buffer Full interrupt has not occurred since the last read of this register. 1 = Indicates that the Transmit Slip Buffer Full interrupt has occurred since the last read of this register.
6	TxSB_EMPT	RUR/ WC	0	**Transmit Slip buffer Empty Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Transmit Slip Buffer Empty interrupt has occurred since the last read of this register. The transmit Slip Buffer Empty interrupt is declared when the transmit slip buffer is emptied. If the transmit slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and this interrupt bit will be set to ‘1’. 0 = Indicates that the Transmit Slip Buffer Empty interrupt has not occurred since the last read of this register. 1 = Indicates that the Transmit Slip Buffer Empty interrupt has occurred since the last read of this register.
5	TxSB_SLIP	RUR/ WC	0	**Transmit Slip Buffer Slips Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Transmit Slip Buffer Slips interrupt has occurred since the last read of this register. The transmit Slip Buffer Slips interrupt is declared when the transmit slip buffer is either filled or emptied. This interrupt bit will be set to ‘1’ in either one of these two conditions: **1.** If the transmit slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and this interrupt bit will be set to ‘1’. **2.** If the transmit slip buffer is full and a WRITE operation occurs, then a full frame of data will be deleted, and this interrupt bit will be set to ‘1’. 0 = Indicates that the Transmit Slip Buffer Slips interrupt has not occurred since the last read of this register. 1 = Indicates that the Transmit Slip Buffer Slips interrupt has occurred since the last read of this register. **NOTE:** *Users still need to read the Transmit Slip Buffer Empty Interrupt (bit 6 of this register) or the Transmit Slip Buffer Full Interrupts (bit 7 of this register) to determine whether transmit slip buffer empties or fills.*

TABLE 88: SLIP BUFFER INTERRUPT STATUS REGISTER (SBISR) HEX ADDRESS: 0xnB08

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
4	SLC®96 LOCK	RO	0	**SLC®96 is in SYNC** This READ ONLY bit field indicates whether or not frame synchronization is achieved when the XRT86VL38 is configured in SLC®96 framing mode. 0 = Indicates that frame synchronization is not achieved in SLC®96 framing mode. 1 = Indicates that frame synchronization is achieved in SLC®96 framing mode.
3	Multiframe LOCK	RO	0	**Multiframe is in SYNC** This READ ONLY bit field indicates whether or not the T1 Receive Framer Block is declaring T1 Multiframe LOCK status. 0 = Indicates that the T1 Receive Framer is currently declaring T1 multiframe LOSS OF LOCK status 0 = Indicates that the T1 Receive Framer is currently declaring T1 multiframe LOCK status
2	RxSB_FULL	RUR/ WC	0	**Receive Slip buffer Full Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receive Slip Buffer Full interrupt has occurred since the last read of this register. The Receive Slip Buffer Full interrupt is declared when the receive slip buffer is filled. If the receive slip buffer is full and a WRITE operation occurs, then a full frame of data will be deleted, and this interrupt bit will be set to ‘1’. 0 = Indicates that the Receive Slip Buffer Full interrupt has not occurred since the last read of this register. 1 = Indicates that the Receive Slip Buffer Full interrupt has occurred since the last read of this register.

TABLE 88: SLIP BUFFER INTERRUPT STATUS REGISTER (SBISR) **HEX ADDRESS: 0xnB08**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	RxSB_EMPT	RUR/ WC	0	**Receive Slip buffer Empty Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receive Slip Buffer Empty interrupt has occurred since the last read of this register. The Receive Slip Buffer Empty interrupt is declared when the receive slip buffer is emptied. If the receive slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and this interrupt bit will be set to ‘1’. 0 = Indicates that the Receive Slip Buffer Empty interrupt has not occurred since the last read of this register. 1 = Indicates that the Receive Slip Buffer Empty interrupt has occurred since the last read of this register.
0	RxSB_SLIP	RUR/ WC	0	**Receive Slip Buffer Slips Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receive Slip Buffer Slips interrupt has occurred since the last read of this register. The Receive Slip Buffer Slips interrupt is declared when the receive slip buffer is either filled or emptied. This interrupt bit will be set to ‘1’ in either one of these two conditions: **1.** If the receive slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and this interrupt bit will be set to ‘1’. **2.** If the receive slip buffer is full and a WRITE operation occurs, then a full frame of data will be deleted, and this interrupt bit will be set to ‘1’. 0 = Indicates that the Receive Slip Buffer Slips interrupt has not occurred since the last read of this register. 1 = Indicates that the Receive Slip Buffer Slips interrupt has occurred since the last read of this register. **NOTE:** *Users still need to read the Receive Slip Buffer Empty Interrupt (bit 1 of this register) or the Receive Slip Buffer Full Interrupts (bit 2 of this register) to determine whether transmit slip buffer empties or fills.*

TABLE 89: SLIP BUFFER INTERRUPT ENABLE REGISTER (SBIER) HEX ADDRESS: 0xnB09

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxFULL_ENB	R/W	0	**Transmit Slip Buffer Full Interrupt Enable** This bit enables or disables the Transmit Slip Buffer Full interrupt within the XRT86VL38 device. Once this interrupt is enabled, the transmit Slip Buffer Full interrupt is declared when the transmit slip buffer is filled. If the transmit slip buffer is full and a WRITE operation occurs, then a full frame of data will be deleted, and the interrupt status bit will be set to ‘1’. 0 - Disables the Transmit Slip Buffer Full interrupt when the Transmit Slip Buffer fills 1 - Enables the Transmit Slip Buffer Full interrupt when the Transmit Slip Buffer fills.
6	TxEMPT_ENB	R/W	0	**Transmit Slip Buffer Empty Interrupt Enable** This bit enables or disables the Transmit Slip Buffer Empty interrupt within the XRT86VL38 device. Once this interrupt is enabled, the transmit Slip Buffer Empty interrupt is declared when the transmit slip buffer is emptied. If the transmit slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and the interrupt status bit will be set to ‘1’. 0 - Disables the Transmit Slip Buffer Empty interrupt when the Transmit Slip Buffer empties 1 - Enables the Transmit Slip Buffer Empty interrupt when the Transmit Slip Buffer empties.
5	TxSLIP_ENB	R/W	0	**Transmit Slip Buffer Slips Interrupt Enable** This bit enables or disables the Transmit Slip Buffer Slips interrupt within the XRT86VL38 device. Once this interrupt is enabled, the transmit Slip Buffer Slips interrupt is declared when either the transmit slip buffer is filled or emptied. If the transmit slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and the interrupt status bit will be set to ‘1’. The interrupt status bit will be set to ‘1’ in either one of these two conditions: **1.** If the transmit slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and this interrupt bit will be set to ‘1’. **2.** If the transmit slip buffer is full and a WRITE operation occurs, then a full frame of data will be deleted, and this interrupt bit will be set to ‘1’. 0 - Disables the Transmit Slip Buffer Slips interrupt when the Transmit Slip Buffer empties or fills 1 - Enables the Transmit Slip Buffer Slips interrupt when the Transmit Slip Buffer empties or fills.
4-3	Reserved	-	-	**Reserved**

TABLE 89: SLIP BUFFER INTERRUPT ENABLE REGISTER (SBIER) **HEX ADDRESS: 0xnB09**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2	RxFULL_ENB	R/W	0	**Receive Slip Buffer Full Interrupt Enable** This bit enables or disables the Receive Slip Buffer Full interrupt within the XRT86VL38 device. Once this interrupt is enabled, the Receive Slip Buffer Full interrupt is declared when the receive slip buffer is filled. If the Receive slip buffer is full and a WRITE operation occurs, then a full frame of data will be deleted, and the interrupt status bit will be set to ‘1’. 0 - Disables the Receive Slip Buffer Full interrupt when the Transmit Slip Buffer fills 1 - Enables the Receive Slip Buffer Full interrupt when the Transmit Slip Buffer fills.
1	RxEMPT_ENB	R/W	0	**Receive Slip buffer Empty Interrupt Enable** This bit enables or disables the Receives Slip Buffer Empty interrupt within the XRT86VL38 device. Once this interrupt is enabled, the Receive Slip Buffer Empty interrupt is declared when the Receive slip buffer is emptied. If the Receive slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and the interrupt status bit will be set to ‘1’. 0 - Disables the Receive Slip Buffer Empty interrupt when the Transmit Slip Buffer empties 1 - Enables the Receive Slip Buffer Empty interrupt when the Transmit Slip Buffer empties.
0	RxSLIP_ENB	R/W	0	**Receive Slip buffer Slips Interrupt Enable** This bit enables or disables the Receive Slip Buffer Slips interrupt within the XRT86VL38 device. Once this interrupt is enabled, the Receive Slip Buffer Slips interrupt is declared when either the Receive slip buffer is filled or emptied. If the Receive slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and the interrupt status bit will be set to ‘1’. The interrupt status bit will be set to ‘1’ in either one of these two conditions: **1.** If the Receive slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and this interrupt bit will be set to ‘1’. **2.** If the Receive slip buffer is full and a WRITE operation occurs, then a full frame of data will be deleted, and this interrupt bit will be set to ‘1’. 0 - Disables the Receive Slip Buffer Slips interrupt when the Transmit Slip Buffer empties or fills 1 - Enables the Receive Slip Buffer Slips interrupt when the Transmit Slip Buffer empties or fills.

TABLE 90: RECEIVE LOOPBACK CODE INTERRUPT AND STATUS REGISTER (RLCISR) HEX ADDRESS: 0xnB0A

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-4	-	-	-	**Reserved (For E1 mode only)**
3	RXASTAT	RO	0	**Receive Loopback Activation Code State** This READ ONLY bit indicates whether or not the Receive T1 Framer Block is currently detecting the Receive Loopback Activation Code, as specified in the Receive Loopback Activation Code Register (RLACR - address 0xn126) if Receive Loopback Activation Code Detection is enabled. 0 = Indicates that the Receive T1 Framer Block is NOT currently detecting the Receive Loopback Activation Code. 1 = Indicates that the Receive T1 Framer Block is currently detecting the Receive Loopback Activation Code.
2	RXDSTAT	RO	0	**Receive Loopback Deactivation Code State** This READ ONLY bit indicates whether or not the Receive T1 Framer Block is currently detecting the Receive Loopback Deactivation Code, as specified in the Receive Loopback Deactivation Code Register (RLDCR - address 0xn127) if Receive Loopback Deactivation Code Detection is enabled. 0 = Indicates that the Receive T1 Framer Block is NOT currently detecting the Receive Loopback Deactivation Code. 1 = Indicates that the Receive T1 Framer Block is currently detecting the Receive Loopback Deactivation Code.
1	RXAINT	RUR/ WC	0	**Change in Receive Loopback Activation Code interrupt Status** This Reset-Upon-Read bit field indicates whether or not the “Change in Receive Loopback Activation Code” interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block detects the Receive Loopback Activation Code. **2.** Whenever the Receive T1 Framer block no longer detects the Receive Loopback Activation Code. 0 = Indicates that the “Change in Receive Loopback Activation Code” interrupt has not occurred since the last read of this register 1 = Indicates that the “Change in Receive Loopback Activation Code” interrupt has occurred since the last read of this register
0	RXDINT	RUR/ WC	0	**Change in Receive Loopback Deactivation Code interrupt Status** This Reset-Upon-Read bit field indicates whether or not the “Change in Receive Loopback Deactivation Code” interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block detects the Receive Loopback Deactivation Code. **2.** Whenever the Receive T1 Framer block no longer detects the Receive Loopback Deactivation Code. 0 = Indicates that the “Change in Receive Loopback Deactivation Code” interrupt has not occurred since the last read of this register 1 = Indicates that the “Change in Receive Loopback Deactivation Code” interrupt has occurred since the last read of this register

TABLE 91: RECEIVE LOOPBACK CODE INTERRUPT ENABLE REGISTER (RLCIER) HEX ADDRESS: 0xnB0B

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-2	Reserved	-	-	**Reserved**
1	RXAENB	R/W	0	**Receive Loopback Activation Code Interrupt Enable** This bit enables or disables the "Change in Receive Loopback Activation Code" interrupt within the T1 Receive Framer. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block detects the Receive Loopback Activation Code. **2.** Whenever the Receive T1 Framer block no longer detects the Receive Loopback Activation Code. 0 - Disables the "Change in Receive Loopback Activation Code" interrupt within the T1 Receive Framer. 1 - Enables the "Change in Receive Loopback Activation Code" interrupt within the T1 Receive Framer.
0	RXDENB	R/W	0	**Receive Loopback Deactivation Code Interrupt Enable** This bit enables or disables the "Change in Receive Loopback Deactivation Code" interrupt within the T1 Receive Framer. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block detects the Receive Loopback Deactivation Code. **2.** Whenever the Receive T1 Framer block no longer detects the Receive Loopback Deactivation Code. 0 - Disables the "Change in Receive Loopback Deactivation Code" interrupt within the T1 Receive Framer. 1 - Enables the "Change in Receive Loopback Deactivation Code" interrupt within the T1 Receive Framer.

TABLE 92: EXCESSIVE ZERO STATUS REGISTER (EXZSR) HEX ADDRESS: 0xnB0E

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-1	Reserved	-	-	**Reserved**
0	EXZ_STATUS	RUR/ WC	0	**Change in Excessive Zero Condition Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Change in Excessive Zero Condition" interrupt within the T1 Receive Framer Block has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block detects the Excessive Zero Condition. **2.** Whenever the Receive T1 Framer block clears the Excessive Zero Condition 0 = Indicates the "Change in Excessive Zero Condition" interrupt has NOT occurred since the last read of this register 1 = Indicates the "Change in Excessive Zero Condition" interrupt has occurred since the last read of this register

TABLE 93: EXCESSIVE ZERO ENABLE REGISTER (EXZER) HEX ADDRESS: 0xnB0F

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-1	-	-	-	**Reserved**
0	EXZ_ENB	R/W	0	**Change in Excessive Zero Condition Interrupt Enable** This bit enables or disables the "Change in Excessive Zero Condition" interrupt within the T1 Receive Framer. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block detects the Excessive Zero Condition. **2.** Whenever the Receive T1 Framer block clears the Excessive Zero Condition 0 - Disables the "Change in Excessive Zero Condition" interrupt within the Receive T1 Framer Block 1 - Enables the "Change in Excessive Zero Condition" interrupt within the Receive T1 Framer Block

TABLE 94: SS7 STATUS REGISTER FOR LAPD1 (SS7SR1) HEX ADDRESS: 0xnB10

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
0	SS7_1_STATUS	RUR/ WC	0	**SS7 Interrupt Status for LAPD Controller 1** This Reset-Upon-Read bit field indicates whether or not the “SS7” interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt when the Received LAPD message is more than 276 Bytes in length. 0 = Indicates that the “SS7” interrupt has not occurred since the last read of this register 1 = Indicates that the “SS7” interrupt has occurred since the last read of this register

TABLE 95: SS7 ENABLE REGISTER FOR LAPD1 (SS7ER1) HEX ADDRESS: 0xnB11

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
0	SS7_1_ENB	R/W	0	**SS7 Interrupt Enable for LAPD Controller 1** This bit enables or disables the “SS7” interrupt within the LAPD Controller 1. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt when the Received LAPD message is more than 276 Bytes in length. 0 - Disables the “SS7” interrupt within the LAPD Controller 1. 1 - Enables the “SS7” interrupt within the LAPD Controller 1.

TABLE 96: RXLOS/CRC INTERRUPT STATUS REGISTER (RLCISR) **HEX ADDRESS: 0XNB12**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-4	-	-	-	Reserved
3	RxLOSINT	RUR/ WC	0	**Change in Receive LOS condition Interrupt Status** This bit indicates whether or not the “Change in Receive LOS condition” interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block declares the Receive LOS condition. **2.** Whenever the Receive T1 Framer block clears the Receive LOS condition. 0 = Indicates that the “Change in Receive LOS Condition” interrupt has not occurred since the last read of this register. 1 = Indicates that the “Change in Receive LOS Condition” interrupt has occurred since the last read of this register.
2-0	Reserved	-	-	

TABLE 97: RXLOS/CRC INTERRUPT ENABLE REGISTER (RLCIER) **HEX ADDRESS: 0XNB13**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	RxLOS_ENB	R/W	0	**Change in Receive LOS Condition Interrupt Enable** This bit enables the “Change in Receive LOS Condition” interrupt. 0 = Enables “Change in Receive LOS Condition” Interrupt. 1 = Disables “Change in Receive LOS Condition” Interrupt.
2-0	-	-	-	Reserved

TABLE 98: DATA LINK STATUS REGISTER 2 (DLSR2) **HEX ADDRESS: 0xnB16**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	MSG TYPE	RO	0	**HDLC2 Message Type Identifier** This READ ONLY bit indicates the type of data link message received by Receive HDLC 2 Controller. Two types of data link messages are supported within the XRT86VL38 device: Message Oriented Signaling (MOS) or Bit-Oriented Signalling (BOS). 0 = Indicates Bit-Oriented Signaling (BOS) type data link message is received 1 = Indicates Message Oriented Signaling (MOS) type data link message is received
6	TxSOT	RUR/ WC	0	**Transmit HDLC2 Controller Start of Transmission (TxSOT) Interrupt Status** This Reset-Upon-Read bit indicates whether or not the “Transmit HDLC2 Controller Start of Transmission (TxSOT) “Interrupt has occurred since the last read of this register. Transmit HDLC2 Controller will declare this interrupt when it has started to transmit a data link message. For sending large HDLC messages, start loading the next available buffer once this interrupt is detected. 0 = Transmit HDLC2 Controller Start of Transmission (TxSOT) interrupt has not occurred since the last read of this register 1 = Transmit HDLC2 Controller Start of Transmission interrupt (TxSOT) has occurred since the last read of this register.
5	RxSOT	RUR/ WC	0	**Receive HDLC2 Controller Start of Reception (RxSOT) Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receive HDLC2 Controller Start of Reception (RxSOT) interrupt has occurred since the last read of this register. Receive HDLC2 Controller will declare this interrupt when it has started to receive a data link message. 0 = Receive HDLC2 Controller Start of Reception (RxSOT) interrupt has not occurred since the last read of this register 1 = Receive HDLC2 Controller Start of Reception (RxSOT) interrupt has occurred since the last read of this register
4	TxEOT	RUR/ WC	0	**Transmit HDLC2 Controller End of Transmission (TxEOT) Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Transmit HDLC2 Controller End of Transmission (TxEOT) Interrupt has occurred since the last read of this register. Transmit HDLC2 Controller will declare this interrupt when it has completed its transmission of a data link message. For sending large HDLC messages, it is critical to load the next available buffer before this interrupt occurs. 0 = Transmit HDLC2 Controller End of Transmission (TxEOT) interrupt has not occurred since the last read of this register 1 = Transmit HDLC2 Controller End of Transmission (TxEOT) interrupt has occurred since the last read of this register

TABLE 98: DATA LINK STATUS REGISTER 2 (DLSR2) HEX ADDRESS: 0xnB16

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	RxEOT	RUR/ WC	0	**Receive HDLC2 Controller End of Reception (RxEOT) Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receive HDLC2 Controller End of Reception (RxEOT) Interrupt has occurred since the last read of this register. Receive HDLC2 Controller will declare this interrupt once it has completely received a full data link message, or once the buffer is full. 0 = Receive HDLC2 Controller End of Reception (RxEOT) interrupt has not occurred since the last read of this register 1 = Receive HDLC2 Controller End of Reception (RxEOT) Interrupt has occurred since the last read of this register
2	FCS Error	RUR/ WC	0	**FCS Error Interrupt Status** This Reset-Upon-Read bit indicates whether or not the FCS Error Interrupt has occurred since the last read of this register. Receive HDLC2 Controller will declare this interrupt when it has detected the FCS error in the most recently received data link message. 0 = FCS Error interrupt has not occurred since the last read of this register 1 = FCS Error interrupt has occurred since the last read of this register
1	Rx ABORT	RUR/ WC	0	**Receipt of Abort Sequence Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receipt of Abort Sequence interrupt has occurred since last read of this register. Receive HDLC2 Controller will declare this interrupt if it detects the Abort Sequence (i.e. a string of seven (7) consecutive 1's) in the incoming data link channel. 0 = Receipt of Abort Sequence interrupt has not occurred since last read of this register 1 = Receipt of Abort Sequence interrupt has occurred since last read of this register
0	RxIDLE	RUR/ WC	0	**Receipt of Idle Sequence Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receipt of Idle Sequence interrupt has occurred since the last read of this register. The Receive HDLC2 Controller will declare this interrupt if it detects the flag sequence octet (0x7E) in the incoming data link channel. If RxIDLE "AND" RxEOT occur together, then the entire HDLC message has been received. 0 = Receipt of Idle Sequence interrupt has not occurred since last read of this register 1 = Receipt of Idle Sequence interrupt has occurred since last read of this register.

TABLE 99: DATA LINK INTERRUPT ENABLE REGISTER 2 (DLIER2) **HEX ADDRESS: 0xnB17**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	-	-	Reserved
6	TxSOT ENB	R/W	0	**Transmit HDLC2 Controller Start of Transmission (TxSOT) Interrupt Enable** This bit enables or disables the “Transmit HDLC2 Controller Start of Transmission (TxSOT) “Interrupt within the XRT86VL38 device. Once this interrupt is enabled, the Transmit HDLC2 Controller will generate an interrupt when it has started to transmit a data link message. 0 = Disables the Transmit HDLC2 Controller Start of Transmission (TxSOT) interrupt. 1 = Enables the Transmit HDLC2 Controller Start of Transmission (TxSOT) interrupt.
5	RxSOT ENB	R/W	0	**Receive HDLC2 Controller Start of Reception (RxSOT) Interrupt Enable** This bit enables or disables the “Receive HDLC2 Controller Start of Reception (RxSOT) “Interrupt within the XRT86VL38 device. Once this interrupt is enabled, the Receive HDLC2 Controller will generate an interrupt when it has started to receive a data link message. 0 = Disables the Receive HDLC2 Controller Start of Reception (RxSOT) interrupt. 1 = Enables the Receive HDLC2 Controller Start of Reception (RxSOT) interrupt.
4	TxEOT ENB	R/W	0	**Transmit HDLC2 Controller End of Transmission (TxEOT) Interrupt Enable** This bit enables or disables the “Transmit HDLC2 Controller End of Transmission (TxEOT) “Interrupt within the XRT86VL38 device. Once this interrupt is enabled, the Transmit HDLC2 Controller will generate an interrupt when it has finished transmitting a data link message. 0 = Disables the Transmit HDLC2 Controller End of Transmission (TxEOT) interrupt. 1 = Enables the Transmit HDLC2 Controller End of Transmission (TxEOT) interrupt.
3	RxEOT ENB	R/W	0	**Receive HDLC2 Controller End of Reception (RxEOT) Interrupt Enable** This bit enables or disables the “Receive HDLC2 Controller End of Reception (RxEOT) “Interrupt within the XRT86VL38 device. Once this interrupt is enabled, the Receive HDLC2 Controller will generate an interrupt when it has finished receiving a complete data link message. 0 = Disables the Receive HDLC2 Controller End of Reception (RxEOT) interrupt. 1 = Enables the Receive HDLC2 Controller End of Reception (RxEOT) interrupt.

TABLE 99: DATA LINK INTERRUPT ENABLE REGISTER 2 (DLIER2) HEX ADDRESS: 0xnB17

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2	FCS ERR ENB	R/W	0	**FCS Error Interrupt Enable** This bit enables or disables the “Received FCS Error “Interrupt within the XRT86VL38 device. Once this interrupt is enabled, the Receive HDLC2 Controller will generate an interrupt when it has detected the FCS error within the incoming data link message. 0 = Disables the “Receive FCS Error” interrupt. 1 = Enables the “Receive FCS Error” interrupt.
1	RxABORT ENB	R/W	0	**Receipt of Abort Sequence Interrupt Enable** This bit enables or disables the “Receipt of Abort Sequence“Interrupt within the XRT86VL38 device. Once this interrupt is enabled, the Receive HDLC2 Controller will generate an interrupt when it has detected the Abort Sequence (i.e. a string of seven (7) consecutive 1’s) within the incoming data link channel. 0 = Disables the “Receipt of Abort Sequence” interrupt. 1 = Enables the “Receipt of Abort Sequence” interrupt.
0	RxIDLE ENB	R/W	0	**Receipt of Idle Sequence Interrupt Enable** This bit enables or disables the “Receipt of Idle Sequence“Interrupt within the XRT86VL38 device. Once this interrupt is enabled, the Receive HDLC2 Controller will generate an interrupt when it has detected the Idle Sequence Octet (i.e. 0x7E) within the incoming data link channel. 0 = Disables the “Receipt of Idle Sequence” interrupt. 1 = Enables the “Receipt of Idle Sequence” interrupt.

TABLE 100: SS7 STATUS REGISTER FOR LAPD2 (SS7SR2) HEX ADDRESS: 0XnB18

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
0	SS7_2_STATUS	RUR/ WC	0	**SS7 Interrupt Status for LAPD Controller 2** This Reset-Upon-Read bit field indicates whether or not the “SS7” interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt when the Received LAPD message is more than 276 Bytes in length. 0 = Indicates that the “SS7” interrupt has not occurred since the last read of this register 1 = Indicates that the “SS7” interrupt has occurred since the last read of this register

TABLE 101: SS7 ENABLE REGISTER FOR LAPD2 (SS7ER2) HEX ADDRESS: 0XnB19

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
0	SS7_2_ENB	R/W	0	**SS7 Interrupt Enable for LAPD Controller 2** This bit enables or disables the “SS7” interrupt within the LAPD Controller 2. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt when the Received LAPD message is more than 276 Bytes in length. 0 - Disables the “SS7” interrupt within the LAPD Controller 2. 1 - Enables the “SS7” interrupt within the LAPD Controller 2.

TABLE 102: DATA LINK STATUS REGISTER 3 (DLSR3) **HEX ADDRESS: 0XNB26**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	MSG TYPE	RUR/ WC	0	**HDLC3 Message Type Identifier** This READ ONLY bit indicates the type of data link message received by Receive HDLC 3 Controller. Two types of data link messages are supported within the XRT86VL38 device: Message Oriented Signaling (MOS) or Bit-Oriented Signalling (BOS). 0 = Indicates Bit-Oriented Signaling (BOS) type data link message is received 1 = Indicates Message Oriented Signaling (MOS) type data link message is received
6	TxSOT	RUR/ WC	0	**Transmit HDLC3 Controller Start of Transmission (TxSOT) Interrupt Status** This Reset-Upon-Read bit indicates whether or not the “Transmit HDLC3 Controller Start of Transmission (TxSOT) “Interrupt has occurred since the last read of this register. Transmit HDLC3 Controller will declare this interrupt when it has started to transmit a data link message. For sending large HDLC messages, start loading the next available buffer once this interrupt is detected. 0 = Transmit HDLC3 Controller Start of Transmission (TxSOT) interrupt has not occurred since the last read of this register 1 = Transmit HDLC3 Controller Start of Transmission interrupt (TxSOT) has occurred since the last read of this register.
5	RxSOT	RUR/ WC	0	**Receive HDLC3 Controller Start of Reception (RxSOT) Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receive HDLC3 Controller Start of Reception (RxSOT) interrupt has occurred since the last read of this register. Receive HDLC3 Controller will declare this interrupt when it has started to receive a data link message. 0 = Receive HDLC3 Controller Start of Reception (RxSOT) interrupt has not occurred since the last read of this register 1 = Receive HDLC3 Controller Start of Reception (RxSOT) interrupt has occurred since the last read of this register
4	TxEOT	RUR/ WC	0	**Transmit HDLC3 Controller End of Transmission (TxEOT) Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Transmit HDLC3 Controller End of Transmission (TxEOT) Interrupt has occurred since the last read of this register. Transmit HDLC3 Controller will declare this interrupt when it has completed its transmission of a data link message. For sending large HDLC messages, it is critical to load the next available buffer before this interrupt occurs. 0 = Transmit HDLC3 Controller End of Transmission (TxEOT) interrupt has not occurred since the last read of this register 1 = Transmit HDLC3 Controller End of Transmission (TxEOT) interrupt has occurred since the last read of this register

TABLE 102: DATA LINK STATUS REGISTER 3 (DLSR3) **HEX ADDRESS: 0xnB26**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	RxEOT	RUR/ WC	0	**Receive HDLC3 Controller End of Reception (RxEOT) Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receive HDLC3 Controller End of Reception (RxEOT) Interrupt has occurred since the last read of this register. Receive HDLC3 Controller will declare this interrupt once it has completely received a full data link message, or once the buffer is full. 0 = Receive HDLC3 Controller End of Reception (RxEOT) interrupt has not occurred since the last read of this register 1 = Receive HDLC3 Controller End of Reception (RxEOT) Interrupt has occurred since the last read of this register
2	FCS Error	RUR/ WC	0	**FCS Error Interrupt Status** This Reset-Upon-Read bit indicates whether or not the FCS Error Interrupt has occurred since the last read of this register. Receive HDLC3 Controller will declare this interrupt when it has detected the FCS error in the most recently received data link message. 0 = FCS Error interrupt has not occurred since the last read of this register 1 = FCS Error interrupt has occurred since the last read of this register
1	Rx ABORT	RUR/ WC	0	**Receipt of Abort Sequence Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receipt of Abort Sequence interrupt has occurred since last read of this register. Receive HDLC3 Controller will declare this interrupt if it detects the Abort Sequence (i.e. a string of seven (7) consecutive 1's) in the incoming data link channel. 0 = Receipt of Abort Sequence interrupt has not occurred since last read of this register 1 = Receipt of Abort Sequence interrupt has occurred since last read of this register
0	RxIDLE	RUR/ WC	0	**Receipt of Idle Sequence Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receipt of Idle Sequence interrupt has occurred since the last read of this register. The Receive HDLC3 Controller will declare this interrupt if it detects the flag sequence octet (0x7E) in the incoming data link channel. If RxIDLE "AND" RxEOT occur together, then the entire HDLC message has been received. 0 = Receipt of Idle Sequence interrupt has not occurred since last read of this register 1 = Receipt of Idle Sequence interrupt has occurred since last read of this register.

TABLE 103: DATA LINK INTERRUPT ENABLE REGISTER 3 (DLIER3) HEX ADDRESS: 0xnB27

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	-	-	**Reserved**
6	TxSOT ENB	R/W	0	**Transmit HDLC3 Controller Start of Transmission (TxSOT) Interrupt Enable** This bit enables or disables the "Transmit HDLC3 Controller Start of Transmission (TxSOT) "Interrupt within the XRT86VL38 device. Once this interrupt is enabled, the Transmit HDLC3 Controller will generate an interrupt when it has started to transmit a data link message. 0 = Disables the Transmit HDLC3 Controller Start of Transmission (TxSOT) interrupt. 1 = Enables the Transmit HDLC3 Controller Start of Transmission (TxSOT) interrupt.
5	RxSOT ENB	R/W	0	**Receive HDLC3 Controller Start of Reception (RxSOT) Interrupt Enable** This bit enables or disables the "Receive HDLC3 Controller Start of Reception (RxSOT) "Interrupt within the XRT86VL38 device. Once this interrupt is enabled, the Receive HDLC3 Controller will generate an interrupt when it has started to receive a data link message. 0 = Disables the Receive HDLC3 Controller Start of Reception (RxSOT) interrupt. 1 = Enables the Receive HDLC3 Controller Start of Reception (RxSOT) interrupt.
4	TxEOT ENB	R/W	0	**Transmit HDLC3 Controller End of Transmission (TxEOT) Interrupt Enable** This bit enables or disables the "Transmit HDLC3 Controller End of Transmission (TxEOT) "Interrupt within the XRT86VL38 device. Once this interrupt is enabled, the Transmit HDLC3 Controller will generate an interrupt when it has finished transmitting a data link message. 0 = Disables the Transmit HDLC3 Controller End of Transmission (TxEOT) interrupt. 1 = Enables the Transmit HDLC3 Controller End of Transmission (TxEOT) interrupt.
3	RxEOT ENB	R/W	0	**Receive HDLC3 Controller End of Reception (RxEOT) Interrupt Enable** This bit enables or disables the "Receive HDLC3 Controller End of Reception (RxEOT) "Interrupt within the XRT86VL38 device. Once this interrupt is enabled, the Receive HDLC3 Controller will generate an interrupt when it has finished receiving a complete data link message. 0 = Disables the Receive HDLC3 Controller End of Reception (RxEOT) interrupt. 1 = Enables the Receive HDLC3 Controller End of Reception (RxEOT) interrupt.

TABLE 103: DATA LINK INTERRUPT ENABLE REGISTER 3 (DLIER3) HEX ADDRESS: 0xnB27

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2	FCS ERR ENB	R/W	0	**FCS Error Interrupt Enable** This bit enables or disables the “Received FCS Error “Interrupt within the XRT86VL38 device. Once this interrupt is enabled, the Receive HDLC3 Controller will generate an interrupt when it has detected the FCS error within the incoming data link message. 0 = Disables the “Receive FCS Error” interrupt. 1 = Enables the “Receive FCS Error” interrupt.
1	RxABORT ENB	R/W	0	**Receipt of Abort Sequence Interrupt Enable** This bit enables or disables the “Receipt of Abort Sequence“ Interrupt within the XRT86VL38 device. Once this interrupt is enabled, the Receive HDLC3 Controller will generate an interrupt when it has detected the Abort Sequence (i.e. a string of seven (7) consecutive 1’s) within the incoming data link channel. 0 = Disables the “Receipt of Abort Sequence” interrupt. 1 = Enables the “Receipt of Abort Sequence” interrupt.
0	RxIDLE ENB	R/W	0	**Receipt of Idle Sequence Interrupt Enable** This bit enables or disables the “Receipt of Idle Sequence“ Interrupt within the XRT86VL38 device. Once this interrupt is enabled, the Receive HDLC3 Controller will generate an interrupt when it has detected the Idle Sequence Octet (i.e. 0x7E) within the incoming data link channel. 0 = Disables the “Receipt of Idle Sequence” interrupt. 1 = Enables the “Receipt of Idle Sequence” interrupt.

TABLE 104: SS7 STATUS REGISTER FOR LAPD3 (SS7SR3) **HEX ADDRESS: 0xnB28**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
0	SS7_3_STATUS	RUR/ WC	0	**SS7 Interrupt Status for LAPD Controller 3** This Reset-Upon-Read bit field indicates whether or not the “SS7” interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt when the Received LAPD message is more than 276 Bytes in length. 0 = Indicates that the “SS7” interrupt has not occurred since the last read of this register 1 = Indicates that the “SS7” interrupt has occurred since the last read of this register

TABLE 105: SS7 ENABLE REGISTER FOR LAPD3 (SS7ER3) **HEX ADDRESS: 0xnB29**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
0	SS7_3_ENB	R/W	0	**SS7 Interrupt Enable for LAPD Controller 3** This bit enables or disables the “SS7” interrupt within the LAPD Controller 3. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt when the Received LAPD message is more than 276 Bytes in length. 0 - Disables the “SS7” interrupt within the LAPD Controller 3. 1 - Enables the “SS7” interrupt within the LAPD Controller 3.

TABLE 106: CUSTOMER INSTALLATION ALARM STATUS REGISTER (CIASR) **HEX ADDRESS: 0xnB40**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
[7:6]	Reserved	-	-	**Reserved**
5	RxAIS-CI_state	RO	0	**Receive Alarm Indication Signal-Customer Installation (AIS-CI) State** This READ ONLY bit field indicates whether or not the Receive T1 Framer is currently detecting the Alarm Indication Signal-Customer Installation (AIS-CI) condition. Alarm Indication Signal-Customer Installation (AIS-CI) is intended for use in a network to differentiate between an issue within the network or the Customer Installation (CI). AIS-CI is an all ones signal with an embedded signature of 01111100 11111111 (right-to left) which recurs at 386 bit intervals in-the DS-1 signal. 0 = Indicates the Receive T1 Framer is currently NOT detecting the AIS-CI condition 1 = Indicates the Receive T1 Framer is currently detecting the AIS-CI condition **NOTE:** *This bit only works if AIS-CI detection is enabled (Register 0xn11C)*
4	RxRAI-CI_state	RO	0	**Rx RAI-CI State** This READ ONLY bit field indicates whether or not the Receive T1 Framer is currently declaring the Remote Alarm Indication - Customer Installation (RAI-CI) condition. (This is for T1 ESF framing mode only) Remote Alarm Indication - Customer Installation (RAI-CI) is intended for use in a network to differentiate between an issue within the network or the Customer Installation (CI). RAI-CI is a repetitive pattern with a period of 1.08 seconds. It is comprised of 0.99 seconds of RAI message (00000000 11111111 Right-to-left) and a 90 ms of RAI-CI signature (00111110 11111111 Right to left) to form a RAI-CI signal. 0 = Indicates the Receive T1 Framer is currently NOT detecting the RAI-CI condition 1 = Indicates the Receive T1 Framer is currently detecting the RAI-CI condition **NOTE:** *This bit only works if RAI-CI detection is enabled (Register 0xn11C)*
[3:2]	Reserved	-	-	**Reserved**

TABLE 106: CUSTOMER INSTALLATION ALARM STATUS REGISTER (CIASR) **HEX ADDRESS: 0xnB40**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	RxAIS-CI	RUR/ WC	0	**Change in Receive AIS-CI Condition Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the “Change in AIS-CI Condition” interrupt within the T1 Receive Framer Block has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block detects the AIS-CI Condition. **2.** Whenever the Receive T1 Framer block clears the AIS-CI Condition 0 = Indicates the “Change in AIS-CI Condition” interrupt has NOT occurred since the last read of this register 1 = Indicates the “Change in AIS-CI Condition” interrupt has occurred since the last read of this register
0	RxRAI-CI	RUR/ WC	0	**Change in Receive RAI-CI Condition Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the “Change in RAI-CI Condition” interrupt within the T1 Receive Framer Block has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block detects the RAI-CI Condition. **2.** Whenever the Receive T1 Framer block clears the RAI-CI Condition 0 = Indicates the “Change in RAI-CI Condition” interrupt has NOT occurred since the last read of this register 1 = Indicates the “Change in RAI-CI Condition” interrupt has occurred since the last read of this register

TABLE 107: CUSTOMER INSTALLATION ALARM STATUS REGISTER (CIAIER) **HEX ADDRESS: 0xnB41**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	RxAIS-CI_ENB	R/W	0	**Change in Receive AIS-CI Condition Interrupt Enable** This bit enables or disables the “Change in AIS-CI Condition” interrupt within the T1 Receive Framer Block. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block detects the AIS-CI Condition. **2.** Whenever the Receive T1 Framer block clears the AIS-CI Condition 0 - Disables the “Change in AIS-CI Condition” interrupt. 1 - Enables the “Change in AIS-CI Condition” interrupt.
0	RxRAI-CI_ENB	R/W	0	**Change in Receive RAI-CI Condition Interrupt Enable** This bit enables or disables the “Change in RAI-CI Condition” interrupt within the T1 Receive Framer Block. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block detects the RAI-CI Condition. **2.** Whenever the Receive T1 Framer block clears the AIS-CI Condition 0 - Disables the “Change in RAI-CI Condition” interrupt. 1 - Enables the “Change in RAI-CI Condition” interrupt.

2.0 LINE INTERFACE UNIT (LIU SECTION) REGISTERS

TABLE 108: LIU CHANNEL CONTROL REGISTER 0 (LIUCCR0) **HEX ADDRESS: 0X0FN0**

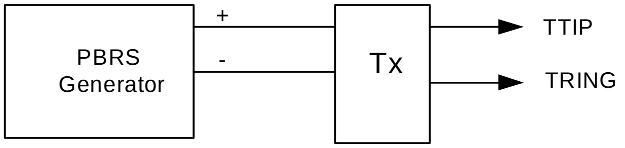
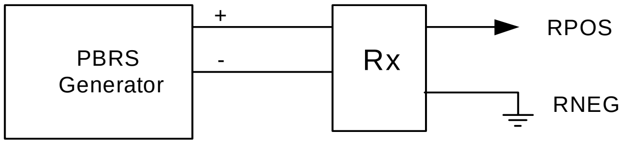
BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	QRSS_n/ PRBS_n	R/W	0	**QRSS/PRBS Select Bits** These bits are used to select between QRSS and PRBS. 0 = PRBS_n (2^{15} - 1) 1 = QRSS_n (2^{20} - 1)
6	PRBS_Rx_n/ PRBS_$\overline{\text{Tx}}$_n	R/W	0	**PRBS Receive/Transmit Select:** This bit is used select where the output of the PRBS Generator is directed. 0 = PRBS Generator is output on TTIP and TRING 1 = PRBS Generator is output on RPOS and RCLK Bit 6 = "0"  Bit 6 = "1" 
5	RXON_n	R/W	0	**Receiver ON:** This bit permits the user to either turn on or turn off the Receive Section of XRT86VL38. If the user turns on the Receive Section, then XRT86VL38 will begin to receive the incoming data-stream via the RTIP and RRING input pins. Conversely, if the user turns off the Receive Section, then the entire Receive Section except the MCLKIN Phase Locked Loop (PLL) will be powered down. 0 = Shuts off the Receive Section of XRT86VL38. 1 = Turns on the Receive Section of XRT86VL38.
4-0	EQC[4:0]	R/W	00000	**Equalizer Control [4:0]:** These bits are used to control the transmit pulse shaping, transmit line build-out (LBO) and receive sensitivity level. The Transmit Pulse Shape can be controlled by adjusting the Transmit Line Build-Out Settings for different cable length in T1 mode. Transmit pulse shape can also be controlled by using the Arbitrary mode, where users can specify the amplitude of the pulse shape by using the 8 Arbitrary Pulse Segments provided in the LIU registers (0x0Fn8-0xnFnF), where n is the channel number. The XRT86VL38 device supports both long haul and short haul applications which can also be selected using the EQC[4:0] bits. Table 109.presents the corresponding Transmit Line Build Out and Receive Sensitivity settings using different combinations of these five EQC[4:0] bits.

TABLE 109: EQUALIZER CONTROL AND TRANSMIT LINE BUILD OUT

EQC[4:0]	T1 MODE/RECEIVE SENSITIVITY	TRANSMIT LBO	CABLE
0x00h	T1 Long Haul/36dB	0dB	100Ω TP
0x01h	T1 Long Haul/36dB	-7.5dB	100Ω TP
0x02h	T1 Long Haul/36dB	-15dB	100Ω TP
0x03h	T1 Long Haul/36dB	-22.5dB	100Ω TP
0x04h	T1 Long Haul/45dB	0dB	100Ω TP
0x05h	T1 Long Haul/45dB	-7.5dB	100Ω TP
0x06h	T1 Long Haul/45dB	-15dB	100Ω TP
0x07h	T1 Long Haul/45dB	-22.5dB	100Ω TP
0x08h	T1 Short Haul/15dB	0 to 133 feet (0.6dB)	100Ω TP
0x09h	T1 Short Haul/15dB	133 to 266 feet (1.2dB)	100Ω TP
0x0Ah	T1 Short Haul/15dB	266 to 399 feet (1.8dB)	100Ω TP
0x0Bh	T1 Short Haul/15dB	399 to 533 feet (2.4dB)	100Ω TP
0x0Ch	T1 Short Haul/15dB	533 to 655 feet (3.0dB)	100Ω TP
0x0Dh	T1 Short Haul/15dB	Arbitrary Pulse	100Ω TP
0x0Eh	T1 Gain Mode/29dB	0 to 133 feet (0.6dB)	100Ω TP
0x0Fh	T1 Gain Mode/29dB	133 to 266 feet (1.2dB)	100Ω TP
0x10h	T1 Gain Mode/29dB	266 to 399 feet (1.8dB)	100Ω TP
0x11h	T1 Gain Mode/29dB	399 to 533 feet (2.4dB)	100Ω TP
0x12h	T1 Gain Mode/29dB	533 to 655 feet (3.0dB)	100Ω TP
0x13h	T1 Gain Mode/29dB	Arbitrary Pulse	100Ω TP
0x14h	T1 Gain Mode/29dB	0dB	100Ω TP
0x15h	T1 Gain Mode/29dB	-7.5dB	100Ω TP
0x16h	T1 Gain Mode/29dB	-15dB	100Ω TP
0x17h	T1 Gain Mode/29dB	-22.5dB	100Ω TP
0x18h	E1 Long Haul/36dB	ITU G.703	75Ω Coax
0x19h	E1 Long Haul/36dB	ITU G.703	120Ω TP
0x1Ah	E1 Long Haul/45dB	ITU G.703	75Ω Coax
0x1Bh	E1 Long Haul/45dB	ITU G.703	120Ω TP
0x1Ch	E1 Short Haul/15dB	ITU G.703	75Ω Coax
0x1Dh	E1 Short Haul/15dB	ITU G.703	120Ω TP
0x1Eh	E1 Gain Mode/29dB	ITU G.703	75Ω Coax
0x1Fh	E1 Gain Mode/29dB	ITU G.703	120Ω TP

TABLE 110: LIU CHANNEL CONTROL REGISTER 1 (LIUCCR1) **HEX ADDRESS: 0X0FN1**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>7</td><td>RXTSEL_n</td><td>R/W</td><td>0</td><td>Receiver Termination Select:
Upon power up, the receivers are in “High” impedance. The LIU provides an option for user to have either software or hardware control over receive termination. If RxTCNTL (bit 6 in Register 0x0FE2) is set to’0’, receive termination can be selected by programming this register bit. To switch control to the hardware pin (RxTSEL pin), RxTCNTL must be programmed to “1”. Once control has been granted to the hardware pin, RxTSEL must be pulled “High” to switch to internal termination.
If RxTCNTL is set to’0’, receive termination can be selected by setting this bit according to the following table:
<table>
<tr><th>RXTSEL</th><th>RX Termination</th></tr>
<tr><td>0</td><td>"High" Impedance</td></tr>
<tr><td>1</td><td>Internal</td></tr>
</table></td></tr>
<tr><td>6</td><td>TXTSEL_n</td><td>R/W</td><td>0</td><td>Transmit Termination Select:
This bit is used to select between internal termination or “High” impedance modes for the T1 transmitter according to the following table:
<table>
<tr><th>TXTSEL</th><th>TX Termination</th></tr>
<tr><td>0</td><td>"High" Impedance</td></tr>
<tr><td>1</td><td>Internal</td></tr>
</table></td></tr>
<tr><td>5-4</td><td>TERSEL[1:0]</td><td>R/W</td><td>00</td><td>Termination Impedance Select [1:0]:
These bits are used to control the transmit and receive termination impedance when the LIU block is configured in Internal Termination Mode.
In internal termination mode, (i.e., TXTSEL = “1” and RXTSEL = “1”), internal transmit and receive termination can be selected according to the following table:
<table>
<tr><th>TERSEL1</th><th>TERSEL0</th><th>Internal Transmit and Receive Termination</th></tr>
<tr><td>0</td><td>0</td><td>100Ω</td></tr>
<tr><td>0</td><td>1</td><td>110Ω</td></tr>
<tr><td>1</td><td>0</td><td>75Ω</td></tr>
<tr><td>1</td><td>1</td><td>120Ω</td></tr>
</table>
NOTE: <i>In the internal termination mode, the transmitter output should be AC coupled to the transformer.</i></td></tr>
</table>

TABLE 110: LIU CHANNEL CONTROL REGISTER 1 (LIUCCR1) **HEX ADDRESS: 0X0FN1**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>3</td><td>RxJASEL_n</td><td>R/W</td><td>0</td><td>Receive Jitter Attenuator Enable
This bit permits the user to enable or disable the Jitter Attenuator in the Receive Path within the XRT86VL38 device.
0 = Disables the Jitter Attenuator to operate in the Receive Path within the Receive T1 LIU Block.
1 = Enables the Jitter Attenuator to operate in the Receive Path within the Receive T1 LIU Block.</td></tr>
<tr><td>2</td><td>TxJASEL_n</td><td>R/W</td><td>0</td><td>Transmit Jitter Attenuator Enable
This bit permits the user to enable or disable the Jitter Attenuator in the Transmit Path within the XRT86VL38 device.
0 = Disables the Jitter Attenuator to operate in the Transmit Path within the Transmit T1 LIU Block.
1 = Enables the Jitter Attenuator to operate in the Transmit Path within the Transmit T1 LIU Block.</td></tr>
<tr><td>1</td><td>JABW_n</td><td>R/W</td><td>0</td><td>Jitter Attenuator Bandwidth Select:
In T1 mode, the Jitter Attenuator Bandwidth is always 3Hz, and this bit has no effect on the Jitter Attenuator Bandwidth. The FIFOS (bit D0 of this register) will be used to select the FIFO size, according to the table below.
<table>
<tr><th>Mode</th><th>JABW bit D1</th><th>FIFOS_n bit D0</th><th>JA B-W Hz</th><th>FIFO Size</th></tr>
<tr><td>T1</td><td>0</td><td>0</td><td>3</td><td>32</td></tr>
<tr><td>T1</td><td>0</td><td>1</td><td>3</td><td>64</td></tr>
<tr><td>T1</td><td>1</td><td>0</td><td>3</td><td>32</td></tr>
<tr><td>T1</td><td>1</td><td>1</td><td>3</td><td>64</td></tr>
<tr><td>E1</td><td>0</td><td>0</td><td>10</td><td>32</td></tr>
<tr><td>E1</td><td>0</td><td>1</td><td>10</td><td>64</td></tr>
<tr><td>E1</td><td>1</td><td>0</td><td>1.5</td><td>64</td></tr>
<tr><td>E1</td><td>1</td><td>1</td><td>1.5</td><td>64</td></tr>
</table></td></tr>
<tr><td>0</td><td>FIFOS_n</td><td>R/W</td><td>0</td><td>FIFO Size Select: See table of bit D1 above for the function of this bit.</td></tr>
</table>

TABLE 111: LIU CHANNEL CONTROL REGISTER 2 (LIUCCR2) HEX ADDRESS: 0X0FN2

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>7</td><td>INVQRSS_n</td><td>R/W</td><td>0</td><td>Invert QRSS Pattern:
This bit inverts the output PRBS/QRSS pattern if the LIU Block is configured to transmit a PRBS/QRSS pattern.
0 = Invert PRBS, NOT Invert QRSS
1 = NOT Invert PRBS, Invert QRSS</td></tr>
<tr><td>6-4</td><td>TXTEST[2:0]</td><td>R/W</td><td>000</td><td>Transmit Test Pattern [2:0]:
These bits are used to configure the Transmit T1 LIU Block to generate and transmit test patterns according to the following table. Use of these bits automatically places the LIU section in Single Rail mode. When this happens, the Framer section must be placed in Single Rail mode in Reg 0xn101.
<table>
<tr><th>TXTEST2</th><th>TXTEST1</th><th>TXTEST0</th><th>Test Pattern</th></tr>
<tr><td>0</td><td>X</td><td>X</td><td>No Pattern</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>TDQRSS</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>TAOS</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>TLUC</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>TLDC</td></tr>
</table>
TDQRSS (Transmit/Detect Quasi-Random Signal):
QRSS pattern is a 2^{20}-1 pseudo-random bit sequence (PRBS) with no more than 14 consecutive zeros.
TAOS (Transmit All Ones):
Whenever the user implements this configuration setting, the Transmit T1 LIU Block will ignore the data that it is accepting from the Transmit T1 Framer block (as well as the upstream system-side terminal equipment) and overwrite this data with the All Ones Pattern.
TLUC (Transmit Network Loop-Up Code):
The Transmit T1 LIU Block will generate and transmit the Network Loop-Up Code of “00001” to the line for the selected channel number n.
When Network Loop-Up code is being transmitted, the XRT86VL38 will ignore the “Automatic Loop-Code detection and Remote Loop-Back activation” (NLCDE1 =“1”, NLCDE0 =“1” of register 0x0Fn3) in order to avoid activating Remote Digital Loop-Back automatically when the remote terminal responds to the Loop-Back request.
TLDC (Transmit Network Loop-Down Code):
The Transmit T1 LIU Block will generate and transmit the Network Loop-Down Code of “001” to the line for the selected channel number n.</td></tr>
</table>

TABLE 111: LIU CHANNEL CONTROL REGISTER 2 (LIUCCR2) HEX ADDRESS: 0X0FN2

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	TXON_n	R/W	0	**Transmitter ON:** This bit permits the user to either turn on or turn off the Transmit Driver of XRT86VL38. If the user turns on the Transmit Driver, then XRT86VL38 will begin to transmit T1 data (on the line) via the TTIP and TRING output pins. Conversely, if the user turns off the Transmit Driver, then the TTIP and TRING output pins will be tri-stated. 0 = Shuts off the Transmit Driver associated with the XRT86VL38 device and tri-states the TTIP and TRING output pins. 1 = Turns on the Transmit Driver associated with the XRT86VL38 device. ***NOTE:*** *If the user wishes to exercise software control over the state of the Transmit Driver of the XRT86VL38, then it is imperative that the user pull the TxON pin to a logic "HIGH" level.*
2-0	LOOP2_n	R/W	000	**Loop-Back control [2:0]:** These bits control the Loop-Back Modes of the LIU section, according to the table below.

LOOP2	LOOP1	LOOP0	Loop-Back Mode
0	X	X	No Loop-Back
1	0	0	Dual Loop-Back
1	0	1	Analog Loop-Back
1	1	0	Remote Loop-Back
1	1	1	Digital Loop-Back

Table 112: LIU Channel Control Register 3 (LIUCCR3) **Hex Address: 0x0Fn3**

<table>
<tr><th>Bit</th><th>Function</th><th>Type</th><th>Default</th><th>Description-Operation</th></tr>
<tr><td>7-6</td><td>NLCDE[1:0]</td><td>R/W</td><td>00</td><td>Network Loop Code Detection Enable [1:0]:
These bits are used to control the Loop-Code detection on the receive path of each channel, according to the table below. This part must be in Single Rail mode to detect.
<table>
<tr><th>NLCDE[1:0]</th><th>Network Loop Code Detection Enable</th></tr>
<tr><td>00</td><td>Disables Loop Code Detection</td></tr>
<tr><td>01</td><td>Enables Loop-Up Code Detection on the Receive Path.</td></tr>
<tr><td>10</td><td>Enables Loop-Down Code Detection on the Receive Path.</td></tr>
<tr><td>11</td><td>Enables Automatic Loop-Up Code Detection on the Receive Path and Remote Loop-Back Activation upon detecting Loop-Up Code.</td></tr>
</table>
Loop-Up Code Detection Enable:
The XRT86VL38 is configured to monitor the receive data for the Loop-Up code Pattern (i.e. a string of four ‘0’s followed by one ‘1’ pattern). When the presence of the “00001” pattern is detected for more than 5 seconds, the status of the NLCD bit (bit 3 of register 0x0Fn5) is set to “1” and if the NLCD interrupt is enabled (bit 3 of register 0x0Fn4), an interrupt will be generated.
Loop-Down Code Detection Enable:
The XRT86VL38 is configured to monitor the receive data for the Loop-Down code Pattern (i.e. a string of two ‘0’s followed by one ‘1’ pattern). When the presence of the “001” pattern is detected for more than 5 seconds, the status of the NLCD bit (bit 3 of register 0x0Fn5) is set to “1” and if the NLCD interrupt is enabled (bit 3 of register 0x0Fn4), an interrupt will be generated.
Automatic Loop-Up Code Detection and Remote Loop Back Activation Enable:
When this mode is enabled, the state of the NLCD bit (bit 3 of register 0x0Fn5) is reset to “0” and the XRT86VL38 is configured to monitor the receive data for the Loop-Up code. If the “00001” pattern is detected for longer than 5 seconds, then the NLCD bit (bit 3 of register 0x0Fn5) is set “1”, and Remote Loop-Back is activated. Once the remote loop-back is activated, the XRT86VL38 is automatically programmed to monitor the receive data for the Loop-Down code. The NLCD bit stays set even after the chip stops receiving the Loop-Up code.
The Remote Loop-Back condition is removed only when the XRT86VL38 receives the Loop-Down code for more than 5 seconds or if the Automatic Loop-Code detection mode is terminated.</td></tr>
<tr><td>5-2</td><td>Reserved</td><td>R/W</td><td>0</td><td>This Bit Is Not Used</td></tr>
</table>

TABLE 112: LIU CHANNEL CONTROL REGISTER 3 (LIUCCR3) HEX ADDRESS: 0X0FN3

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	INSBER_n	R/W	0	**Insert Bit Error:** This bit is used to insert a single bit error on the transmitter of the T1 LIU Block. When the T1 LIU Block is configured to transmit and detect the QRSS pattern, (i.e., TxTEST[2:0] bits set to 'b100'), a "0" to "1" transition of this bit will insert a bit error in the transmitted QRSS pattern of the selected channel number n. The state of this bit is sampled on the rising edge of the respective TCLK_n. ***NOTE:*** *To ensure the insertion of bit error, a "0" should be written in this bit location before writing a "1".*
0	Reserved	R/W	0	This Bit Is Not Used

TABLE 113: LIU CHANNEL CONTROL INTERRUPT ENABLE REGISTER (LIUCCIER) HEX ADDRESS: 0X0FN4

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	RO	0	This Bit Is Not Used
6	DMOIE_n	R/W	0	**Change of Transmit DMO (Drive Monitor Output) Condition Interrupt Enable:** This bit permits the user to either enable or disable the “Change of Transmit DMO Condition” Interrupt. If the user enables this interrupt, then the XRT86VL38 device will generate an interrupt any time when either one of the following events occur. **1.** Whenever the Transmit Section toggles the DMO Status bit (Bit 6 or Register 0x0Fn5) to “1”. **2.** Whenever the Transmit Section toggles the DMO Status bit (Bit 6 or Register 0x0Fn5) to “0”. 0 – Disables the “Change in the DMO Condition” Interrupt. 1 – Enables the “Change in the DMO Condition” Interrupt.
5	FLSIE_n	R/W	0	**FIFO Limit Status Interrupt Enable:** This bit permits the user to either enable or disable the “FIFO Limit Status” Interrupt. If the user enables this interrupt, then the XRT86VL38 device will generate an interrupt when the jitter attenuator Read/Write FIFO pointers are within +/- 3 bits. 0 = Disables the “FIFO Limit Status” Interrupt 1 = Enables the “FIFO Limit Status” Interrupt
4	Reserved	-	-	This bit is not used.
3	NLCDIE_n	R/W	0	**Change in Network Loop-Code Detection Interrupt Enable:** This bit permits the user to either enable or disable the “Change in Network Loop-Code Detection” Interrupt. If the user enables this interrupt, then the XRT86VL38 device will generate an interrupt any time when either one of the following events occur. **1.** Whenever the Receive Section (within XRT86VL38) detects the Network Loop-Code (Loop-Up or Loop-Down depending on which Loop-Code the Receive LIU is configured to detect). **2.** Whenever the Receive Section (within XRT86VL38) no longer detects the Network Loop-Code (Loop-Up or Loop-Down depending on which Loop-Code the Receive LIU is configured to detect). 0 – Disables the “Change in Network Loop-Code Detection” Interrupt. 1 – Enables the “Change in Network Loop-Code Detection” Interrupt.
2	Reserved	-	-	This bit is not used

TABLE 113: LIU CHANNEL CONTROL INTERRUPT ENABLE REGISTER (LIUCCIER) HEX ADDRESS: 0X0FN4

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	RLOSIE_n	R/W	0	**Change of the Receive LOS (Loss of Signal) Defect Condition Interrupt Enable:** This bit permits the user to either enable or disable the "Change of the Receive LOS Defect Condition" Interrupt. If the user enables this interrupt, then the XRT86VL38 device will generate an interrupt any time when either one of the following events occur. **1.** Whenever the Receive Section (within XRT86VL38) declares the LOS Defect Condition. **2.** Whenever the Receive Section (within XRT86VL38) clears the LOS Defect condition. 0 – Disables the "Change in the LOS Defect Condition" Interrupt. 1 – Enables the "Change in the LOS Defect Condition" Interrupt.
0	QRPDIE_n	R/W	0	**Change in QRSS Pattern Detection Interrupt Enable:** This bit permits the user to either enable or disable the "Change in QRSS Pattern Detection" Interrupt. If the user enables this interrupt, then the XRT86VL38 device will generate an interrupt any time when either one of the following events occur. **1.** Whenever the Receive Section (within XRT86VL38) detects the QRSS Pattern. **2.** Whenever the Receive Section (within XRT86VL38) no longer detects the QRSS Pattern. 0 – Disables the "Change in QRSS Pattern Detection" Interrupt. 1 – Enables the "Change in QRSS Pattern Detection" Interrupt.

NOTE: *Register 0x0FN4, 0x0FN5 and 0x0FN6 only work if the LIU is placed in Single Rail mode. If done so, the Framer block must also be placed in Single Rail mode in Register 0xn101.*

TABLE 114: LIU CHANNEL CONTROL STATUS REGISTER (LIUCCSR) **HEX ADDRESS: 0X0FN5**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	RO	0	
6	DMO_n	RO	0	**Driver Monitor Output (DMO) Status:** This READ-ONLY bit indicates whether or not the Transmit Section is currently declaring the DMO Alarm condition. The Transmit Section will check the Transmit Output T1 Line signal for bipolar pulses via the TTIP and TRING output signals. If the Transmit Section were to detect no bipolar signal for 128 consecutive bit-periods, then it will declare the Transmit DMO Alarm condition. This particular alarm can be used to check for fault conditions on the Transmit Output Line Signal path. The Transmit Section will clear the Transmit DMO Alarm condition the instant that it detects some bipolar activity on the Transmit Output Line signal. 0 = Indicates that the Transmit Section of XRT86VL38 is NOT currently declaring the Transmit DMO Alarm condition. 1 = Indicates that the Transmit Section of XRT86VL38 is currently declaring the Transmit DMO Alarm condition. ***NOTE:*** *If the DMO interrupt is enabled (DMOIE - bit D6 of register 0x0Fn4), any transition on this bit will generate an Interrupt.*
5	FLS_n	RO	0	**FIFO Limit Status:** This READ-ONLY bit indicates whether or not the XRT86VL38 is currently declaring the FIFO Limit Status. This bit is set to a “1” to indicate that the jitter attenuator Read/Write FIFO pointers are within +/- 3 bits. 0 = Indicates that the XRT86VL38 is NOT currently declaring the FIFO Limit Status. 1 = Indicates that the XRT86VL38 is currently declaring the FIFO Limit Status. ***NOTE:*** *If the FIFO Limit Status Interrupt is enabled, (FLSIE bit - bit D5 of register 0x0Fn4), any transition on this bit will generate an Interrupt.*
4	Reserved	-	0	This Bit Is Not Used

TABLE 114: LIU CHANNEL CONTROL STATUS REGISTER (LIUCCSR) **HEX ADDRESS: 0X0FN5**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	NLCD_n	RO	0	**Network Loop-Code Detection Status Bit:** This bit operates differently in the Manual or the Automatic Network Loop-Code detection modes. **Manual Loop-Up Code detection mode** (.i.e If NLCDE1 = “0” and NLCDE0 = “1”), this bit gets set to “1” as soon as the Loop-Up Code (“00001”) is detected in the receive data for longer than 5 seconds. This bit stays high as long as the Receive T1 LIU Block detects the presence of the Loop-Up code in the receive data and it is reset to “0” as soon as it stops receiving the Loop-Up Code. If the NLCD interrupt is enabled, the XRT86VL38 will initiate an interrupt on every transition of the NLCD status bit. **Manual Loop-Down Code detection mode** (i.e., If NLCDE1 = “1” and NLCDE0 = “0”), this bit gets set to “1” as soon as the Loop-Down Code (“001”) is detected in the receive data for longer than 5 seconds. This bit stays high as long as the Receive T1 LIU Block detects the presence of the Loop-Down code in the receive data and it is reset to “0” as soon as it stops receiving the Loop-Down Code. If the NLCD interrupt is enabled, the XRT86VL38 will initiate an interrupt on every transition of the NLCD status bit. **Automatic Loop-code detection mode** (i.e., If NLCDE1 = “1” and NLCDE0 =”1”), the state of the NLCD status bit is reset to “0” and the XRT86VL38 is programmed to monitor the receive input data for the Loop-Up code. This bit is set to a “1” to indicate that the Network Loop Code is detected for more than 5 seconds. Simultaneously, the Remote Loop-Back condition is automatically activated and the XRT86VL38 is programmed to monitor the receive data for the Network Loop Down code. The NLCD bit stays ‘high’ as long as the Remote Loop-Back condition is in effect even if the chip stops receiving the Loop-Up code. Remote Loop-Back is removed only if the XRT86VL38 detects the Loop-Down Code “001” pattern for longer than 5 seconds in the receive data. Upon detecting the Loop-Down Code “001” pattern, the XRT86VL38 will reset the NLCD status bit and an interrupt will be generated if the NLCD interrupt enable bit is enabled. Users can monitor the state of this bit to determine if the Remote Loop-Back is activated.
2	Reserved	-	0	This Bit Is Not Used
1	RLOS_n	RO	0	**Receive Loss of Signal Defect Condition Status:** This READ-ONLY bit indicates whether or not the Receive LIU Block is currently declaring the LOS defect condition. 0 = Indicates that the Receive Section is NOT currently declaring the LOS Defect Condition. 1 = Indicates that the Receive Section is currently declaring the LOS Defect condition. ***NOTE:*** *If the RLOSIE bit (bit D1 of Register 0x0Fn4) is enabled, any transition on this bit will generate an Interrupt.*

TABLE 114: LIU CHANNEL CONTROL STATUS REGISTER (LIUCCSR) **HEX ADDRESS: 0X0FN5**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
0	QRPD_n	RO	0	**Quasi-random Pattern Detection Status:** This READ-ONLY bit indicates whether or not the Receive LIU Block is currently declaring the QRSS Pattern LOCK status. 0 = Indicates that the XRT86VL38 is NOT currently declaring the QRSS Pattern LOCK. 1 = Indicates that the XRT86VL38 is currently declaring the QRSS Pattern LOCK. ***NOTE:*** *If the QRPDIE bit (bit D0 of register 0x0Fn4) is enabled, any transition on this bit will generate an Interrupt.*

NOTE: *Register 0x0FN4, 0x0FN5 and 0x0FN6 only work if the LIU is placed in Single Rail mode. If done so, the Framer block must also be placed in Single Rail mode in Register 0xn101.*

TABLE 115: LIU CHANNEL CONTROL INTERRUPT STATUS REGISTER (LIUCCISR) HEX ADDRESS: 0X0FN6

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	RO	0	
6	DMOIS_n	RUR/ WC	0	**Change of Transmit DMO (Drive Monitor Output) Condition Interrupt Status:** This RESET-upon-READ bit indicates whether or not the “Change of the Transmit DMO Condition” Interrupt has occurred since the last read of this register. 0 = Indicates that the “Change of the Transmit DMO Condition” Interrupt has NOT occurred since the last read of this register. 1 = Indicates that the “Change of the Transmit DMO Condition” Interrupt has occurred since the last read of this register. This bit is set to a “1” every time when DMO_n status bit (bit 6 of Register 0x0Fn5) has changed since the last read of this register. **NOTE:** *Users can determine the current state of the “Transmit DMO Condition” by reading out the content of bit 6 within Register 0x0Fn5*
5	FLSIS_n	RUR/ WC	0	**FIFO Limit Interrupt Status:** This RESET-upon-READ bit indicates whether or not the “FIFO Limit” Interrupt has occurred since the last read of this register. 0 = Indicates that the “FIFO Limit Status” Interrupt has NOT occurred since the last read of this register. 1 = Indicates that the “FIFO Limit Status” Interrupt has occurred since the last read of this register. This bit is set to a “1” every time when FIFO Limit Status bit (bit 5 of Register 0x0Fn5) has changed since the last read of this register. **NOTE:** *Users can determine the current state of the “FIFO Limit” by reading out the content of bit 5 within Register 0x0Fn5*
4	Reserved	-	-	This bit is not used
3	NLCDIS_n	RUR/ WC	0	**Change in Network Loop-Code Detection Interrupt Status:** This RESET-upon-READ bit indicates whether or not the “Change in Network Loop-Code Detection” Interrupt has occurred since the last read of this register. 0 = Indicates that the “Change in Network Loop-Code Detection” Interrupt has NOT occurred since the last read of this register. 1 = Indicates that the “Change in Network Loop-Code Detection” Interrupt has occurred since the last read of this register. This bit is set to a “1” every time when NLCD status bit (bit 3 of Register 0x0Fn5) has changed since the last read of this register. **NOTE:** *Users can determine the current state of the “Network Loop-Code Detection” by reading out the content of bit 3 within Register 0x0Fn5*
2	Reserved	-	-	This bit is not used

TABLE 115: LIU CHANNEL CONTROL INTERRUPT STATUS REGISTER (LIUCCISR) HEX ADDRESS: 0X0FN6

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	RLOSIS_n	RUR/ WC	0	**Change of Receive LOS (Loss of Signal) Defect Condition Interrupt Status:** This RESET-upon-READ bit indicates whether or not the “Change of the Receive LOS Defect Condition” Interrupt has occurred since the last read of this register. 0 = Indicates that the “Change of the Receive LOS Defect Condition” Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the “Change of the Receive LOS Defect Condition” Interrupt has occurred since the last read of this register. **NOTE:** *The user can determine the current state of the “Receive LOS Defect condition” by reading out the contents of Bit 1 (Receive LOS Defect Condition Status) within Register 0xnFn5.*
0	QRPDIS_n	RUR/ WC	0	**Change in Quasi-Random Pattern Detection Interrupt Status:** This RESET-upon-READ bit indicates whether or not the “Change in QRSS Pattern Detection” Interrupt has occurred since the last read of this register. 0 = Indicates that the “Change in QRSS Pattern Detection” Interrupt has NOT occurred since the last read of this register. 1 = Indicates that the “Change in QRSS Pattern Detection” Interrupt has occurred since the last read of this register. This bit is set to a “1” every time when QRPD status bit (bit 0 of Register 0x0Fn5) has changed since the last read of this register. **NOTE:** *Users can determine the current state of the “QRSS Pattern Detection” by reading out the content of bit 0 within Register 0x0Fn5*

NOTE: *Register 0x0FN4, 0x0FN5 and 0x0FN6 only work if the LIU is placed in Single Rail mode. If done so, the Framer block must also be placed in Single Rail mode in Register 0xn101.*

TABLE 116: LIU CHANNEL CONTROL CABLE LOSS REGISTER (LIUCCCCR) HEX ADDRESS: 0X0FN7

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	RO	0	
6	Reserved	RO	0	
5-0	CLOS[5:0]	RO	0	**Cable Loss [5:0]:** These bits represent the six bit receive selective equalizer setting which is also a binary word that represents the cable attenuation indication within ±1dB. CLOS5_n is the most significant bit (MSB) and CLOS0_n is the least significant bit (LSB).

TABLE 117: LIU CHANNEL CONTROL ARBITRARY REGISTER 1 (LIUCCAR1) HEX ADDRESS: 0X0FN8

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	R/W	0	
6-0	Arb_Seg1	R/W	0	**Arbitrary Transmit Pulse Shape, Segment 1:** These seven bits form the first of the eight segments of the transmit shape pulse when the XRT86VL38 is configured in “Arbitrary Mode”. These seven bits represent the amplitude of the nth channel's arbitrary pulse in signed magnitude format with Bit 6 as the sign bit and Bit 0 as the least significant bit (LSB). ***NOTE:*** *Arbitrary mode is enabled by writing to the EQC[4:0] bits in register 0x0Fn0.*

TABLE 118: LIU CHANNEL CONTROL ARBITRARY REGISTER 2 (LIUCCAR2) HEX ADDRESS: 0X0FN9

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	R/W	0	
6-0	Arb_Seg2	R/W	0	**Arbitrary Transmit Pulse Shape, Segment 2** These seven bits form the second of the eight segments of the transmit shape pulse when the XRT86VL38 is configured in “Arbitrary Mode”. These seven bits represent the amplitude of the nth channel's arbitrary pulse in signed magnitude format with Bit 6 as the sign bit and Bit 0 as the least significant bit (LSB). ***NOTE:*** *Arbitrary mode is enabled by writing to the EQC[4:0] bits in register 0x0Fn0.*

TABLE 119: LIU CHANNEL CONTROL ARBITRARY REGISTER 3 (LIUCCAR3) HEX ADDRESS: 0X0FNA

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	R/W	0	
6-0	Arb_seg3	R/W	0	**Arbitrary Transmit Pulse Shape, Segment 3** These seven bits form the third of the eight segments of the transmit shape pulse when the XRT86VL38 is configured in “Arbitrary Mode”. These seven bits represent the amplitude of the nth channel's arbitrary pulse in signed magnitude format with Bit 6 as the sign bit and Bit 0 as the least significant bit (LSB). ***NOTE:*** *Arbitrary mode is enabled by writing to the EQC[4:0] bits in register 0x0Fn0.*

TABLE 120: LIU CHANNEL CONTROL ARBITRARY REGISTER 4 (LIUCCAR4) HEX ADDRESS: 0X0FNB

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	R/W	0	
6-0	Arb_seg4	R/W	0	**Arbitrary Transmit Pulse Shape, Segment 4** These seven bits form the forth of the eight segments of the transmit shape pulse when the XRT86VL38 is configured in “Arbitrary Mode”. These seven bits represent the amplitude of the nth channel's arbitrary pulse in signed magnitude format with Bit 6 as the sign bit and Bit 0 as the least significant bit (LSB). *Arbitrary mode is enabled by writing to the EQC[4:0] bits in register 0x0Fn0.*

TABLE 121: LIU CHANNEL CONTROL ARBITRARY REGISTER 5 (LIUCCAR5) HEX ADDRESS: 0X0FNC

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	R/W	0	
6-0	Arb_seg5	R/W	0	**Arbitrary Transmit Pulse Shape, Segment 5** These seven bits form the fifth of the eight segments of the transmit shape pulse when the XRT86VL38 is configured in “Arbitrary Mode”. These seven bits represent the amplitude of the nth channel's arbitrary pulse in signed magnitude format with Bit 6 as the sign bit and Bit 0 as the least significant bit (LSB). *Arbitrary mode is enabled by writing to the EQC[4:0] bits in register 0x0Fn0.*

TABLE 122: LIU CHANNEL CONTROL ARBITRARY REGISTER 6 (LIUCCAR6) HEX ADDRESS: 0X0FND

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	R/W	0	
6-0	Arb_seg6	R/W	0	**Arbitrary Transmit Pulse Shape, Segment 6** These seven bits form the sixth of the eight segments of the transmit shape pulse when the XRT86VL38 is configured in “Arbitrary Mode”. These seven bits represent the amplitude of the nth channel's arbitrary pulse in signed magnitude format with Bit 6 as the sign bit and Bit 0 as the least significant bit (LSB). *Arbitrary mode is enabled by writing to the EQC[4:0] bits in register 0x0Fn0.*

TABLE 123: LIU CHANNEL CONTROL ARBITRARY REGISTER 7 (LIUCCAR7) HEX ADDRESS: 0X0FNE

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	R/W	0	
6	Arb_seg7	R/W	0	**Arbitrary Transmit Pulse Shape, Segment 7** These seven bits form the seventh of the eight segments of the transmit shape pulse when the XRT86VL38 is configured in “Arbitrary Mode”. These seven bits represent the amplitude of the nth channel's arbitrary pulse in signed magnitude format with Bit 6 as the sign bit and Bit 0 as the least significant bit (LSB). *Arbitrary mode is enabled by writing to the EQC[4:0] bits in register 0x0Fn0.*

TABLE 124: LIU CHANNEL CONTROL ARBITRARY REGISTER 8 (LIUCCAR8) HEX ADDRESS: 0X0FNF

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	R/W	0	
6	Arb_seg8	R/W	0	**Arbitrary Transmit Pulse Shape, Segment 8** These seven bits form the eight of the eight segments of the transmit shape pulse when the XRT86VL38 is configured in “Arbitrary Mode”. These seven bits represent the amplitude of the nth channel's arbitrary pulse in signed magnitude format with Bit 6 as the sign bit and Bit 0 as the least significant bit (LSB). *Arbitrary mode is enabled by writing to the EQC[4:0] bits in register 0x0Fn0.*

TABLE 125: LIU GLOBAL CONTROL REGISTER 0 (LIUGCR0) **HEX ADDRESS: 0X0FE0**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	SR	R/W	0	**Single Rail mode** This bit must set to "1" for Single Rail mode to use LIU diagnotic features. The Framer section must be programmed as well in Register 0xn101. 0 - Dual Rail 1 - Single Rail
6	ATAOS	R/W	0	**Automatic Transmit All Ones Upon RLOS:** This bit enables automatic transmission of All Ones Pattern upon detecting the Receive Loss of Signal (RLOS) condition. Once this bit is enabled, the Transmit T1 Framer Block will automatically transmit an All “Ones” data to the line for the channel that detects an RLOS condition. 0 = Disables the “Automatic Transmit All Ones” feature upon detecting RLOS 1 = Enables the “Automatic Transmit All Ones” feature upon detecting RLOS
5	RCLKE	R/W	0	**Receive Clock Data (Framer Bypass mode)** 0 = RPOS/RNEG data is updated on the rising edge of RCLK 1 = RPOS/RNEG data is updated on the falling edge of RCLK
4	TCLKE	R/W	0	**Transmit Clock Data (Framer Bypass mode)** 0 = TPOS/TNEG data is sampled on the falling edge of TCLK 1 = TPOS/TNEG data is sampled on the rising edge of TCLK
3	DATAP	R/W	0	**Data Polarity** 0 = Transmit input and receive output data is active “High” 1 = Transmit input and receive output data is active “Low”
2	Reserved			This Bit Is Not Used

TABLE 125: LIU GLOBAL CONTROL REGISTER 0 (LIUGCR0) HEX ADDRESS: 0x0FE0

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	GIE	R/W	0	**Global Interrupt Enable:** This bit allows users to enable or disable the global interrupt generation for all channels within the T1 LIU Block. Once this global interrupt is disabled, no interrupt will be generated to the Microprocessor Interrupt Pin even when the individual “source” interrupt status bit pulses ‘high’. If this global interrupt is enabled, users still need to enable the individual “source” interrupt in order for the T1 LIU Block to generate an interrupt to the Microprocessor pin. 0 - Disables the global interrupt generation for all channels within the T1 LIU Block. 1 - Enables the global interrupt generation for all channels within the T1 LIU Block.
0	SRESET	R/W	0	**Software Reset µP Registers:** This bit allows users to reset the XRT86VL38 device. Writing a “1” to this bit and keeping it at ’1’ for longer than 10µs initiates a device reset through the microprocessor interface. Once the XRT86VL38 is reset, all internal circuits are placed in the reset state except the microprocessor register bits. 0 = Disables software reset to the XRT86VL38 device. 1 = Enables software reset to the XRT86VL38 device.

TABLE 126: LIU GLOBAL CONTROL REGISTER 1 (LIUGCR1) HEX ADDRESS: 0x0FE1

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>7</td><td>Reserved</td><td>R/W</td><td>0</td><td></td></tr>
<tr><td>6</td><td>Reserved</td><td>R/W</td><td>0</td><td></td></tr>
<tr><td>5-4</td><td>Gauge [1:0]</td><td>R/W</td><td>00</td><td>Wire Gauge Selector [1:0]:
This bit together with Guage0 bit (bit 4 within this register) are used to select the wire gauge size as shown in the table below.
<table>
<tr><th>GAUGE1</th><th>GAUGE0</th><th>Wire Size</th></tr>
<tr><td>0</td><td>0</td><td>22 and 24 Gauge</td></tr>
<tr><td>0</td><td>1</td><td>22 Gauge</td></tr>
<tr><td>1</td><td>0</td><td>24 Gauge</td></tr>
<tr><td>1</td><td>1</td><td>26 Gauge</td></tr>
</table></td></tr>
<tr><td>3</td><td>Reserved</td><td></td><td></td><td>This bit is not used</td></tr>
</table>

TABLE 126: LIU GLOBAL CONTROL REGISTER 1 (LIUGCR1) **HEX ADDRESS: 0X0FE1**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2	RXMUTE	R/W	0	**Receive Output Mute:** This bit permits the user to configure the Receive T1 Block to automatically pull its Recovered Data Output pins to GND anytime (and for the duration that) the Receive T1 LIU Block declares the LOS defect condition. In other words, if this feature is enabled, the Receive T1 LIU Block will automatically “mute” the Recovered data that is being routed to the Receive T1 Framer block anytime (and for the duration that) the Receive T1 LIU Block declares the LOS defect condition. 0 – Disables the “Muting upon LOS” feature. 1 – Enables the “Muting upon LOS” feature. ***NOTE:** The receive clock is not muted when this feature is enabled.*
1	EXLOS			**Extended LOS Enable:** This bit allows users to extend the number of zeros at the receive input of each channel before RLOS is declared. When Extended LOS is enabled, the Receive T1 LIU Block will declare RLOS condition when it receives 4096 number of consecutive zeros at the receive input. When Extended LOS is disabled, the Receive T1 LIU Block will declare RLOS condition when it receives 175 number of consecutive zeros at the receive input. 0 = Disables the Extended LOS Feature. 1 = Enables the Extended LOS Feature.
0	$\overline{\text{ICT}}$	R/W	0	**In-Circuit-Testing Enable:** This bit allows users to tristate the output pins of all channels for in-circuit testing purposes. When In-Circuit-Testing is enabled, all output pins of the XRT86VL38 are “Tri-stated”. When In-Circuit-Testing is disabled, all output pins will resume to normal condition. 0 = Disables the In-Circuit-Testing Feature. 1 = Enables the In-Circuit-Testing Feature.

TABLE 127: LIU GLOBAL CONTROL REGISTER 2 (LIUGCR2) **HEX ADDRESS: 0X0FE2**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Force to "0"	R/W	0	**Set to "0"**
6	RxTCNTL	R/W	0	**Receive Termination Select Control** This bit sets the LIU to control the RxTSEL function with either the individual channel register bit or the global hardware pin. 0 = Control of the receive termination is set to the register bits 1 = Control of the receive termination is set to the hardware pin
5-0	Reserved	R/W	0	This Bit Is Not Used

TABLE 128: LIU GLOBAL CONTROL REGISTER 3 (LIUGCR3) HEX ADDRESS: 0X0FE4

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>7-6</td><td>MCLKnT1[1:0]</td><td>R/W</td><td>00</td><td>Master T1 Output Clock Reference [1:0]
These two bits allow users to select the programmable output clock rates for the T1MCLKnOUT pin, according to the table below.
<table>
<tr><th>MCLKNT1[1:0]</th><th>CLOCK RATE OF THE T1MCLKNOUT OUTPUT PIN</th></tr>
<tr><td>00</td><td>1.544MHz</td></tr>
<tr><td>01</td><td>3.088MHz</td></tr>
<tr><td>10</td><td>6.176MHz</td></tr>
<tr><td>11</td><td>12.352MHz</td></tr>
</table></td></tr>
<tr><td>5-4</td><td>MCLKnE1[1:0]</td><td>R/W</td><td>00</td><td>Master E1 Output Clock Reference [1:0]:
These two bits allow users to select the programmable output clock rates for the E1MCLKnOUT pin, according to the table below:
<table>
<tr><th>MCLKNE1[1:0]</th><th>CLOCK RATE OF THE E1MCLKNOUT OUTPUT PIN</th></tr>
<tr><td>00</td><td>2.048MHz</td></tr>
<tr><td>01</td><td>4.096MHz</td></tr>
<tr><td>10</td><td>8.192MHz</td></tr>
<tr><td>11</td><td>16.384MHz</td></tr>
</table></td></tr>
<tr><td>3-0</td><td>Reserved</td><td>R/W</td><td>0</td><td>This Bit Is Not Used.</td></tr>
</table>

TABLE 129: LIU GLOBAL CONTROL REGISTER 4 (LIUGCR4) HEX ADDRESS: 0X0FE9

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>7-4</td><td>Reserved</td><td>R/W</td><td>0</td><td></td></tr>
<tr><td>3-0</td><td>CLKSEL[3:0]</td><td>R/W</td><td>1100</td><td>Clock Select Input [3:0]
These four bits allow users to select the programmable input clock rates for the MCLKIN input pin, according to the table below.
<table>
<tr><th>CLKSEL[3:0]</th><th>CLOCK RATE OF THE MCLKIN INPUT PIN</th></tr>
<tr><td>0000</td><td>2.048MHz</td></tr>
<tr><td>0001</td><td>1.544MHz</td></tr>
<tr><td>0010</td><td>8kHz</td></tr>
<tr><td>0011</td><td>16kHz</td></tr>
<tr><td>0100</td><td>56kHz</td></tr>
<tr><td>0101</td><td>64kHz</td></tr>
<tr><td>0110</td><td>128kHz</td></tr>
<tr><td>0111</td><td>256kHz</td></tr>
<tr><td>1000</td><td>4.096MHz</td></tr>
<tr><td>1001</td><td>3.088MHz</td></tr>
<tr><td>1010</td><td>8.192MHz</td></tr>
<tr><td>1011</td><td>6.176MHz</td></tr>
<tr><td>1100</td><td>16.384MHz</td></tr>
<tr><td>1101</td><td>12.352MH</td></tr>
<tr><td>1110</td><td>2.048MHz</td></tr>
<tr><td>1111</td><td>1.544MHz</td></tr>
</table>
NOTE: <i>User must provide any one of the above clock frequencies to the MCLKIN input pin for the device to be functional.</i></td></tr>
</table>

TABLE 130: LIU GLOBAL CONTROL REGISTER 5 (LIUGCR5) **HEX ADDRESS: 0X0FEA**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	GCHIS7	RUR/ WC	0	**Global Channel 7 Interrupt Status Indicator** This Reset-Upon-Read bit field indicates whether or not an interrupt has occurred on Channel 7 within the XRT86VL38 device since the last read of this register. 0 = Indicates that No interrupt has occurred on Channel 7 within the XRT86VL38 device since the last read of this register. 1 = Indicates that an interrupt has occurred on Channel 7 within the XRT86VL38 device since the last read of this register.
6	GCHIS6	RUR/ WC	0	**Global Channel 6 Interrupt Status Indicator** This Reset-Upon-Read bit field indicates whether or not an interrupt has occurred on Channel 6 within the XRT86VL38 device since the last read of this register. 0 = Indicates that No interrupt has occurred on Channel 6 within the XRT86VL38 device since the last read of this register. 1 = Indicates that an interrupt has occurred on Channel 6 within the XRT86VL38 device since the last read of this register.
5	GCHIS5	RUR/ WC	0	**Global Channel 5 Interrupt Status Indicator** This Reset-Upon-Read bit field indicates whether or not an interrupt has occurred on Channel 5 within the XRT86VL38 device since the last read of this register. 0 = Indicates that No interrupt has occurred on Channel 5 within the XRT86VL38 device since the last read of this register. 1 = Indicates that an interrupt has occurred on Channel 5 within the XRT86VL38 device since the last read of this register.
4	GCHIS4	RUR/ WC	0	**Global Channel 4 Interrupt Status Indicator** This Reset-Upon-Read bit field indicates whether or not an interrupt has occurred on Channel 4 within the XRT86VL38 device since the last read of this register. 0 = Indicates that No interrupt has occurred on Channel 4 within the XRT86VL38 device since the last read of this register. 1 = Indicates that an interrupt has occurred on Channel 4 within the XRT86VL38 device since the last read of this register.
3	GCHIS3	RUR/ WC	0	**Global Channel 3 Interrupt Status Indicator** This Reset-Upon-Read bit field indicates whether or not an interrupt has occurred on Channel 3 within the XRT86VL38 device since the last read of this register. 0 = Indicates that No interrupt has occurred on Channel 3 within the XRT86VL38 device since the last read of this register. 1 = Indicates that an interrupt has occurred on Channel 3 within the XRT86VL38 device since the last read of this register.

TABLE 130: LIU GLOBAL CONTROL REGISTER 5 (LIUGCR5) **HEX ADDRESS: 0x0FEA**

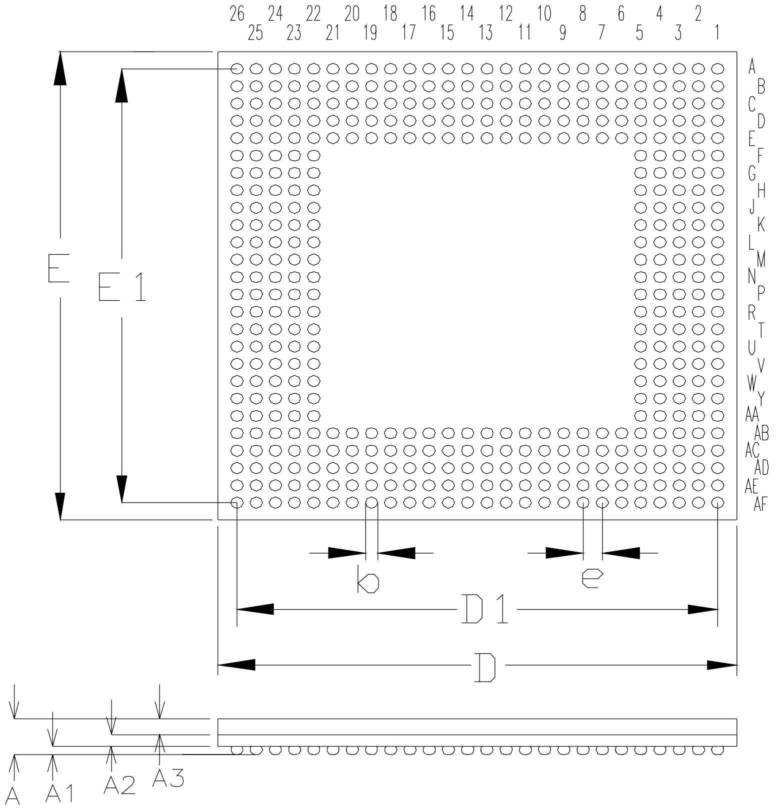
BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2	GCHIS2	RUR/ WC	0	**Global Channel 2 Interrupt Status Indicator** This Reset-Upon-Read bit field indicates whether or not an interrupt has occurred on Channel 2 within the XRT86VL38 device since the last read of this register. 0 = Indicates that No interrupt has occurred on Channel 2 within the XRT86VL38 device since the last read of this register. 1 = Indicates that an interrupt has occurred on Channel 2 within the XRT86VL38 device since the last read of this register.
1	GCHIS1	RUR/ WC	0	**Global Channel 1 Interrupt Status Indicator** This Reset-Upon-Read bit field indicates whether or not an interrupt has occurred on Channel 1 within the XRT86VL38 device since the last read of this register. 0 = Indicates that No interrupt has occurred on Channel 1 within the XRT86VL38 device since the last read of this register. 1 = Indicates that an interrupt has occurred on Channel 1 within the XRT86VL38 device since the last read of this register.
0	GCHIS0	RUR/ WC	0	**Global Channel 0 Interrupt Status Indicator** This Reset-Upon-Read bit field indicates whether or not an interrupt has occurred on Channel 0 within the XRT86VL38 device since the last read of this register. 0 = Indicates that No interrupt has occurred on Channel 0 within the XRT86VL38 device since the last read of this register. 1 = Indicates that an interrupt has occurred on Channel 0 within the XRT86VL38 device since the last read of this register.

ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT86VL38IB	420 Plastic Ball Grid Array	-40°C to +85°C
XRT86VL38IB484	484 Shrink Thin Ball Grid Array	-40°C to +85°C

PACKAGE DIMENSIONS FOR 420 PLASTIC BALL GRID ARRAY

420 Plastic Ball Grid Array
(35.0 mm x 35.0 mm, PBGA)
Rev. 1.00



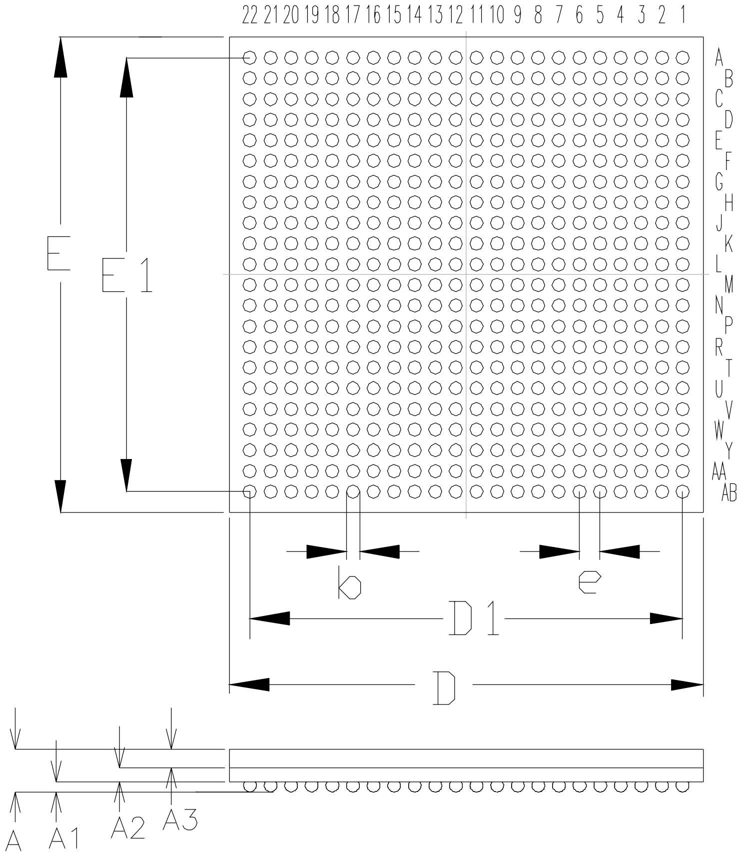
Note: The control dimension is in millimeter.

	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.085	0.098	2.16	2.50
A1	0.020	0.028	0.50	0.70
A2	0.020	0.024	0.51	0.61
A3	0.045	0.047	1.15	1.19
D	1.370	1.386	34.80	35.20
D1	1.2500 BSC		31.75 BSC	
E	1.370	1.386	34.80	35.20
E1	1.2500 BSC		31.75 BSC	
b	0.024	0.035	0.60	0.90
e	0.0500 BSC		1.27 TYP.	

PACKAGE DIMENSIONS FOR 484 SHRINK THIN BALL GRID ARRAY

484 Shrink Thin Ball Grid Array
(23.0 mm x 23.0 mm, STBGA)

Rev. 1.00



Note: The control dimension is in millimeter.

	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.071	0.082	1.80	2.08
A1	0.019	0.022	0.47	0.57
A2	0.019	0.022	0.48	0.56
A3	0.033	0.037	0.85	0.95
D	0.898	0.913	22.80	23.20
D1	0.8268 BSC		21.00 BSC	
E	0.898	0.913	22.80	23.20
E1	0.8268 BSC		21.00 BSC	
b	0.024	0.028	0.60	0.70
e	0.0394 BSC		1.00 BSC	

REVISION HISTORY

REVISION #	DATE	DESCRIPTION
V1.2.0	January 29, 2007	Released to Production.

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Datasheet January 2007.