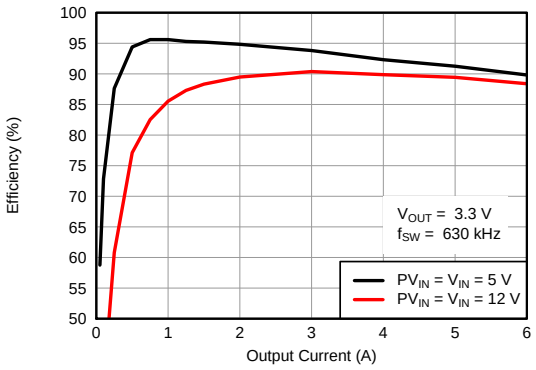
TPS84620 4.5-V to 14.5-V Input, 6-A Synchronous Buck, Integrated Power Solution

1 FEATURES

- Complete Integrated Power Solution Allows Small Footprint, Low-Profile Design
- Efficiencies Up To 96%
- Wide-Output Voltage Adjust 1.2 V to 5.5 V, with 1% Reference Accuracy
- Optional Split Power Rail allows Input Voltage Down to 1.7 V
- Adjustable Switching Frequency (480 kHz to 780 kHz)
- Synchronizes to an External Clock
- Adjustable Slow Start
- Output Voltage Sequencing / Tracking
- Power Good Output
- Programmable Undervoltage Lockout (UVLO)
- Output Overcurrent Protection
- Over Temperature Protection
- Pre-bias Output Start-up
- Operating Temperature Range: –40°C to +85°C
- Enhanced Thermal Performance: 13°C/W
- Meets EN55022 Class B Emissions
- For Design Help Including SwitcherPro™ visit http://www.ti.com/tps84620

2 APPLICATIONS

- Broadband and Communications Infrastructure
- Automated Test and Medical Equipment
- Compact PCI / PCI Express / PXI Express
- DSP and FPGA Point of Load Applications
- High Density Distributed Power Systems



3 DESCRIPTION

The TPS84620RUQ is an easy-to-use integrated power solution that combines a 6-A DC/DC converter with power MOSFETs, an inductor, and passives into a low profile, BQFN package. This total power solution allows as few as 3 external components and eliminates the loop compensation and magnetics part selection process.

The 9×15×2.8 mm BQFN package is easy to solder onto a printed circuit board and allows a compact point-of-load design with greater than 90% efficiency and excellent power dissipation with a thermal impedance of 13°C/W junction to ambient. The device delivers the full 6-A rated output current at 85°C ambient temperature without airflow.

The TPS84620 offers the flexibility and the feature-set of a discrete point-of-load design and is ideal for powering performance DSPs and FPGAs. Advanced packaging technology afford a robust and reliable power solution compatible with standard QFN mounting and testing techniques.

SIMPLIFIED APPLICATION

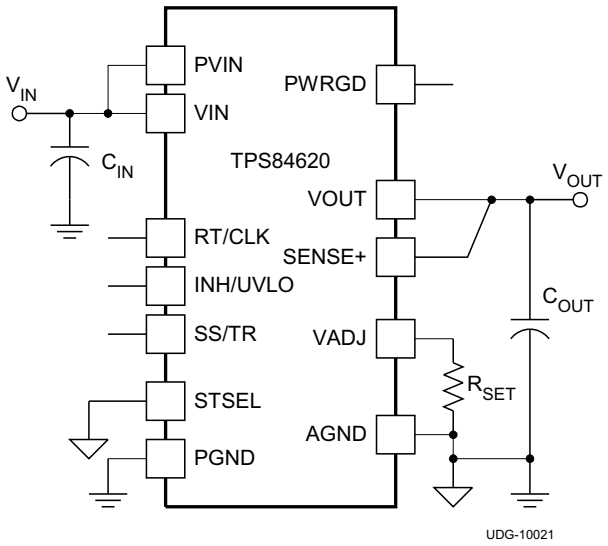


Table 1. ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this datasheet, or see the TI website at www.ti.com.

4 Specifications

4.1 ABSOLUTE MAXIMUM RATINGS(1)

over operating temperature range (unless otherwise noted)			
		VALUE	UNIT
Input Voltage	VIN	–0.3 to 16	V
	PVIN	–0.3 to 16	V
	INH/UVLO	–0.3 to 6	V
	VADJ	–0.3 to 3	V
	PWRGD	–0.3 to 6	V
	SS/TR	–0.3 to 3	V
	STSEL	–0.3 to 3	V
	RT/CLK	–0.3 to 6	V
Output Voltage	PH	–1 to 20	V
	PH 10-ns Transient	–3 to 20	V
V_{DIFF} (GND to exposed thermal pad)		–0.2 to 0.2	V
Source Current	RT/CLK	±100	µA
	PH	Current Limit	A
Sink Current	PH	Current Limit	A
	PVIN	Current Limit	A
	PWRGD	–0.1 to 5	mA
Operating Junction Temperature		–40 to 125(2)	°C
Storage Temperature		–65 to 150	°C
Peak Reflow Case Temperature(3)(4)		245	°C
Maximum Number of Reflows Allowed(3)(4)		3	
Mechanical Shock	Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted	1500	G
Mechanical Vibration	Mil-STD-883D, Method 2007.2, 20-2000Hz	20	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) See the temperature derating curves in the Typical Characteristics section for thermal information.
(3) For soldering specifications, refer to the *Soldering Requirements for BQFN Packages* application note.
(4) Devices with a date code prior to week 14 2018 (1814) have a peak reflow case temperature of 240°C with a maximum of one reflow.

4.2 THERMAL INFORMATION

THERMAL METRIC(1)		LMZ31506H RUQ47 47 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	13	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	9	
θ_{JB}	Junction-to-board thermal resistance(4)	6	
ψ_{JT}	Junction-to-top characterization parameter(5)	2.5	
ψ_{JB}	Junction-to-board characterization parameter(6)	5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	3.8	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

4.3 PACKAGE SPECIFICATIONS

TPS84620		UNIT
Weight		1.26 grams
Flammability	Meets UL 94 V-O	
MTBF Calculated reliability	Per Bellcore TR-332, 50% stress, T_A = 40°C, ground benign	33.9 MHrs

4.4 ELECTRICAL CHARACTERISTICS

over -40°C to 85°C free-air temperature, PVIN = VIN = 12 V, V_{OUT} = 1.8 V, I_{OUT} = 6A, C_{IN1} = 2x 22 µF ceramic, C_{IN2} = 68 µF poly-tantalum, C_{OUT1} = 4x 47 µF ceramic (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{OUT}	Output current	T_A = 85°C, natural convection		0		6	A
VIN	Input bias voltage range	Over I_{OUT} range		4.5		14.5	V
PVIN	Input switching voltage range	Over I_{OUT} range		1.7 (1)		14.5	V
UVLO	VIN Undervoltage lockout	VIN = increasing			4.0	4.5	V
		VIN = decreasing		3.5	3.85		
$V_{OUT(adj)}$	Output voltage adjust range	Over I_{OUT} range		1.2		5.5	V
V_{OUT}	Set-point voltage tolerance	T_A = 25°C, I_{OUT} = 0A				±1.0% (2)	
	Temperature variation	-40°C ≤ T_A ≤ +85°C, I_{OUT} = 0A			±0.3%		
	Line regulation	Over PVIN range, T_A = 25°C, I_{OUT} = 0A			±0.1%		
	Load regulation	Over I_{OUT} range, T_A = 25°C			±0.1%		
	Total output voltage variation	Includes set-point, line, load, and temperature variation				±1.5% (2)	
η	Efficiency	PVIN = VIN = 12 V, I_O = 3 A	V_{OUT} = 5V, f_{SW} = 780kHz		93 %		
			V_{OUT} = 3.3V, f_{SW} = 630kHz		90 %		
			V_{OUT} = 2.5V, f_{SW} = 530kHz		89 %		
			V_{OUT} = 1.8V, f_{SW} = 480kHz		87 %		
			V_{OUT} = 1.5V, f_{SW} = 480kHz		85 %		
			V_{OUT} = 1.2V, f_{SW} = 480kHz		83 %		
		PVIN = VIN = 5 V, I_O = 3 A	V_{OUT} = 3.3V, f_{SW} = 630kHz		94 %		
			V_{OUT} = 2.5V, f_{SW} = 530kHz		92 %		
			V_{OUT} = 1.8V, f_{SW} = 480kHz		90 %		
			V_{OUT} = 1.5V, f_{SW} = 480kHz		88 %		
			V_{OUT} = 1.2V, f_{SW} = 480kHz		86 %		
	Output voltage ripple	20 MHz bandwith			30		mV_{PP}
I_{LIM}	Overcurrent threshold				11		A
	Transient response	1.0 A/µs load step from 50 to 100% $I_{OUT(max)}$	Recovery time		80		µs
			V_{OUT} over/undershoot		60		mV
V_{INH-H}	Inhibit Control	Inhibit High Voltage		1.30		Open (3)	V
V_{INH-L}		Inhibit Low Voltage		–0.3		1.05	
	INH Input current	INH < 1.1 V			-1.15		µA
	INH Hysteresis current	INH > 1.26 V			-3.4		µA
$I_{I(stby)}$	Input standby current	INH pin to AGND			2	4	µA
Power Good	PWRGD Thresholds	V_{OUT} rising	Good		94%		
			Fault		109%		
		V_{OUT} falling	Fault		91%		
			Good		106%		
	PWRGD Low Voltage	I(PWRGD) = 2 mA				0.3	V
f_{SW}	Switching frequency	Over VIN and I_{OUT} ranges, RT/CLK pin OPEN		400	480	560	kHz
f_{CLK}	Synchronization frequency	CLK Control		480		780	kHz
V_{CLK-H}	CLK High-Level Threshold			2.0		5.5	V
V_{CLK-L}	CLK Low-Level Threshold					0.8	V
D_{CLK}	CLK Duty cycle			20%		80%	
	Thermal Shutdown	Thermal shutdown		160	175		°C
		Thermal shutdown hysteresis			10		°C

(1) The minimum PVIN voltage is 1.7V or (V_{OUT}+ 0.5V) , whichever is greater. VIN must be greater than 4.5V.
(2) The stated limit of the set-point voltage tolerance includes the tolerance of both the internal voltage reference and the internal adjustment resistor. The overall output voltage tolerance will be affected by the tolerance of the external R_{SET} resistor.
(3) This control pin has an internal pullup. If this pin is left open circuit, the device operates when input power is applied. A small low-leakage (<300 nA) MOSFET is recommended for control. See the application section for further guidance.

ELECTRICAL CHARACTERISTICS (continued)

over -40°C to 85°C free-air temperature, PVIN = VIN = 12 V, V_{OUT} = 1.8 V, I_{OUT} = 6A,
C_{IN1} = 2x 22 µF ceramic, C_{IN2} = 68 µF poly-tantalum, C_{OUT1} = 4x 47 µF ceramic (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{IN}	External input capacitance	Ceramic	44 (4)			µF
		Non-ceramic	68 (4)			
C_{OUT}	External output capacitance	Ceramic	47 (5)	200	1500	µF
		Non-ceramic		220 (5)	5000	
		Equivalent series resistance (ESR)			35	mΩ

(4) A minimum of 100µF of polymer tantalum and/or ceramic external capacitance is required across the input (VIN and PVIN connected) for proper operation. Locate the capacitor close to the device. See Table 7 for more details. When operating with split VIN and PVIN rails, place 4.7µF of ceramic capacitance directly at the VIN pin.

(5) The amount of required output capacitance varies depending on the output voltage (see Table 5). The amount of required capacitance must include at least 1x 47µF ceramic capacitor. Locate the capacitance close to the device. Adding additional capacitance close to the load improves the response of the regulator to load transients. See Table 5 and Table 7 more details.

5 DEVICE INFORMATION

FUNCTIONAL BLOCK DIAGRAM

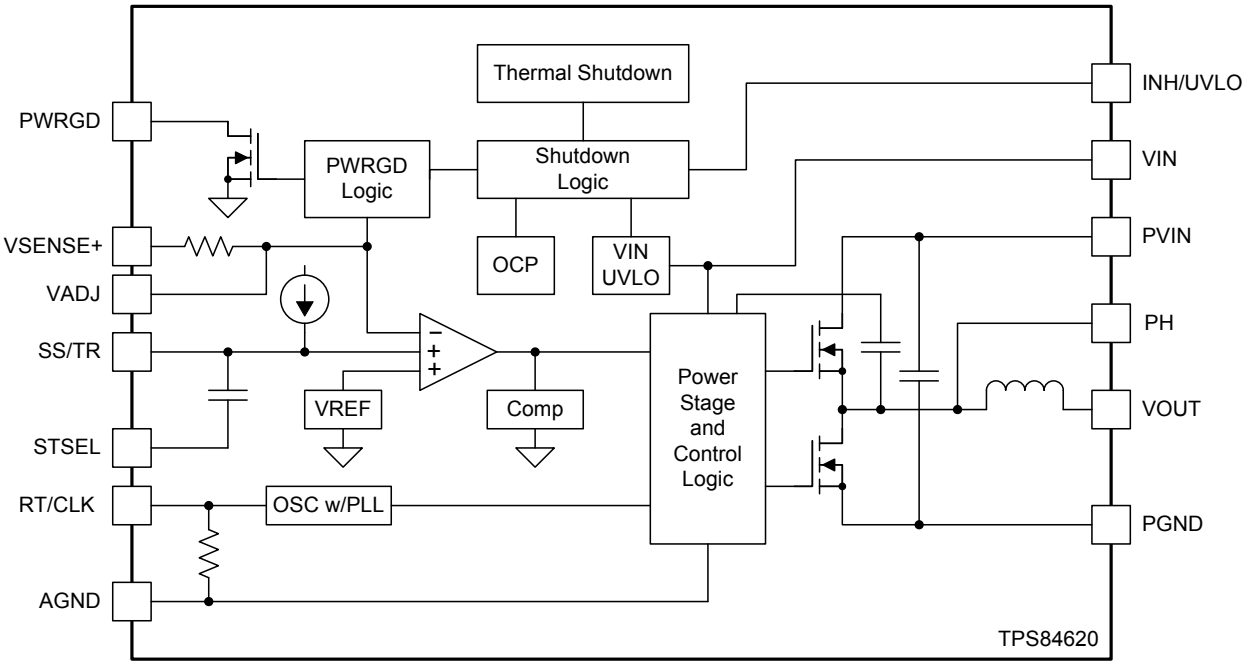


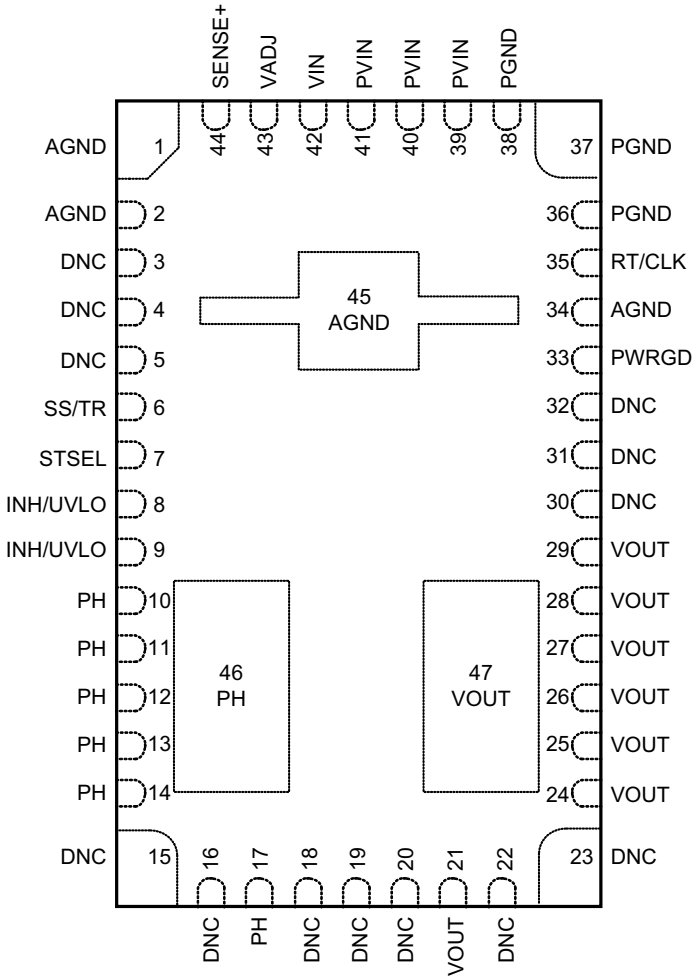
Table 2. PIN DESCRIPTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
AGND	1	Zero VDC reference for the analog control circuitry. Connect AGND to PGND at a single point. Connect near the output capacitors.
	2	
	34	
	45	
INH/UVLO	8	Inhibit and UVLO adjust pin. Use an open drain or open collector output logic to control the INH function. A resistor divider between this pin, AGND and VIN adjusts the UVLO voltage. Tie both pins together when using this control.
	9	
DNC	3	Do not connect. These pins must remain isolated from one another. Do not connect these pins to AGND or to any voltage. These pins must be soldered to isolated pads.
	4	
	5	
	15	
	16	
	18	
	19	
	20	
	22	
	23	
	30	
	31	
	32	
PGND	36	Common ground connection for the PVIN, VIN, and VOUT power connections.
	37	
	38	
PH	10	Phase switch node. These pins should be connected by a small copper island under the device for thermal relief. Do not place any external component on this pin or tie it to a pin of another function.
	11	
	12	
	13	
	14	
	17	
	46	
PWRGD	33	Power good fault pin. Asserts low if the output voltage is low. A pull-up resistor is required.
PVIN	39	Input switching voltage. this pin supplies voltage the power switches of the converter.
	40	
	41	
RT/CLK	35	This pin automatically selects between RT mode and CLK mode. An external timing resistor adjusts the switching frequency of the device. In CLK mode, the device synchronizes to an external clock.
SENSE+	44	Remote sense connection. Connect this pin to VOUT at the load for improved regulation. This pin must be connected to VOUT at the load, or at the device pins.
SS/TR	6	Slow-start and tracking pin. Connecting an external capacitor to this pin adjusts the output voltage rise time. A voltage applied to this pin allows for tracking and sequencing control.
STSEL	7	Slow-start or track feature select. Connect this pin to AGND to enable the internal SS capacitor with a SS interval of approximately 1.1 ms. Leave this pin open to enable the TR feature.
VADJ	43	Connecting a resistor between this pin and AGND sets the output voltage.
VIN	42	Input bias voltage pin. Supplies the control circuitry of the power converter.

Table 2. PIN DESCRIPTIONS (continued)

TERMINAL		DESCRIPTION
NAME	NO.	
VOUT	21	Output voltage. Connect output capacitors between these pins and PGND.
	24	
	25	
	26	
	27	
	28	
	29	
	47	

RUQ PACKAGE
47 PIN
TOP VIEW



6 TYPICAL CHARACTERISTICS (PVIN = VIN = 12 V) (1) (2)

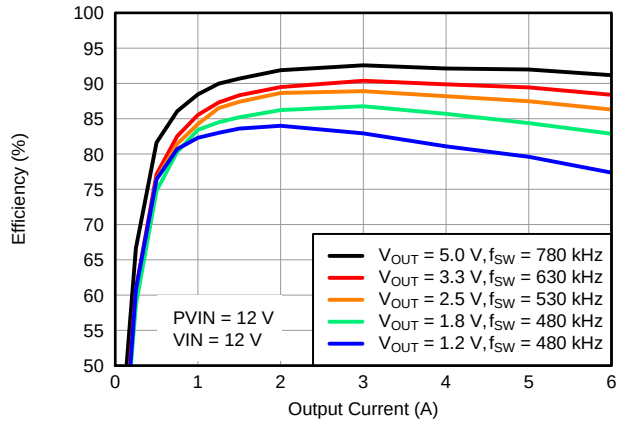


Figure 1. Efficiency vs. Output Current

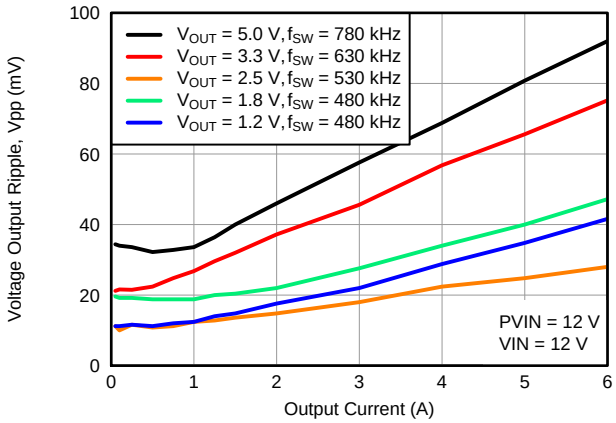


Figure 2. Voltage Ripple vs. Output Current

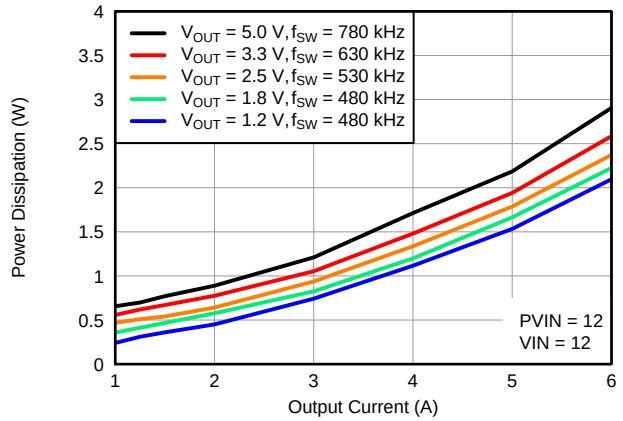


Figure 3. Power Dissipation vs. Output Current

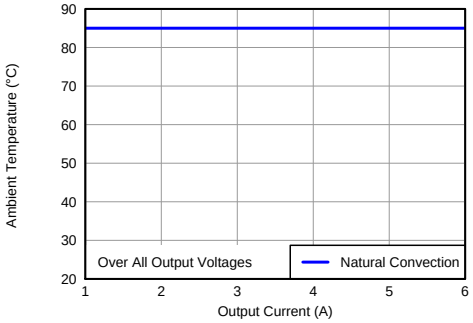


Figure 4. Safe Operating Area

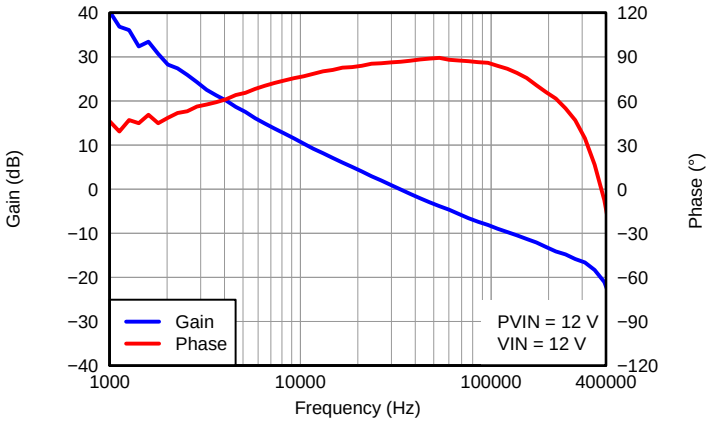


Figure 5. V_{OUT}=1.2 V, I_{OUT}=3 A, C_{OUT1}=47 µF ceramic, C_{OUT2}= 330 µF POSCAP, f_{SW}=480 kHz

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 1, Figure 2, and Figure 3.

(2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm double-sided PCB with 1 oz. copper. Applies to Figure 4.

7 TYPICAL CHARACTERISTICS (PVIN = VIN = 5 V) (1) (2)

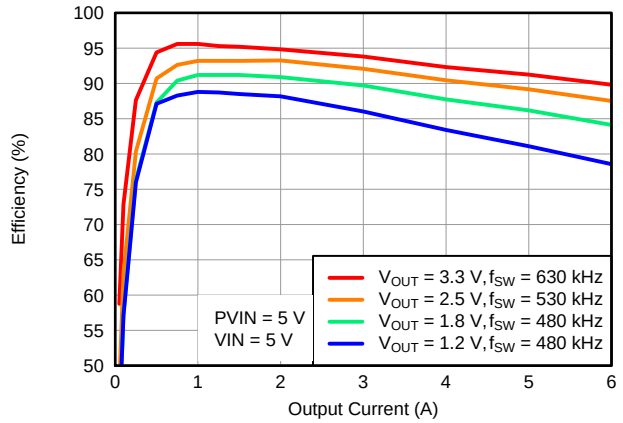


Figure 6. Efficiency vs. Output Current

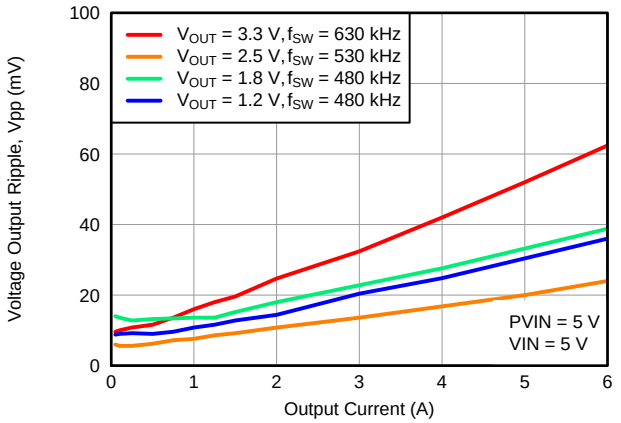


Figure 7. Voltage Ripple vs. Output Current

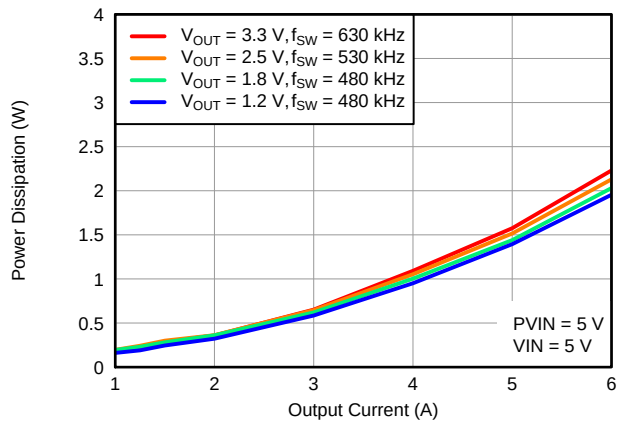


Figure 8. Power Dissipation vs. Output Current

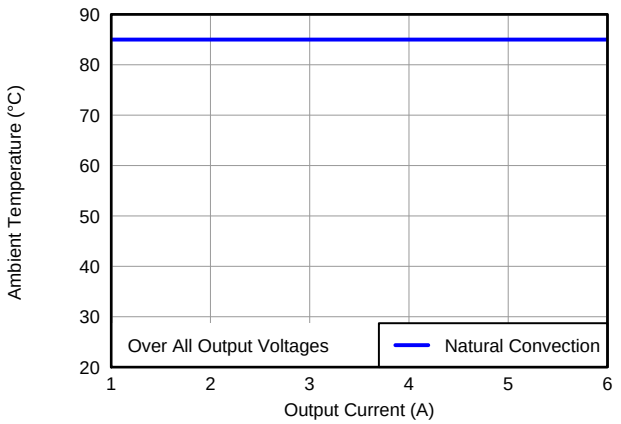


Figure 9. Safe Operating Area

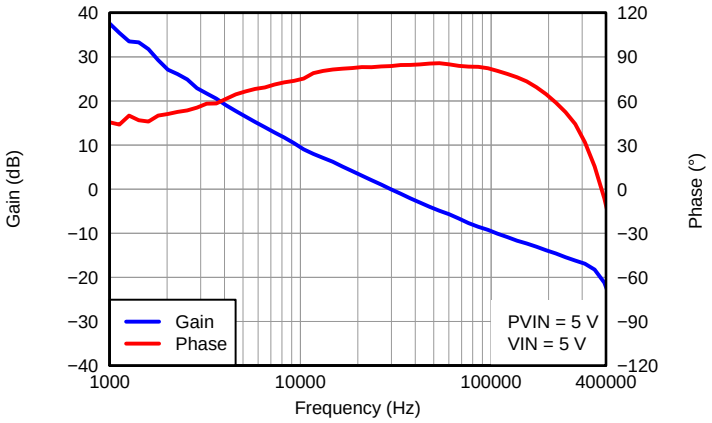


Figure 10. V_{OUT}=1.2 V, I_{OUT}=3 A, C_{OUT1}=47 µF ceramic, C_{OUT2}= 330 µF POSCAP, f_{SW}=480 kHz

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 6, Figure 7, and Figure 8.

(2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm double-sided PCB with 1 oz. copper. Applies to Figure 9.

8 TYPICAL CHARACTERISTICS (PVIN = 12 V, VIN = 5 V) (1) (2)

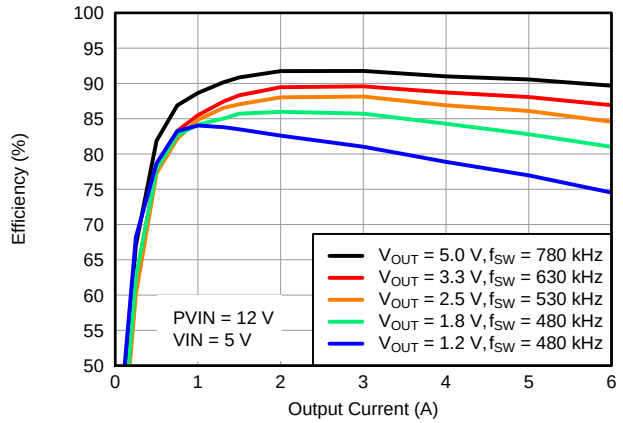


Figure 11. Efficiency vs. Output Current

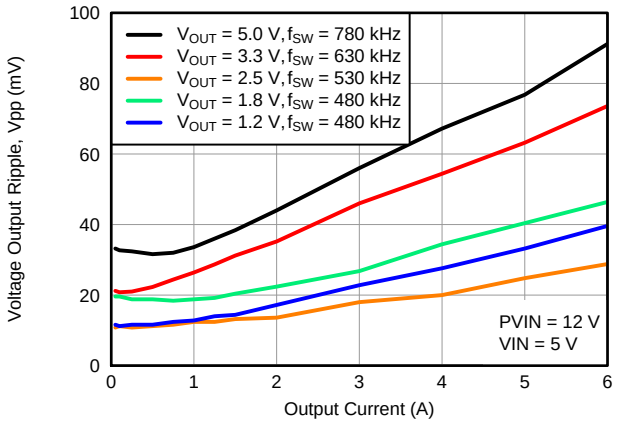


Figure 12. Voltage Ripple vs. Output Current

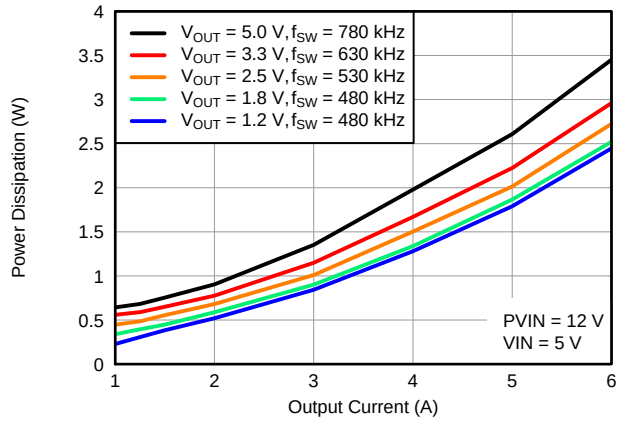


Figure 13. Power Dissipation vs. Output Current

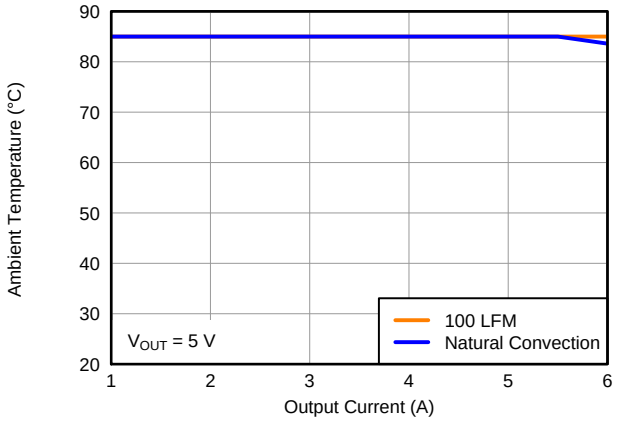


Figure 14. Safe Operating Area

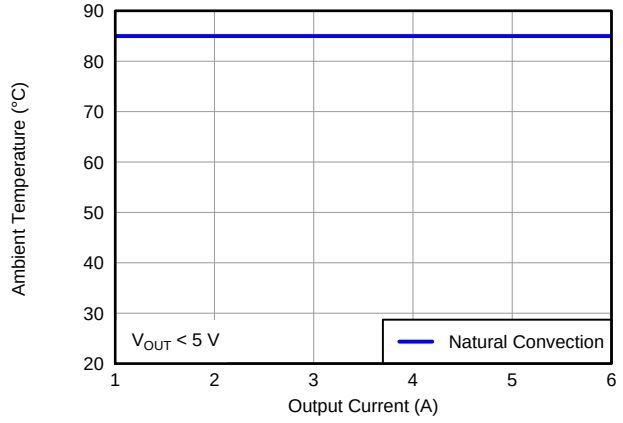


Figure 15. Safe Operating Area

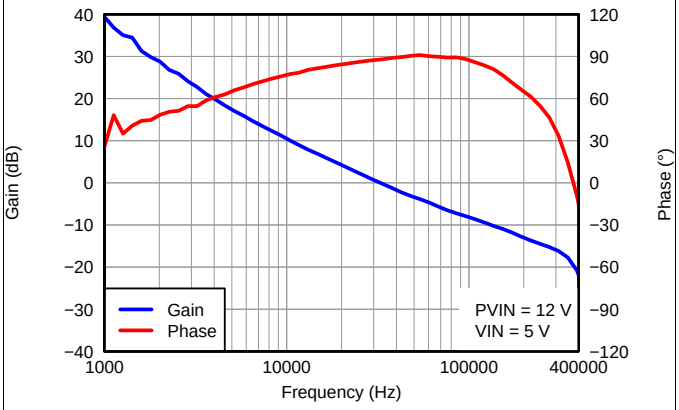


Figure 16. V_{OUT}=1.2 V, I_{OUT}=3 A, C_{OUT1}=47 µF ceramic, C_{OUT2}= 330 µF POSCAP, f_{SW}=480 kHz

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 11, Figure 12, and Figure 13.

(2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm double-sided PCB with 1 oz. copper. Applies to Figure 14 and Figure 15.

9 APPLICATION INFORMATION

9.1 ADJUSTING THE OUTPUT VOLTAGE

The VADJ control sets the output voltage of the TPS84620. The output voltage adjustment range is from 1.2V to 5.5V. The adjustment method requires the addition of R_{SET}, which sets the output voltage, the connection of SENSE+ to VOUT, and in some cases R_{RT} which sets the switching frequency. The R_{SET} resistor must be connected directly between the VADJ (pin 43) and AGND (pin 45). The SENSE+ pin (pin 44) must be connected to VOUT either at the load for improved regulation or at VOUT of the device. The R_{RT} resistor must be connected directly between the RT/CLK (pin 35) and AGND (pin 34).

Table 3 gives the standard external R_{SET} resistor for a number of common bus voltages, along with the required R_{RT} resistor for that output voltage.

Table 3. Standard R_{SET} Resistor Values for Common Output Voltages

RESISTORS	OUTPUT VOLTAGE V_{OUT} (V)					
	1.2	1.5	1.8	2.5	3.3	5.0
R_{SET} (kΩ)	2.87	1.62	1.13	0.665	0.453	0.267
R_{RT} (kΩ)	open	open	open	1000	332	165

For other output voltages, the value of the required resistor can either be calculated using the following formula, or simply selected from the range of values given in Table 4.

$$R_{SET} = \frac{1.43}{\left(\left(\frac{V_{OUT}}{0.8}\right) - 1\right)} \ (k\Omega) \quad (1)$$

Table 4. Standard R_{SET} Resistor Values

V_{OUT} (V)	R_{SET} (kΩ)	R_{RT}(kΩ)	f_{SW}(kHz)	V_{OUT} (V)	R_{SET} (kΩ)	R_{RT}(kΩ)	f_{SW}(kHz)
1.2	2.87	open	480	3.4	0.442	332	630
1.3	2.26	open	480	3.5	0.422	332	630
1.4	1.91	open	480	3.6	0.402	332	630
1.5	1.62	open	480	3.7	0.392	332	630
1.6	1.43	open	480	3.8	0.374	249	680
1.7	1.27	open	480	3.9	0.365	249	680
1.8	1.13	open	480	4.0	0.357	249	680
1.9	1.02	open	480	4.1	0.348	249	680
2.0	0.953	open	480	4.2	0.332	196	730
2.1	0.866	open	480	4.3	0.324	196	730
2.2	0.806	open	480	4.4	0.316	196	730
2.3	0.750	open	480	4.5	0.309	196	730
2.4	0.715	open	480	4.6	0.301	196	730
2.5	0.665	open	480	4.7	0.294	196	730
2.6	0.634	1000	530	4.8	0.287	165	780
2.7	0.604	1000	530	4.9	0.280	165	780
2.8	0.562	1000	530	5.0	0.267	165	780
2.9	0.536	1000	530	5.1	0.267	165	780
3.0	0.511	499	580	5.2	0.261	165	780
3.1	0.499	499	580	5.3	0.255	165	780
3.2	0.475	499	580	5.4	0.249	165	780
3.3	0.453	332	630	5.5	0.243	165	780

9.2 CAPACITOR RECOMMENDATIONS FOR THE TPS84620 POWER SUPPLY

9.2.1 Capacitor Technologies

9.2.1.1 Electrolytic, Polymer-Electrolytic Capacitors

When using electrolytic capacitors, high-quality, computer-grade electrolytic capacitors are recommended. Polymer-electrolytic type capacitors are recommended for applications where the ambient operating temperature is less than 0°C. The Sanyo OS-CON capacitor series is suggested due to the lower ESR, higher rated surge, power dissipation, ripple current capability, and small package size. Aluminum electrolytic capacitors provide adequate decoupling over the frequency range of 2 kHz to 150 kHz, and are suitable when ambient temperatures are above 0°C.

9.2.1.2 Ceramic Capacitors

The performance of aluminum electrolytic capacitors is less effective than ceramic capacitors above 150 kHz. Multilayer ceramic capacitors have a low ESR and a resonant frequency higher than the bandwidth of the regulator. They can be used to reduce the reflected ripple current at the input as well as improve the transient response of the output.

9.2.1.3 Tantalum, Polymer-Tantalum Capacitors

Polymer-tantalum type capacitors are recommended for applications where the ambient operating temperature is less than 0°C. The Sanyo POSCAP series and Kemet T530 capacitor series are recommended rather than many other tantalum types due to their lower ESR, higher rated surge, power dissipation, ripple current capability, and small package size. Tantalum capacitors that have no stated ESR or surge current rating are not recommended for power applications.

9.2.2 Input Capacitor

The TPS84620 requires a minimum input capacitance of 100 µF of ceramic and/or polymer-tantalum capacitors. The ripple current rating of the capacitor must be at least 450 mArms. Table 7 includes a preferred list of capacitors by vendor.

9.2.3 Output Capacitor

The required output capacitance is determined by the output voltage of the TPS84620. See Table 5 for the amount of required capacitance. The required output capacitance can be comprised of either all ceramic capacitors, or a combination of ceramic and bulk capacitors. The required output capacitance must include at least 1x 47 µF ceramic capacitor. When adding additional non-ceramic bulk capacitors, low-ESR devices like the ones recommended in Table 7 are required. The required capacitance above the minimum is determined by actual transient deviation requirements. See Table 6 for typical transient response values for several output voltage, input voltage and capacitance combinations. Table 7 includes a preferred list of capacitors by vendor.

Table 5. Required Output Capacitance

V_{OUT} RANGE (V)		MINIMUM REQUIRED C_{OUT} (µF)
MIN	MAX	
1.2	< 3.0	200 (1)
3.0	< 4.0	100 (1)
4.0	5.5	47 µF ceramic

(1) Minimum required must include at least one 47 µF ceramic capacitor.

Table 6. Output Voltage Transient Response

C_{IN1} = 2 x 22 µF CERAMIC, C_{IN2} = 68 µF POSCAP, LOAD STEP = 3 A, 1 A/µs						
V_{OUT} (V)	PV_{IN} (V)	C_{OUT1} Ceramic	C_{OUT2} BULK	VOLTAGE DEVIATION (mV)	PEAK-PEAK (mV)	RECOVERY TIME (µs)
1.2	3.3	4x 47 µF	None	73	137	70
		1x 47 µF	330 µF	50	90	75
	5	4x 47 µF	None	63	117	70
		1x 47 µF	330 µF	45	85	75
	12	4x 47 µF	None	45	109	70
		1x 47 µF	330 µF	35	70	75
1.5	3.3	4x 47 µF	None	80	160	80
		1x 47 µF	220 µF	65	130	70
	5	4x 47 µF	None	60	115	80
		1x 47 µF	220 µF	60	120	70
	12	4x 47 µF	None	45	98	80
		1x 47 µF	220 µF	50	100	70
1.8	3.3	4x 47 µF	None	90	180	80
		1x 47 µF	220 µF	72	142	110
	5	4x 47 µF	None	80	160	80
		1x 47 µF	220 µF	67	132	110
	12	4x 47 µF	None	60	120	80
		1x 47 µF	220 µF	60	119	110
2.5	3.3	4x 47 µF	None	108	214	75
		1x 47 µF	100 µF	93	186	110
	5	4x 47 µF	None	100	200	75
		1x 47 µF	100 µF	92	180	110
	12	4x 47 µF	None	88	174	75
		1x 47 µF	100 µF	80	157	110
3.3	5	2x 47 µF	None	160	320	100
		1x 47 µF	100 µF	110	220	100
	12	2x 47 µF	None	140	280	100
		1x 47 µF	100 µF	100	200	100
5.0	5	1x 47 µF	None	200	400	100
		1x 47 µF	100 µF	150	300	130
	12	1x 47 µF	None	180	360	100
		1x 47 µF	100 µF	150	300	130

Table 7. Recommended Input/Output Capacitors(1)

VENDOR	SERIES	PART NUMBER	CAPACITOR CHARACTERISTICS		
			WORKING VOLTAGE (V)	CAPACITANCE (µF)	ESR (2) (mΩ)
Murata	X5R	GRM32ER61E226K	16	22	2
TDK	X5R	C3225X5R0J476K	6.3	47	2
Murata	X5R	GRM32ER60J476M	6.3	47	2
Sanyo	POSCAP	16TQC68M	16	68	50
Kemet	T520	T520V107M010ASE025	10	100	25
Sanyo	POSCAP	6TPE100MI	6.3	100	25
Sanyo	POSCAP	2R5TPE220M7	2.5	220	7
Kemet	T530	T530D227M006ATE006	6.3	220	6
Kemet	T530	T530D337M006ATE010	6.3	330	10
Sanyo	POSCAP	2TPF330M6	2.0	330	6
Sanyo	POSCAP	6TPE330MFL	6.3	330	15

(1) **Capacitor Supplier Verification**
Please verify availability of capacitors identified in this table.
RoHS, Lead-free and Material Details
Please consult capacitor suppliers regarding material composition, RoHS status, lead-free status, and manufacturing process requirements.
(2) Maximum ESR @ 100kHz, 25°C.

9.3 Transient Response

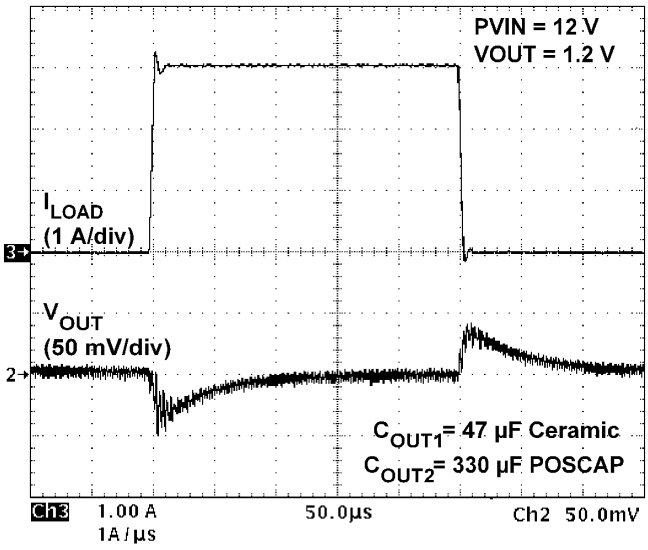


Figure 17. PVIN = 12V, VOUT = 1.2V, 3A Load Step

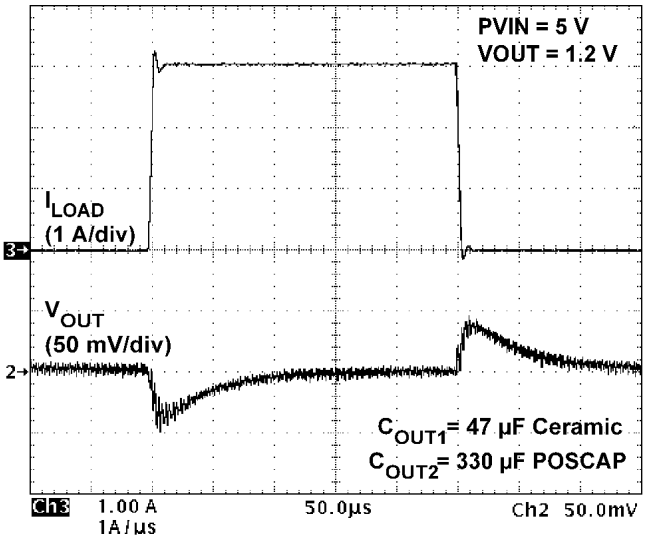


Figure 18. PVIN = 5V, VOUT = 1.2V, 3A Load Step

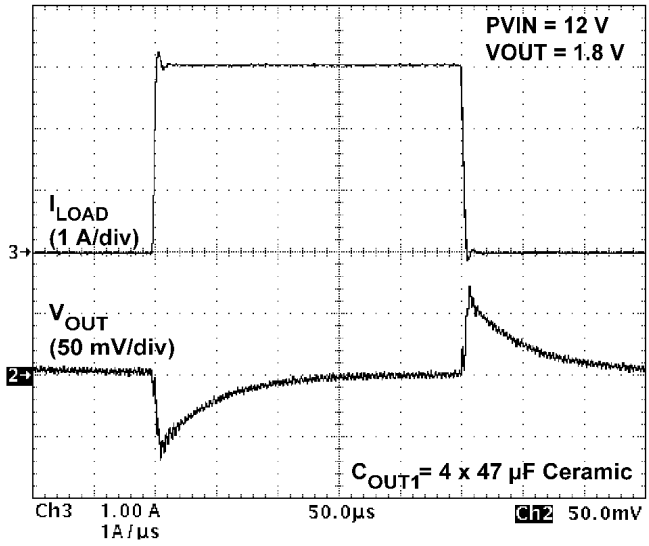


Figure 19. PVIN = 12V, VOUT = 1.8V, 3A Load Step

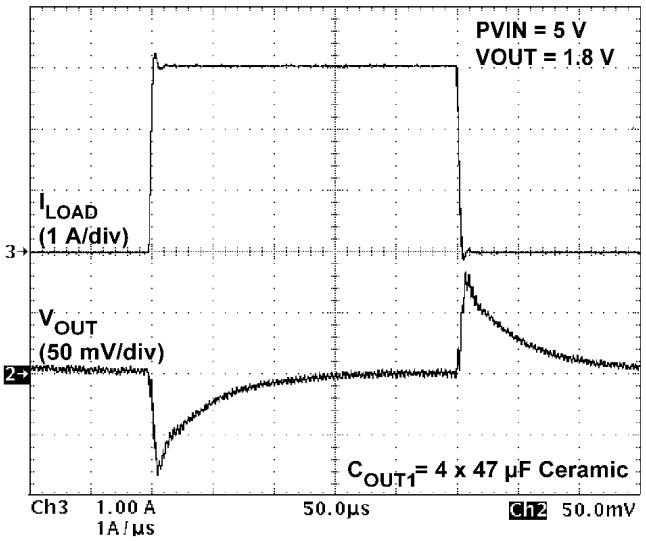


Figure 20. PVIN = 5V, VOUT = 1.8V, 3A Load Step

Transient Response (continued)

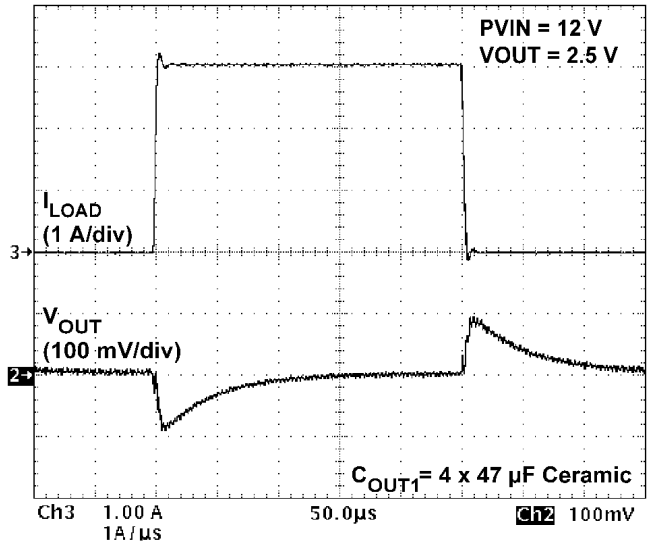


Figure 21. PVIN = 12V, VOUT = 2.5V, 3A Load Step

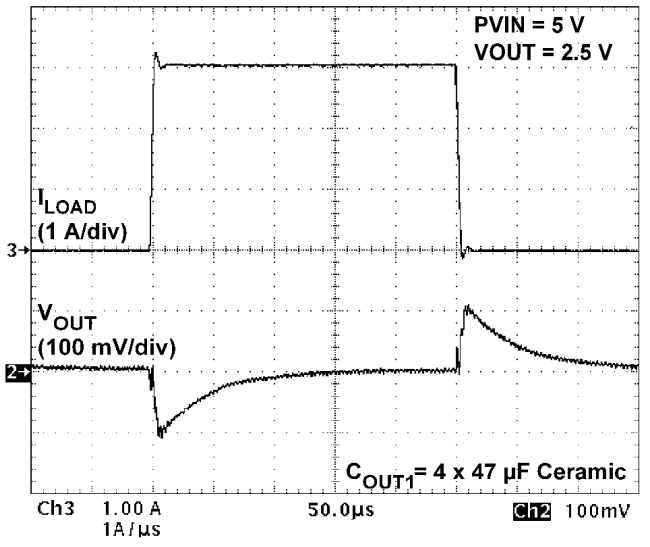


Figure 22. PVIN = 5V, VOUT = 2.5V, 3A Load Step

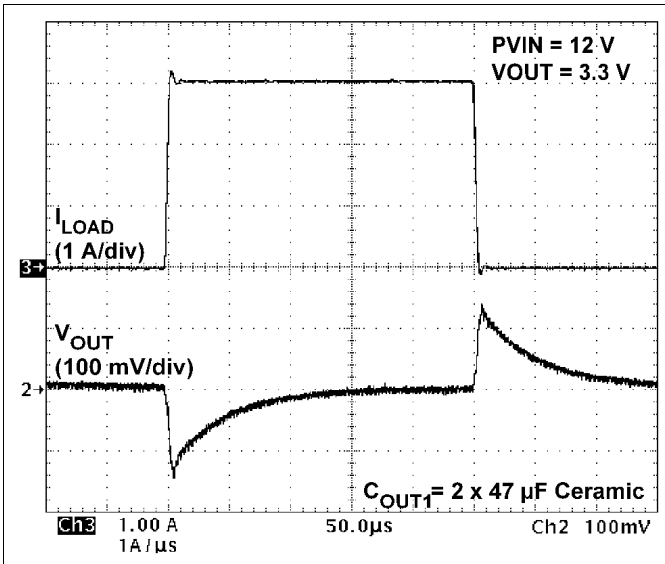


Figure 23. PVIN = 12V, VOUT = 3.3V, 3A Load Step

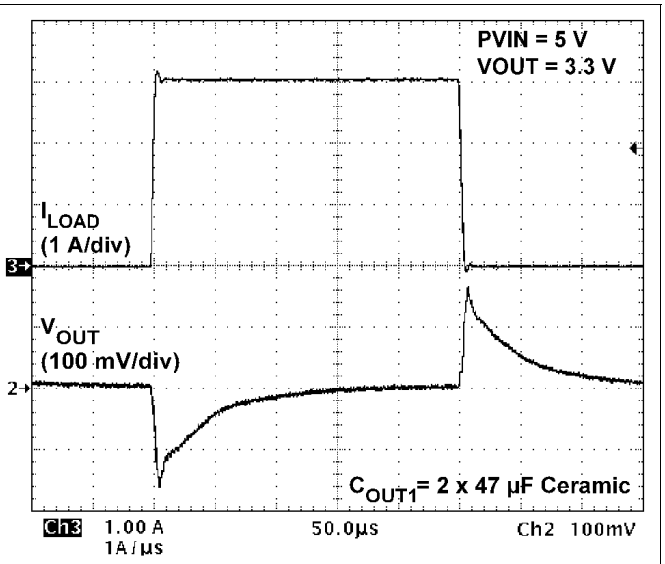


Figure 24. PVIN = 5V, VOUT = 3.3V, 3A Load Step

9.4 Application Schematics

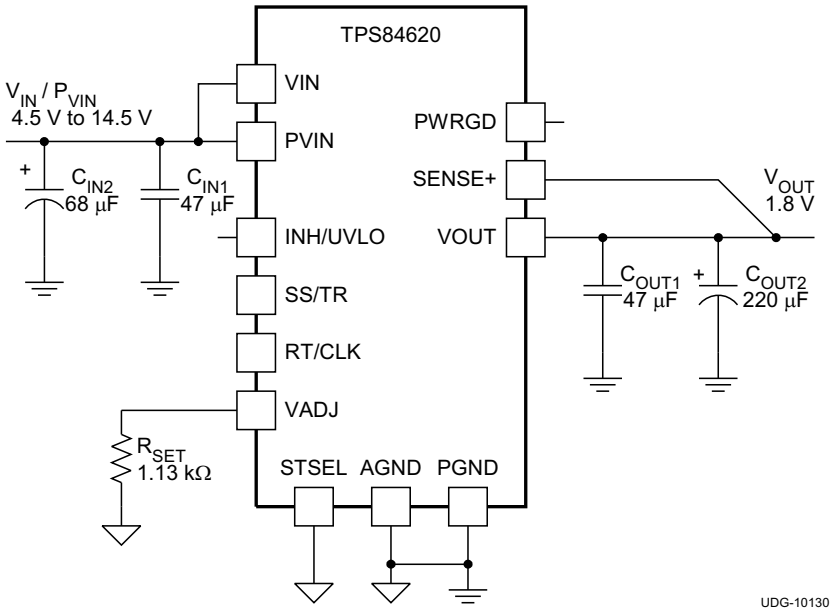


Figure 25. Typical Schematic
PVIN = VIN = 4.5 V to 14.5 V, VOUT = 1.8 V

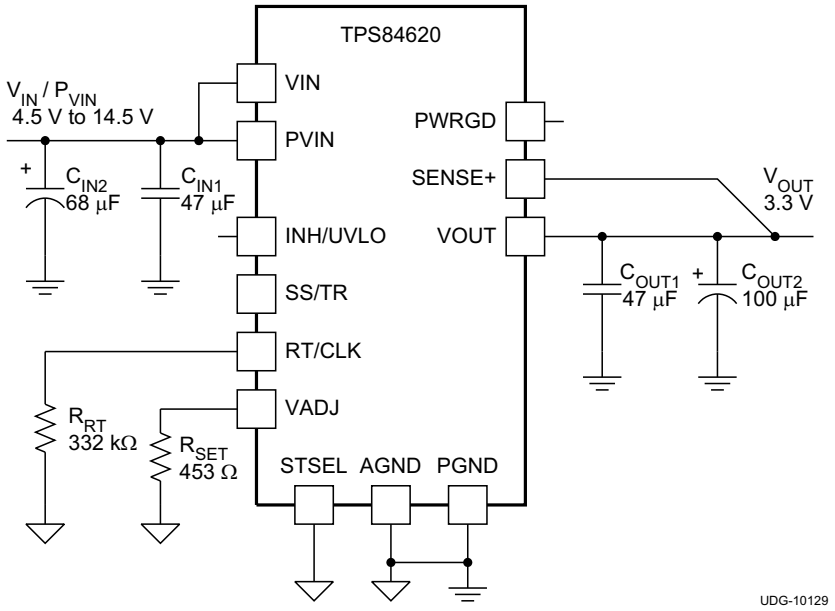


Figure 26. Typical Schematic
PVIN = VIN = 4.5 V to 14.5 V, VOUT = 3.3 V

Application Schematics (continued)

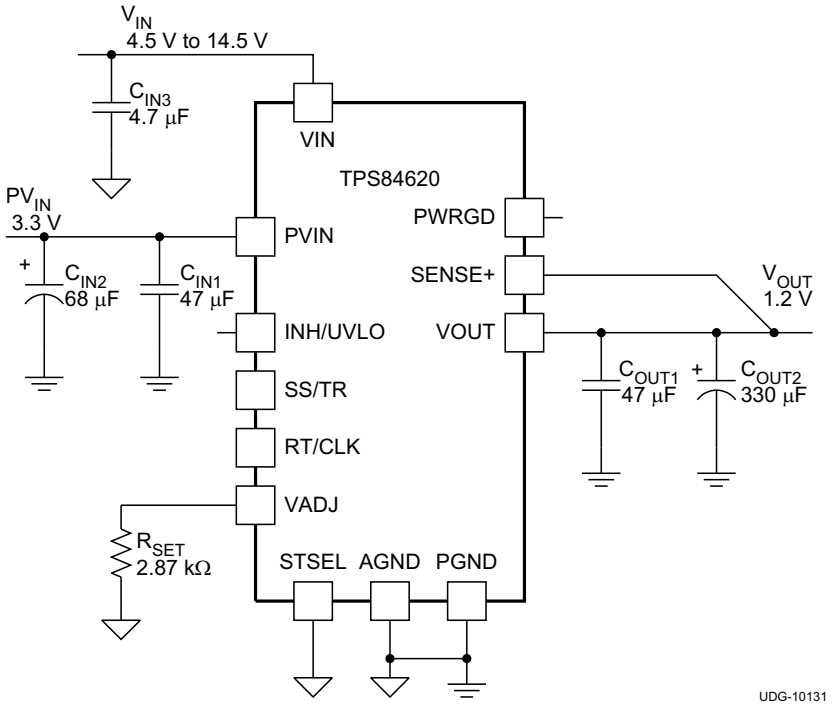


Figure 27. Typical Schematic
PVIN = 3.3 V, VIN = 4.5 V to 14.5 V, VOUT = 1.2 V

9.5 VIN and PVIN Input Voltage

The TPS84620 allows for a variety of applications by using the VIN and PVIN pins together or separately. The VIN voltage supplies the internal control circuits of the device. The PVIN voltage provides the input voltage to the power converter system.

If tied together, the input voltage for the VIN pin and the PVIN pin can range from 4.5 V to 14.5 V. If using the VIN pin separately from the PVIN pin, the VIN pin must be between 4.5 V and 14.5 V, and the PVIN pin can range from as low as 1.7 V to 14.5 V. A voltage divider connected to the INH/UVLO pin can adjust the either input voltage UVLO appropriately. See the Programmable Undervoltage Lockout (UVLO) section of this datasheet for more information.

9.6 Power Good (PWRGD)

The PWRGD pin is an open drain output. Once the voltage on the SENSE+ pin is between 94% and 106% of the set voltage, the PWRGD pin pull-down is released and the pin floats. The recommended pull-up resistor value is between 10 kΩ and 100 kΩ to a voltage source that is 5.5 V or less. The PWRGD pin is in a defined state once VIN is greater than 1.0 V, but with reduced current sinking capability. The PWRGD pin achieves full current sinking capability once the VIN pin is above 4.5V. The PWRGD pin is pulled low when the voltage on SENSE+ is lower than 91% or greater than 109% of the nominal set voltage. Also, the PWRGD pin is pulled low if the input UVLO or thermal shutdown is asserted, the INH pin is pulled low, or the SS/TR pin is below 1.4 V.

9.7 Power-Up Characteristics

When configured as shown in the front page schematic, the TPS84620 produces a regulated output voltage following the application of a valid input voltage. During the power-up, internal soft-start circuitry slows the rate that the output voltage rises, thereby limiting the amount of in-rush current that can be drawn from the input source. The soft-start circuitry introduces a short time delay from the point that a valid input voltage is recognized. Figure 28 shows the start-up waveforms for a TPS84620, operating from a 5-V input (PVIN=VIN) and with the output voltage adjusted to 1.8 V. Figure 29 shows the start-up waveforms for a TPS84620 starting up into a pre-biased output voltage. The waveforms were measured with a 3-A constant current load.

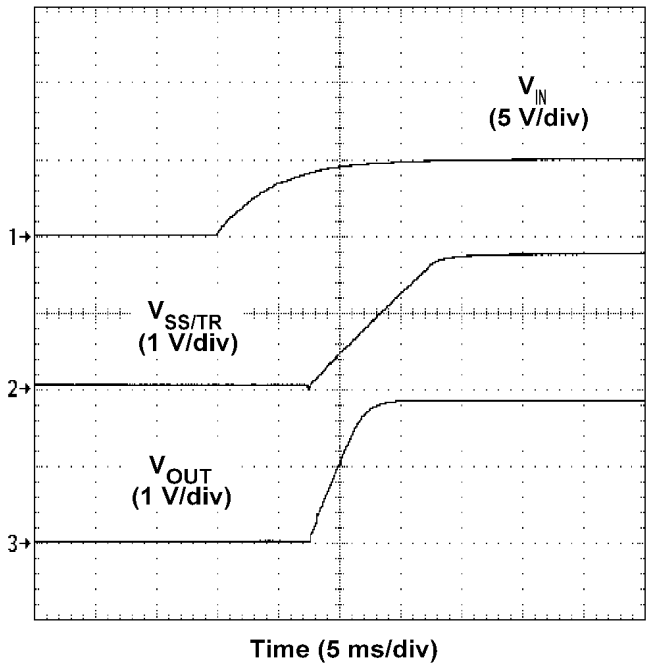


Figure 28. Start-Up Waveforms

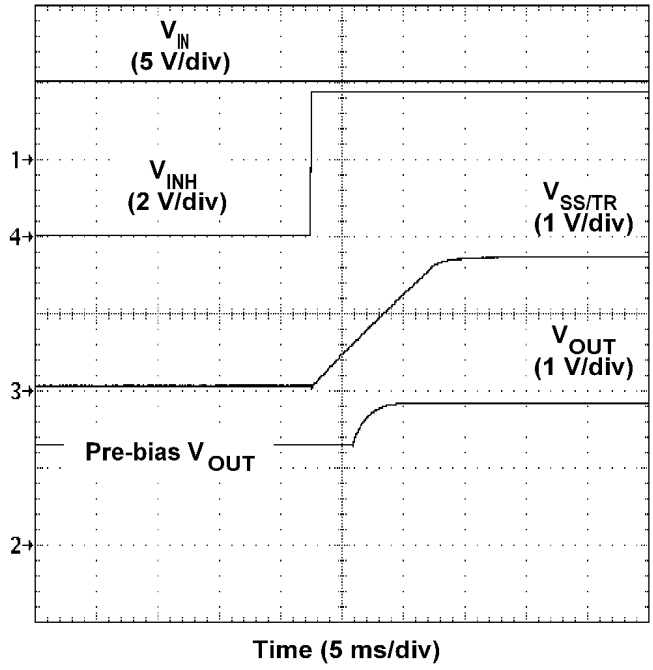


Figure 29. Start-up into Pre-bias

9.8 Pre-Biased Start-Up

The TPS84620 has been designed to prevent discharging a pre-biased output. During monotonic pre-biased startup, the TPS84620 does not allow current to sink until the SS/TR pin voltage is higher than 1.4 V.

9.9 Remote Sense

The SENSE+ pin must be connected to V_{OUT} at the load, or at the device pins.

Connecting the SENSE+ pin to V_{OUT} at the load improves the load regulation performance of the device by allowing it to compensate for any I-R voltage drop between its output pins and the load. An I-R drop is caused by the high output current flowing through the small amount of pin and trace resistance. This should be limited to a maximum of 300 mV.

NOTE

The remote sense feature is not designed to compensate for the forward drop of nonlinear or frequency dependent components that may be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the SENSE+ connection, they are effectively placed inside the regulation control loop, which can adversely affect the stability of the regulator.

9.10 Output On/Off Inhibit (INH)

The INH pin provides electrical on/off control of the device. Once the INH pin voltage exceeds the threshold voltage, the device starts operation. If the INH pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low quiescent current state.

The INH pin has an internal pull-up current source, allowing the user to float the INH pin for enabling the device. If an application requires controlling the INH pin, use an open drain/collector device, or a suitable logic gate to interface with the pin.

Figure 30 shows the typical application of the inhibit function. The Inhibit control has its own internal pull-up to VIN potential. An open-collector or open-drain device is recommended to control this input.

Turning Q1 on applies a low voltage to the inhibit control (INH) pin and disables the output of the supply, shown in Figure 31. If Q1 is turned off, the supply executes a soft-start power-up sequence, as shown in Figure 32. A regulated output voltage is produced within 10 ms. The waveforms were measured with a 3-A constant current load.

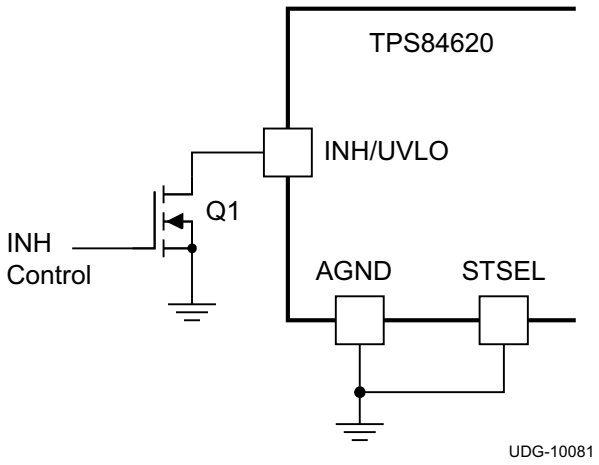


Figure 30. Typical Inhibit Control

Output On/Off Inhibit (INH) (continued)

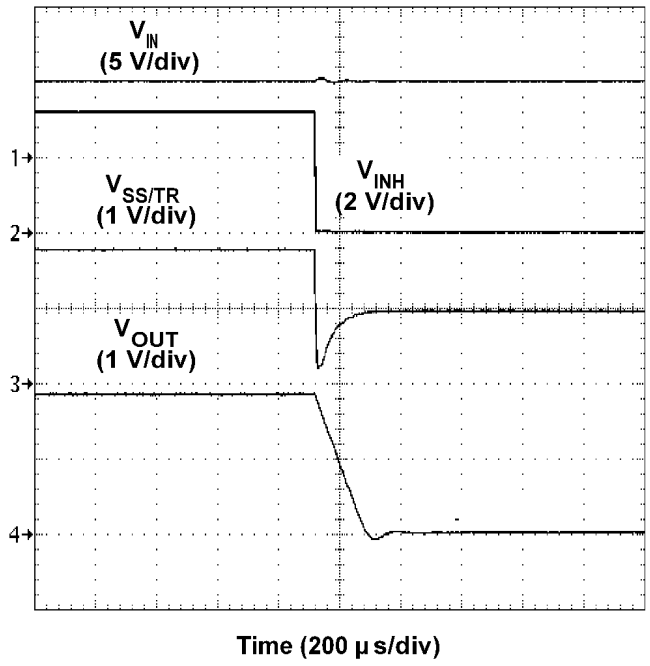


Figure 31. Inhibit Turn-Off

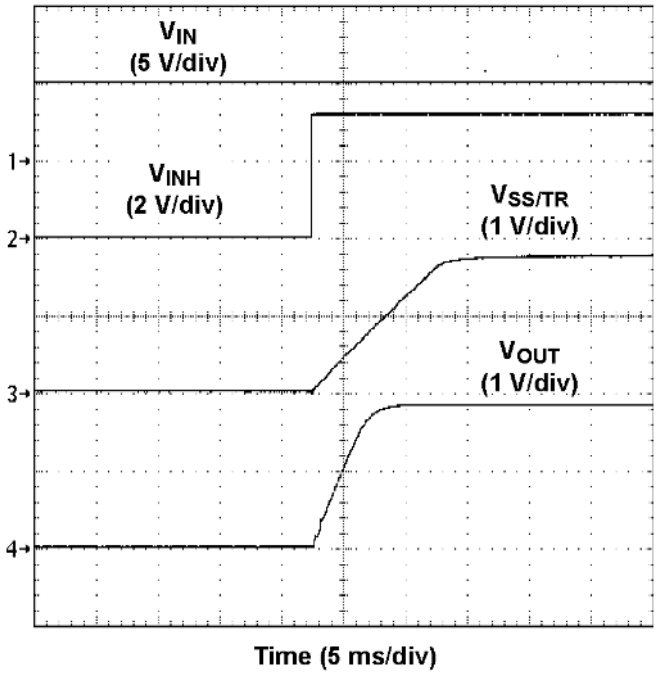


Figure 32. Inhibit Turn-On

9.11 Slow Start (SS/TR)

Connecting the STSEL pin to AGND and leaving SS/TR pin open enables the internal SS capacitor with a slow start interval of approximately 1.1 ms. Adding additional capacitance between the SS pin and AGND increases the slow start time. Table 8 shows an additional SS capacitor connected to the SS/TR pin and the STSEL pin connected to AGND. See Table 8 below for SS capacitor values and timing interval.

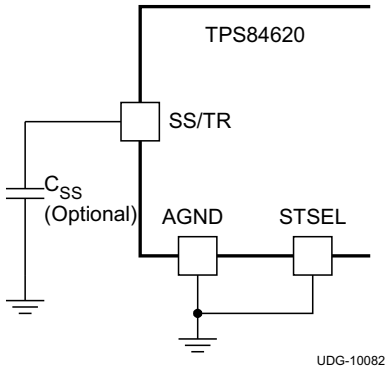


Figure 33. Slow-Start Capacitor (C_{SS}) and STSEL Connection

Table 8. Slow-Start Capacitor Values and Slow-Start Time

C_{SS} (pF)	open	2200	4700	10000	15000	22000	25000
SS Time (msec)	1.1	1.9	2.8	4.6	6.4	8.8	9.8

9.12 Overcurrent Protection

For protection against load faults, the TPS84620 uses current limiting. The device is protected from overcurrent conditions by cycle-by-cycle current limiting. During an overcurrent condition the output current is limited and the output voltage is reduced, as shown in Figure 34. When the overcurrent condition is removed, the output voltage returns to the established voltage, as shown in Figure 35.

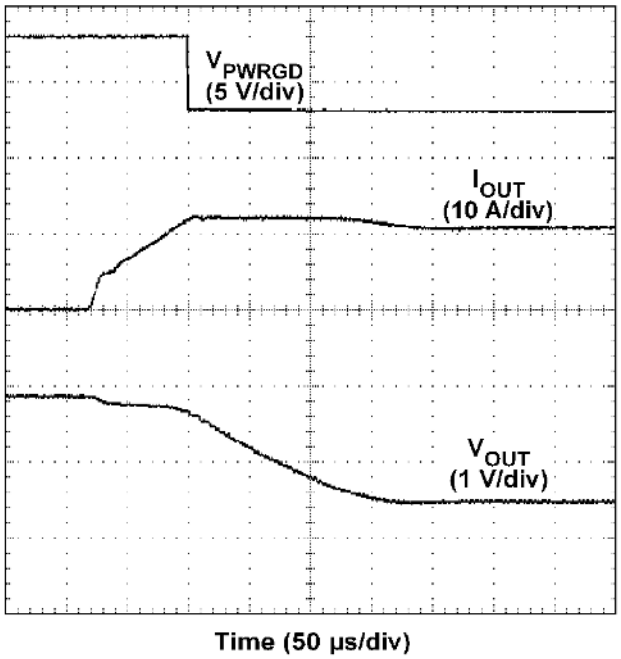


Figure 34. Overcurrent Limiting

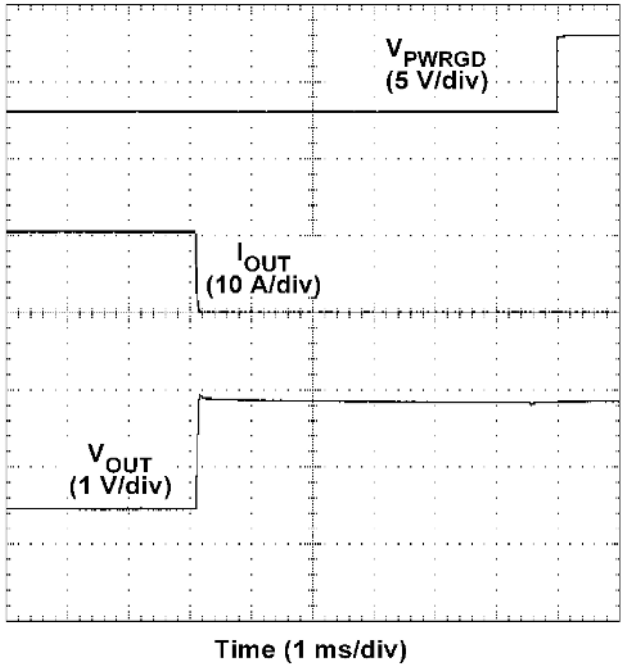


Figure 35. Removal of Overcurrent Condition

9.13 Synchronization (CLK)

An internal phase locked loop (PLL) has been implemented to allow synchronization between 480 kHz and 780 kHz, and to easily switch from RT mode to CLK mode. To implement the synchronization feature, connect a square wave clock signal to the RT/CLK pin with a duty cycle between 20% to 80%. The clock signal amplitude must transition lower than 0.8 V and higher than 2.0 V. The start of the switching cycle is synchronized to the falling edge of RT/CLK pin. In applications where both RT mode and CLK mode are needed, the device can be configured as shown in .

Before the external clock is present, the device works in RT mode and the switching frequency is set by RT resistor. When the external clock is present, the CLK mode overrides the RT mode. The first time the CLK pin is pulled above the RT/CLK high threshold (2.0 V), the device switches from RT mode to th CLK mode and the RT/CLK pin becomes high impedance as the PLL starts to lock onto the frequency of the external clock. It is not recommended to switch from CLK mode back to RT mode because the internal switching frequency drops to 100 kHz first before returning to the switching frequency set by the RT resistor (R_{RT}).

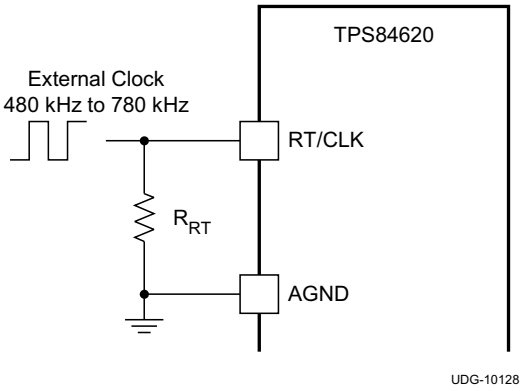


Figure 36. CLK/RT Configuration

The synchronization frequency must be selected based on the output voltages of the devices being synchronized. Table 9 shows the allowable frequencies for a given range of output voltages. For the most efficient solution, always synchronize to the lowest allowable frequency. For example, an application requires synchronizing three TPS84620 devices with output voltages of 1.2 V, 1.8 V and 2. 5 V, all powered from PVIN = 12 V. Table 9 shows that all three output voltages can be synchronized to either 530 kHz, 580 kHz, or 630 kHz. For best efficiency, choose 530 kHz as the sychronization frequency.

Table 9. Synchronization Frequency vs Output Voltage

SYNCHRONIZATION FREQUENCY (kHz)	R_{RT} (kΩ)	PVIN = 12 V		PVIN = 5 V	
		V_{OUT} RANGE (V)		V_{OUT} RANGE (V)	
		MIN	MAX	MIN	MAX
480	OPEN	1.2	2.5	1.2	4.5
530	1000	1.2	2.9		
580	499	1.2	3.2		
630	332	1.2	3.7		
680	249	1.3	4.1		
730	196	1.4	4.7		
780	165	1.5	5.5		

9.14 Sequencing (SS/TR)

Many of the common power supply sequencing methods can be implemented using the SS/TR, INH and PWRGD pins. The sequential method is illustrated in Figure 37 using two TPS84620 devices. The PWRGD pin of the first device is coupled to the INH pin of the second device which enables the second power supply once the primary supply reaches regulation. Figure 38 shows sequential turn-on waveforms of two TPS84620 devices.

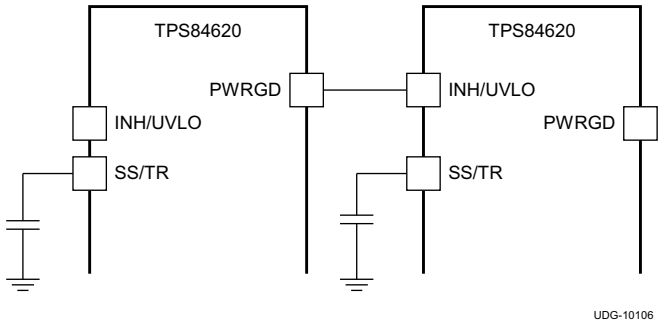


Figure 37. Sequencing Schematic

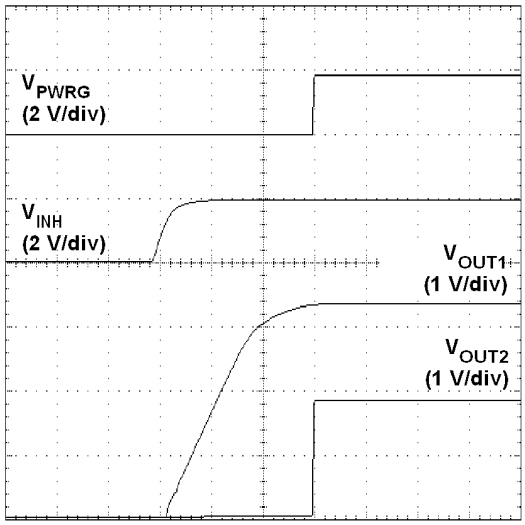


Figure 38. Sequencing Waveforms

Simultaneous power supply sequencing can be implemented by connecting the resistor network of R1 and R2 shown in Figure 39 to the output of the power supply that needs to be tracked or to another voltage reference source. Figure 40 shows simultaneous turn-on waveforms of two TPS84620 devices. Use Equation 2 and Equation 3 to calculate the values of R1 and R2.

$$R1 = \frac{(V_{OUT2} \times 12.6)}{0.8} (k\Omega) \quad (2)$$

$$R2 = \frac{0.8 \times R1}{(V_{OUT2} - 0.8)} (k\Omega) \quad (3)$$

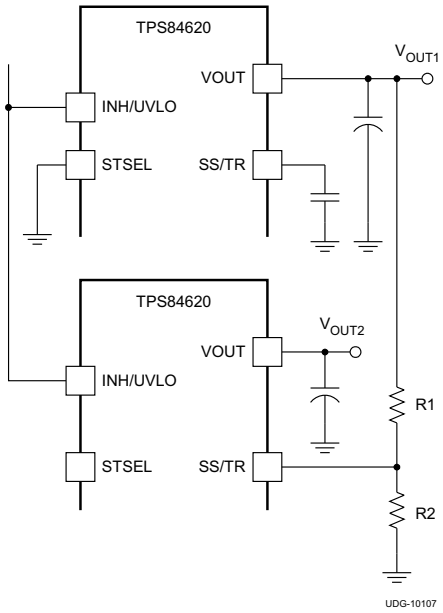


Figure 39. Simultaneous Tracking Schematic

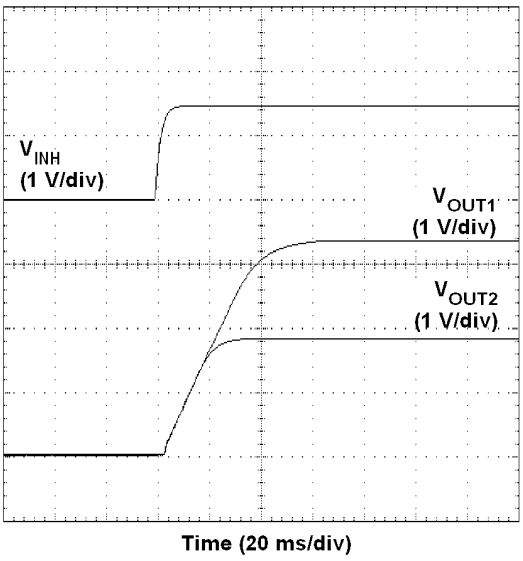


Figure 40. Simultaneous Tracking Waveforms

9.15 Programmable Undervoltage Lockout (UVLO)

The TPS84620 implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO rising threshold is 4.5 V(max) with a typical hysteresis of 150 mV.

If an application requires either a higher UVLO threshold on the VIN pin or a higher UVLO threshold for a combined VIN and PVIN, then the UVLO pin can be configured as shown in Figure 41 or Figure 42. Table 10 lists standard values for R_{UVLO1} and R_{UVLO2} to adjust the VIN UVLO voltage up.

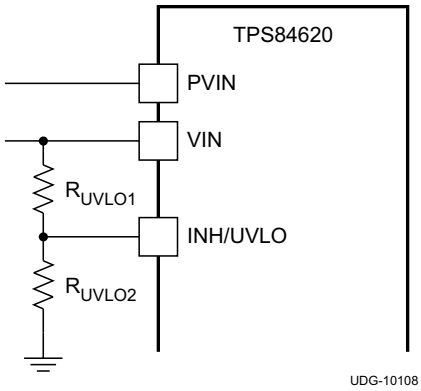


Figure 41. Adjustable VIN UVLO

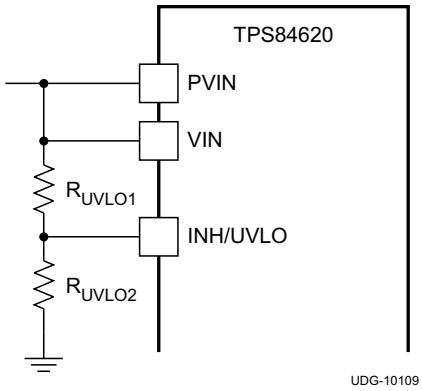


Figure 42. Adjustable VIN and PVIN Undervoltage Lockout

Table 10. Standard Resistor values for Adjusting VIN UVLO

VIN UVLO (V)	5.0	5.5	6.0	6.5	7.0	7.5	8.0	8.5	9.0	9.5	10.0
R_{UVLO1} (kΩ)	68.1	68.1	68.1	68.1	68.1	68.1	68.1	68.1	68.1	68.1	68.1
R_{UVLO2} (kΩ)	21.5	18.7	16.9	15.4	14.0	13.0	12.1	11.3	10.5	9.76	9.31
Hysteresis (V)	400	415	430	450	465	480	500	515	530	550	565

For a split rail application, if a secondary UVLO on PVIN is required, VIN must be ≥ 4.5V. Figure 43 shows the PVIN UVLO configuration. Use Table 11 to select R_{UVLO1} and R_{UVLO2} for PVIN. If PVIN UVLO is set for less than 3.0 V, a 5.1-V zener diode should be added to clamp the voltage on the UVLO pin below 6 V.

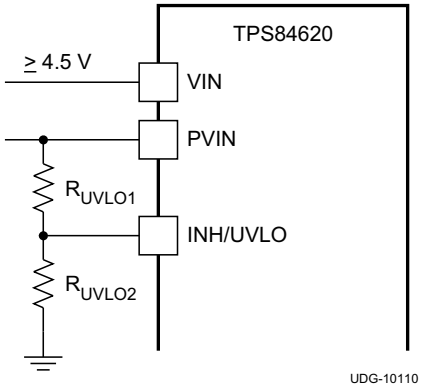


Figure 43. Adjustable PVIN Undervoltage Lockout, (VIN ≥4.5 V)

Table 11. Standard Resistor Values for Adjusting PVIN UVLO, (VIN ≥4.5 V)

PVIN UVLO (V)	2.0	2.5	3.0	3.5	4.0	4.5	
R_{UVLO1} (kΩ)	68.1	68.1	68.1	68.1	68.1	68.1	For higher PVIN UVLO voltages see Table UV for resistor values
R_{UVLO2} (kΩ)	95.3	60.4	44.2	34.8	28.7	24.3	
Hysteresis (V)	300	315	335	350	365	385	

9.16 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 175°C typically. The device reinitiates the power up sequence when the junction temperature drops below 165°C typically.

9.17 Layout Considerations

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. Figure 44, shows a typical PCB layout. Some considerations for an optimized layout are:

- Use large copper areas for power planes (VIN, VOUT, and PGND) to minimize conduction loss and thermal stress.
- Place ceramic input and output capacitors close to the device pins to minimize high frequency noise.
- Locate additional output capacitors between the ceramic capacitor and the load.
- Place a dedicated AGND copper area beneath the TPS84620.
- Isolate the PH copper area from the VOUT copper area using the AGND copper area.
- Connect the AGND and PGND copper area at one point; near the output capacitors.
- Place R_{SET}, R_{RT}, and C_{SS} as close as possible to their respective pins.
- Use multiple vias to connect the power planes to internal layers.

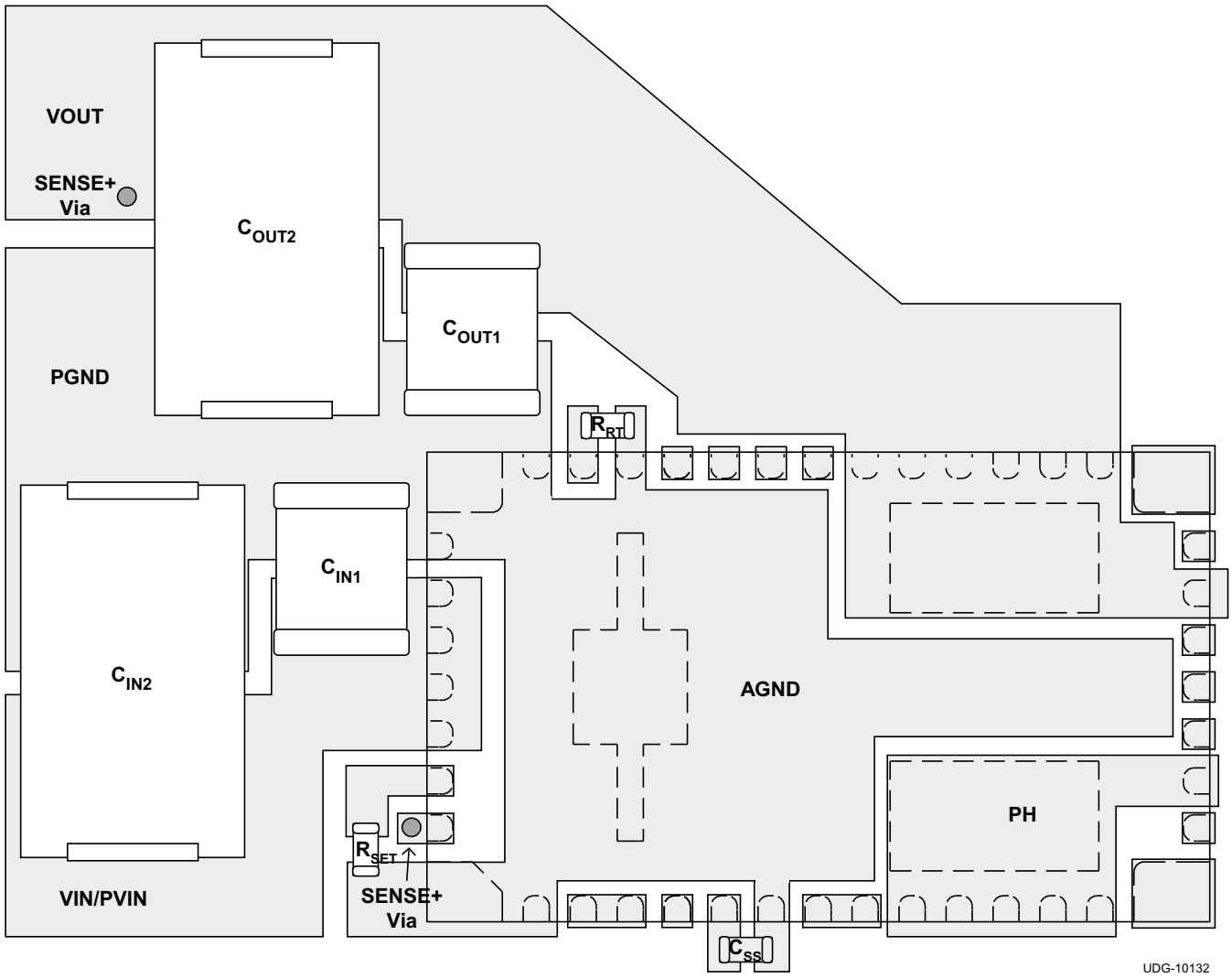


Figure 44. Typical Recommended Layout

9.18 EMI

The TPS84620 is compliant with EN55022 Class B radiated emissions. Figure 45 and Figure 46 show typical examples of radiated emissions plots for the TPS84620 operating from 5V and 12V respectively. Both graphs include the plots of the antenna in the horizontal and vertical positions.

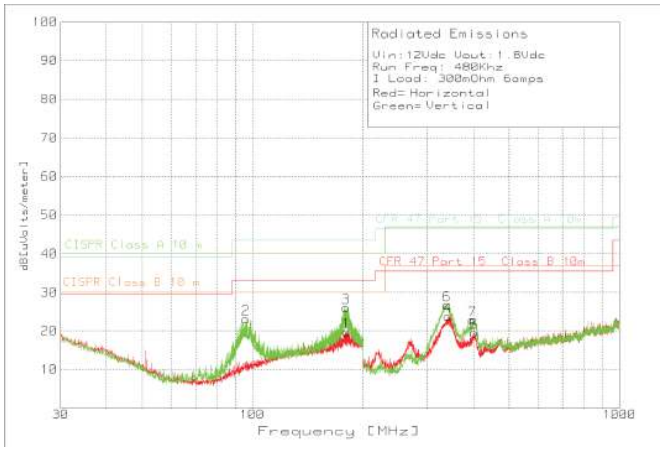


Figure 45. Radiated Emissions 5-V Input, 1.8-V Output, 6-A Load (EN55022 Class B)

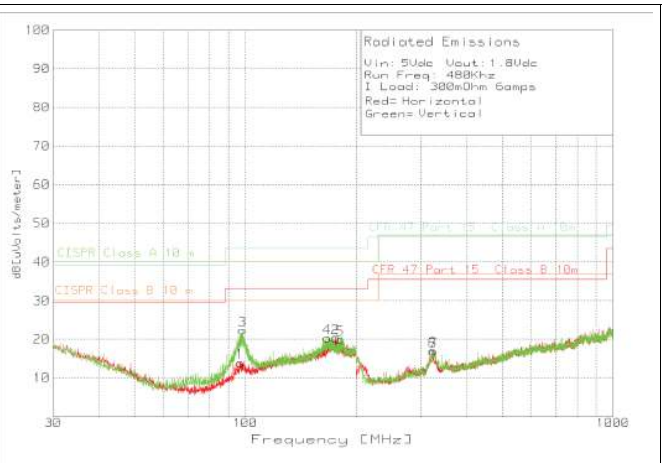


Figure 46. Radiated Emissions 12-V Input, 1.8-V Output, 6-A Load (EN55022 Class B)

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (June 2017) to Revision F **Page**

- Increased the peak reflow temperature and maximum number of reflows to JEDEC specification for improved manufacturability. 2

Changes from Revision D (June 2012) to Revision E **Page**

- Added peak reflow and maximum number of reflows information 2

Changes from Revision C (SEPTEMBER 2011) to Revision D **Page**

- Added correct pin names..... 8

Changes from Revision B (APRIL 2011) to Revision C **Page**

- Changed footnote (3) from "A small low-leakage (<100 nA) MOSFET is recommended for control." to "A small low-leakage (<300 nA) MOSFET is recommended for control. "..... 4
- Added clarity to PH pin description 7
- Added clarity to package title..... 8

Changes from Revision A (January 2011) to Revision B **Page**

- Added θ_{JCbot} in THERMAL INFORMATION 3
- Changed updated footnote text reagarding internal pulllup of INH/UVLO pin..... 4
- Added updated more specific values in Table 9 24

Changes from Original (October 2010) to Revision A **Page**

- Changed EN maximum voltage value from 3 V to 6 V..... 2
- Changed (corrected) resistor label from R_{RT} to R_{SET} on schematic 18
- Changed (corrected) minor typographical error on schematic 19
- Changed (corrected) typographical error..... 19
- Changed (corrected) time axis division units label from 5 µs/div to 5 ms/div in Inhibit Turn-On waveform..... 22

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

SwitcherPro, E2E are trademarks of Texas Instruments.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

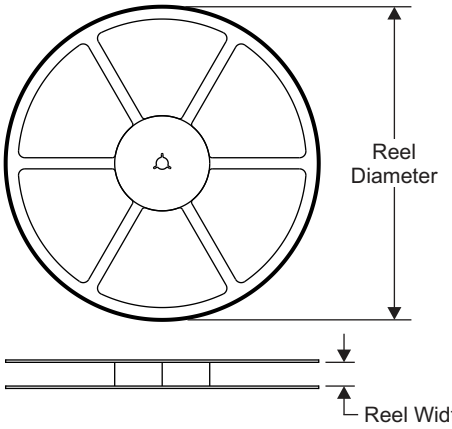
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

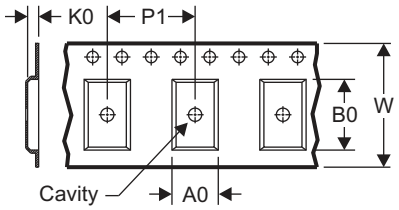
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Tape and Reel Information

REEL DIMENSIONS

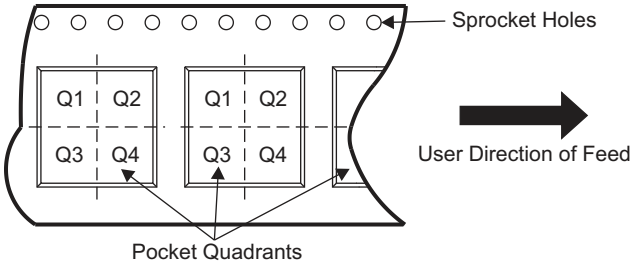


TAPE DIMENSIONS



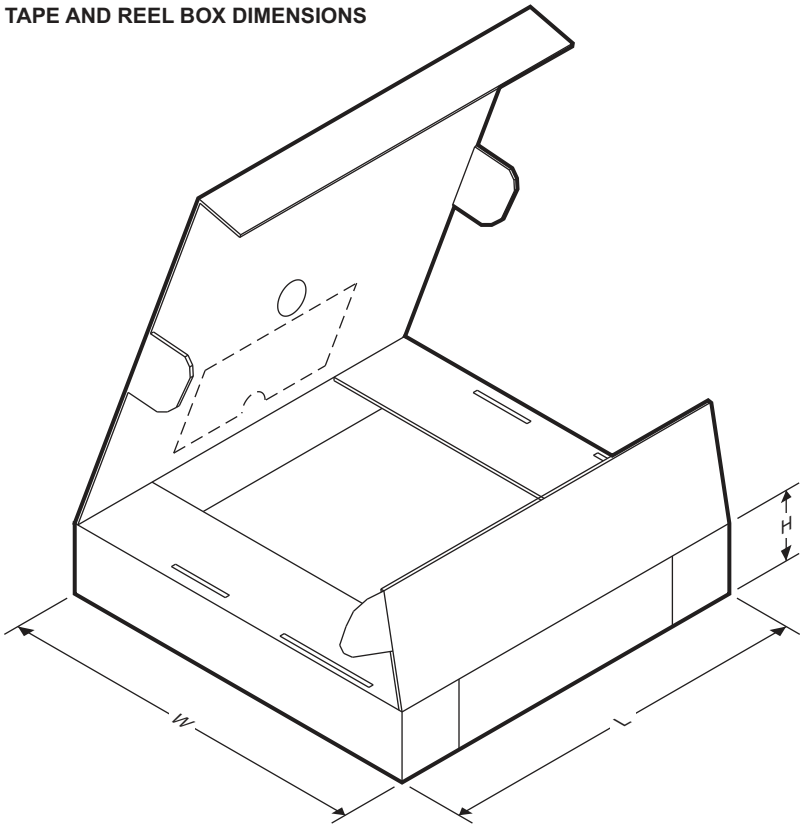
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS84620RUQR	B1QFN	RUQ	47	500	330.0	24.4	9.35	15.35	3.1	16.0	24.0	Q1
TPS84620RUQT	B1QFN	RUQ	47	250	330.0	24.4	9.35	15.35	3.1	16.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS84620RUQR	B1QFN	RUQ	47	500	383.0	353.0	58.0
TPS84620RUQT	B1QFN	RUQ	47	250	383.0	353.0	58.0

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS84620RUQR	ACTIVE	B1QFN	RUQ	47	500	RoHS Exempt & Green	NIPDAU	Level-3-245C-168 HR	-40 to 85	TPS84620	Samples
TPS84620RUQT	ACTIVE	B1QFN	RUQ	47	250	RoHS Exempt & Green	NIPDAU	Level-3-245C-168 HR	-40 to 85	TPS84620	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

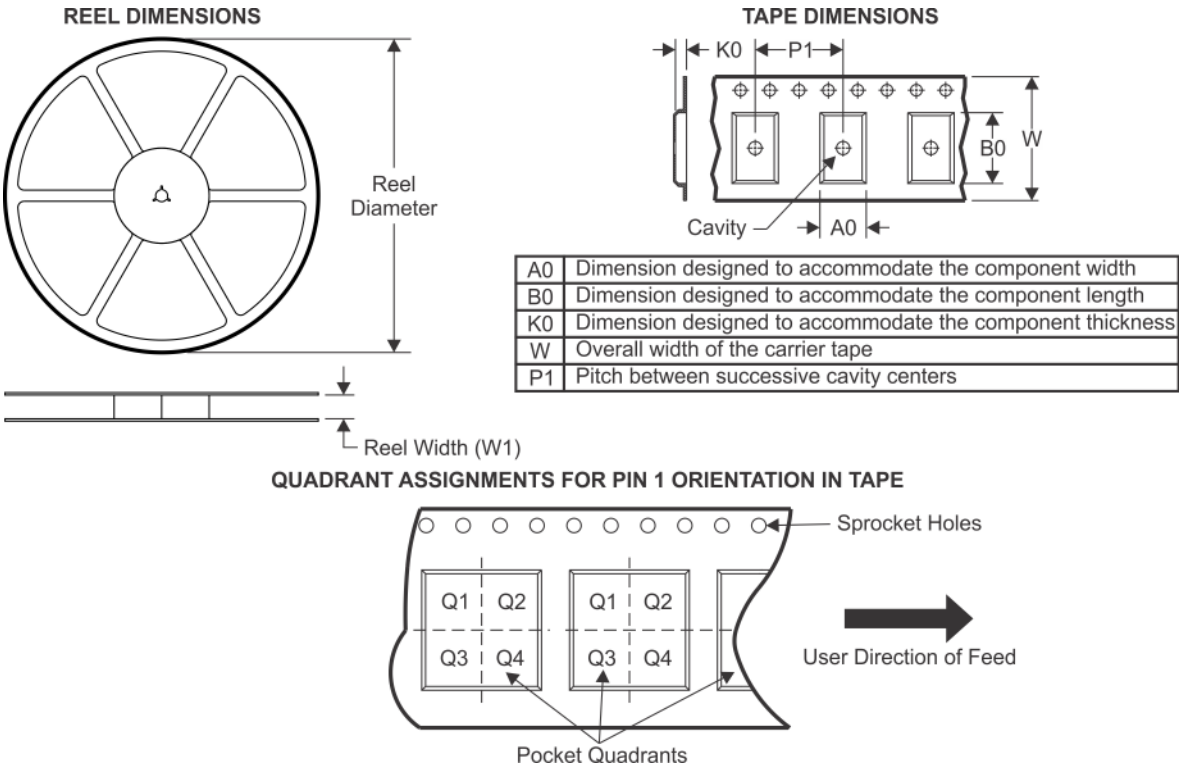
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

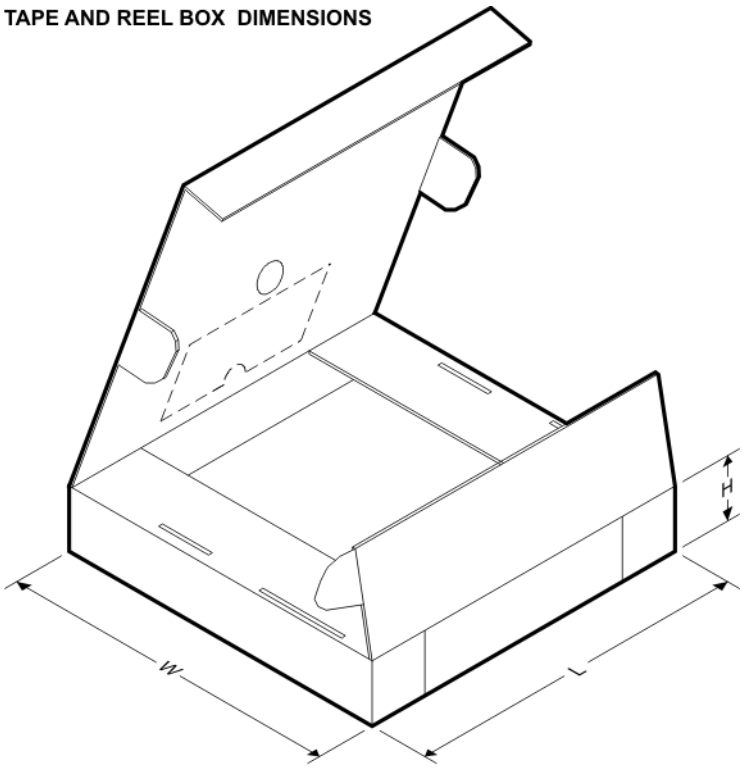


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS84620RUQR	B1QFN	RUQ	47	500	330.0	24.4	9.35	15.35	3.1	16.0	24.0	Q1
TPS84620RUQT	B1QFN	RUQ	47	250	330.0	24.4	9.35	15.35	3.1	16.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

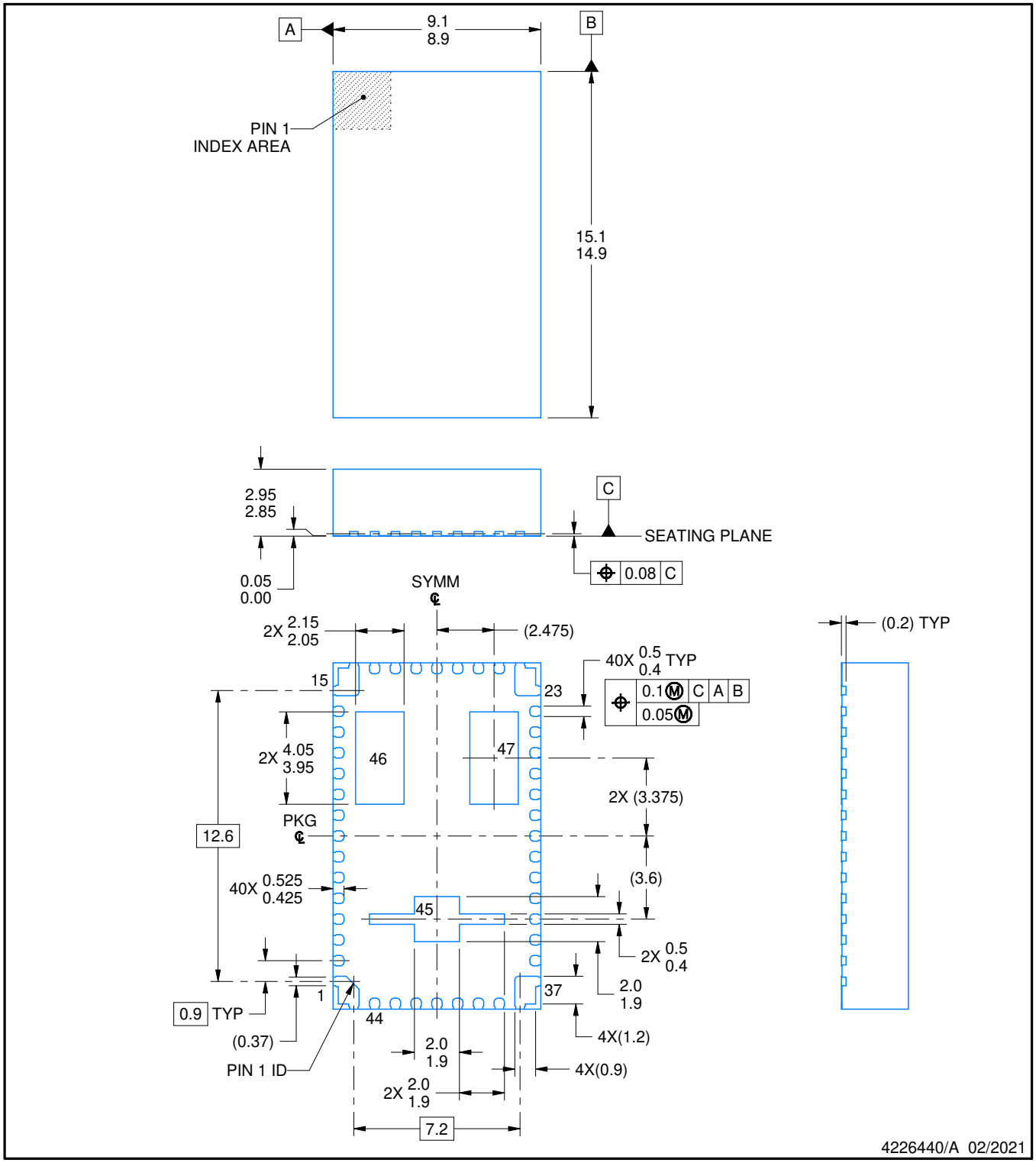
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS84620RUQR	B1QFN	RUQ	47	500	383.0	353.0	58.0
TPS84620RUQT	B1QFN	RUQ	47	250	383.0	353.0	58.0

PACKAGE OUTLINE

RUQ0047A

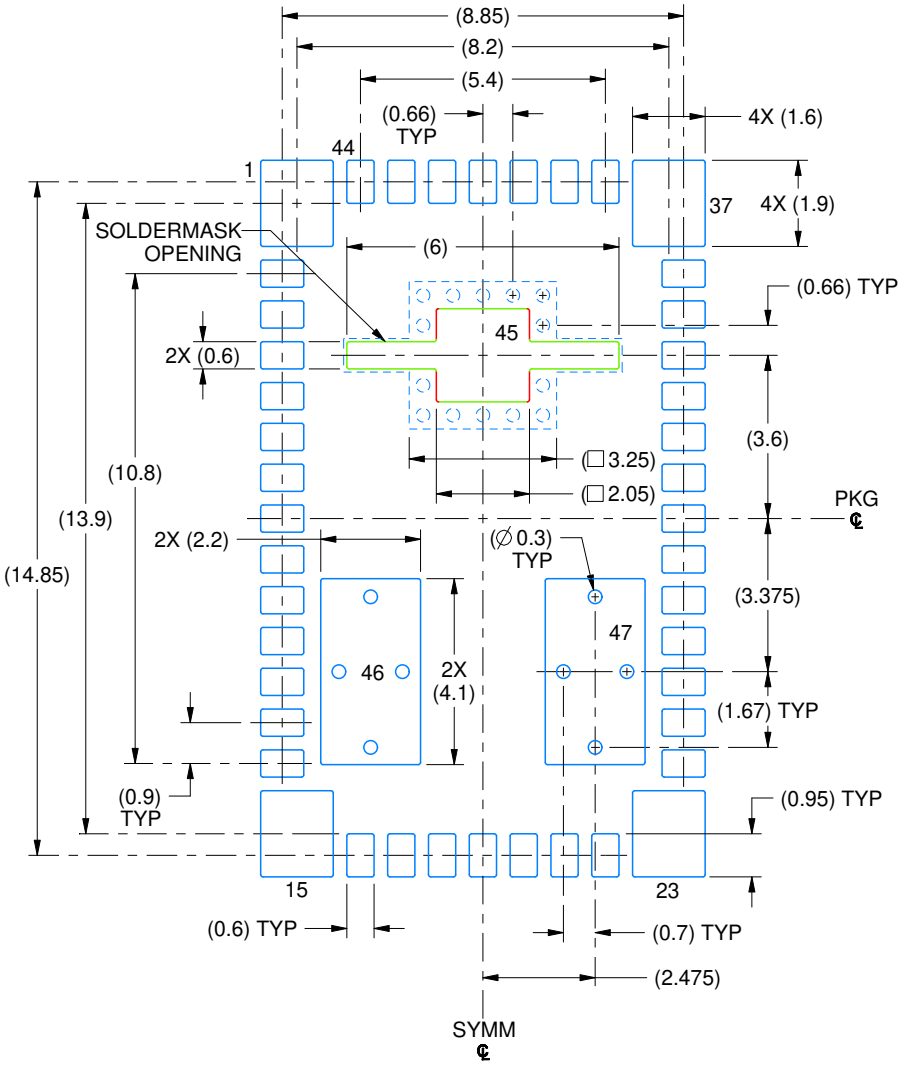
B1QFN - 2.95 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

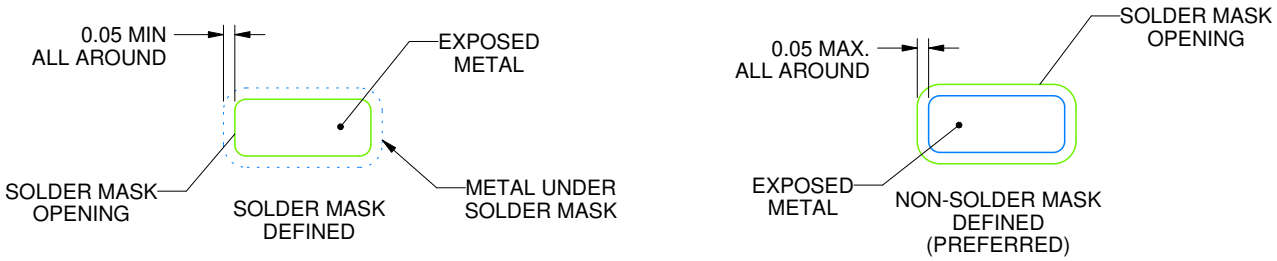


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

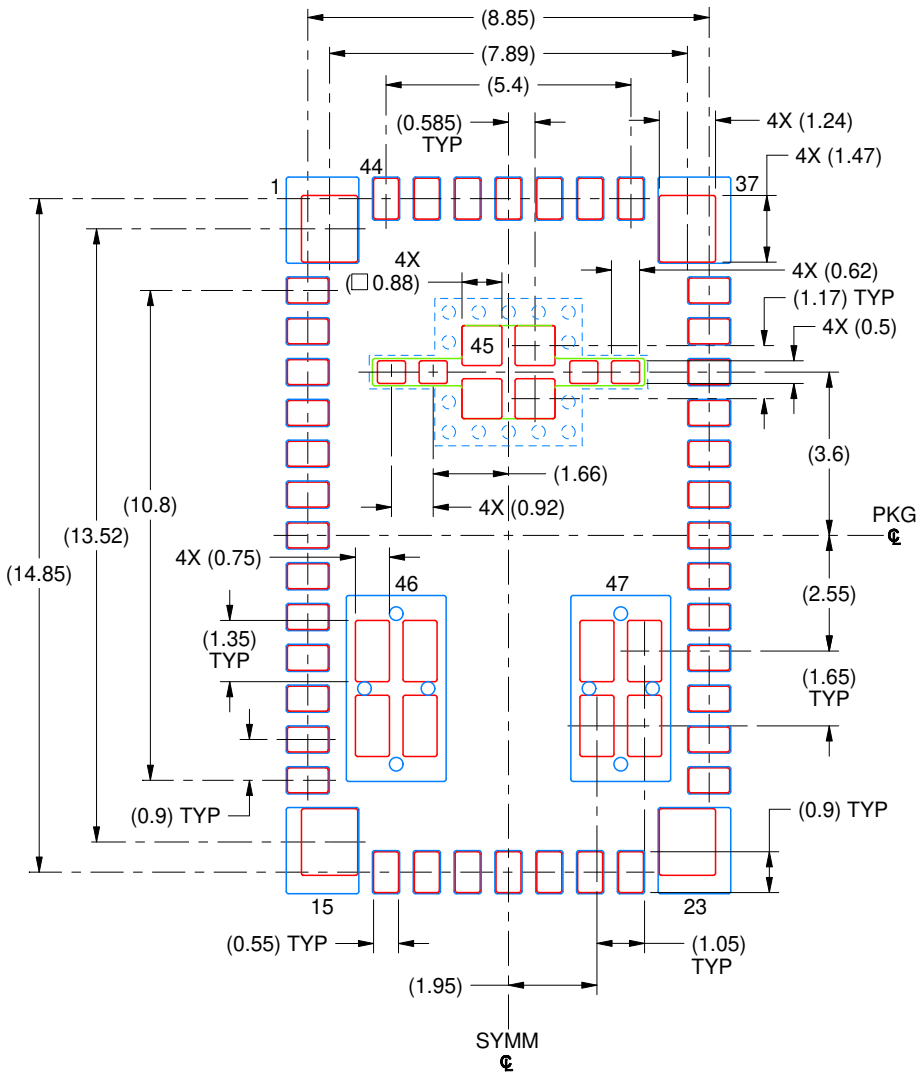


SOLDER MASK DETAIL

4226440/A 02/2021

NOTES: (continued)

4. This package designed to be soldered to a thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm STENCIL THICKNESS

CORNER PINS 1, 15, 23 & 37:
60% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

EXPOSED PAD 45:
66% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

EXPOSED PAD 46 & 47:
45% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:6X

4226440/A 02/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (https:www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265