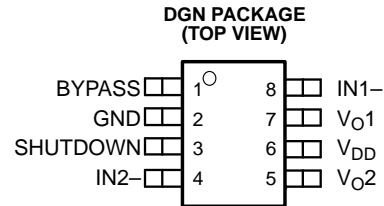




## 150-mW STEREO AUDIO POWER AMPLIFIER

### FEATURES

- 150 mW Stereo Output
- PC Power Supply Compatible
  - Fully Specified for 3.3 V and 5 V Operation
  - Operation to 2.5 V
- Pop Reduction Circuitry
- Internal Mid-Rail Generation
- Thermal and Short-Circuit Protection
- Surface-Mount Packaging
  - PowerPAD™ MSOP
- Pin Compatible With LM4881

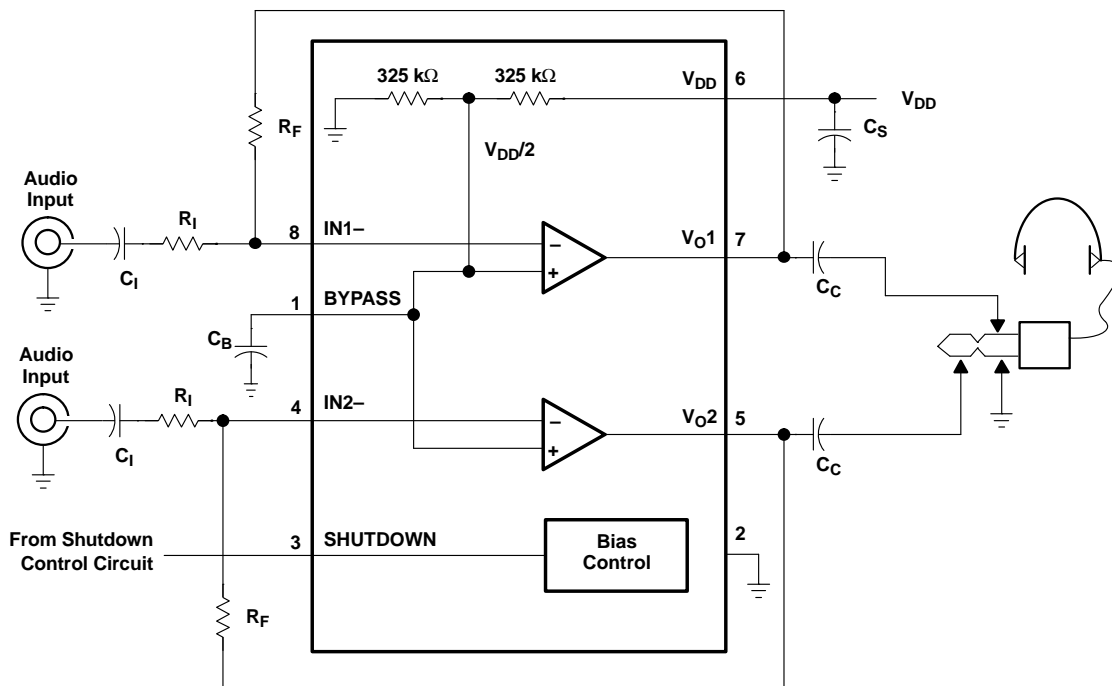


### DESCRIPTION

The TPA102 is a stereo audio power amplifier packaged in an 8-pin PowerPAD™ MSOP package capable of delivering 150 mW of continuous RMS power per channel into 8-Ω loads. Amplifier gain is externally configured by means of two resistors per input channel and does not require external compensation for settings of 1 to 10.

THD+N when driving an 8-Ω load from 5 V is 0.1% at 1 kHz, and less than 2% across the audio band of 20 Hz to 20 kHz. For 32-Ω loads, the THD+N is reduced to less than 0.06% at 1 kHz, and is less than 1% across the audio band of 20 Hz to 20 kHz. For 10-kΩ loads, the THD+N performance is 0.01% at 1 kHz, and less than 0.02% across the audio band of 20 Hz to 20 kHz.

### TYPICAL APPLICATION CIRCUIT



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**AVAILABLE OPTIONS**

T <sub>A</sub>	PACKAGED DEVICE	MSOP Symbolization
	MSOP <sup>(1)</sup>	
-40°C to 85°C	TPA102DGN	TI AAC

(1) The DGN package is available in left-ended tape and reel only (e.g., TPA102DGNR).

**Terminal Functions**

TERMINAL NAME	NO.	I/O	DESCRIPTION
BYPASS	1	I	Tap to voltage divider for internal mid-supply bias supply. Connect to a 0.1 μF to 1 μF low ESR capacitor for best performance.
GND	2	I	GND is the ground connection.
IN1-	8	I	IN1- is the inverting input for channel 1.
IN2-	4	I	IN2- is the inverting input for channel 2.
SHUTDOWN	3	I	Puts the device in a low quiescent current mode when held high.
V <sub>DD</sub>	6	I	V <sub>DD</sub> is the supply voltage terminal.
V <sub>O1</sub>	7	O	V <sub>O1</sub> is the audio output for channel 1.
V <sub>O2</sub>	5	O	V <sub>O2</sub> is the audio output for channel 2.
Thermal Pad			

**ABSOLUTE MAXIMUM RATINGS**

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		UNIT
V <sub>DD</sub>	Supply voltage	6 V
V <sub>I</sub>	Input voltage	-0.3 V to V <sub>DD</sub> + 0.3 V
	Continuous total power dissipation	Internally limited
T <sub>J</sub>	Operating junction temperature range	-40°C to 150°C
T <sub>stg</sub>	Storage temperature range	-65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**DISSIPATION RATING TABLE**

PACKAGE	T <sub>A</sub> ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 85°C POWER RATING
DGN	2.14 W <sup>(1)</sup>	17.1 mW/°C	1.37 W	1.11 W

(1) See the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before-mentioned document.

**RECOMMENDED OPERATING CONDITIONS**

		MIN	MAX	UNIT
$V_{DD}$	Supply voltage	2.5	5.5	V
$T_A$	Operating free-air temperature	-40	85	°C
$V_{IH}$	High-level input voltage (SHUTDOWN)	$0.80 \times V_{DD}$		V
$V_{IL}$	Low-level input voltage (SHUTDOWN)	$0.25 \times V_{DD}$		V

**DC ELECTRICAL CHARACTERISTICS**

 at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 2.5\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$V_{OO}$	Output offset voltage (measured between output and BYPASS terminal)	$A_v = 2\text{ V/V}$		10	mV	
PSRR	Power supply rejection ratio	$V_{DD} = 3.2\text{ V to } 3.4\text{ V}$		83	dB	
$I_{DD}$	Supply current	SHUTDOWN = 0 V		1.5	3	mA
$I_{DD(SD)}$	Supply current in SHUTDOWN mode	SHUTDOWN = $V_{DD}$		10	50	μA
$Z_I$	Input impedance			>1	MΩ	

**AC OPERATING CHARACTERISTICS**
 $V_{DD} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $R_L = 8\Omega$ 

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_O$	Output power (each channel)	THD ≤ 0.1%		70 <sup>(1)</sup>	mW
THD+N	Total harmonic distortion + noise	$P_O = 70\text{ mW}$ , 20–20 kHz		2%	
$B_{OM}$	Maximum output power BW	G = 10, THD <5%		>20	kHz
	Phase margin	Open loop		58°	
	Supply ripple rejection ratio	f = 1 kHz		68	dB
	Channel/channel output separation	f = 1 kHz		86	dB
SNR	Signal-to-noise ratio	$P_O = 100\text{ mW}$		100	dB
$V_n$	Noise output voltage			9.5	μV(rms)

(1) Measured at 1kHz

**DC ELECTRICAL CHARACTERISTICS**

 at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.5\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$V_{OO}$	Output offset voltage	$A_v = 2\text{ V/V}$		10	mV	
PSRR	Power supply rejection ratio	$V_{DD} = 4.9\text{ V to } 5.1\text{ V}$		76	dB	
$I_{DD}$	Supply current	SHUTDOWN = 0 V		1.5	3	mA
$I_{DD(SD)}$	Supply current in SHUTDOWN mode	SHUTDOWN = $V_{DD}$		60	100	μA
$ I_{IH} $	High-level input current (SHUTDOWN)	$V_{DD} = 5.5\text{ V}$ , $V_I = V_{DD}$		1	μA	
$ I_{IL} $	Low-level input current (SHUTDOWN)	$V_{DD} = 5.5\text{ V}$ , $V_I = 0\text{ V}$		1	μA	
$Z_I$	Input impedance			>1	MΩ	

**AC OPERATING CHARACTERISTICS** $V_{DD} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $R_L = 8\Omega$ 

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_O$	Output power (each channel)	THD $\leq$ 0.1%		70 <sup>(1)</sup>		mW
THD+N	Total harmonic distortion + noise	$P_O = 150\text{ mW}$ , 20–20 kHz		2%		
$B_{OM}$	Maximum output power BW	$G = 10$ , THD <5%		>20		kHz
	Phase margin	Open loop		56°		
	Supply ripple rejection ratio	$f = 1\text{ kHz}$		68		dB
	Channel/Channel output separation	$f = 1\text{ kHz}$		86		dB
SNR	Signal-to-noise ratio	$P_O = 150\text{ mW}$		100		dB
$V_n$	Noise output voltage			9.5		$\mu\text{V(rms)}$

(1) Measured at 1kHz

**AC OPERATING CHARACTERISTICS** $V_{DD} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $R_L = 32\Omega$ 

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_O$	Output power (each channel)	THD $\leq$ 0.1%		40 <sup>(1)</sup>		mW
THD+N	Total harmonic distortion + noise	$P_O = 30\text{ mW}$ , 20–20 kHz		0.5%		
$B_{OM}$	Maximum output power BW	$A_V = 10$ , THD <2%		>20		kHz
	Phase margin	Open loop		58°		
	Supply ripple rejection ratio	$f = 1\text{ kHz}$		68		dB
	Channel/channel output separation	$f = 1\text{ kHz}$		97		dB
SNR	Signal-to-noise ratio	$P_O = 100\text{ mW}$		100		dB
$V_n$	Noise output voltage			9.5		$\mu\text{V(rms)}$

(1) Measured at 1kHz

**AC OPERATING CHARACTERISTICS** $V_{DD} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $R_L = 32\Omega$ 

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_O$	Output power (each channel)	THD $\leq$ 0.1%		40 <sup>(1)</sup>		mW
THD+N	Total harmonic distortion + noise	$P_O = 60\text{ mW}$ , 20–20 kHz		0.4%		
$B_{OM}$	Maximum output power BW	$A_V = 10$ , THD <2%		>20		kHz
	Phase margin	Open loop		56°		
	Supply ripple rejection ratio	$f = 1\text{ kHz}$		68		dB
	Channel/channel output separation	$f = 1\text{ kHz}$		97		dB
SNR	Signal-to-noise ratio	$P_O = 150\text{ mW}$		100		dB
$V_n$	Noise output voltage			9.5		$\mu\text{V(rms)}$

(1) Measured at 1kHz

**TYPICAL CHARACTERISTICS**

**Table of Graphs**

			FIGURE
THD+N	Total harmonic distortion plus noise	vs Frequency	1, 2, 4, 5, 7, 8, 10, 11, 13, 14, 16, 17, 34, 36
		vs Power output	3, 6, 9, 12, 15, 18
	Power supply rejection ratio	vs Frequency	19, 20
$V_n$	Output noise voltage	vs Frequency	21, 22
	Crosstalk	vs Frequency	23-26, 37, 38
	Mute attenuation	vs Frequency	27, 28
	Open-loop gain	vs Frequency	29, 30
	Phase margin		
	Output power	vs Load resistance	31, 32
$I_{DD}$	Supply current	vs Supply voltage	33
SNR	Signal-to-noise ratio	vs Voltage gain	35
	Closed-loop gain	vs Frequency	39-44
	Phase		
	Power dissipation	vs Output power	45, 46

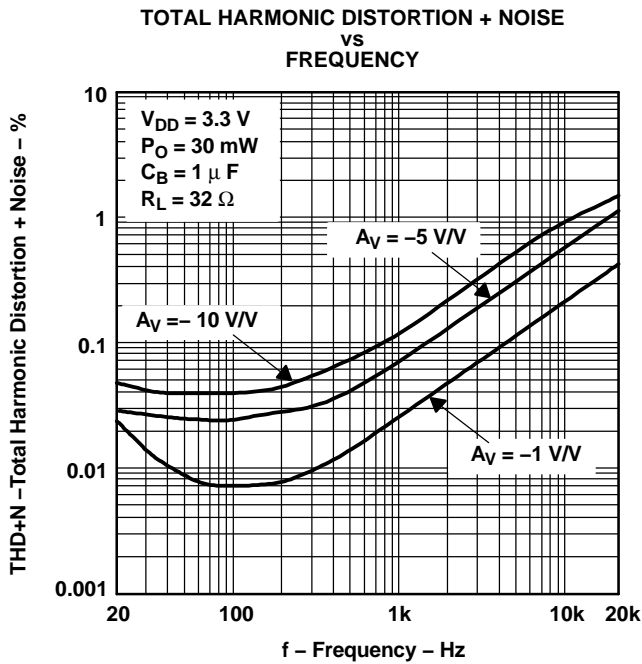


Figure 1.

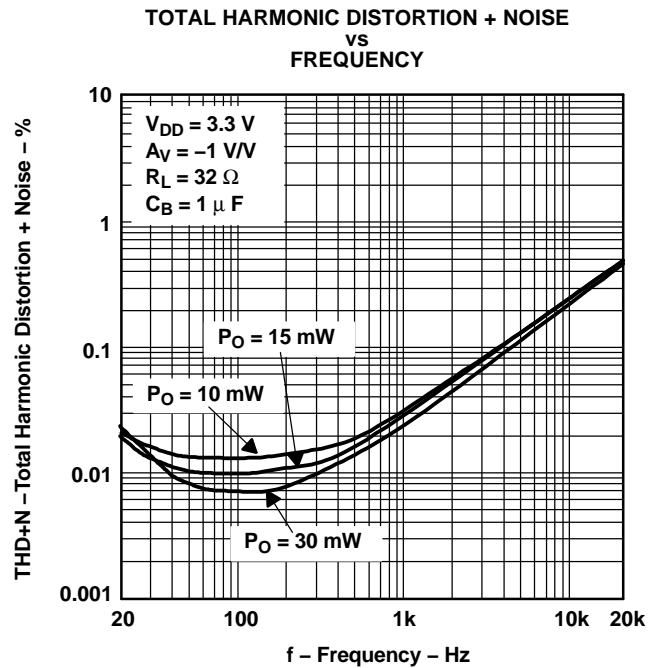


Figure 2.

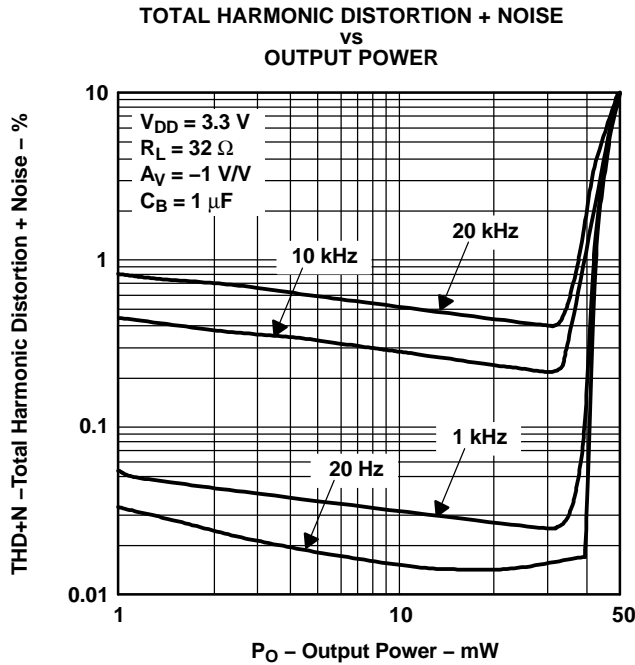


Figure 3.

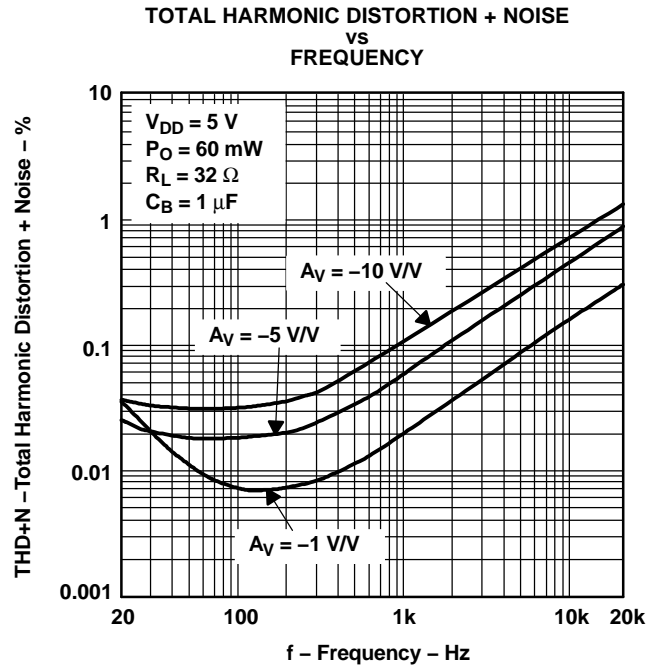


Figure 4.

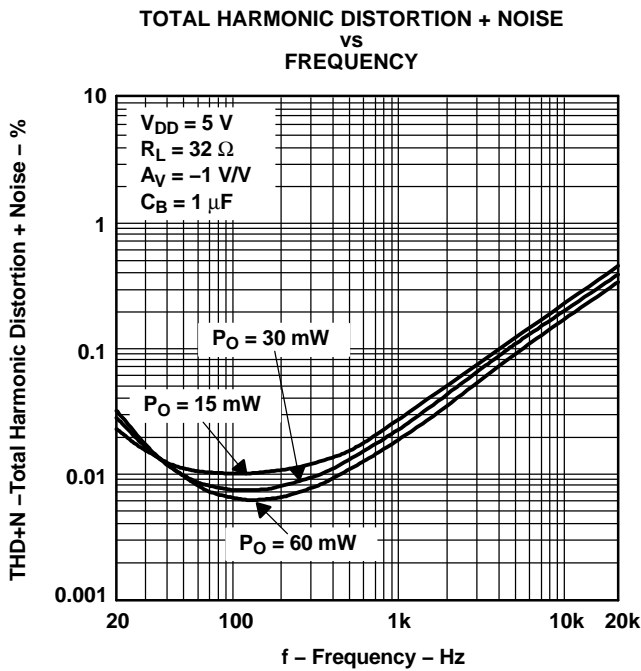


Figure 5.

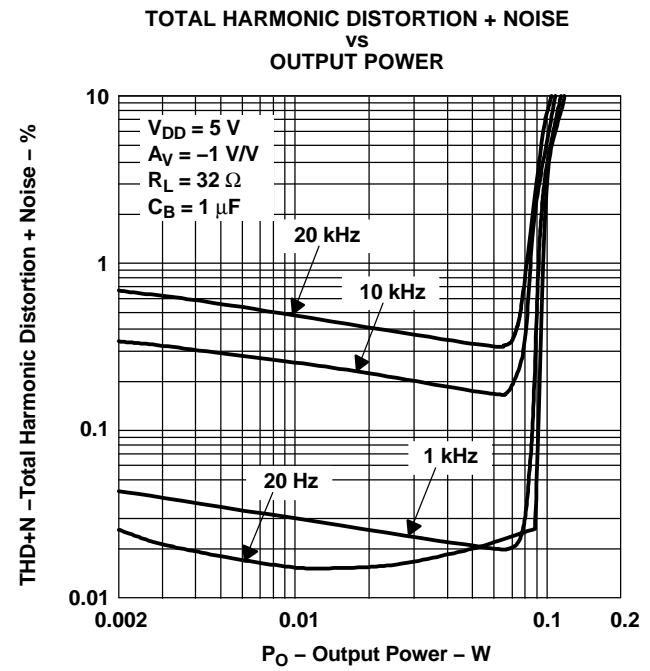


Figure 6.

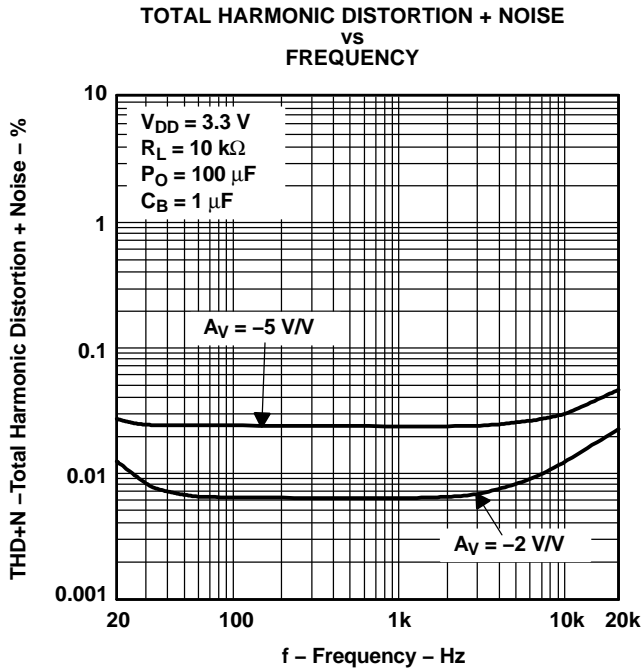


Figure 7.

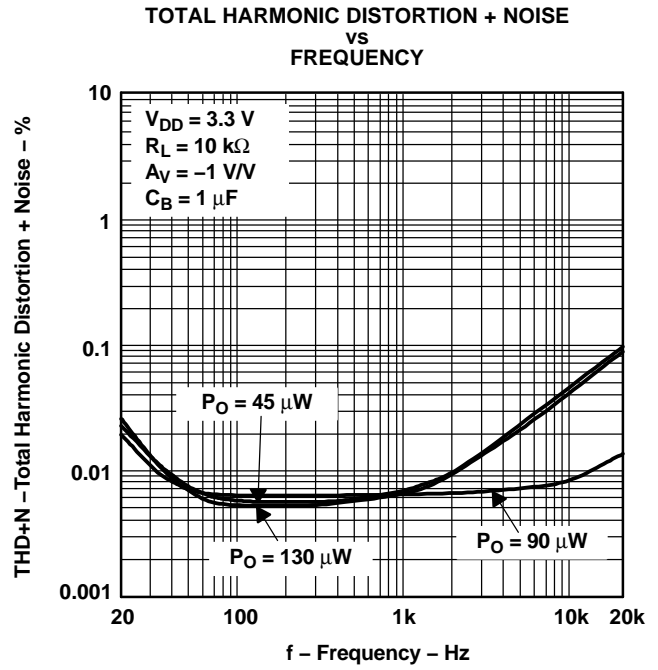


Figure 8.

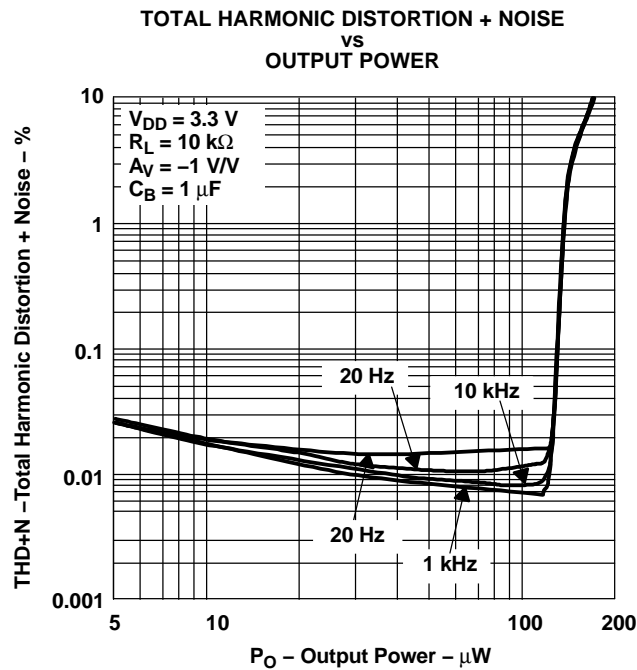


Figure 9.

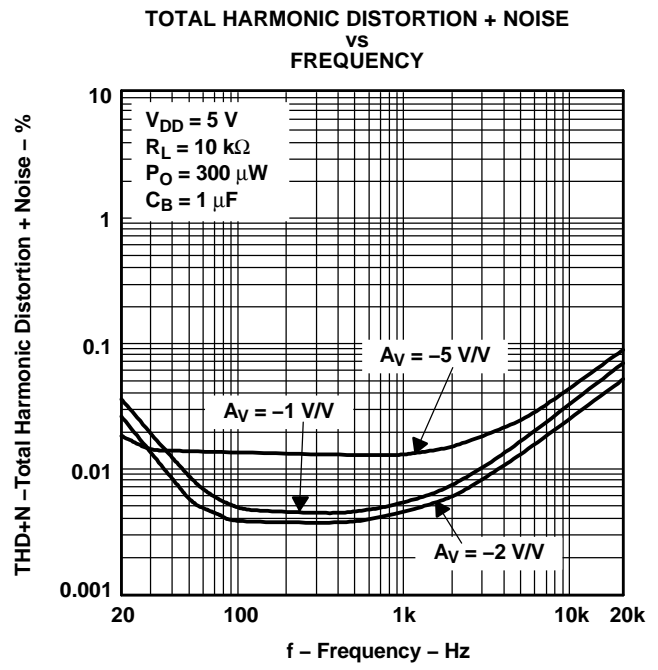


Figure 10.

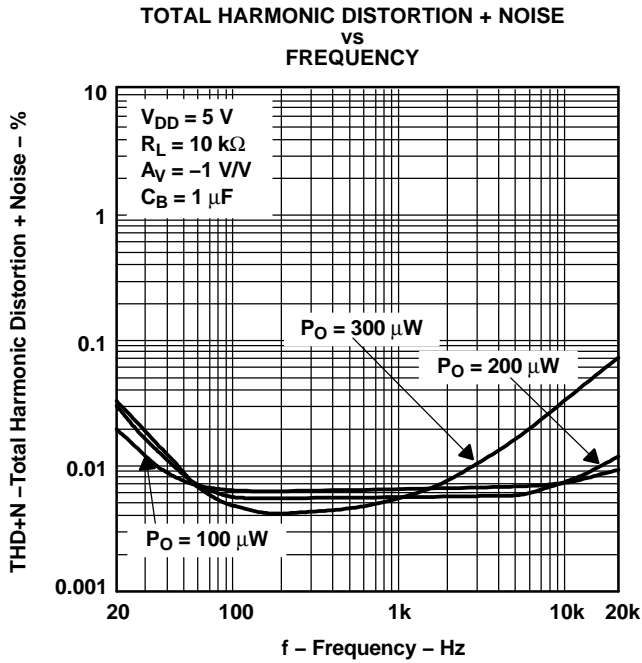


Figure 11.

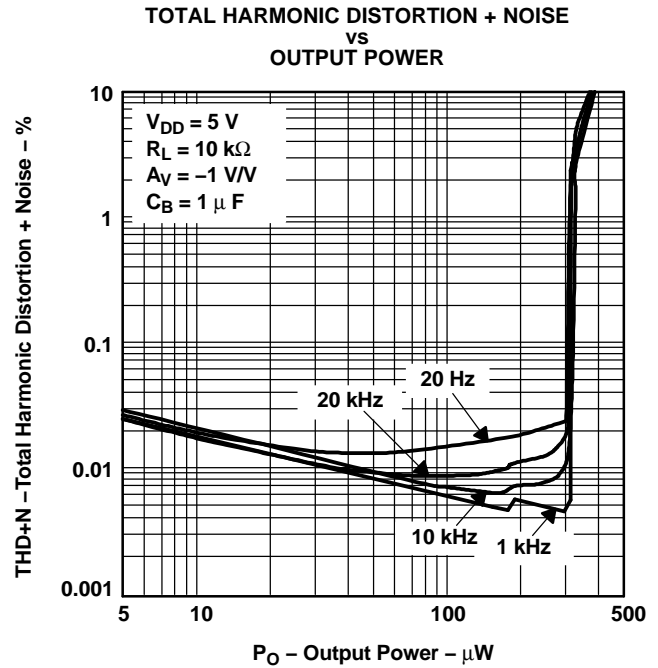


Figure 12.

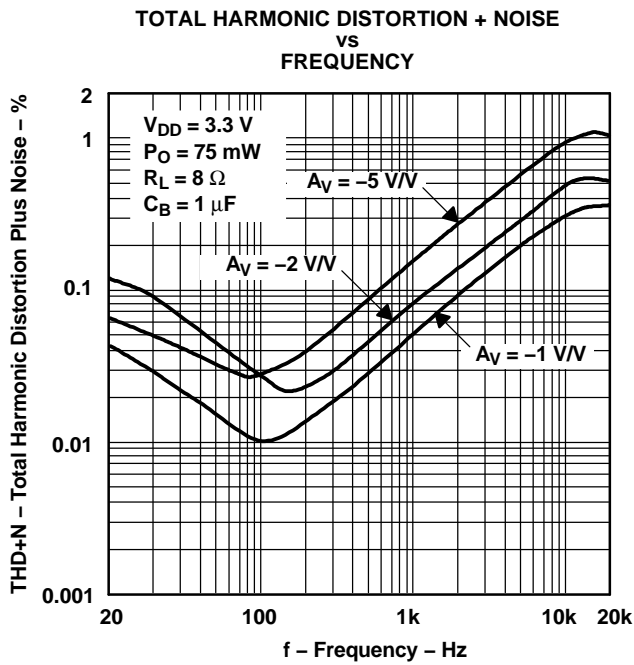


Figure 13.

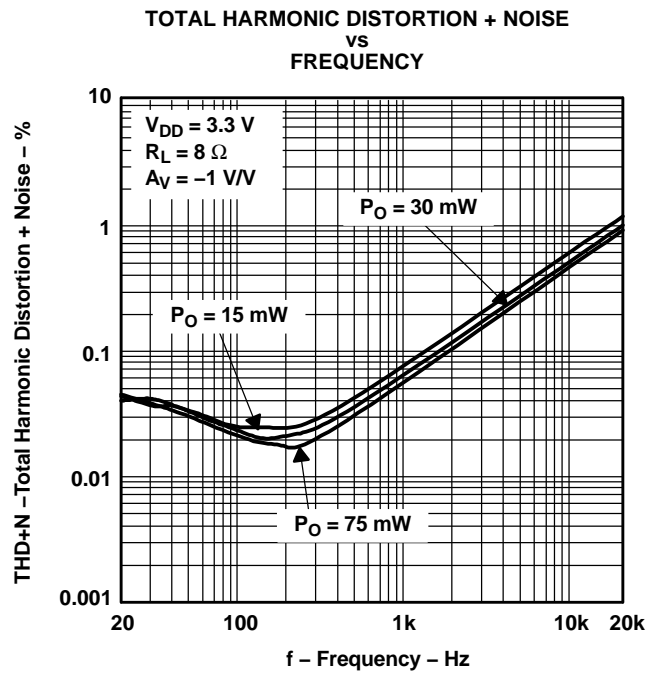


Figure 14.



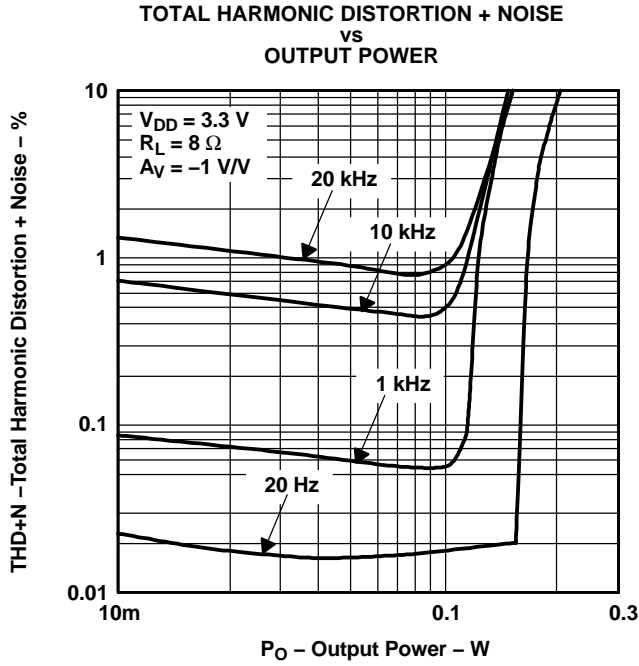


Figure 15.

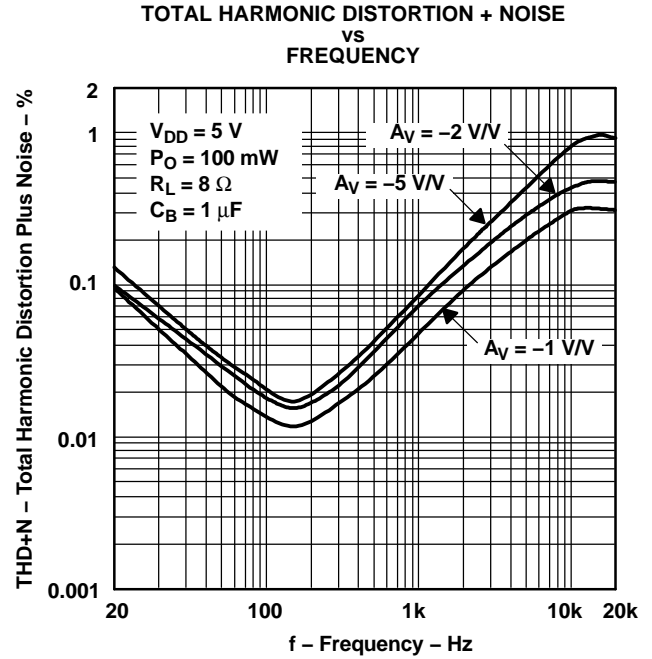


Figure 16.

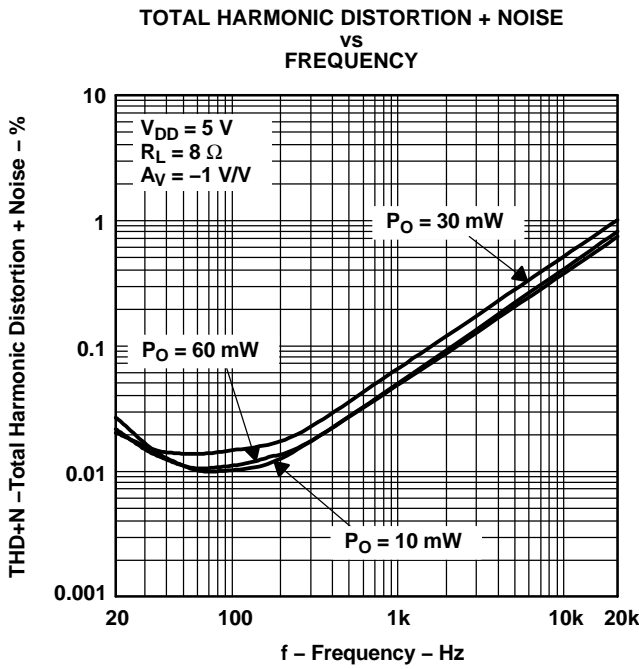


Figure 17.

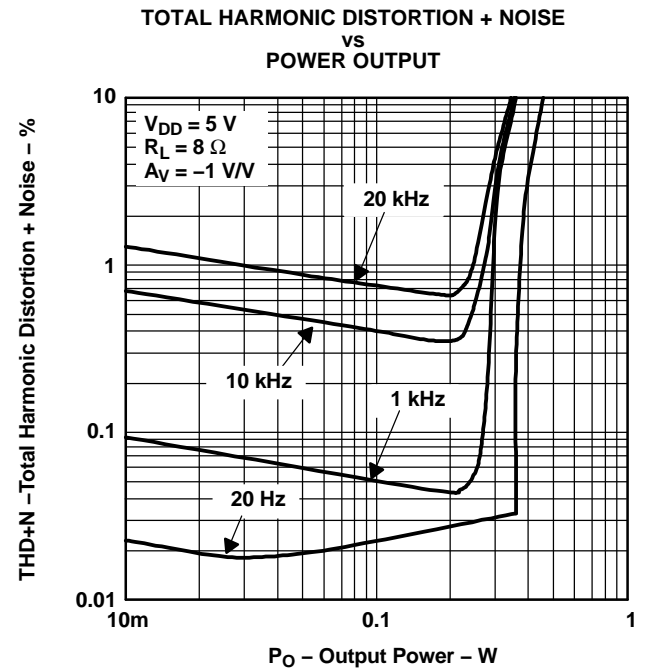


Figure 18.

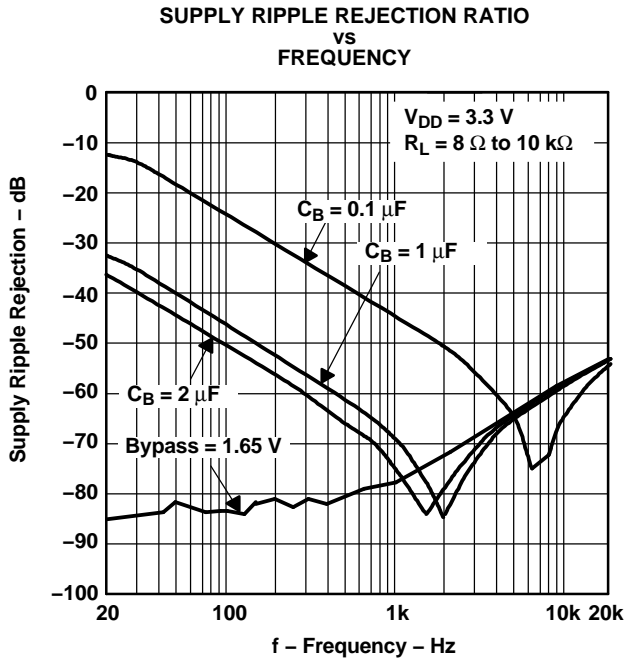


Figure 19.

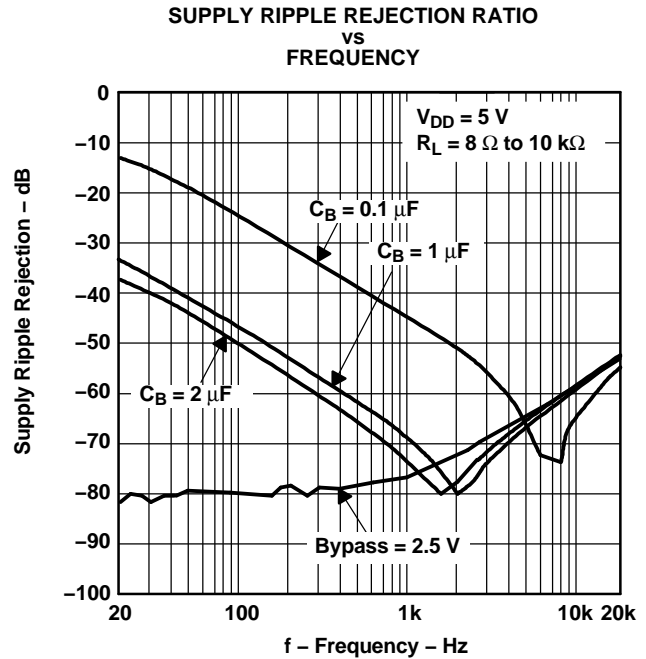


Figure 20.

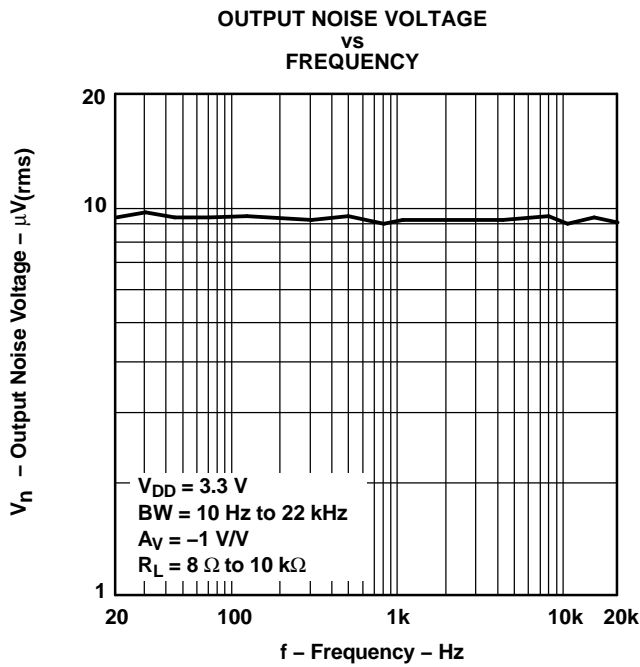


Figure 21.

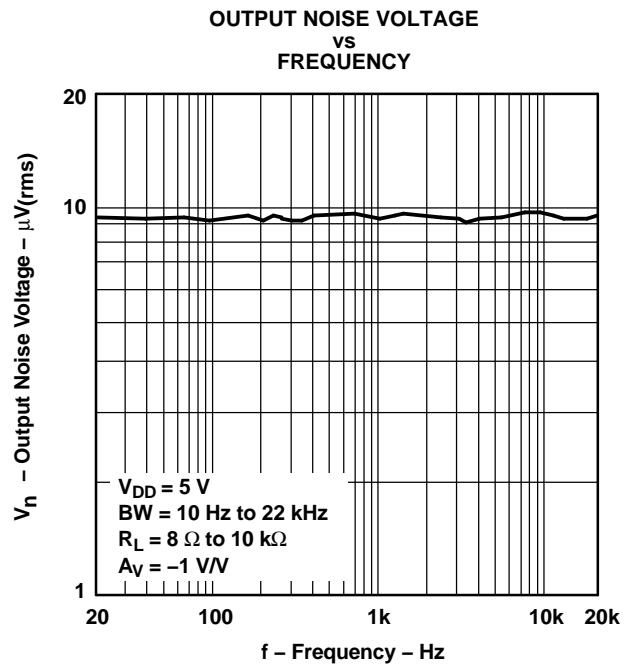


Figure 22.

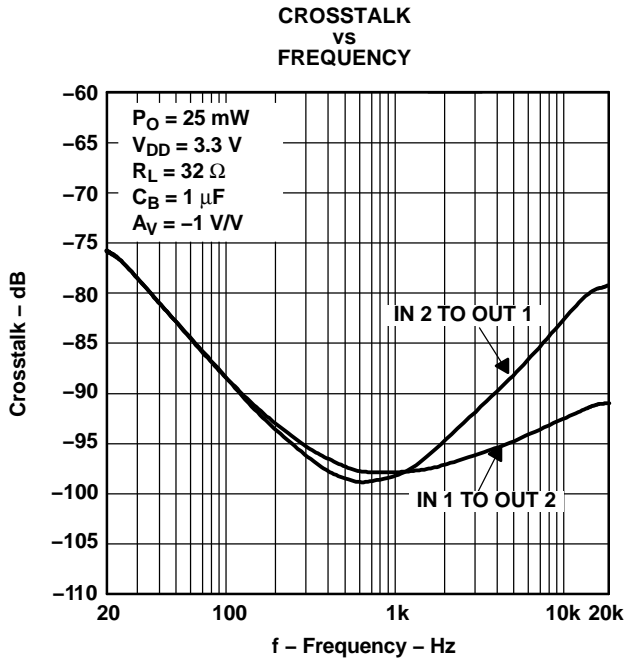


Figure 23.

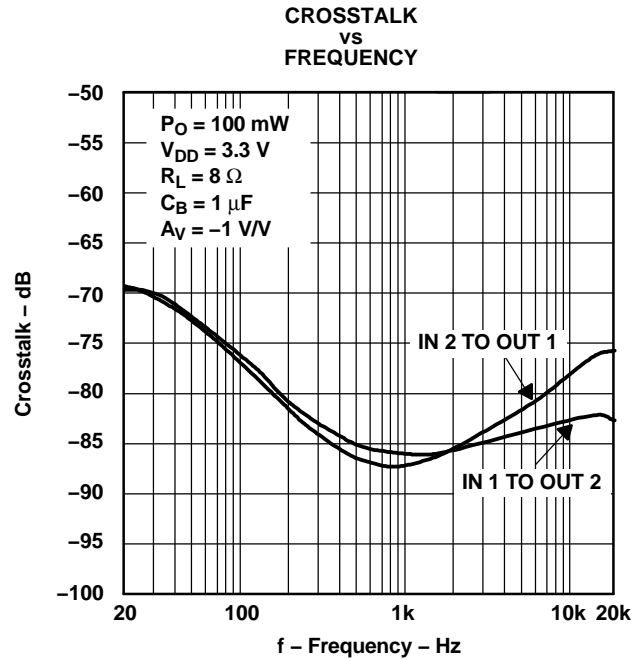


Figure 24.

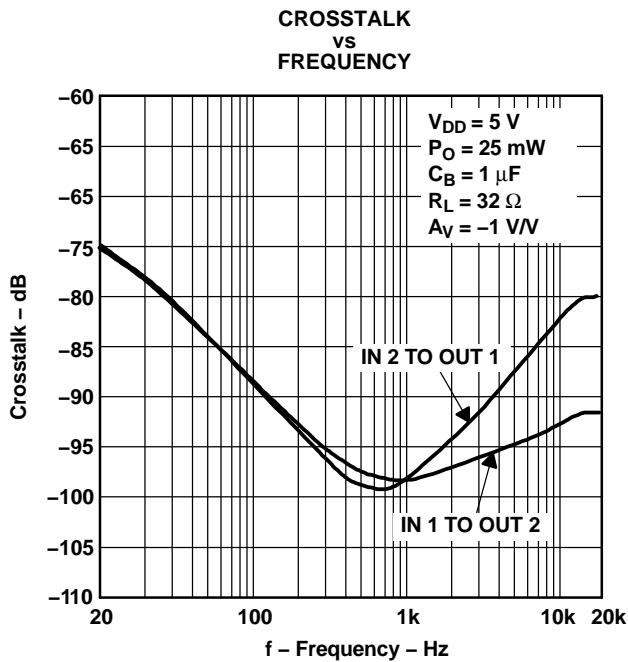


Figure 25.

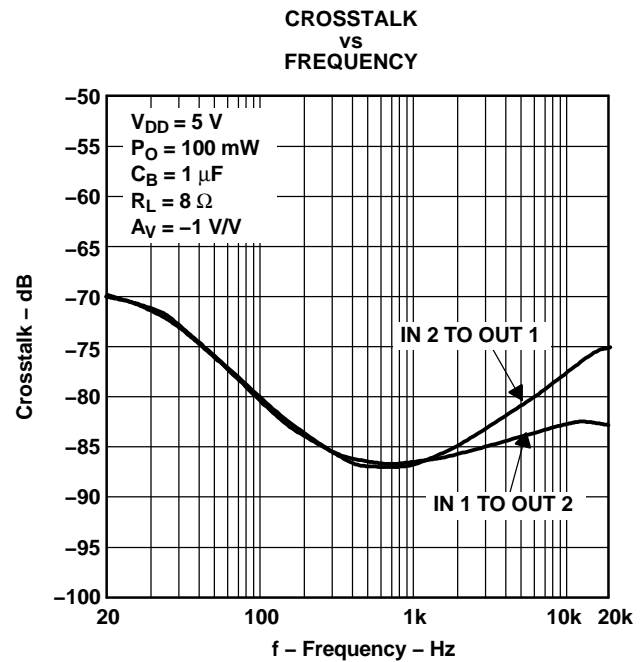


Figure 26.

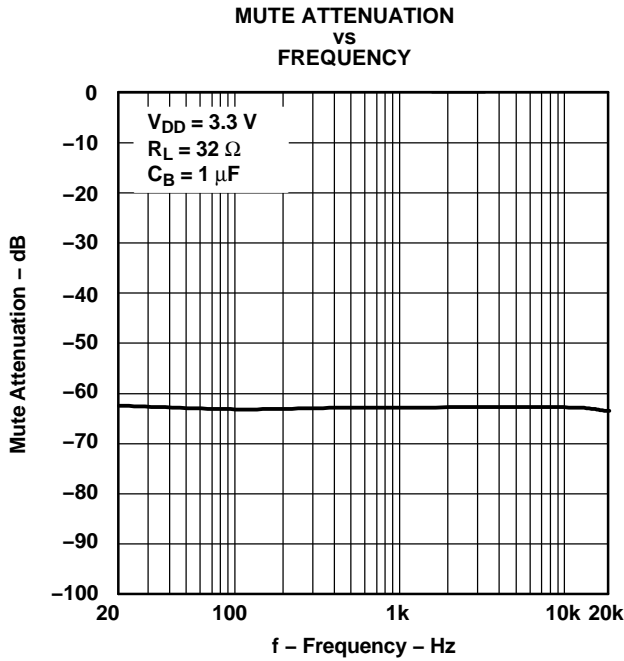


Figure 27.

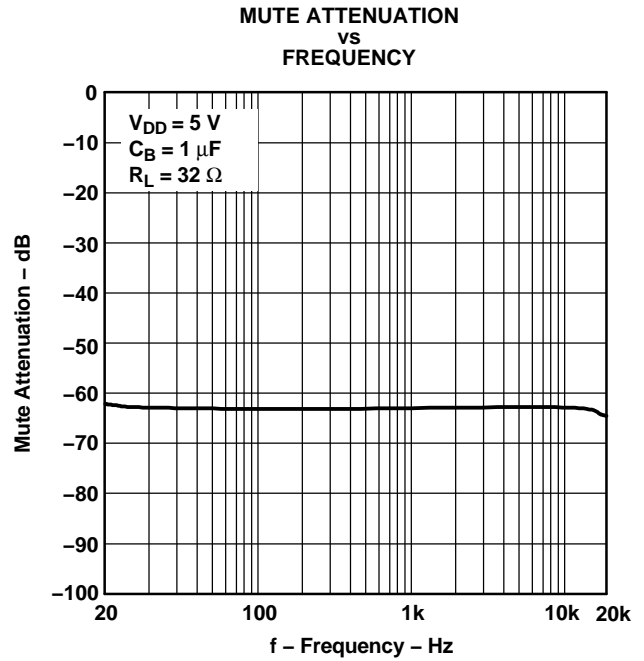


Figure 28.

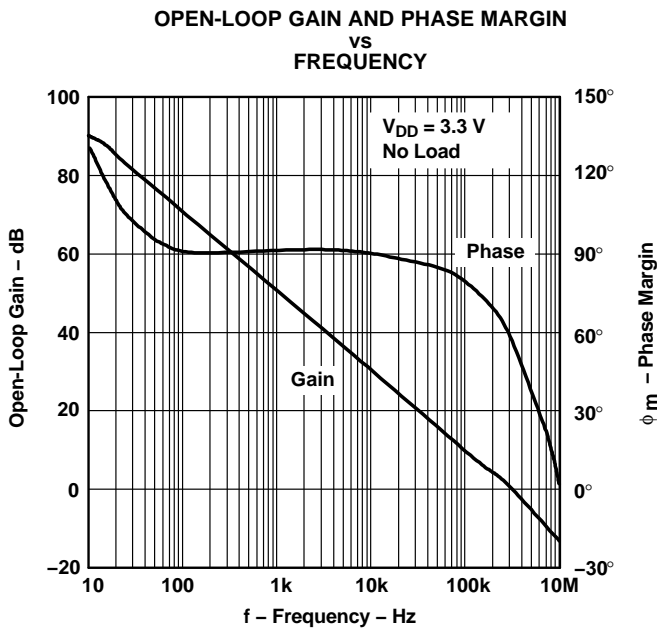


Figure 29.

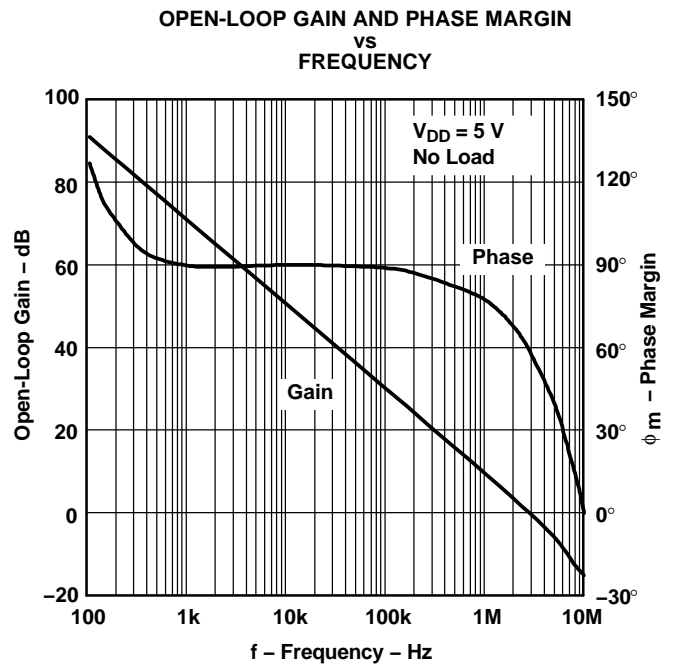


Figure 30.

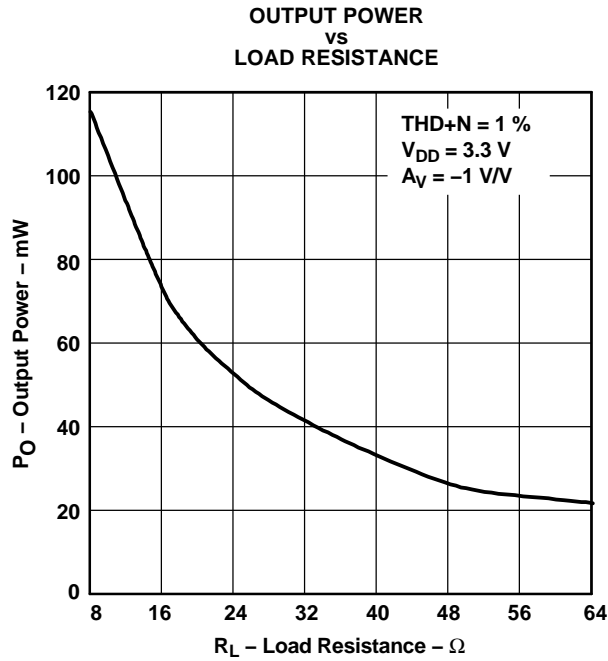


Figure 31.

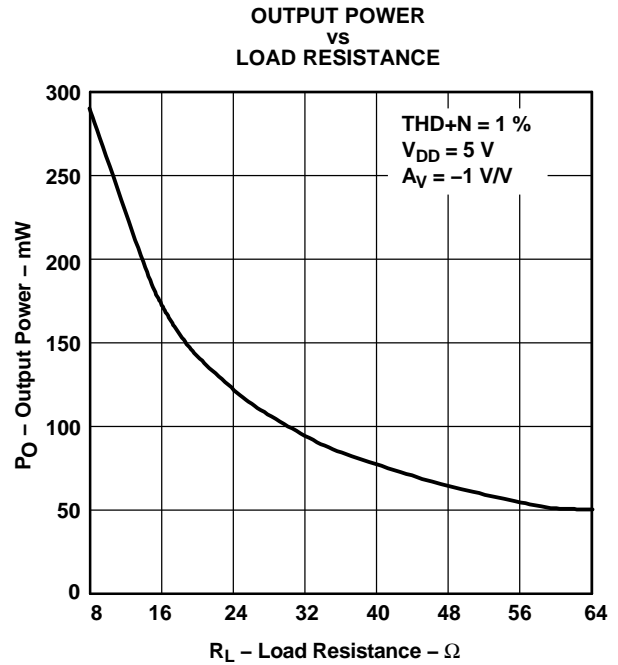


Figure 32.

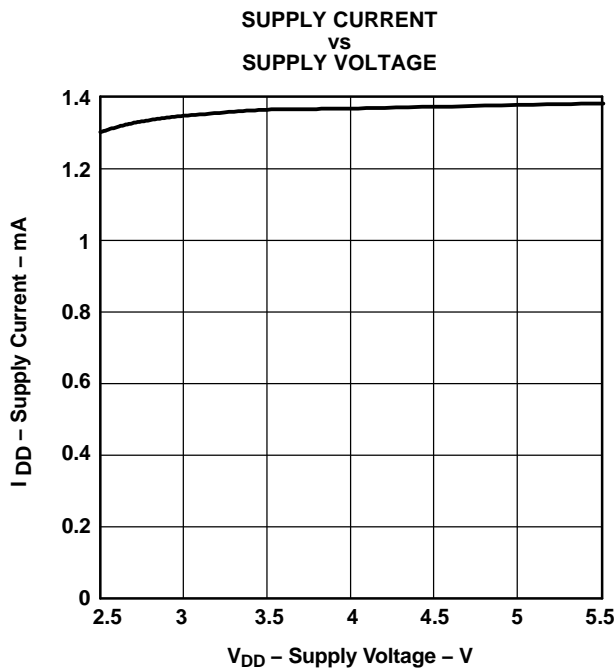


Figure 33.

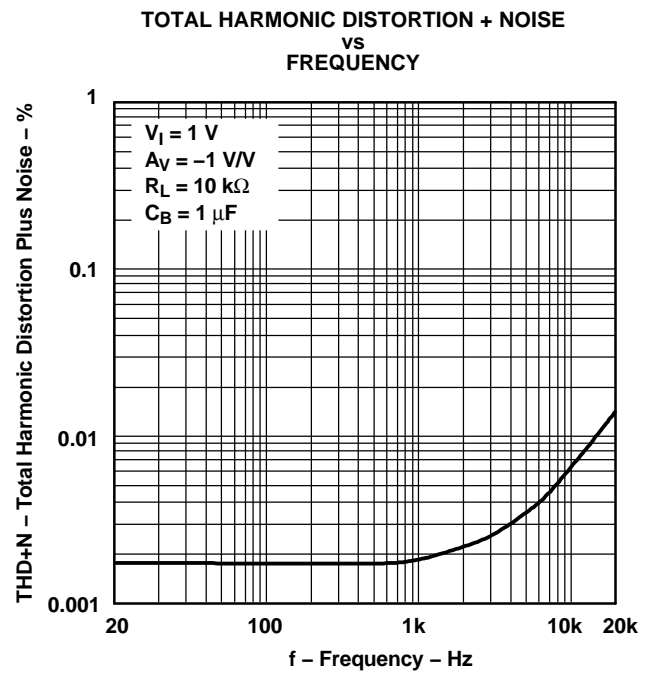
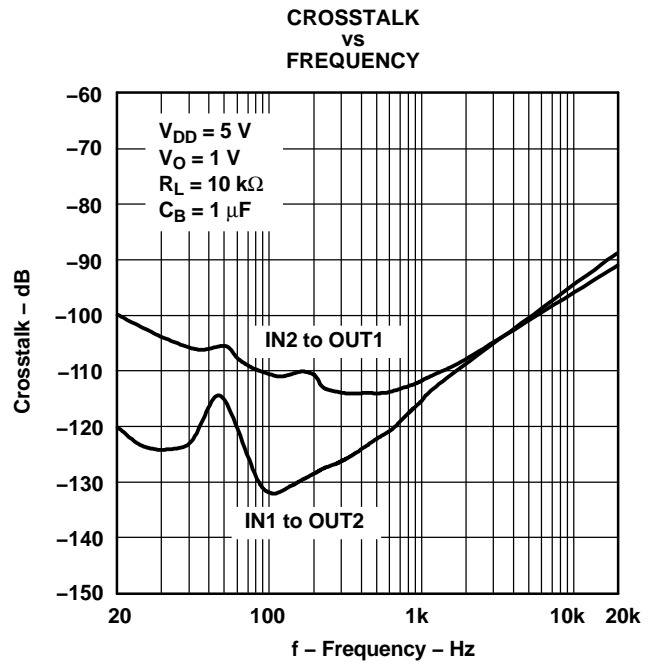
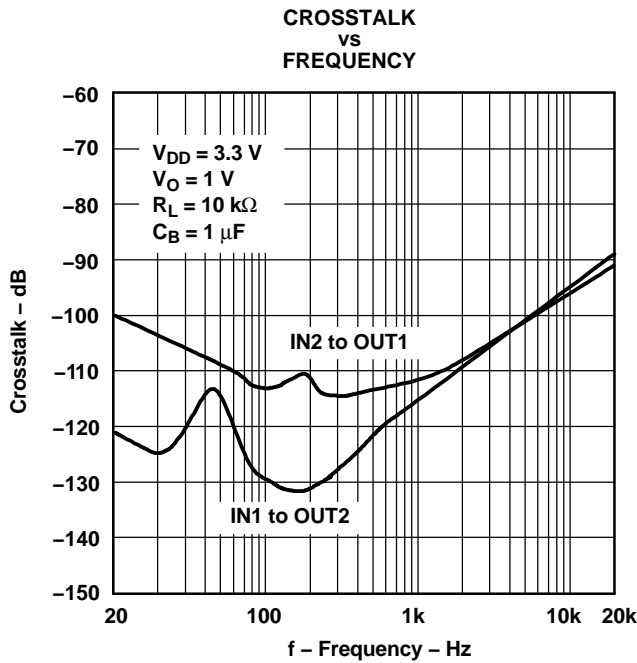
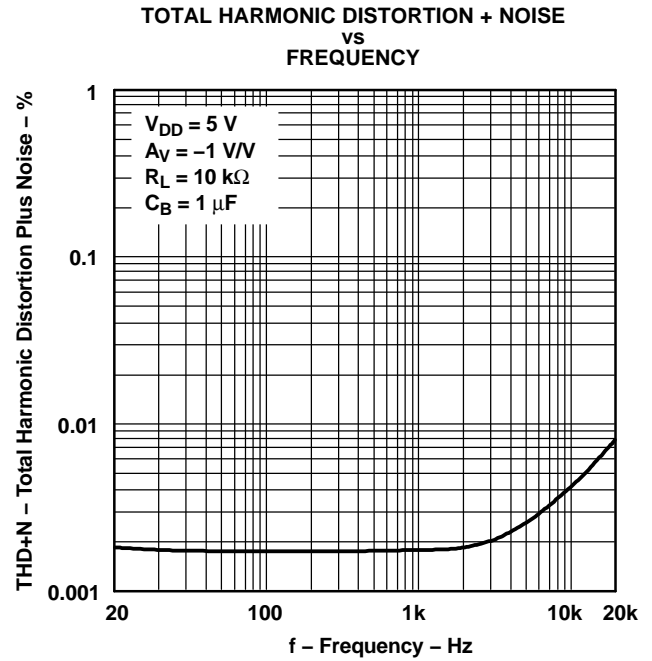
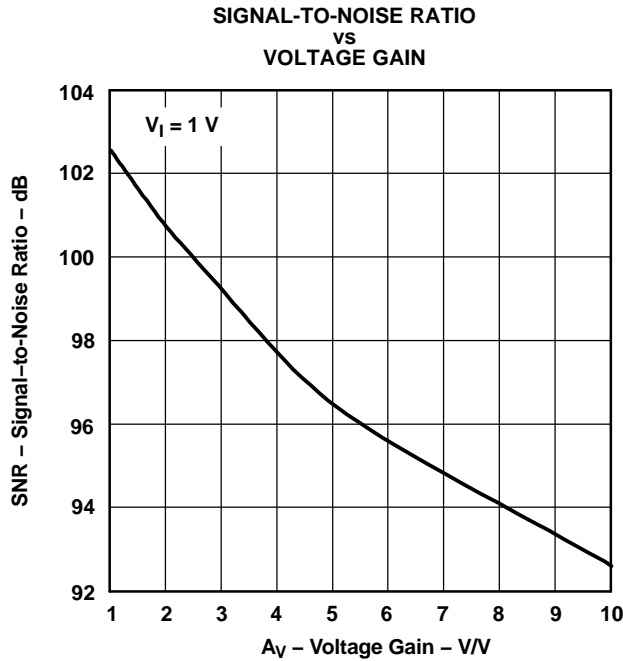


Figure 34.



**CLOSED-LOOP GAIN AND PHASE  
VS  
FREQUENCY**

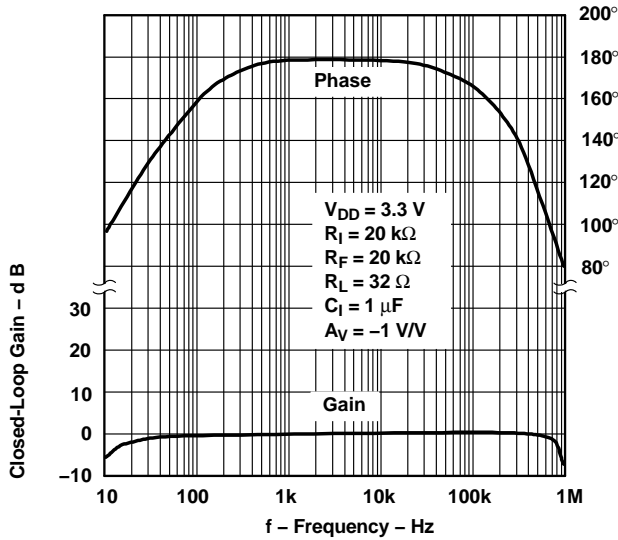


Figure 39.

**CLOSED-LOOP GAIN AND PHASE  
VS  
FREQUENCY**

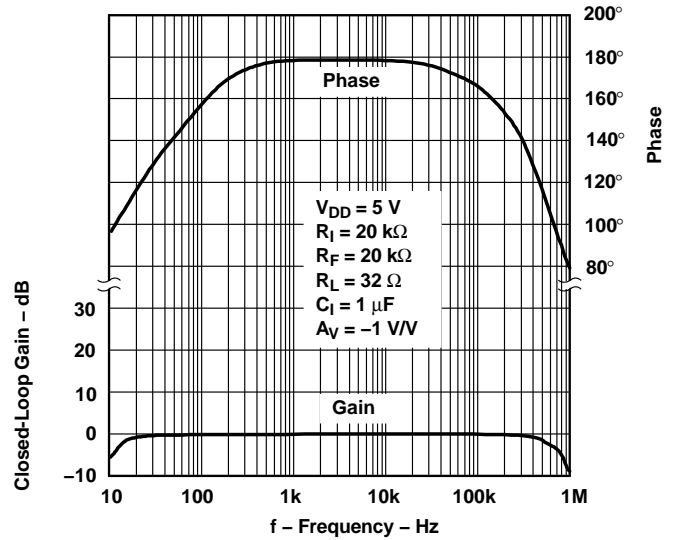


Figure 40.

**CLOSED-LOOP GAIN AND PHASE  
VS  
FREQUENCY**

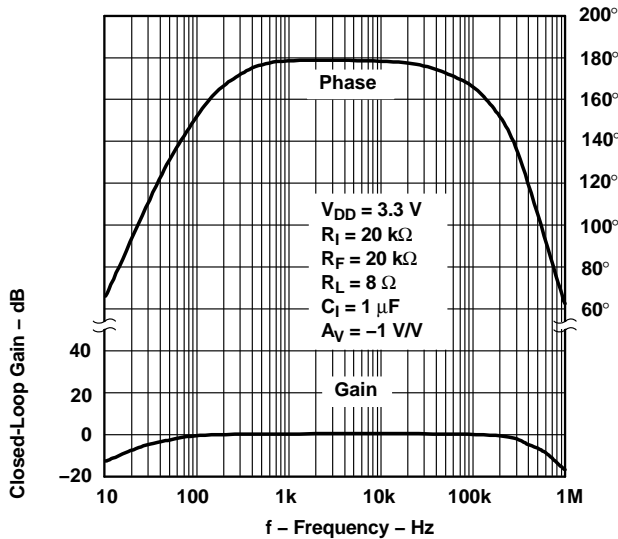


Figure 41.

**CLOSED-LOOP GAIN AND PHASE  
VS  
FREQUENCY**

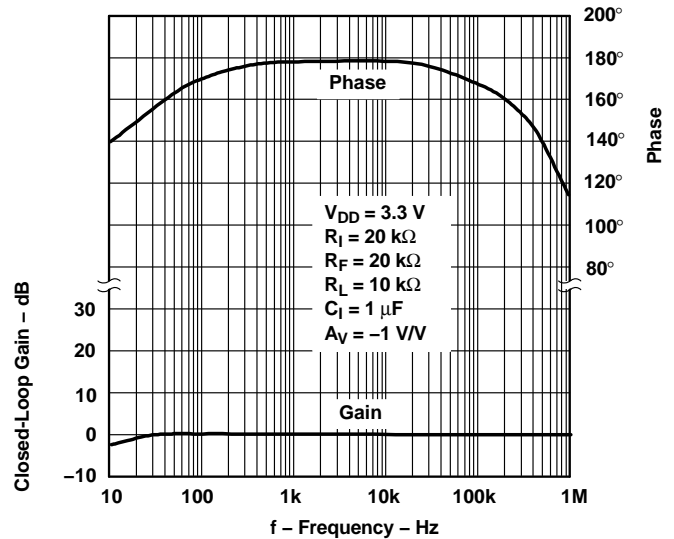


Figure 42.

CLOSED-LOOP GAIN AND PHASE  
VS  
FREQUENCY

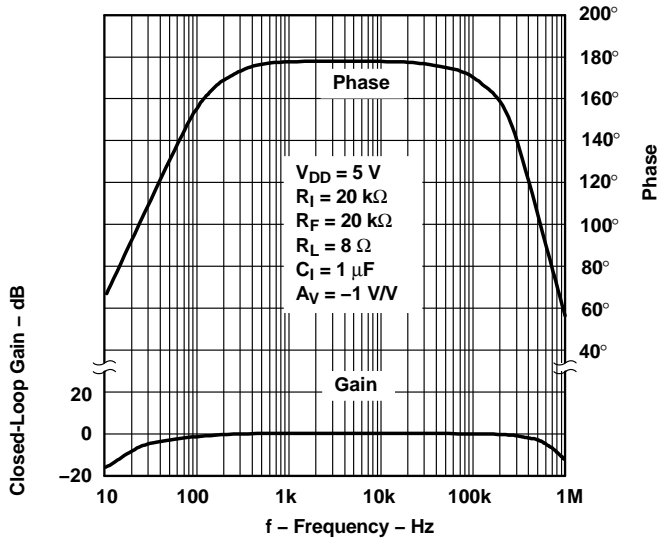


Figure 43.

CLOSED-LOOP GAIN AND PHASE  
VS  
FREQUENCY

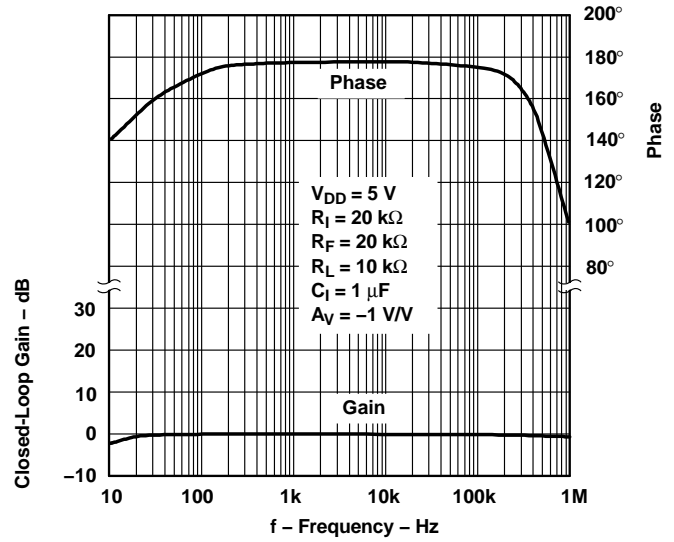


Figure 44.

POWER DISSIPATION/AMPLIFIER  
VS  
OUTPUT POWER

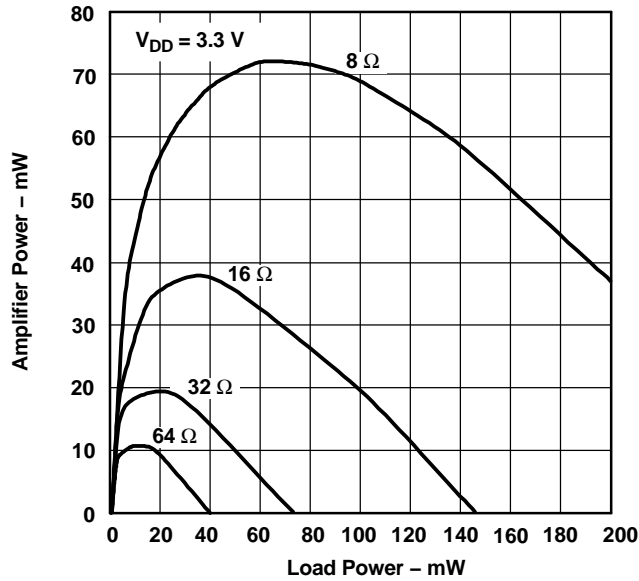


Figure 45.

POWER DISSIPATION/AMPLIFIER  
VS  
OUTPUT POWER

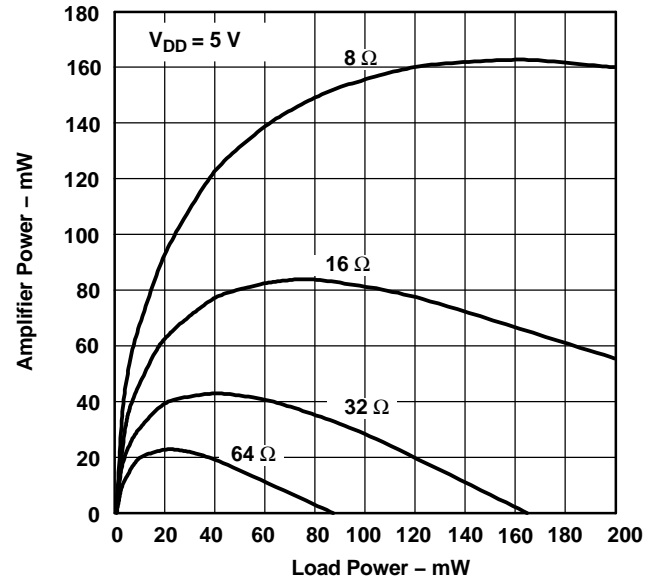


Figure 46.



## APPLICATION INFORMATION

### GAIN SETTING RESISTORS, $R_f$ and $R_i$

The gain for the TPA102 is set by resistors  $R_f$  and  $R_i$  according to Equation 1.

$$\text{Gain} = - \left( \frac{R_f}{R_i} \right) \quad (1)$$

Given that the TPA102 is a MOS amplifier, the input impedance is very high. Consequently input leakage currents are not generally a concern. However, noise in the circuit increases as the value of  $R_f$  increases. In addition, a certain range of  $R_f$  values is required for proper start-up operation of the amplifier. Considering these factors, it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 k $\Omega$  and 20 k $\Omega$ . The effective impedance is calculated using Equation 2.

$$\text{Effective Impedance} = \frac{R_f R_i}{R_f + R_i} \quad (2)$$

For example, if the input resistance is 20 k $\Omega$  and the feedback resistor is 20 k $\Omega$ , the gain of the amplifier is -1, and the effective impedance at the inverting terminal is 10 k $\Omega$ , a value within the recommended range.

For high performance applications, metal-film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of  $R_f$  above 50 k $\Omega$ , the amplifier tends to become unstable due to a pole formed from  $R_f$  and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with  $R_f$ . This, in effect, creates a low-pass filter network with the cutoff frequency defined by Equation 3.

$$f_{c(\text{lowpass})} = \frac{1}{2\pi R_f C_F} \quad (3)$$

For example, if  $R_f$  is 100 k $\Omega$  and  $C_F$  is 5 pF then  $f_{c(\text{lowpass})}$  is 318 kHz, which is well outside the audio range.

### INPUT CAPACITOR, $C_i$

In the typical application, an input capacitor,  $C_i$ , is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case,  $C_i$  and  $R_i$  form a high-pass filter with the corner frequency determined in Equation 4.

$$f_{c(\text{highpass})} = \frac{1}{2\pi R_i C_i} \quad (4)$$

The value of  $C_i$  directly affects the bass (low frequency) performance of the circuit. Consider the example where  $R_i$  is 20 k $\Omega$  and the specification calls for a flat bass response down to 20 Hz. Equation 4 is reconfigured as Equation 5.

$$C_i = \frac{1}{2\pi R_i f_{c(\text{highpass})}} \quad (5)$$

In this example,  $C_i$  is 0.40  $\mu\text{F}$ , so one would likely choose a value in the range of 0.47  $\mu\text{F}$  to 1  $\mu\text{F}$ . A further consideration for this capacitor is the leakage path from the input source through the input network formed by  $R_i$ ,  $C_i$ , and the feedback resistor ( $R_f$ ) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high-gain applications (gain >10). For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, connect the positive side of the capacitor to the amplifier input in most applications. The dc level there is held at  $V_{DD}/2$ —likely higher than the source dc level. It is important to confirm the capacitor polarity in the application.

### POWER SUPPLY DECOUPLING, $C_{(s)}$

The TPA102 is a high-performance CMOS audio amplifier that requires adequate power-supply decoupling to minimize the output total harmonic distortion (THD). Power-supply decoupling also prevents oscillations when long lead lengths are used between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1  $\mu\text{F}$ , placed as close as possible to the device  $V_{DD}$  lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10  $\mu\text{F}$  or greater placed near the power amplifier is recommended.

### MIDRAIL BYPASS CAPACITOR, $C_{(B)}$

The midrail bypass capacitor,  $C_{(B)}$ , serves several important functions. During start up,  $C_{(B)}$  determines the rate at which the amplifier starts up. This helps to push the start-up pop noise into the subaudible range (so low it can not be heard). The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from a 230-k $\Omega$  source inside the amplifier. To keep the start-up pop as low as possible, maintain the relationship shown in Equation 6.

$$\frac{1}{(C_{(B)} \times 230 \text{ k}\Omega)} \leq \frac{1}{(C_i R_i)} \quad (6)$$

Consider an example circuit where  $C_{(B)}$  is 1  $\mu\text{F}$ ,  $C_i$  is 1  $\mu\text{F}$ , and  $R_i$  is 20 k $\Omega$ . Substituting these values into the equation 9 results in:  $6.25 \leq 50$  which satisfies the rule. Bypass capacitor,  $C_{(B)}$ , values of 0.1  $\mu\text{F}$  to 1  $\mu\text{F}$  ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

### OUTPUT COUPLING CAPACITOR, $C_{(C)}$

In a typical single-supply, single-ended (SE) configuration, an output coupling capacitor ( $C_{(C)}$ ) is required to block the dc bias at the output of the amplifier, thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by Equation 7.

$$f_c = \frac{1}{2\pi R_L C_{(C)}} \quad (7)$$

The main disadvantage, from a performance standpoint, is that the typically-small load impedance drives the low-frequency corner higher. Large values of  $C_{(C)}$  are required to pass low frequencies into the load. Consider the example where a  $C_{(C)}$  of 68  $\mu\text{F}$  is chosen and loads vary from 32  $\Omega$  to 47 k $\Omega$ . Table 1 summarizes the frequency response characteristics of each configuration.

**Table 1. Common Load Impedances vs Low-Frequency Output Characteristics in SE Mode**

$R_L$	$C_{(C)}$	LOWEST FREQUENCY
32 $\Omega$	68 $\mu\text{F}$	73 Hz
10,000 $\Omega$	68 $\mu\text{F}$	0.23 Hz
47,000 $\Omega$	68 $\mu\text{F}$	0.05 Hz

As Table 1 indicates, headphone response is adequate, and drive into line level inputs (a home stereo for example) is very good.

The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. With the rules described earlier still valid, add the following relationship:

$$\frac{1}{(C_{(B)} \times 230 \text{ k}\Omega)} \leq \frac{1}{(C_i R_i)} \ll \frac{1}{R_L C_{(C)}} \quad (8)$$

### USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this application. A real capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

### 5-V VERSUS 3.3-V OPERATION

The TPA102 was designed for operation over a supply range of 2.5 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation, since these are considered to be the two most common supply voltages. There are no special considerations for 3.3-V versus 5-V operation as far as supply bypassing, gain setting, or stability. The most important consideration is that of output power. Each amplifier in the TPA102 can produce a maximum voltage swing of  $V_{DD} - 1 \text{ V}$ . This means, for 3.3-V operation, clipping starts to occur when  $V_{O(PP)} = 2.3 \text{ V}$  as opposed when  $V_{O(PP)} = 4 \text{ V}$  while operating at 5 V. The reduced voltage swing subsequently reduces maximum output power into the load before distortion becomes significant.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA102DGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		AAC	<a href="#">Samples</a>
TPA102DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		AAC	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

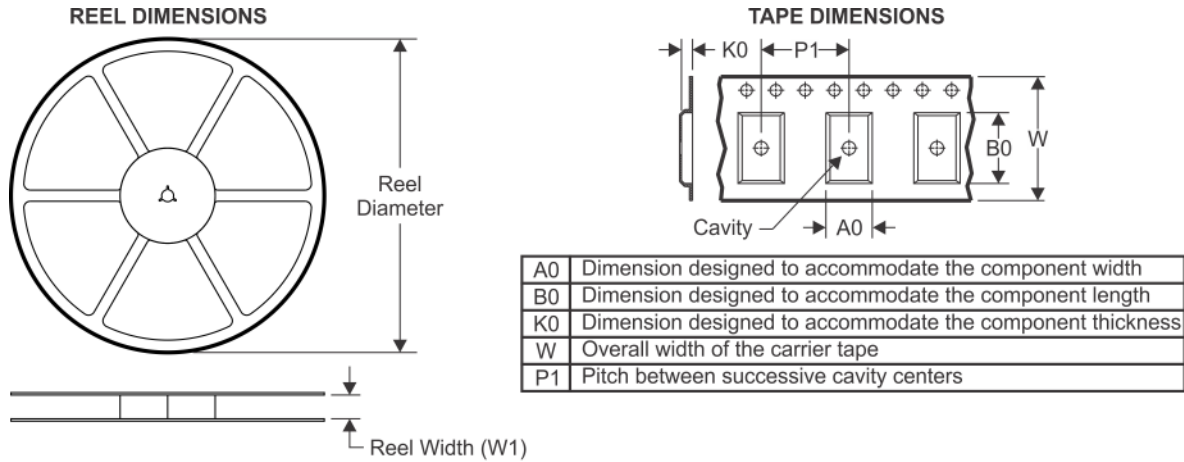
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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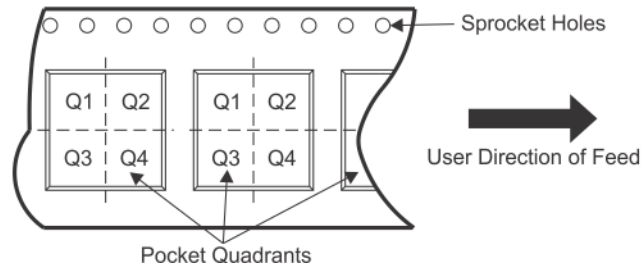
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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA102DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA102DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0

## GENERIC PACKAGE VIEW

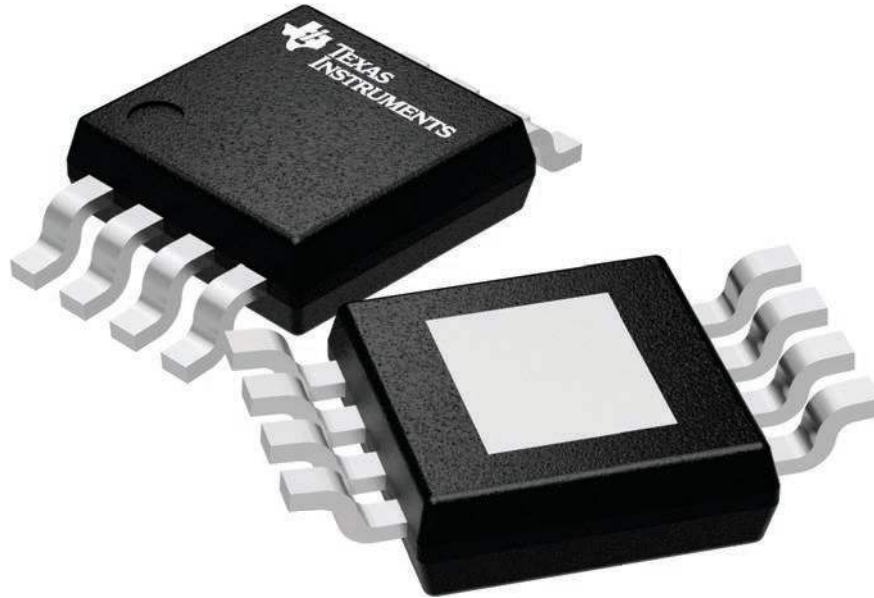
**DGN 8**

**PowerPAD VSSOP - 1.1 mm max height**

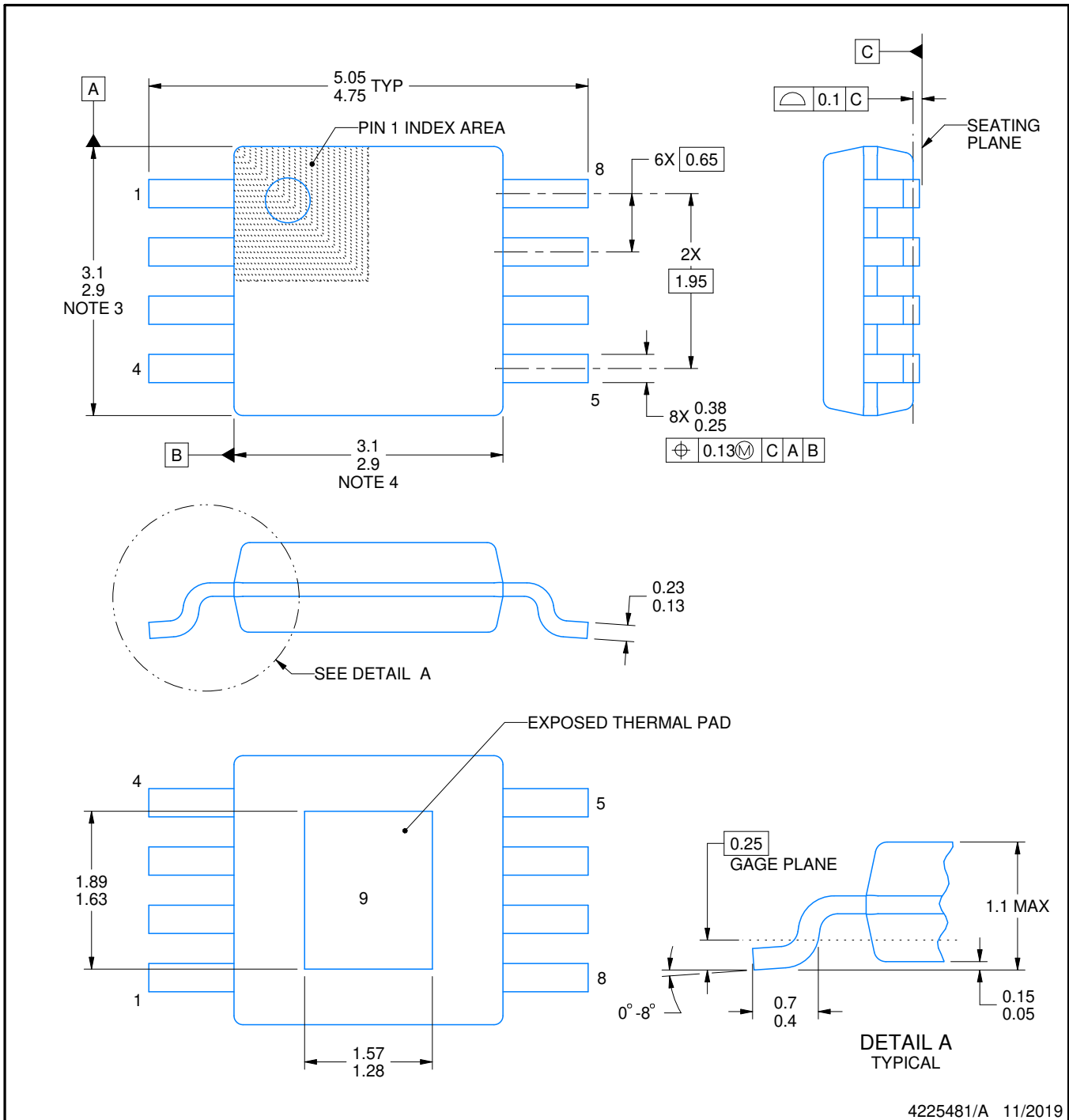
3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225482/A



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PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

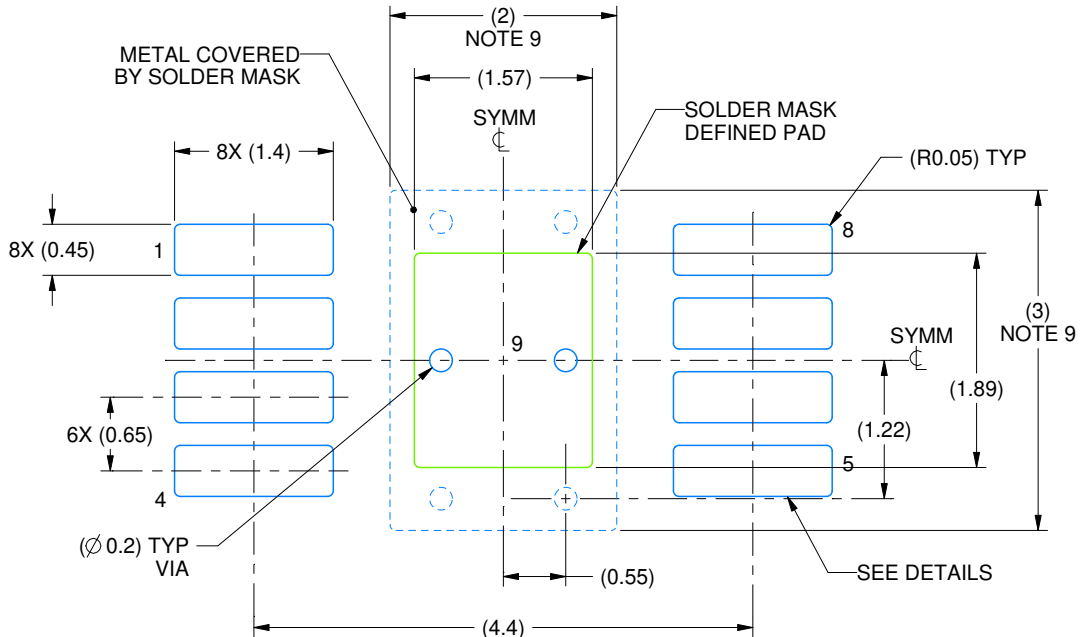


# EXAMPLE BOARD LAYOUT

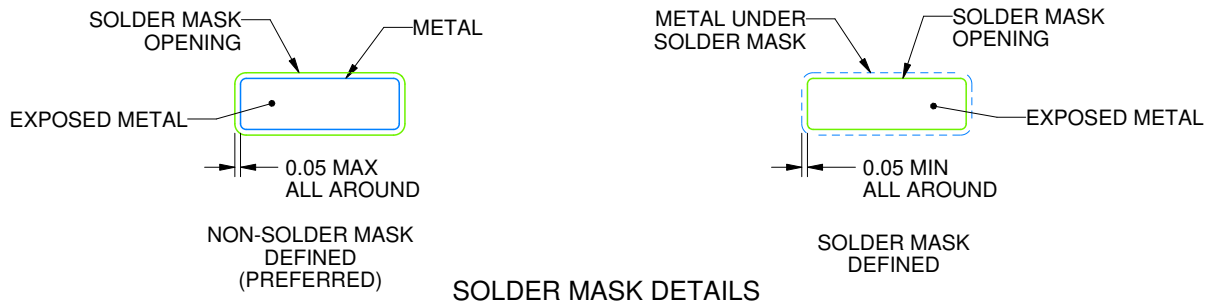
DGN0008D

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

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NOTES: (continued)

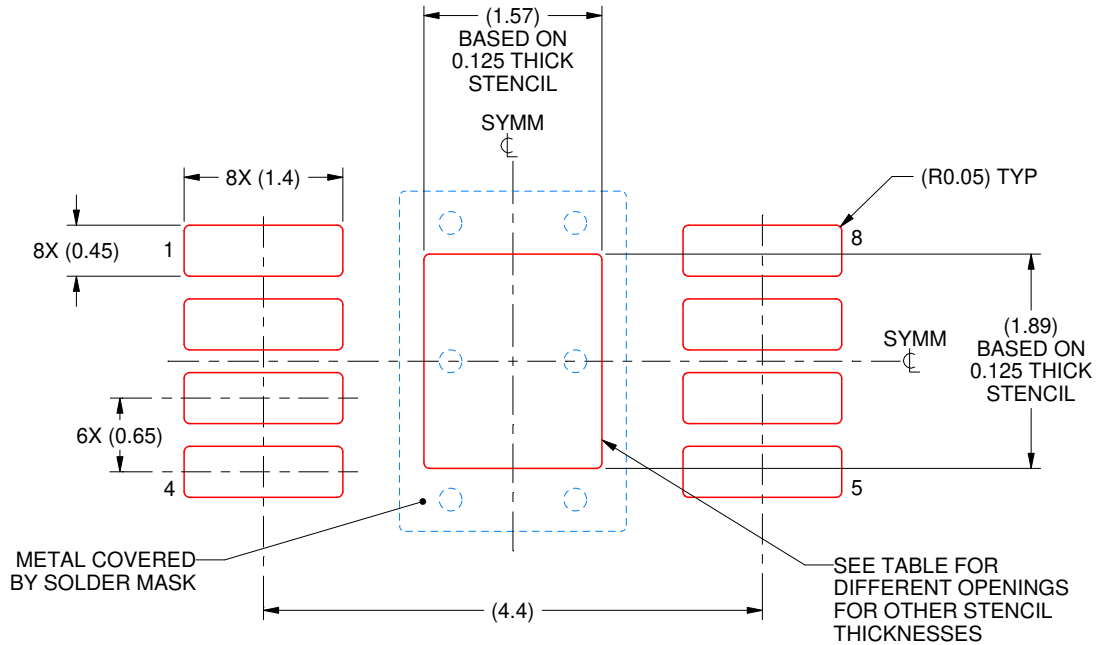
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGN0008D

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



**SOLDER PASTE EXAMPLE**  
 EXPOSED PAD 9:  
 100% PRINTED SOLDER COVERAGE BY AREA  
 SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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