



Phase-Locked Loop Clock Driver with 4 Clock Outputs

Product Features

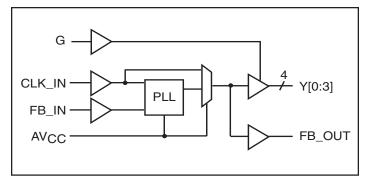
- High-Performance Phase-Locked-Loop Clock Distribution for Networking
- Registered DIMM Synchronous DRAM modules for server/workstation/PC applications
- Allows Clock Input to have Spread Spectrum modulation for EMI reduction
- Zero Input-to-Output delay
- Low jitter: Cycle-to-Cycle jitter ±75ps max.
- On-chip series damping resistor at clock output drivers for low noise and EMI reduction
- Operates at 3.3V V_{CC}
- Wide range of Clock Frequencies 80 to 134 MHz
- Package: Plastic 16-pin QSOP Package (Q)

Plastic 16-pin QSOP Package (QE) Pb-free

Product Description

The PI6C2504A features a low-skew, low-jitter, phase-locked loop (PLL) clock driver, distributing high-frequency clock signals for SDRAM and server applications. By connecting the feedback FB_OUT output to the feedback FB_IN input, the propagation delay from the CLK_IN input to any clock output will be nearly zero.

Logic Block Diagram

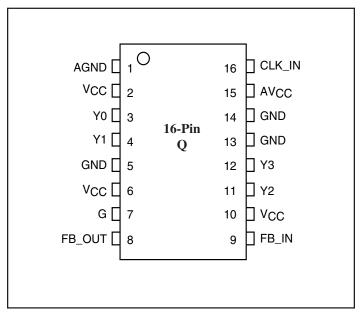


Functional Table

Inputs	Outputs				
G	Y[0:3]	FB_OUT			
L	L	CLK_IN			
Н	CLK_IN	CLK_IN			

Product Pin Configuration

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PS8501A 09/19/05



Pin Functions

Pin Name	Pin No.	Туре	Description
CLK_IN	16	I	Reference Clock input. CLK_IN allows spread spectrum clock input.
FB_IN	9	I	Feedback input. FB_IN provides the feedback signal to the internal PLL.
G	7	I	Output bank enable. When G is LOW, outputs Y[0:3] are disabled to a logic low state.
FB_OUT	8	O	Feedback output. FB_OUT is dedicated for external feedback. FB_OUT has an embedded series-damping resistor of the same value as the clock outputs Yx.
Y[0:3]	3,4,11,12	O	Clock outputs. These outputs provide low-skew copies of CLK_IN Each output has an embedded series-damping resistor.
AV _{CC}	15	Power	Analog power supply. For test purposes, AV_{CC} can be also used to bypass the PLL. When AV_{CC} is strapped to ground, PLL is bypassed and CLK_IN is buffered directly to the device outputs.
AGND	1	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
V _{CC}	2, 6, 10	Power	Power supply.
GND	5, 13, 14	Ground	Ground

DC $Specifications^{(1)}$ (Absolute maximum ratings over operating free-air temperature range)

Symbol	Parameter	Min.	Max.	Units	
VI	Input voltage range		V .05		
V _O	Output voltage range	-0.5	V _{CC} +0.5	V	
V _{I_DC}	DC input voltage		3.8		
I _{O_DC}	DC output current		100	mA	
Power	Maximum power dissipation at $T_A = 55^{\circ}C$ in still air		1.0	W	
T _{STG}	Storage temperature	-65	150	°C	

Note:

1. Stress beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.

Parameter	Test Conditions	V _{CC}	Min.	Тур.	Max.	Units
I_{CC}	$V_I = V_{CC}$ or GND; $I_O = 0^{(2)}$ Standby Current	3.6V			10	μΑ
C_{I}	$V_{\rm I} = V_{\rm CC}$ or GND	3.3V		4		ωŪ
Co	V _O =V _{CC} or GND	3.3 V		6		pF

Note:

2. Continuous Output Current

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V _{CC}	Supply voltage	3.0	3.6	
V _{IH}	High level input voltage	2.0		7.7
V _{IL}	Low level input voltage		0.8	V
$V_{\rm I}$	Input voltage	0	V_{CC}	
T _A	Operating free-air temperature	0	70	°C



$\textbf{Electrical Characteristics} \ (\textbf{Over Recommended Operating Free-Air Temperature Range Pree-Air Te$

Pull Up/Down Currents of PI6C2504A, V_{CC}=3.0V)

Symbol	Parameter	Condition	Min.	Max.	Units
T	Pull-up current	Vout = 2.4V		-13.6	
I _{OH}	Pull-up current	Vout = 2.0V		-22	A
T	Pull-down current	Vout = 0.8V	19		mA
I_{OL}	Pull-down current	Vout = 0.55V	13		

AC Specifications

(Timing requirements over recommended ranges of supply voltage and operating free-air temperature)

Symbol	Parameter	Min.	Max.	Units
F _{CLK}	Clock frequency PI6C2504A	80	134	MHz
D_{CYI}	Input clock duty cycle	40	60	%
	Stabilization Time after power up		1	ms

$\textbf{Switching Characteristics}^{(3)}$

(Over recommended ranges of supply voltage and operating free-air temperature, CL = 30pF)

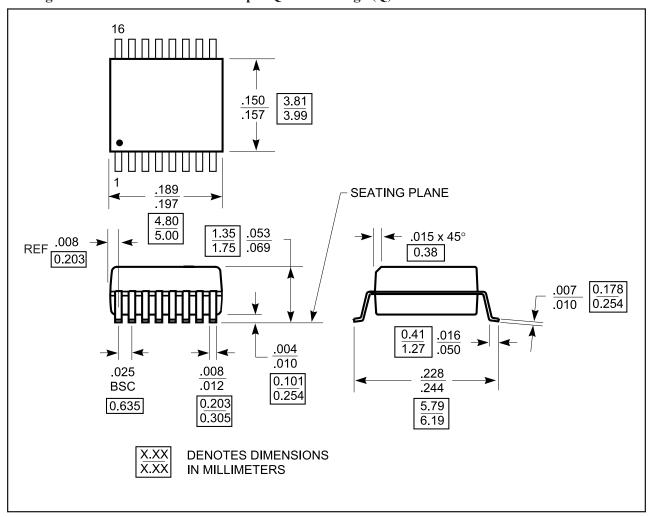
Parameter	From (Input)	To (Output)	$V_{CC} = 3.3V \pm 0.3V, 0-70^{\circ}C$			Units
rarameter	From (mpat)		Min.	Тур.	Max.	Units
tphase error without jitter	CLK_IN↑ at 100 & 66 MHz	FB_IN↑	-150		+150	. ps
Jitter, cycle-to-cycle	At 100 & 66 MHz		-75		+75	Р
Duty cycle		CLV OUT	45		55	%
tr, rise-time, 0.4V to 2.0V		CLK_OUT		1.0		no
tf, fall-time, 2.0V to 0.4V				1.1		ns

Note

3. These switching parameters are guaranteed by design.



Package Mechanical Information: 16-pin QSOP Package (Q).



Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
PI6C2504AQ	Q	16-pin QSOP	Commercial
PI6C2504AQE	QE	16-pin QSOP	Commercial

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