Amulet Technologies

COLOR CHIP FAMILY

AGB75LC04-QU-E
AGB75LC04-BG-E

Data Sheet

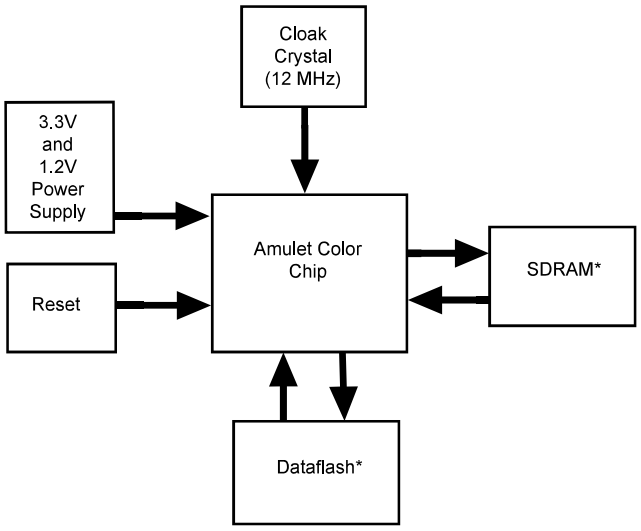
Highly Integrated Amulet GEM Graphical OS Chip™ for Color Graphical User Interfaces

Introduction:
Amulet's new GUI processor for color displays enables OEMs and design firms to take their products to the next level by implementing interactive color-rich GUIs designed in dynamic HTML. The GEM Graphical OS Chip™ includes all of the hardware and software required to turn a color LCD and touch panel into a user interface. Amulet's solution is perfect for many embedded system applications, including appliances, consumer electronics, industrial controls, medical equipment and office automation.

The accelerated graphic memory architecture allows for concurrent access to 3 individual memory subsystems for simultaneous program execution, LCD refresh, and frame buffer rendering.

Features:
- Integrated LCD Controller Supports Passive and Active displays up to 24 bits per pixel
- USB 2.0, TWI, UART, and SPI Interfaces
- Power Management Controller for Low Power Operation
- Directly Connects to 4- and 5-wire Resistive Touch Panels
- Up to 45 General Purpose IO Lines in BGA
- Drag-and-drop GUI Creation in Dynamic HTML
- PNG, GIF, and JPEG Image, and GIF Animation Support
- Built-in Royalty-free Graphical Operating System
- Inexpensive Development Tools
- PC Based UI Simulator Available to SimplifyUI Prototyping
- Built-in copy protection option to protect un-authorized duplication of user's product

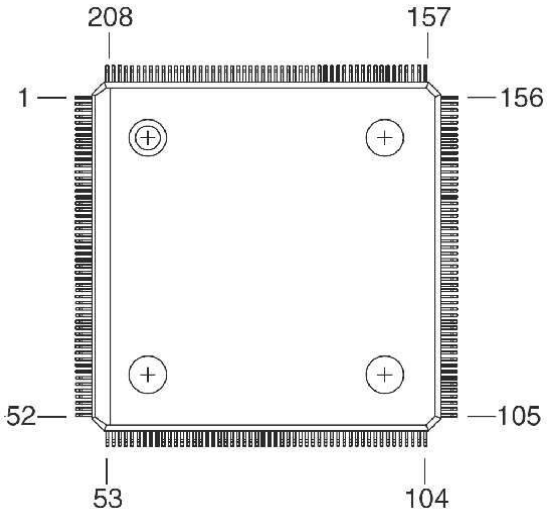
2 Typical Application Circuit

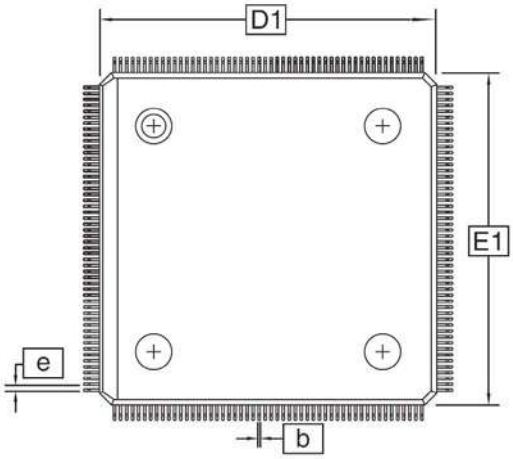


* Typical Serial Flash: Atmel AT45DB321D
* Typical SDRAM: ISSI IS42S32200E-6TL

3 Package and Pinout

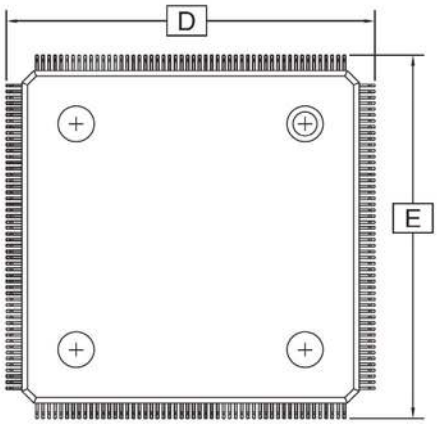
3.1 208-pin PQFP Package (Top View)





Top View

Side View



Bottom View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A1	0.25	–	0.50	
A2	3.20	3.40	3.60	
D	30.60 BSC			
D1	28.00 BSC			2, 3
E	30.60 BSC			
E1	28.00 BSC			2, 3
e	0.50 BSC			
b	0.17	–	0.27	4
L1	1.30 REF			

3.11 Device and 208-pin PQFP Package Maximum Weight

5670.1	mg

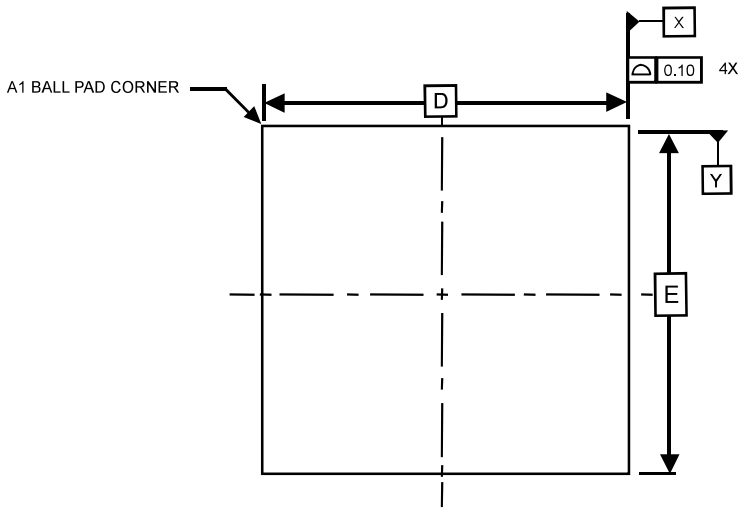
3.12 208-pin PQFP Package Characteristics

Moisture Sensitivity Level	3

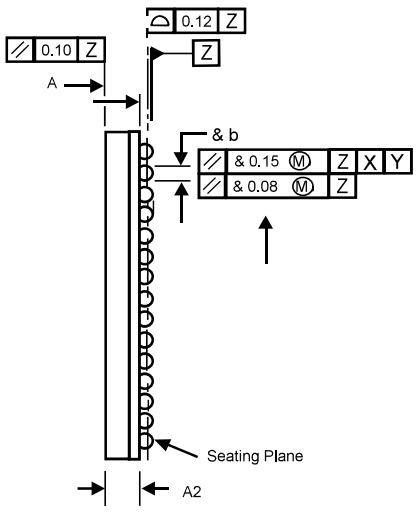
3.13 Package Reference

JEDEC Drawing Reference	MS-029
JESD97 Classification	e3

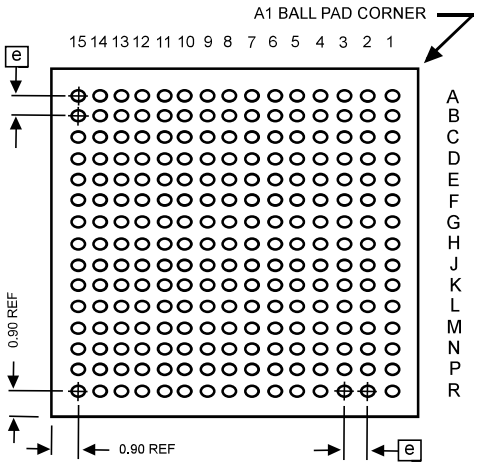
3.2 225-pin BGA Package



Top View



Side View



Bottom View
(225 Solder Balls)

Common Dimensions
(Unit of Measure = mm)

Symbol	MIN	NOM	MAX	NOTE
D		13.00 BSC		
E		13.00 BSC		
A	–	–	1.70	3
A1	0.25	–	–	3
A2	0.85	–	–	
e		0.80 BSC		
b	0.45	0.50	0.55	4

3.21 Device and 225-ball LFBGA Package Maximum Weight

365.2	mg

3.22 225-ball LFBGA Package Characteristics

Moisture Sensitivity Level	3

3.23 Package Reference

JEDEC Drawing Reference	MO-205
JESD97 Classification	e1

3.24 Soldering Information

Ball Land	0.530 mm +/- 0.03
Soldering Mask Opening	0.370 mm to 0.03 mm

Note:

1 The top package body size may be smaller than the bottom package size by as much as 0.15 mm

2 Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.

3 Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm.

3.3 Pin Descriptions

Pin Name	Type	Description
Power Supplies		
VCC 3.3V	Power	Supply Voltage 3.3V
VCORE 1.2V	Power	Supply Voltage 1.2V
GND	Ground	
Clocks, Osillators and PLL		See External Circuit Diagrams
Main OSC XIN	Input	Main Oscillator Input 12MHz
Main OSC XOUT	Output	Main Oscillator Output
PLLA Filter Input	Input	PLLA Filter
Shutdown, Wake-up Logic		
Shut Down Control	Output	Driven to 0. Do not drive over 1.2V
Wake-up Control	Input	0 to1.2V
Reset		
/Reset	I/O	Reset Active Low
External Bus Interface		
DATA0 - DATA31	I/O	Data Bus
ADDR0 - ADDR12	Output	Address Bus
SDRAM		
DQM0	Output	SDRAM makes data output go Hi-Z / blocks data input
DQM2	Output	SDRAM makes data output go Hi-Z / blocks data input
Pin Name	**Type**	**Description**
SDRAM BSO	Output	BS0 - SDRAM Bank Select
SDRAM BS1	Output	BS1 - SDRAM Bank Select
SDRAM CLK	Output	System Clock Active on positive going edge to sample all inputs
SDRAM CLK EN	Output	Active High Clock Enable freezes clock from the next operation
SDRAM WE	Output	Active Low Enables Write operation and Row precharges
SDRAM RAS	Output	Active Low Row Address Strobe
SDRAM CAS	Output	Active Low Column Address Strobe
SDRAM ADDR10	Output	Row and Column addresses
SDCS	Output	SDRAM Controller chip select
A2D/GPIO		See External Circuit Diagrams
A2D Ref	An. Input	Connect to Analog 3.3V
Touch Y-	An. Input	Touch panel Y-
Touch X-	An. Input	Touch panel X-
Touch Y+	An. Input	Touch panel Y+
Touch X+	An. Input	Touch panel X+
A2D	An. Input	A2D or GPIO

LCD Signals		
Pixel Data 0 - 23	Output	LCD Pixel Data
Pixel Clock / DCLK	Output	LCD Drive Signal. LCD crystal polarization clock.
Frame Clock	Output	Clock Pulse. Users can specify the whether to clock on rising or falling edge.
Hsync	Output	Hsync Signal . This output goes active for one clock period after all the serial data for the current line has been shifted to the TFT LCD.
LP	Output	Line Pulse Signal. This output goes active after all the serial data for the current line has been shifted to the STN LCD
Vsync	Output	Vsync Signal. TFT LCD First frame synchronization.
FO	Output	Frame Out Signal. STN LCD first frame synchronization
DISP	Output	Display Control Signal. LCD power (1 = ON, 0 = OFF)
OE	Output	Output Enable
Program Mode	Input	System Power Up Mode (1 = Program, 0 = Normal)
SPI		See External Circuit Diagrams
Pin Name	**Type**	**Description**
SPI SCLK	Output	SPI Clock
SPI MISO	Input	SPI Data In
SPI MOSI	Output	SPI Data Out
SPI CS1	Output	SPI Chip Select
SPI CS2	Output	SPI Chip Select
SPI CS3	Output	SPI Chip Select
SPI Flash CS	I/O	SPI Data Flash Chip Select
TWI		
SDA	I/O	Serial Data
SCL	I/O	Serial Clock
UARTs		
CommU TXD	Output	Asynchronous Serial-Data Output
CommU RXD	Input	Asynchronous Serial-Data Input
ProgU TXD	Output	Asynchronous Serial-Data Output
ProgURXD	Input	Asynchronous Serial-Data Input
UART2 TXD	Output	Asynchronous Serial-Data Output
UART2 RXD	Input	Asynchronous Serial-Data Input
UART2_SCK	Output	Serial Clock

UART2 RTS	Output	Request To Send
UART2 CTS	Input	Clear To Send
USB		See External Circuit Diagrams
USB DDM	Analog	USB Device Port Data -
USB DDP	Analog	USB Device Port Data+
VBUS	Input	Vbus Monitor for host detection
GPIO		
GPIOn	I/O	Has a 100K programmable pull-up
Programmable Timers		
PWM0	Output	Programmable Clock 0
PWM1	Output	Programmable Clock 1
PWM2	Output	Programmable Clock 2
Reserved		
RSVD		Reserved Test Pins
N/C		No Connection

Pin Name	Type	Description
Touch Panel		
TPCal	Input	Touch Panel Calibration (0=Normal, 1=Calibrate)

3.4 208-pin PQPF Package Pinout

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VCC 3.3V + pullup	53	LP / Hsync	105	ADDR5	157	VCORE 1.2V
2	VCC 3.3V + pullup	54	FO / Vsync	106	GND	158	GND
3	DATA31	55	VCC 3.3V	107	VCC 3.3V	159	N/C
4	N/C	56	GND	108	ADDR4	160	GND
5	DATA30	57	DISP	109	ADDR3	161	VCORE 1.2V
6	VCC 3.3V + pullup	58	TWI SDA*	110	VCORE 1.2V	162	Shut Down Control
7	DATA29	59	TWI SCLK*	111	UART2 RXD	163	Wake-Up Control
8	RSVD	60	N/C	112	ADDR2	164	N/C
9	DATA28	61	PWM0	113	UART2 TXD	165	RSVD
10	GND	62	PWM1	114	GND	166	GND
11	DATA27	63	FC / OE	115	N/C	167	A2D Ref
12	VCC 3.3V	64	N/C	116	ADDR1	168	Touch Y-
13	DATA26	65	GND	117	SDRAM CLK EN	169	Touch X-
14	Reset	66	GND	118	ADDR0	170	Touch Y+
15	DATA25	67	PWM2	119	SDRAM WE	171	Touch X+
16	N/C	68	VCC 3.3V	120	VCC 3.3V	172	A2D4 / GPIO4*
17	DATA24	69	Pixel Data 12	121	SDRAM CLK	173	VCC 3.3V
18	CommU RXD	70	Pixel Data 0	122	SDRAM DQM2	174	GND
19	Pixel Data 8	71	Pixel Data 13	123	Pixel Data 20	175	GND
20	CommU TXD	72	Pixel Data 1	124	GND	176	DATA23
21	Pixel Data 9	73	Pixel Data 14	125	SDRAM DQM0	177	VCC 3.3V
22	VCORE 1.2V	74	Pixel Data 2	126	DATA15	178	DATA22
23	Pixel Data 10	75	Pixel Data 15	127	DATA14	179	GND
24	GND	76	VCORE 1.2V	128	DATA13	180	DATA21
25	Pixel Data 11	77	VCC 3.3V	129	DATA12	181	SDRAM CS
26	Program Mode	78	Pixel Data 3	130	DATA11	182	DATA20
27	TPCal	79	GND	131	DATA10	183	VCORE 1.2V
28	ADDR6	80	Pixel Data 4	132	DATA9	184	DATA19
29	ADDR7	81	Pixel Data 5	133	DATA8	185	DATA18
30	VCC 3.3V	82	Pixel Data 6	134	DATA7	186	DATA17
31	ADDR8	83	Pixel Data 7	135	GND	187	DATA16
32	ADDR9	84	VBUS	136	DATA6	188	N/C
33	N/C	85	SDRAM DQM3	137	VCC 3.3V	189	N/C
34	ADDR11	86	ProgU TXD	138	DATA5	190	SPI CS3
35	ADDR12	87	Pixel Data 16	139	Pixel Data 21	191	SPI CS2
36	VCORE 1.2V	88	GND	140	GND	192	SPI CS1
37	GND	89	Pixel Data 17	141	Pixel Data 22	193	GND
38	GND	90	ProgU RXD	142	Pixel Data 23	194	VCORE 1.2V
39	SDRAM CAS	91	Pixel Data 18	143	UART2 SCK	195	GND
40	N/C	92	SPI MISO	144	VCORE 1.2V	196	SDRAM DQM1
41	SDRAM RAS	93	Pixel Data 19	145	UART2 RTS	197	N/C
42	SDRAM BS 0	94	VCC 3.3V	146	GND	198	VCC 3.3V
43	ADDR10	95	N/C	147	UART2 CTS	199	VCORE 1.2V
44	VCC 3.3V	96	VCORE 1.2V	148	USB DDM	200	GND
45	SDRAM BS1	97	GPIO2*	149	USB DDP	201	GND

Pin	Name	Pin	Name	Pin	Name	Pin	Name
46	N/C	98	SPI MOSI	150	GPIO3*	202	Main OSC XIN
47	N/C	99	SPI SCLK	151	VCC 3.3V	203	Main OSC XOUT
48	N/C	100	GND	152	DATA4	204	VCORE 1.2V
49	N/C	101	SPI Flash CS	153	DATA3	205	VCC 3.3V
50	GND	102	N/C	154	DATA2	206	GND
51	N/C	103	N/C	155	DATA1	207	PLLA Filter Input
52	Pixel Clock	104	VCC 3.3V	156	DATA0	208	GND

NOTE: Multi-function Pin. See Multiplex I/O Section for more information.

3.5 225-pin BGA Package Pinout

Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	GPIO4	D13	LP / Hsync	H10	VCORE 1.2V	M7	DATA22
A2	SPI SCLK	D14	GPIO35	H11	DATA5	M8	A2D7 / GPIO44*
A3	SPI MOSI	D15	GPIO6	H12	TPCal	M9	N/C
A4	N/C	E1	ADDR1	H13	Program Mode	M10	GPIO30
A5	Pixel Data 17	E2	ADDR2	H14	ADDR7	M11	GND
A6	VBUS	E3	GPIO40*	H15	ADDR8	M12	N/C
A7	Pixel Data 5	E4	UART2 TXD	J1	DATA7	M13	VCC 3.3V + pullup
A8	Pixel Data 15	E5	VCC 3.3V	J2	DATA6	M14	DATA28
A9	Pixel Data 12	E6	SPI Flash CS	J3	Pixel Data 23	M15	N/C
A10	N/C	E7	N/C	J4	DATA8	N1	GPIO21
A11	N/C	E8	Pixel Data 1	J5	USB DDP	N2	GPIO24
A12	GPIO12	E9	Pixel Data 0	J6	DATA2	N3	VCORE 1.2V
A13	DISP	E10	TWI SCLK	J7	GND	N4	N/C
A14	GPIO36	E11	GPIO11	J8	GND	N5	Touch X+
A15	N/C	E12	Pixel Clock	J9	GND	N6	VCC 3.3V
B1	ADDR4	E13	GPIO7	J10	N/C	N7	DATA20
B2	GPIO15	E14	N/C	J11	Pixel Data 9	N8	SPI CS3
B3	GPIO14	E15	ADDR10	J12	CommU RXD	N9	GPIO27
B4	GPIO2	F1	SDRAM WE	J13	CommU TXD	N10	N/C
B5	ProgU TXD	F2	ADDR0	J14	Pixel Data 11	N11	PLLA Filter Input
B6	Pixel Data 16	F3	UART2 RXD	J15	ADDR6	N12	Main OSC XIN
B7	Pixel Data 7	F4	SDRAM CLK EN	K1	Pixel Data 21	N13	VCC 3.3.V
B8	Pixel Data 3	F5	GPIO19	K2	Pixel Data 22	N14	DATA29
B9	Pixel Data 14	F6	SDRAM DQM0	K3	GPIO3	N15	Reset
B10	PWM2	F7	VCC 3.3V	K4	UART2 CTS	P1	DATA4
B11	PWM0	F8	Pixel Data 18	K5	GPIO22	P2	DATA3
B12	TWI SDA	F9	VCC 3.3V	K6	Wake-Up Control	P3	Shut Down Control
B13	GPIO9	F10	N/C	K7	VCC 3.3V	P4	RSVD
B14	GPIO34	F11	GPIO8	K8	VCORE 1.2V	P5	Touch Y-
B15	N/C	F12	GPIO5	K9	VCC 3.3V	P6	A2D5 / GPIO42
C1	GPIO18	F13	ADDR12	K10	Main OSC XOUT	P7	DATA21
C2	N/C	F14	SDRAM BS0	K11	DATA25	P8	DATA16
C3	GPIO16	F15	N/C	K12	VCC 3.3V + pullup	P9	SPI CS1
C4	GPIO39	G1	Pixel Data 20	K13	DATA24	P10	GPIO28

Pin	Name	Pin	Name	Pin	Name	Pin	Name
C5	SPI MISO	G2	SDRAM CLK	K14	Pixel Data 8	P11	GND
C6	Pixel Data 19	G3	SDRAM DQM2	K15	Pixel Data 10	P12	SDRAM DQM1
C7	ProgU RXD	G4	DATA14	L1	UART2 SCK	P13	VCORE 1.2V
C8	Pixel Data 4	G5	DATA15	L2	UART2 RTS	P14	RSVD
C9	Pixel Data 13	G6	VCORE 1.2V	L3	DATA1	P15	DATA27
C10	FC/ OE	G7	GND	L4	GPIO25	R1	N/C
C11	GPIO10	G8	GND	L5	VCORE 1.2V	R2	A2D Ref
C12	GPIO38	G9	GND	L6	GNDBU	R3	Touch Y+
C13	N/C	G10	VCC 3.3V	L7	A2D4 / GPIO4*	R4	A2D6 / GPIO43*
C14	N/C	G11	SDRAM RAS	L8	SDRAM CS	R5	GND
C15	SDRAM BS 1	G12	N/C*	L9	DATA17	R6	DATA23
D1	GPIO20	G13	ADDR9	L10	GND	R7	DATA19
D2	ADDR3	G14	SDRAM CAS	L11	DATA31	R8	N/C
D3	ADDR5	G15	ADDR11	L12	VCC 3.3V + pullup	R9	SPI CS2
D4	N/C	H1	DATA10	L13	GPIO33	R10	GPIO26
D5	GPIO17	H2	DATA9	L14	DATA30	R11	GPIO29
D6	GPIO13	H3	DATA13	L15	DATA18	R12	GPIO31
D7	SDRAM DQM3	H4	DATA11	M1	USB DDM	R13	GPIO32
D8	Pixel Data 6	H5	DATA12	M2	GPIO23	R14	VCORE 1.2V
D9	Pixel Data 2	H6	VCC 3.3V	M3	DATA0	R15	DATA26
D10	PWM1	H7	GND	M4	GND		
D11	GPIO37	H8	GND	M5	GND		
D12	FO / Vsync	H9	GND	M6	Touch X-		

NOTE: Multi-function Pin. See Multiplex I/O Section for more information.

3.6 Multiplex I/O

The pins shown in the following tables have multiple function per pin. The tables describe the peripheral function, general purpose input and general purpose output.

4 Function Pins:

Pin	Function A	Function B	General Purpose Input	General Purpose Output
58 / B12	TWI_SDA	UART2 RXD	Yes (GPIO0)	Yes (GPIO0)
59 / E10	TWI_SCLK	UART2 TXD	Yes (GPIO1)	Yes (GPIO1)

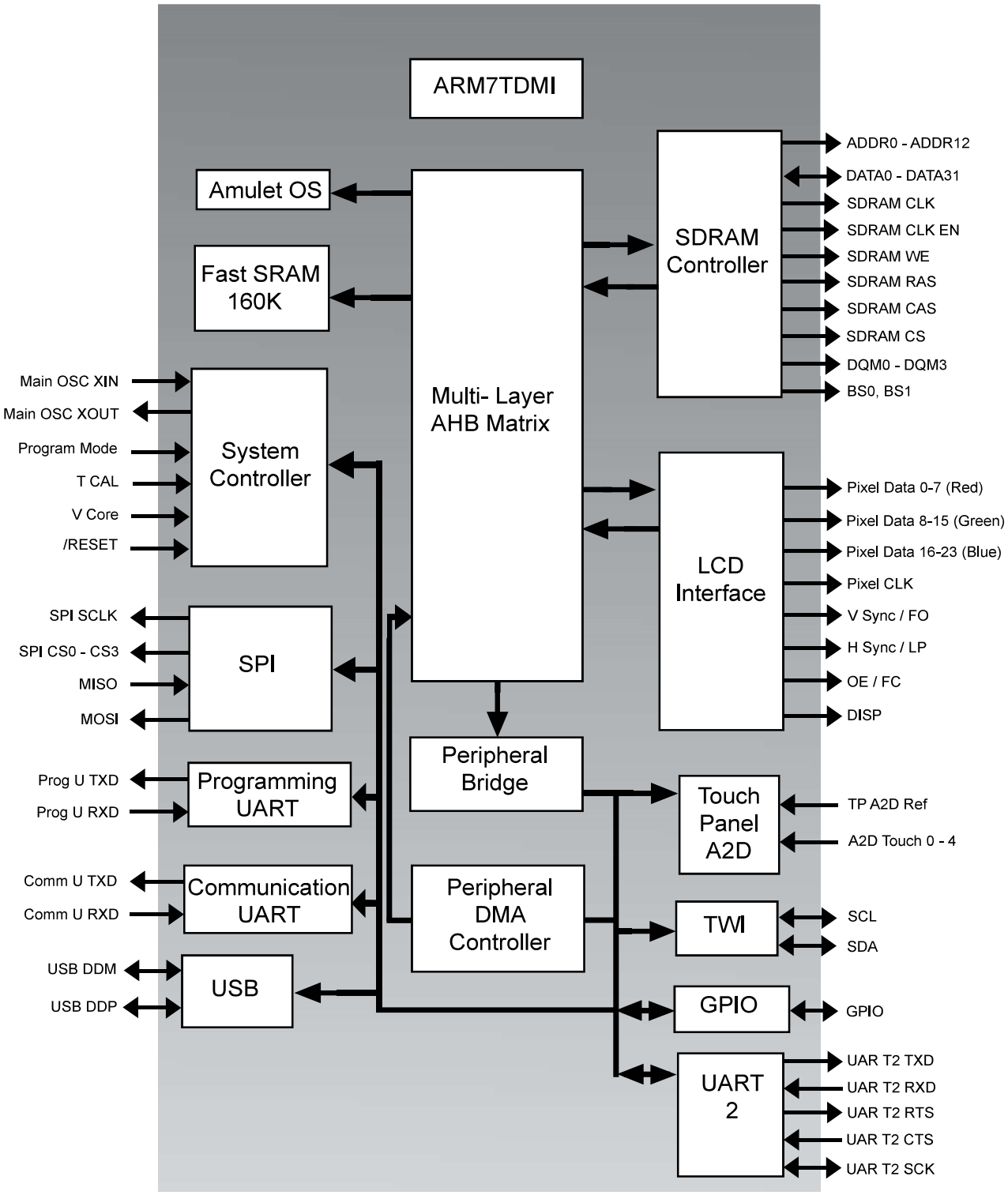
3 Function Pins:

Pin	Function A	General Purpose Input	General Purpose
208 PQFP			
172	A2D (A2D4)	Yes (GPIO4)	Yes (GPIO4)
225 BGA			
N5	A2D (A2D3)	Yes (GPIO3)	Yes (GPIO3)
L7	A2D (A2D4)	Yes (GPIO4)	Yes (GPIO4)
P6	A2D (A2D5)	Yes (GPIO42)	Yes (GPIO42)
R4	A2D (A2D6)	Yes (GPIO43)	Yes (GPIO43)
M8	A2D (A2D7)	Yes (GPIO 44)	Yes (GPIO44)

2 Function Pins:

Pin	General Purpose Input	General Purpose Output
208 PQFP		
97	Yes (GPIO2)	Yes (GPIO2)
150	Yes (GPIO3)	Yes (GPIO3)
225 BGA		
B4	Yes (GPIO2)	Yes (GPIO2)
K3	Yes (GPIO3)	Yes (GPIO3)
F12	Yes (GPIO5)	Yes (GPIO5)
D15	Yes (GPIO6)	Yes (GPIO6)
E13	Yes (GPIO7)	Yes (GPIO7)
F11	Yes (GPIO8)	Yes (GPIO8)
B13	Yes (GPIO9)	Yes (GPIO9)
C11	Yes (GPIO10)	Yes (GPIO10)
E11	Yes (GPIO11)	Yes (GPIO11)
A12	Yes (GPIO12)	Yes (GPIO12)
D6	Yes (GPIO13)	Yes (GPIO13)
B3	Yes (GPIO14)	Yes (GPIO14)
B2	Yes (GPIO15)	Yes (GPIO15)
C3	Yes (GPIO16)	Yes (GPIO16)
D5	Yes (GPIO17)	Yes (GPIO17)
C1	Yes (GPIO18)	Yes (GPIO18)
F5	Yes (GPIO19)	Yes (GPIO19)
D1	Yes (GPIO20)	Yes (GPIO20)
N1	Yes (GPIO21)	Yes (GPIO21)
K5	Yes (GPIO22)	Yes (GPIO22)
M2	Yes (GPIO23)	Yes (GPIO23)
N2	Yes (GPIO24)	Yes (GPIO24)
L4	Yes (GPIO25)	Yes (GPIO25)
R10	Yes (GPIO26)	Yes (GPIO26)
N9	Yes (GPIO27)	Yes (GPIO27)
P10	Yes (GPIO28)	Yes (GPIO28)
R11	Yes (GPIO29)	Yes (GPIO29)
M10	Yes (GPIO30)	Yes (GPIO30)
R12	Yes (GPIO31)	Yes (GPIO31)
R13	Yes (GPIO32)	Yes (GPIO32)
L13	Yes (GPIO33)	Yes (GPIO33)
B14	Yes (GPIO34)	Yes (GPIO34)
D14	Yes (GPIO35)	Yes (GPIO35)
A14	Yes (GPIO36)	Yes (GPIO36)
D11	Yes (GPIO37)	Yes (GPIO37)
C12	Yes (GPIO38)	Yes (GPIO38)
C4	Yes (GPIO39)	Yes (GPIO39)
E3	Yes (GPIO40)	Yes (GPIO40)
A1	Yes (GPIO41)	Yes (GPIO41)

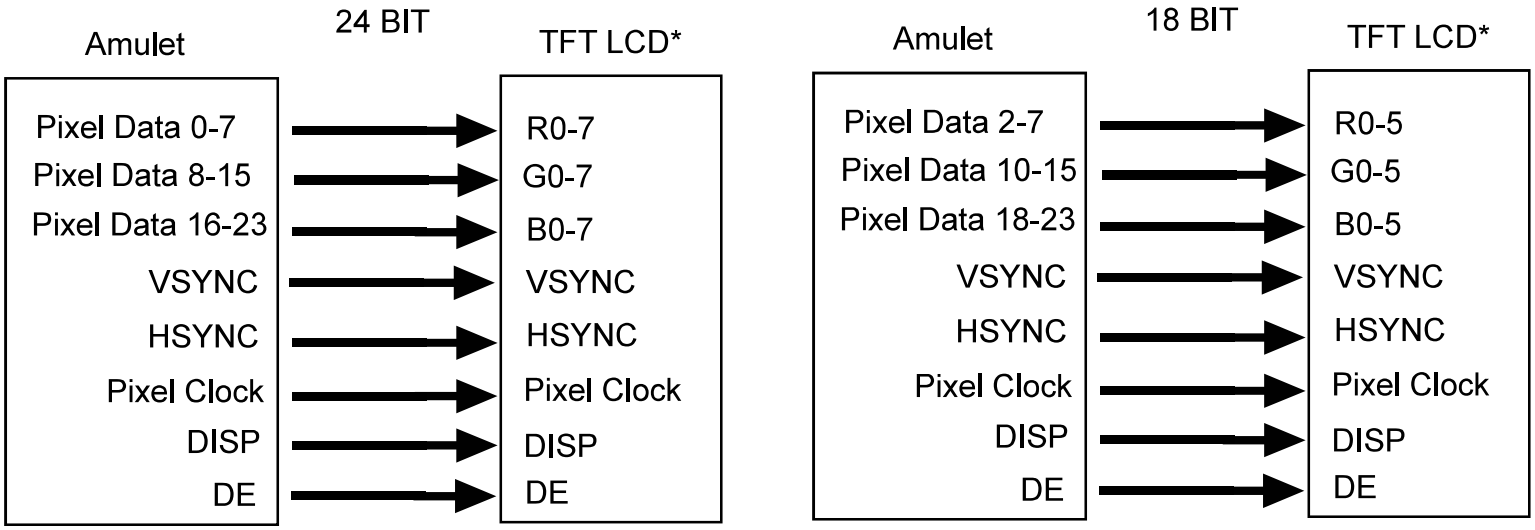
4 Block Diagram



5 Connection Diagrams

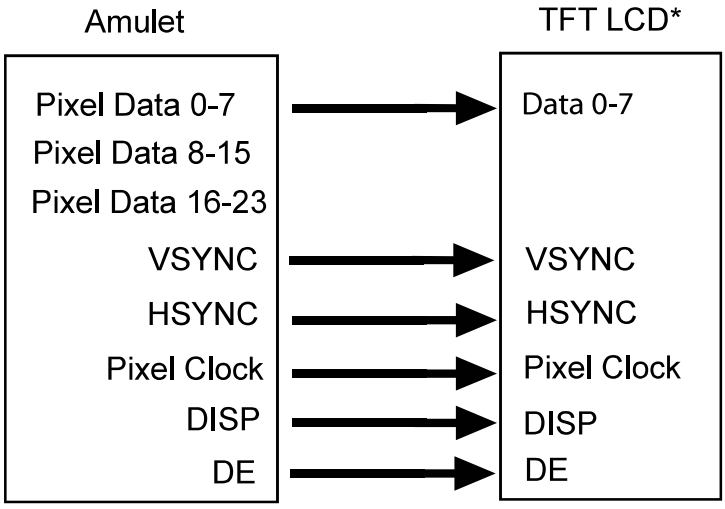
5.1 LCD Connections

5.11 TFT LCD Connection



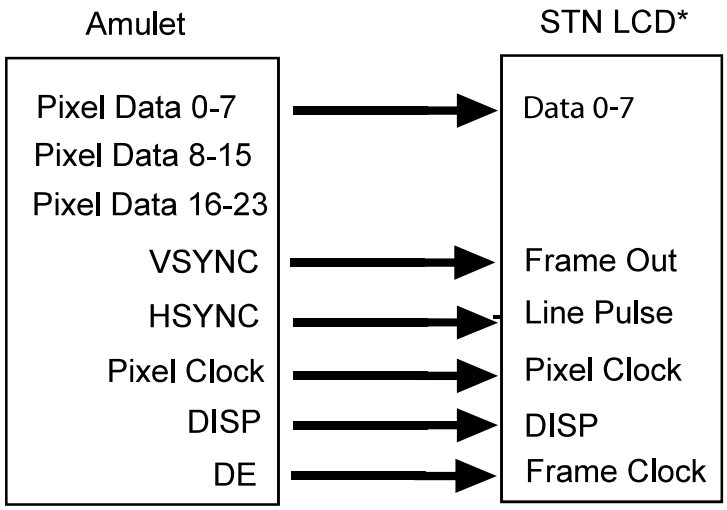
**Note: These diagrams assume LSB is always 0. Some displays may vary*

5.12 TFT UPS052 LCD Connection



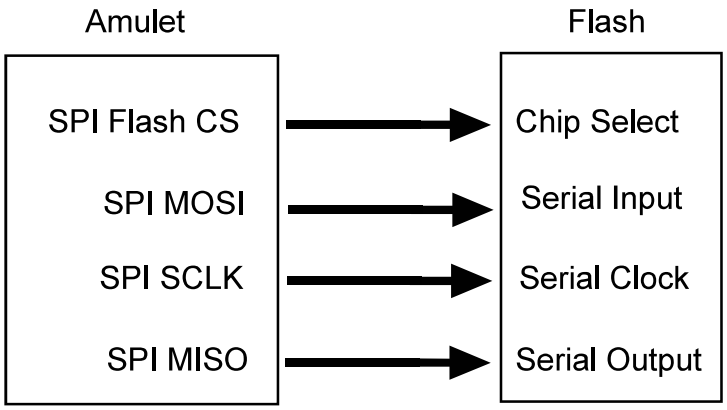
**Note: These diagrams assume LSB is always 0. Some displays may vary*

5.13 STN LCD Connection



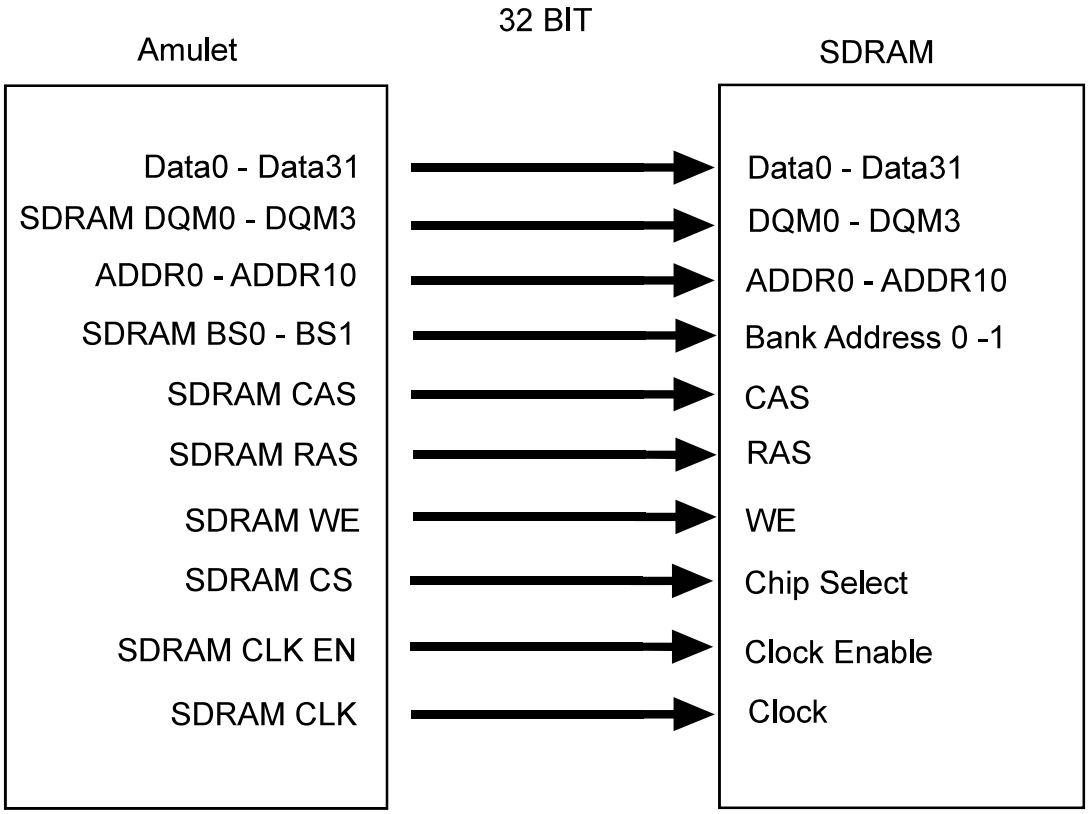
**Note: These diagrams assume LSB is always 0. Some displays may vary*

5.2 Flash Connection



5.3 SDRAM Connection

5.31 32-bit Data SDRAM



6 Pixel Data Connections for color depth support

6.1 TFT LCD Connection Table, 1 clock per pixel

Pixel Data Connection →

LCD Bit Depth ↓

Amulet	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
24	R0	R1	R2	R3	R4	R5	R6	R7	G0	G1	G2	G3	G4	G5	G6	G7	B0	B1	B2	B3	B4	B5	B6	B7
18	N/C	N/C	R0	R1	R2	R3	R4	R5	N/C	N/C	G0	G1	G2	G3	G4	G5	N/C	N/C	B0	B1	B2	B3	B4	B5
16	N/C	N/C	N/C	R0	R1	R2	R3	R4	N/C	N/C	G0	G1	G2	G3	G4	G5	N/C	N/C	N/C	B0	B1	B2	B3	B4
15	N/C	N/C	N/C	R0	R1	R2	R3	R4	N/C	N/C	N/C	G0	G1	G2	G3	G4	N/C	N/C	N/C	B0	B1	B2	B3	B4

Note: Amulet Pins 0, 8, and 16 are the least significant bits of the Red, Green, and Blue pixel data, respectively

6.2 TFT UPS052 LCD Connection Table

Pixel Data Connection →

LCD Bit Depth ↓

Amulet	0	1	2	3	4	5	6	7
24	0	1	2	3	4	5	6	7
18	N/C	N/C	0	1	2	3	4	5
15	N/C	N/C	N/C	0	1	2	3	4

6.3 STN LCD Connection Table

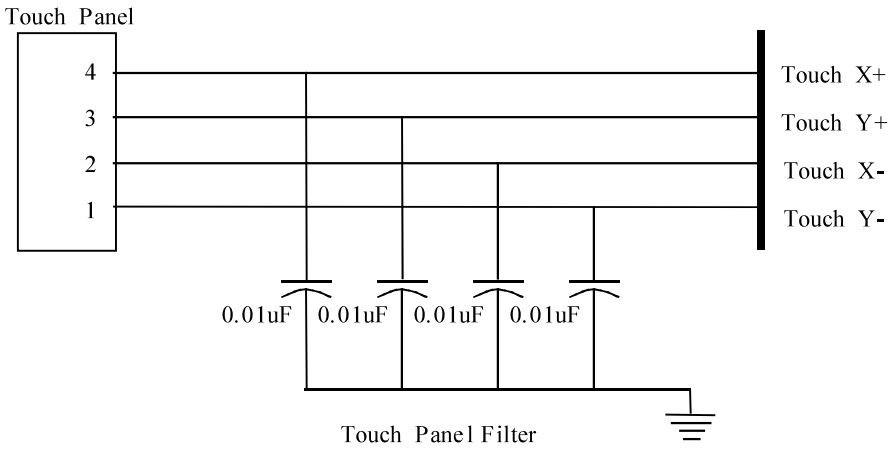
Pixel Data Connection →

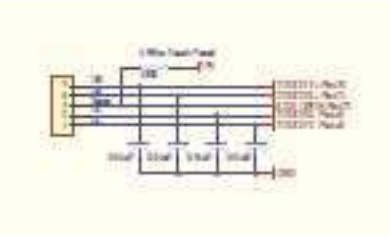
LCD Bit Depth ↓

Amulet	0	1	2	3	4	5	6	7
8	0	1	2	3	4	5	6	7
4	0	1	2	3	N/C	N/C	N/C	N/C

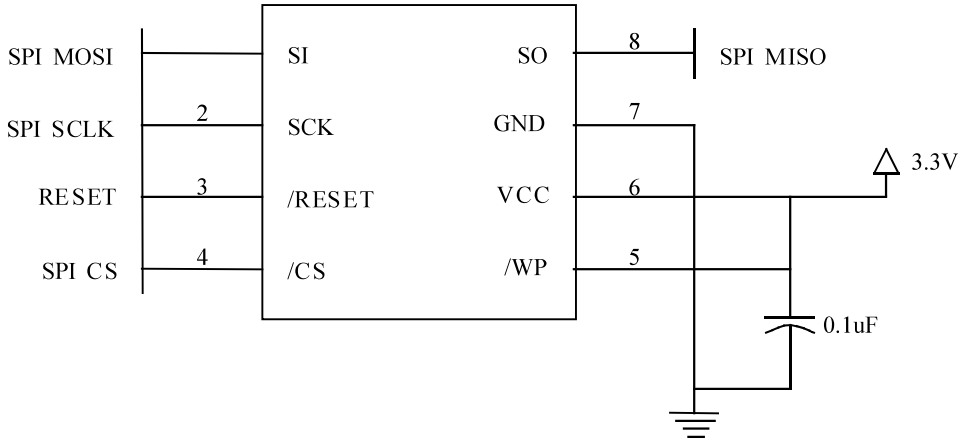
7 External Circuit Diagrams

7.1 4 Wire Touch Panel Filter+

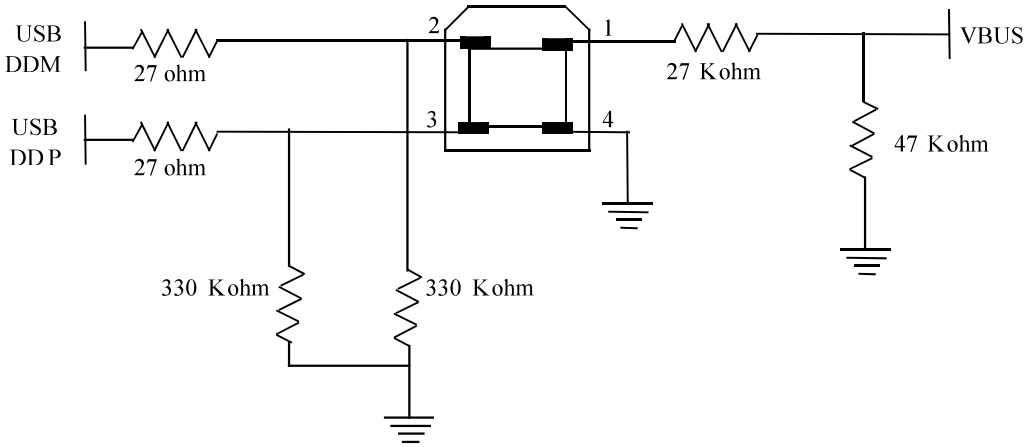




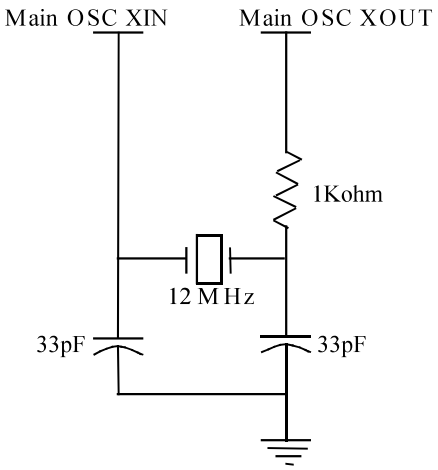
7.2 Serial Data Flash



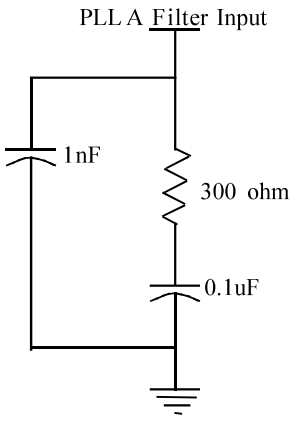
7.3 USB Interface



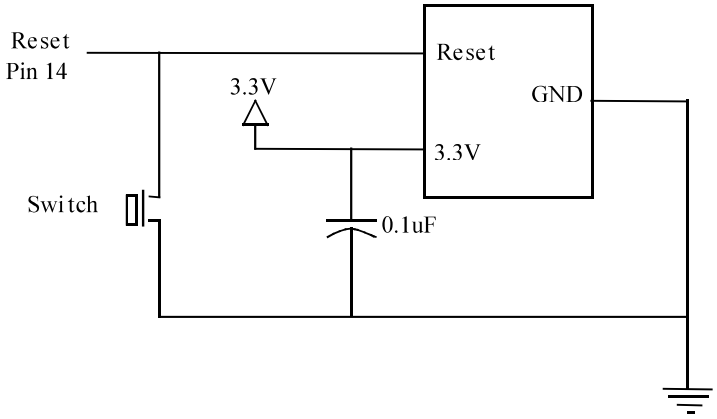
7.4 Main OSC Interface



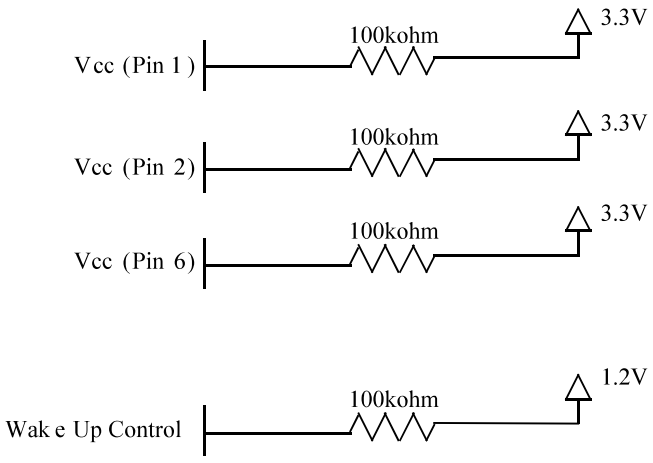
7.5 PLLA Filter



7.6 Reset Circuit



7.7 Mandatory Pullups



8 Environmental, Electrical and Power Specifications

AGB75LC04-XX-X: 208 pin: AGB75LC04-QU-E / 225 pin: AGB75LC04-BG-E

8.1 Recommended Operating Conditions

Power supply V_{cc}	3.0V to 3.6V, 3.3V nominal
Power supply V_{core}	1.08V to 1.32V, 1.2V nominal

8.2 Environmental Specifications

Operating temperature	-40 to +85°C
Storage temperature	- 60°C to +150°C

8.3 DC Characteristics

V_{core} Supply current	22mA @ 1.2V		
V_{DDIO} Supply current	TBD		
V_L Input Low Level Voltage	-0.3V to 0.8V		
V_H Input High Level Voltage	2V to (V_{CC} + 0.3V)		
R_{pullup} Pull Up Resistance	70 kOhm to 175 kOhm, 100 kOhm nominal		
I_O Output Current	8mA		
I_{SC} Static Current	Vcore = 1.2V, excluding Power on Reset All inputs driven, NRST=1	T = 25°C	600uA
	Vcore = 1.2V, logic cells consumption, including Power on Reset All inputs driven, WKUP=0	T = 25°C	30uA

*The DC characteristics above are applicable to the operating temperature range: T_A = -40°C to 85°C, unless otherwise specified and are certified for a junction temperature up to T_J = 100°C. The values are estimated values with operating conditions as follows:

- $V_{DDIO} = V_{DDPLLA} = V_{AVDD} = 3.3V$
- $V_{DDCORE} = V_{DDBU} = V_{DDOSC} = V_{DDOSC32} = 1.2V$
- TA = 25°C
- There is no consumption on the I/Os of the device

8.4 SDRAM

8.41 Capacitance Load on Data, Control and Address Lines

3.3V	50pF
1.8V	30pF

8.42 Capacitance Load on SDCK Pad

3.3V	10pF
1.8V	10pF

8.5 RoHS compliant Package Options

208-PQFP	28x28x3.4mm, 0.5 mm pin pitch
225-ball LFBGA	13x13x1.4mm, 0.8 mm ball pitch

8.6 Power Consumption

The advanced power management controller has a very slow clock operating mode and software programmable power optimization capabilities. Along with a reset controller and shutdown controller, this gives the **AGB75LC04-XX-X** several low-power options.

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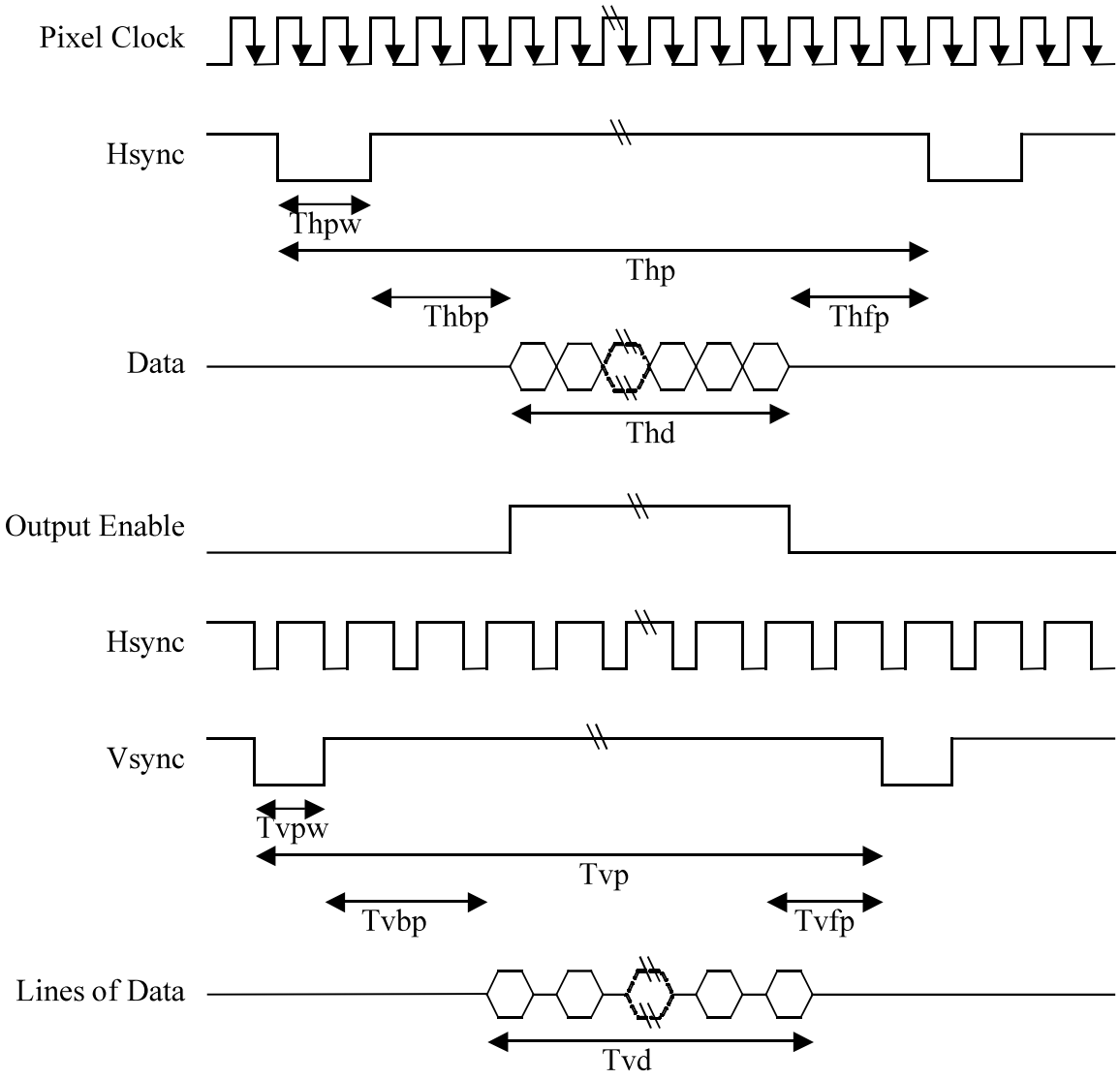
9 Timing Specifications

9.1 LCD

The following tables and figures show basic information on interfacing with the LCD controller. For more detailed information on how to configure the LCD controller, please refer to the HTML Compiler Help files.

9.11 TFT

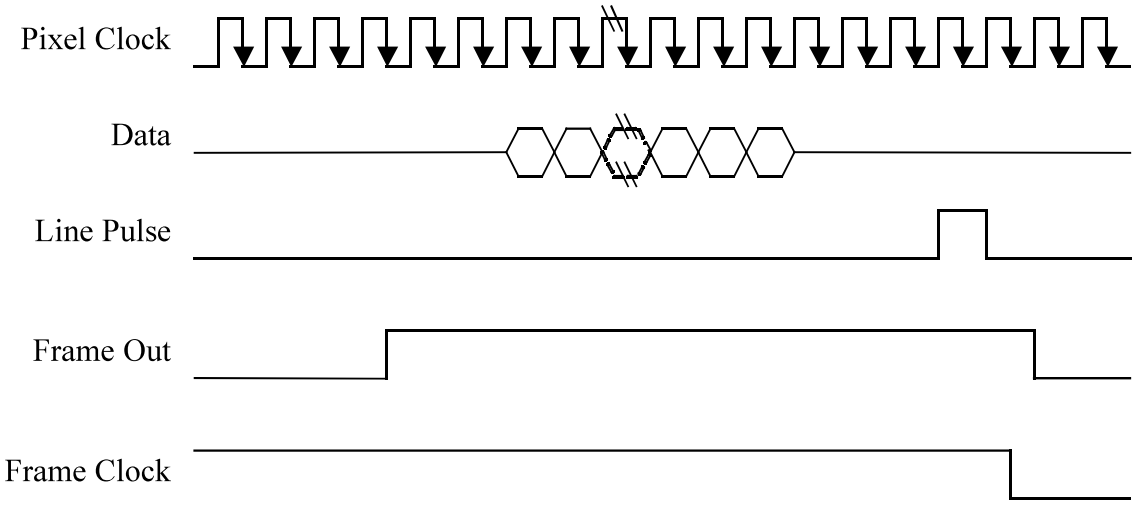
Item	Symbol	Unit
Hsync Pulse Width	Thpw	Pixel Clock
Hsync Back Porch	Thbp	Pixel Clock
Hsync Period	Thp	Pixel Clock
Hsync Display Data	Thd	Pixel Clock
Hsync Front Porch	Thfp	Pixel Clock
Vsync Pulse Width	Tvpw	Hsync
Vsync Back Porch	Tvbp	Hsync
Vsync Period	Tvp	Hsync
Vsync Display Data	Tvd	Hsync
Vsync Front Porch	Tvfp	Hsync



Item		Typical	Unit
Pixel Data	Setup Time	0.75 * Pixel Clock Period	ns
	Hold Time	0.25 * Pixel Clock Period	ns

9.12 STN

Item	Symbol	Unit
Line Pulse Width	Thpw	System Clock
Line Pulse Porch	Thbp	System Clock
Frame Frequency	Thp	80MHz Clock



9.121 STN Monochrome and Grayscale

Item		Typical	Unit
Pixel Data	Setup Time	0.75 * Pixel Clock Period	ns
	Hold Time	0.25 * Pixel Clock Period	ns

9.122 STN Color

Item		Typical	Unit
Pixel Data	Setup Time	0.5 * Pixel Clock Period	ns
	Hold Time	0.5 * Pixel Clock Period	ns

9.2 SPI

Item		Min	Max	Unit
MISO	Setup Time before SPI SCLK rises	3.66		ns
	Hold Time after SPI SCLK rises	0		ns
	Setup Time before SPI SCLK falls	3.52		ns
	Hold Time after SPI SCLK falls	0		ns

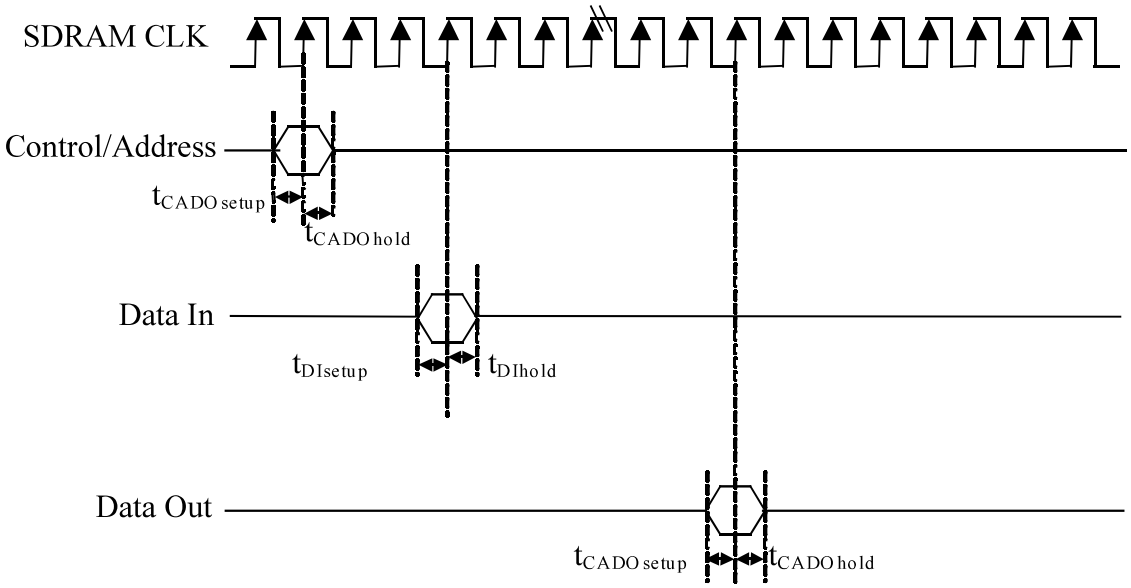
SPI SCLK rising to MOSI Valid		-0.6	ns
SPI SCLK rising to MOSI change	-0.81		ns
SPI SCLK falling to MOSI Valid		-0.19	ns
SPI SCLK falling to MOSI change	-0.67		ns

NOTE: Load Capacitance is 8pF for MISO and 6pF for SPI SCLK and MOSI

9.3 TWI

Item		Typical	Unit
Serial Data	Setup Time	TBD	ns
	Hold Time	TBD	ns

9.4 SDRAM



Item		Symbol	Typical	Unit
Control/Address/Data Out[1]	Setup Time	$t_{CADOsetup}$	5.51	ns
	Hold Time	$t_{CADOhold}$	5.95	ns
Data Input	Setup Time	$t_{DIsetup}$	0.6	ns
	Hold Time	t_{DIhold}	0.62	ns

9.41 SDRAM PC100 Characteristics (3.3V Supply, CL=2)

Item	Min	Max	Unit
SDRAM Frequency		100	MHz
Control/Address/Data in Setup[1]	2		ns
Control/Address/Data in Hold[1]	1		
Data Out Access Time after SDRAM CLK rising		6	ns
Data Out Change Time after SDRAM CLK rising	3		ns

9.42 SDRAM PC133 Characteristics (3.3V Supply, CL=3)

Item	Min	Max	Unit
SDRAM Frequency		133	MHz
Control/Address/Data in Setup[1]	1.5		ns
Control/Address/Data in Hold[1]	0.8		
Data Out Access Time after SDRAM CLK rising		5.4	ns
Data Out Change Time after SDRAM CLK rising	3.0		ns

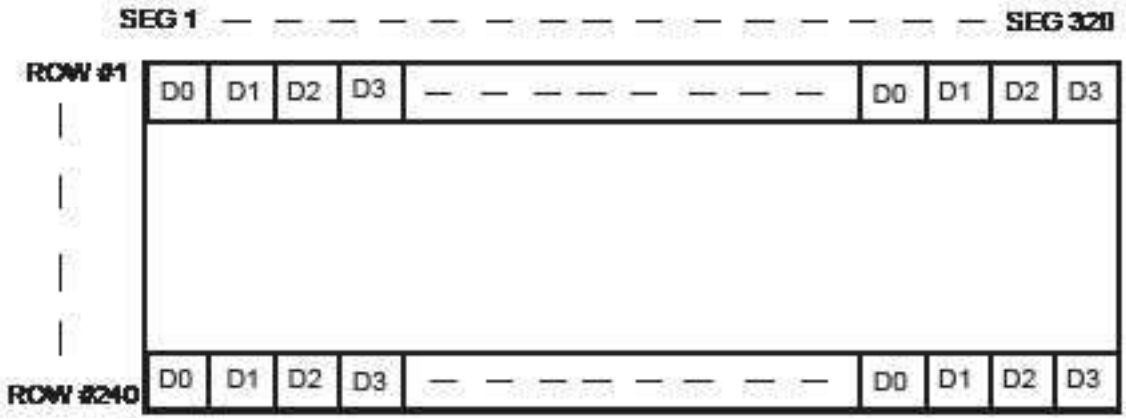
9.5 USB

Item	Min	Max	Unit
Transition Rise Time[2]	4	20	ns
Transition Fall Time[2]	4	20	ns
Rise/Fall Time Matching[2]	90	111.11	%

NOTE:

1. *Control/Address is the set of the following timings: ADDR0-ADDR12, SDRAM10, SDRAM CAS, SDRAM RAS, SDRAM CLK, SDRAM CLK EN, BSx, DOMx and SDRAM WE.*
2. *In Full Speed wit Load Capacitance of 50pF.*

10 Display Data Pattern



11 System Parameters

LCDs supported	Up to 800xRGBx600 resolution. Active and Passive display support
Interfaces supported	USB, UART, TWI and SPI
Number of GPIO	39 pins on the LFBGA and up to 5 pins on the PQFP package
Integrated Touch panel Decoder	4- or 5-wire, calibration, noise filtering, gesture recognition
SDRAM	32-bit parallel interface
Flash	4Mbit to 64Mbit serial data flash

12 Revision History

Date	Revision	Notes
12 February 2009	2.0	First complete datasheet
7 May 2009	2.1	Rename SDRAM Blank Select to BSx Added BGA Information Added Packaging Information.

13 Ordering Information

Ordering Code	Package	Package Type	Temperature Operating Range
STK-480272C	208 PQFP	RoHS Compliant	-20°C to 60°C
AGB75LC04-QU-E	208 PQFP	RoHS Compliant	Industrial -40°C to 85°C
AGB75LC04-BG-E	225 BGA	RoHS Compliant	Industrial -40°C to 85°C

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