DEMO CIRCUIT 1451A
QUICK START GUIDE

LTC3127EDD
1A Buck-Boost DC/DC Converter with Programmable Input Current Limit

DESCRIPTION

Demonstration circuit 1451A is a Buck-Boost DC/DC converter featuring the LTC3127EDD and is ideally suited for pulsed load applications where the input current needs to be limited. Demonstration circuit 1451A is configured for 1.0A maximum input current limit and can handle pulsed load currents of up to 2A, with duty cycles of up to 15%. The input voltage range is 1.8-5.5V.

The fixed input current limit can be adjusted by replacing one resistor (R6).

The LTC3127 datasheet gives a complete description of the part operation and application information and must be read in conjunction with this quick start guide for demo circuit 1451A.

The Demonstration Circuit has been set up with storage capacitors to supply a 2A pulsed load while allowing VOUT to droop approximately 200mV while the input current is limited. Space is provided, and alternate part footprints have been built into the PCB to allow experimentation with larger capacitors for more energy storage. In a typical application, the larger output capacitors may be used. Refer to the datasheet for more information including equations to properly size the output capacitors for a given application.

Design files for this circuit board are available. Call the LTC factory.

TABLE 1. Typical Specifications (25°C)

Input Voltage Range	1.8V-5.5V
VOUT	3.8V
Iin	Average Iin limited to 1.0A
IOUT	1.0A for VIN =5.0V
Efficiency	≈ 90% at VIN=3.3V, IOUT = 0.5A

QUICK START PROCEDURE

Using short twisted pair leads for any power connections and with all loads and power supplies off, refer to Figure 1 for the proper measurement and equipment setup. The Power Supply (PS) should not be connected to the circuit until told to do so in the procedure below.

When measuring the input or output voltage ripple, care must be taken to avoid a long ground lead on the oscilloscope probe. Measure the input or output voltage ripple by touching the probe tip directly across VOUT and GND terminals. See Figure 2 for proper scope probe technique.

1. Jumper, Power Supply and LOAD Settings to start:
   PS= OFF
   Signal Generator = OFF
   LOADS = OFF
   JP1 (RUN) = ON
   JP2 (MODE) = FCC

2. Turn on PS and slowly increase voltage until the voltage at VIN is 3.3V. Monitor input current. If input current exceeds 50 mA turn off PS1 and look for shorts.
3. Confirm VOUT= 3.8V
4. Set LOAD on VOUT to 0.5A . Verify VOUT=3.8V.
5. Set VIN = 5.0V, confirm VOUT = 3.8V
6. Set VIN = 3.3V. Increase LOAD on VOUT until VOUT ≈2.5V. Verify Iin ≈1.0A
7. Remove LOAD from VOUT-GND terminals.

The board is now ready for operation. Several variations of this design are possible, including increasing the energy storage by populating CO5, and/or CO6. Please refer to the datasheet for design equations.

The next section describes pulsed load testing.

PULSED LOAD TESTING

Demonstration circuit 1451A can be setup for simple evaluation of pulse loads – please see optional circuit (Dynamic Load Circuit) in Figure 1 and Figure 4 for proper setup. The circuit is capable of pulsed loads of up to 2A with duty cycles up to 15%. Starting from step 7 in the quick start procedure above, follow the procedure below:
Disconnect all loads from Vout as the pulse load circuitry is on board.

The pulsed load current is measured by connecting IOSTEP to an oscilloscope using a BNC cable and setting the oscilloscope to 10mV/div.

Input current and output voltage can be measured with an oscilloscope for evaluation.

8. Connect Signal Generator with an adjustable output amplitude between IOSTEP CLK and GND as shown in Figure 1. Adjust the signal generator output to produce a pulse of 2A as measured at J1 (IOSTEP, 10mV/DIV) with an ON time of 576 uS and a period of 4.6 mS shown in Figure 3. Adjust the period and duty cycle of this signal to match that of the required load prior to attaching the pulse generator. The amplitude can vary but is approximately 2Vpp for a 2A step. Oscilloscope termination should be 1MΩ.
9. Verify VOUT ΔVpp $\leq$ 300mV.

An example result showing Vout and a pulse load Iout is given in Figure 3.

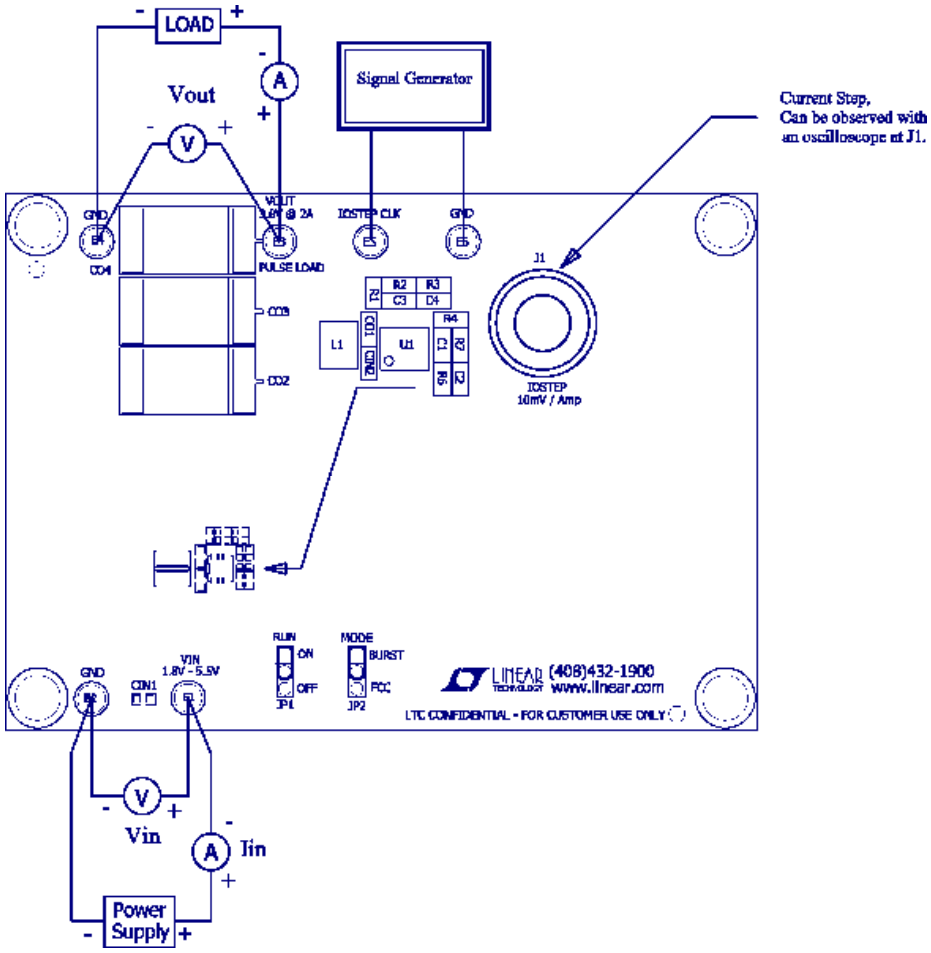

Figure 1. Connection Diagram

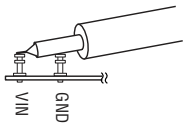

Figure 2. Measuring Input or Output Ripple

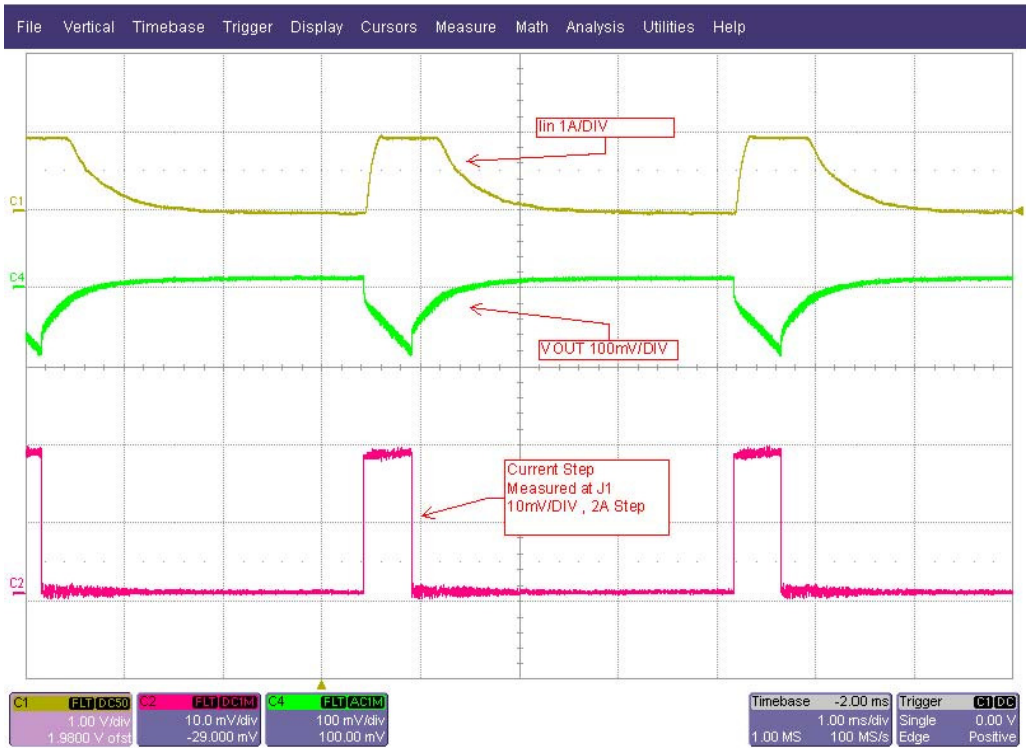

Figure 3. Step Load Response

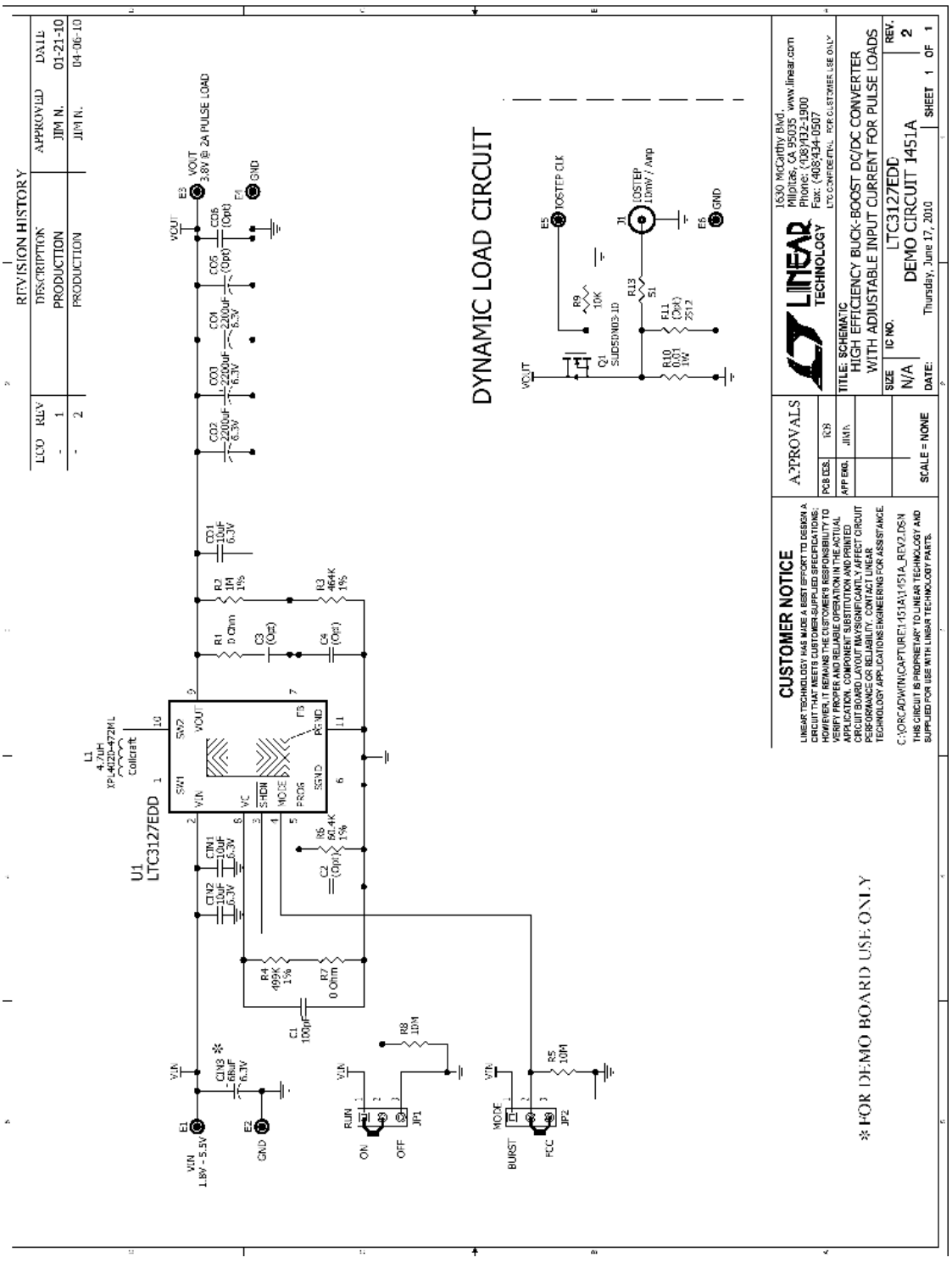

Figure 4. Circuit Schematic

Item	Qty	Reference	Part Description	Manufacturer / Part #
1	3	CO1,CIN1,CIN2	Cap., X5R 10uF 6.3V 20%	TDK C1608X5R0J106M
2	1	CIN3	Cap., POSCAP 68uF 6.3V 20%	SANYO 6TPB68M
3	3	CO2,CO3,CO4	Cap., Tant. 2200uF 6.3V 20%	Vishay 592D228X06R3X2T20H
4	1	C1	Cap., NPO 100pF 25V 10% 0402	AVX AVX 04023A101KAT2A
5	1	L1	Inductor, 4.7uH	Coilcraft XPL4020-472ML
6	1	R1	Res/Jumper, Chip 0 Ohm 1/16W 1 AMP	Vishay CRCW04020000ZOEA
7	1	R2	Res., Chip 1M 0.06W 1%	Vishay CRCW04021M00FKED
8	1	R3	Res., Chip 464K 0.06W 1%	Vishay CRCW0402464KFKED
9	1	R4	Res., Chip 499K 0.06W 1% 0402	Vishay CRCW0402499KFKED
10	2	R5,R8	Res., Chip 10M 0.06W 5%	Vishay CRCW040210M0JNED
11	1	R6	Res., Chip 60.4K 1% 0402	Vishay CRCW040260K4FKED
12	1	R7	Res/Jumper, Chip 0 Ohm 1/16W 0402	Vishay CRCW04020000Z0EA
13	1	U1	I.C., Volt. Reg.	Linear Tech. Corp. LTC3127EDD
			Optional Components for Demo Board	
1	0	CO5 (Opt)	Cap., Tant. 2200uF 6.3V 20%	Vishay 592D228X06R3X2T20H
2	0	CO6 (Opt)	Cap., 22mF 10V -20/=80%	AVX BZ054B223ZS
3	0	C2,C3,C4 (Opt)	Cap., 0402	
			Hardware for Demo Board Only	
1	5	E1,E2,E3,E4,E5,E6	Turret, Testpoint	Mill Max 2501-2-00-80-00-00-07-0
2	2	JP2,JP1	Headers, 3 Pins 2mm Ctrs.	Samtec TMM-103-02-L-S
3	1	J1	BNC Connector	Connex 112404
4	1	Q1	Mosfet, N-Channel 30V	Siliconix SUD50N03-10-E3
5	1	R9	Res., Chip 10K 0.06W 5% 0603	Vishay CRCW060310K0JNEA
6	1	R10	Res., Chip 0.01 1W 5%	Panasonic ERJM1WSF10MU
7	0	R11 (Opt)	Res., 2512 TBD	
8	1	R13	Res., Chip 51 0.06W 5% 0402	Vishay CRCW040251R0JNED
9	3	XJP1,XJP2,XJP3	Shunt, 2mm Ctrs.	Samtec 2SN-BK-G
10	4		STANDOFF, SNAP ON	KEYSTONE_8831

Figure 5. Bill of Materials