NCP383

Adjustable Current-Limiting Power-Distribution Switches

The NCP383 is a single input dual outputs power−distribution switch designed for applications where heavy capacitive loads and short−circuits are likely to be encountered, incorporating two very low $R_{DS(on)}$, N−channel MOSFETs in a single package. Each channel of the device limits the output current to a desired level by switching into a constant−current mode when the output load exceeds the current−limit threshold or a short circuit is present. The current−limit threshold is externally fixed by a pull down resistor placed between I_{lim} and GND. The power−switches rise and fall times are controlled to minimize current ringing during turn on/off.

An internal reverse−voltage detection comparator disables the power−switch if the output voltage is higher than the input voltage to protect devices on the input side of the switches.

The /FLAGx logic output asserts low during over−current, reverse−voltage or over temperature conditions. The switch is controlled by a logic enable input active low.

Features

- 2.7 V – 5.5 V Operating Range
- Current limit: Adjustable up to 2.8 A
- ± 7.5% Current Limit Accuracy at 2.8 A
- Very fast Over−Current Detection Response: 2 μs (typ)
- 1 μA Maximum Standby Supply Current
- Under Voltage Lock−out (UVLO)
- Soft−Start Prevents Inrush Current
- Thermal Protection
- Soft Turn−off
- Reverse Voltage Protection
- Enable Active Low
- μDFN 3x3 mm
- Compliance to IEC61000−4−2 (Level 4) 8.0 kV (Contact) – 15 kV (Air)
- UL Listed – File E343275
- CB – IEC60950−ED2 Certified
- CB – IEC60950−ED2−AM1 Certified
- This is a Pb−Free Device

Typical Applications

- Laptops
- USB Ports/Hubs
- TVs

ON Semiconductor®

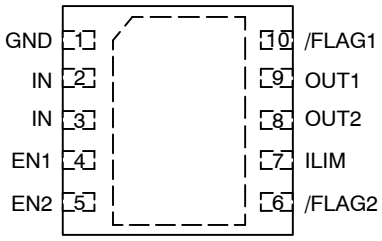
http://onsemi.com

UDFN10
CASE 517CC

MARKING DIAGRAM

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(*Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

Exposed pad must be soldered to PCB Ground plane.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

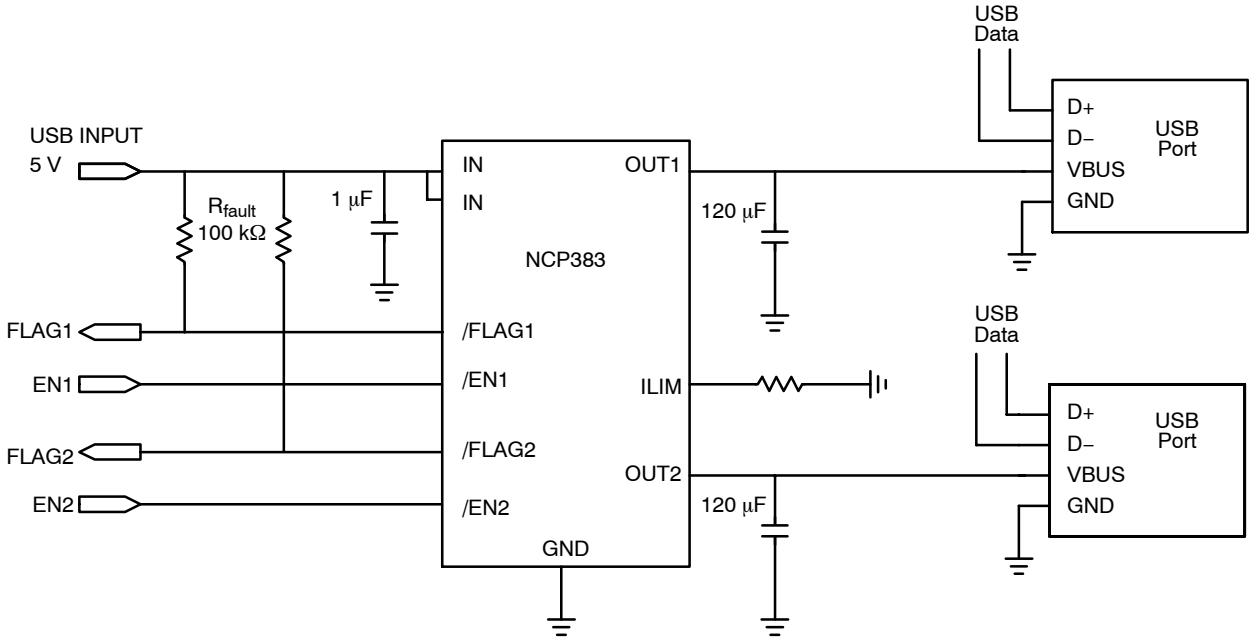


Figure 1. Typical Application Circuit: NCP383xMUAJxx

Adjustable Current limit on Channel 1 and Channel 2

PIN FUNCTION DESCRIPTION

Pin Name	Number	Type	Description
GND	1	P	Ground connection.
IN	2, 3	P	Power−switch input voltage; connect a 1 μF or greater ceramic capacitor from IN to GND as close as possible to the IC. Both IN pins must be hardwired together on the PCB.
/EN1	4	I	Enable 1 input, logic low turns on power switch 1 − If channel 1 is not used, do not leave this pin unconnected. Pull it to V_{IN}
/EN2	5	I	Enable 2 input, logic low turns on power switch 2. If channel 2 is not used, do not leave this pin unconnected. Pull it to V_{IN}
/FLAG2	6	O	Active−low open−drain output 2, asserted during overcurrent, overtemperature, or reverse−voltage conditions. Connect a 10kΩ or greater resistor pull−up, otherwise leave unconnected.
ILIM	7	O	External resistor used to set current−limit threshold; recommended 20kΩ < R_{ILIM} < 120 kΩ.
OUT2	8	O	Power−switch output2; connect a 1 μF ceramic capacitor from OUT2 to GND as close as possible to the IC is recommended. A 120 μF or greater ceramic capacitor from OUT2 to GND must be connected if the USB requirement is not met.
OUT1	9	O	Power−switch output1; connect a 1 μF ceramic capacitor from OUT1 to GND as close as possible to the IC is recommended. A 120 μF or greater ceramic capacitor from OUT1 to GND must be connected if the USB requirement is not met.
/FLAG1	10	O	Active−low open−drain output 1, asserted during overcurrent, overtemperature, or reverse−voltage conditions. Connect a 10 kΩ or greater resistor pull−up, otherwise leave unconnected.
PAD	11	Therm	Exposed Thermal Pad: Must be soldered to PCB Ground plane

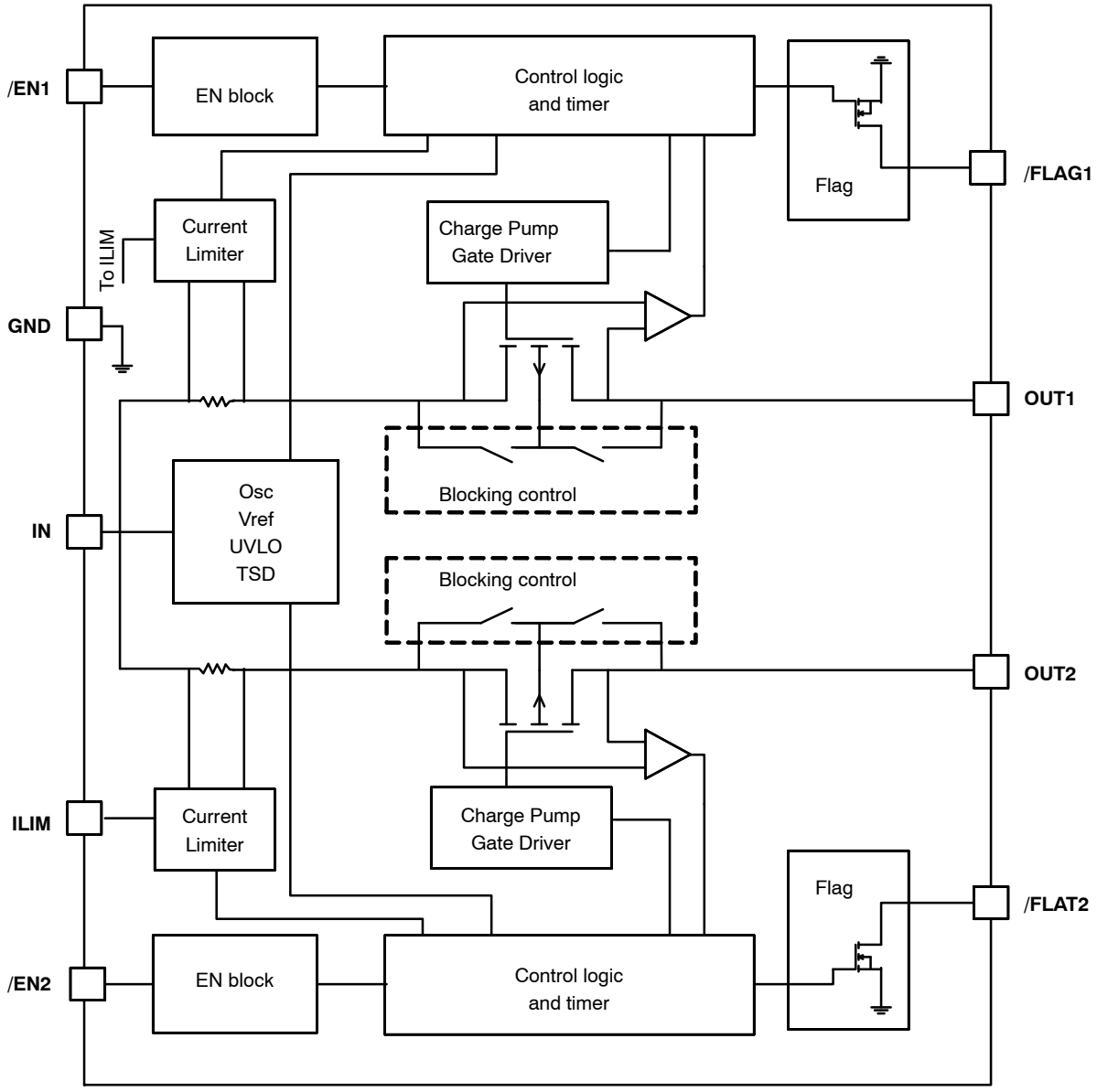


Figure 2. Block Diagram

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
From IN to OUT1, From IN to OUT2 Supply Voltage (Note 1)	V_{IN} , V_{OUT1},V_{OUT2}	−7.0 to +7.0	V
IN, OUT1,OUT2, /EN1, /EN2, /FLAG1, /FLAG2, ILIM Pins: In/Output (Note 1)	V_{IN} , V_{OUT1}, V_{OUT2},V_{EN1} , V_{EN2} , V_{FLAG1},V_{FLAG2}, V_{ILIM},	−0.3 to +7.0	V
/FLAG1, /FLAG2 Sink Current	I_{SINK}	2	mA
ESD Withstand Voltage (IEC 61000−4−2) (output only, when bypassed with 1.0 μF capacitor minimum)	ESD IEC	15 Air, 8 contact	kV
Human Body Model (HBM) ESD Rating are (Note 2)	ESD HBM	2000	V
Machine Model (MM) ESD Rating are (Note 2)	ESD MM	200	V
Latch−up protection (All Pins) (Note 3)	LU	100	mA
Maximum Junction Temperature (Note 4)	T_J	−40 to + TSD	°C
Storage Temperature Range	T_{STG}	−40 to + 150	°C
Moisture Sensitivity (Note 5)	MSL	Level 1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. According to JEDEC standard JESD22−A108
2. This device series contains ESD protection and passes the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114 for all pins.
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115 for all pins.
3. Latch up Current Maximum Rating: +100 mA per JEDEC standard: JESD78 class II.
4. A thermal shutdown protection avoids irreversible damage on the device due to power dissipation
5. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020

OPERATING CONDITIONS

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IN}	Operational Power Supply			2.7		5.5	V
V_{ENX}	Enable Voltage			0		5.5	
T_A	Ambient Temperature Range			−40	25	+85	°C
I_{SINK}	/FLAG sink current					1	mA
C_{IN}	Decoupling input capacitor			1			μF
C_{OUTX}	Decoupling output capacitor	USB port per Hub		120			μF
$R_{\theta JA}$	Thermal Resistance Junction to Air	DFN−10−12 package (Notes 6 and 7)			85		°C/W
T_J	Junction Temperature Range			−40	25	+125	°C
I_{OUTX}	Recommended Maximum DC current	Per Channel				2.5	A
P_D	Power Dissipation Rating (Note 8)	$T_A \le 25$ °C	DFN−10 package	850			mW
		$T_A = 85$ °C	DFN−10 package	428			

6. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020
7. The $R_{\theta JA}$ is dependent of the PCB heat dissipation. Announced thermal resistance is the unless PCB dissipation and can be improve with final PCB layout.
8. The maximum power dissipation (P_D) is given by the following formula:

$$P_D = \frac{T_{JMAX} - T_A}{R_{\theta JA}}$$

ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_A between −40°C to +85°C and T_J up to + 125°C for V_{IN} between 2.5 V to 5.5 V (Unless otherwise noted). Typical values are referenced to T_A = + 25°C and V_{IN} = 5 V.

Symbol	Parameter	Conditions	Conditions	Min	Typ	Max	Unit
POWER SWITCH							
$R_{DS(on)}$	Static drain−source on−state resistance, per channel	T_J = 25°C			45	70	mΩ
		−40°C < T_J < 125°C				95	
T_R	Output rise time	V_{IN} = 5 V	C_{LOAD} = 1μF, R_{LOAD} = 100 Ω (Note 9)	1.5	2.5	4	ms
T_F	Output fall time	V_{IN} = 5 V		0.1		0.5	
Logic Pins							
V_{IHEN}	High−level input voltage			1.2			V
V_{ILEN}	Low−level input voltage					0.4	V
I_{ENx}	Input current	V_{ENx} = 0 V, $V_{/ENx}$ = 5 V		−0.5		0.5	μA
T_{ON}	Turn on time	C_{LOAD} = 1μF, R_{LOAD} = 100 Ω (Note 9)		1	–	9	ms
T_{OFF}	Turn off time			1		3	ms
CURRENT LIMIT							
I_{OCP}	Current−limit threshold (Maximum DC output current I_{OUTX} delivered to load)	Ilimx = 90k (Note 10)		0.5	0.6	0.7	A
		Ilimx = 56k		0.9	1	1.1	
		Ilimx = 20k (Note 10)		2.58	2.8	3.01	
T_{DET}	Response time to short circuit	V_{IN} = 5 V (Note 10)			2		μs
T_{REG}	Regulation time			1	2	3	ms
T_{OCP}	Over current protection time			19	24	29	ms
UNDERVOLTAGE LOCKOUT							
V_{UVLO}	IN pin low−level input voltage	V_{IN} rising		–	2.45	2.5	V
V_{HYST}	IN pin hysteresis	T_J = 25°C		25			mV
T_{RUVLO}	Re−arming Time			7	12	15	ms
SUPPLY CURRENT							
I_{INOFF}	Low−level output supply current.	V_{IN} = 5 V, No load on OUTX, Device OFF V_{ENX}= 0 V or $V_{/ENX}$= 5 V − T_J = 25°C				1	μA
I_{INON}	High−level output supply current.	V_{IN} = 5 V, No load on OUTX Device ON − R_{ILIM} = 56 kΩ − V_{ENX}= 5 V				99	μA
I_{REV}	Reverse leakage current	V_{OUTX} = 5 V, V_{IN} = 0 V	T_J = 25°C			1	μA
/FLAGx PINS							
V_{OL}	/FLAGX output low voltage	$I_{/FLAGX}$ = 1 mA				400	mV
I_{LEAK}	Off−state leakage	$V_{/FLAGX}$ = 5 V				1	μA
T_{FGL}	/FLAGX deglitch	/FLAGX de−assertion time due to overcurrent		3	5	7	ms
T_{FOCP}	/FLAGX deglitch	/FLAGX assertion due to overcurrent		5	7	12	ms
T_{FREV}	/FLAGX deglitch	/FLAGX assertion due to reverse−voltage		3	5	7	ms
REVERSE VOLTAGE PROTECTION							
V_{REV}	Reverse voltage threshold	V_{OUT} − V_{IN} drop			150		mV
V_{RHYST}	Reverse voltage threshold hysteresis	V_{OUT} − V_{IN} drop decrease			30		mV
THERMAL SHUTDOWN							
T_{SD}	Thermal shutdown threshold				140		°C
T_{SDOCP}	Thermal regulation threshold				125		°C
T_{RST}	Thermal regulation rearming threshold				115		°C

9. Parameters are guaranteed for CLOAD and RLOAD connected to the OUT pin with respect to the ground.
10. Guaranteed by design and by characterization

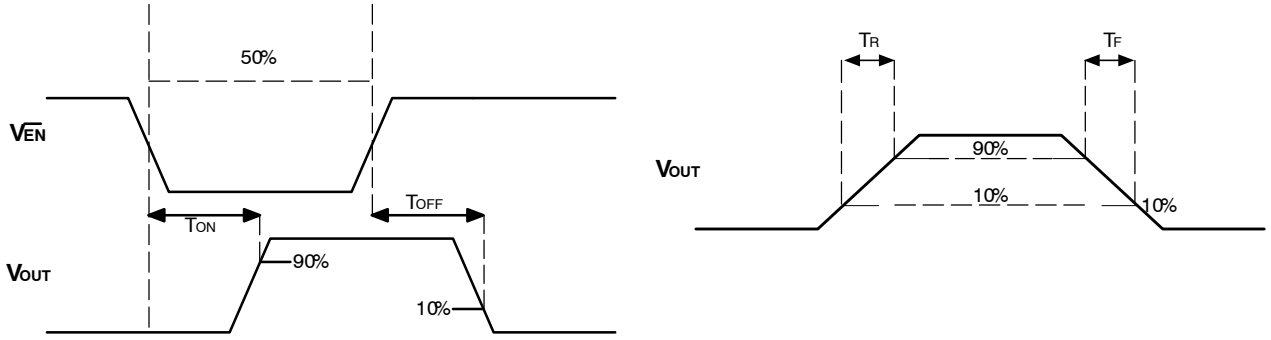


Figure 3. Ton, Toff, Trise, and Tfall

FUNCTIONAL DESCRIPTION

Overview

The NCP383 is a dual high side N channel MOSFET power distribution switches designed to protect the input supply voltage in case of heavy capacitive loads, short circuit or over current. In addition, the high side MOSFETs are turned off during under voltage, thermal shutdown or reverse voltage condition. Thanks to the soft start circuitry, NCP383 is able to limit large current and voltage surges.

Overcurrent Protection

NCP383 switches into a constant current regulation mode when the output current is above the I_{OCP} threshold. Depending on the load, the output voltage is decreased accordingly.

– In case of hot plug with heavy capacitive load, the output voltage is brought down to the capacitor voltage. The NCP383 will limit the current to the I_{OCP} threshold value until the charge of the capacitor is completed.

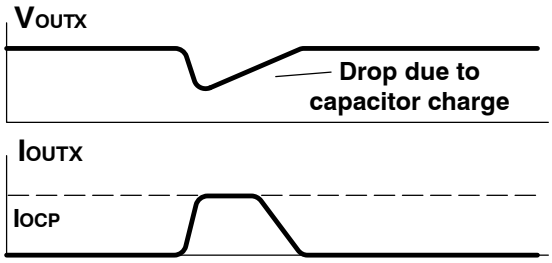


Figure 4. Heavy Capacitive Load

– In case of overload, the current is limited to the I_{OCP} value and the voltage value is reduced according to the load by the following relation:

$$V_{OUTX} = R_{LOADX} \times I_{OCP} \quad \text{(eq. 1)}$$

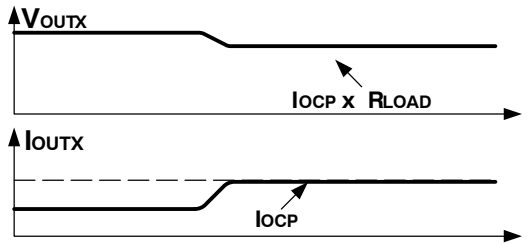


Figure 5. Overload

– In case of short circuit or huge load, the current is limited to the I_{OCP} value within T_{DET} time until the short condition is removed. If the output remains shorted or tied to a very low voltage, the junction temperature of the chip exceeds T_{SDOCP} value and the device enters in thermal shutdown (MOSFET is turned−off).

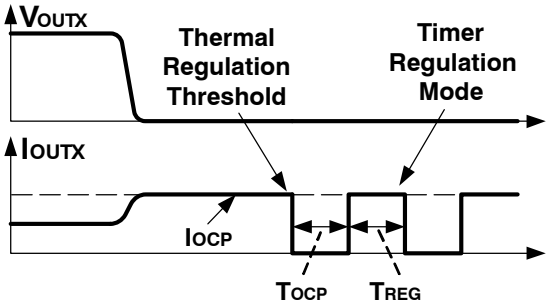


Figure 6. Short Circuit

Then, the device enters in timer regulation mode, described in 2 phases:

– Off−phase: Power MOSFET is off during T_{OCP} to allow the die temperature to drop.
– On−phase: regulation current mode during $T_{REG.}$ The current is regulated to the I_{OCP} level.

The timer regulation mode allows the device to handle high thermal dissipation (in case of short circuit for example) within temperature operating condition.

NCP383 stays in on−phase/off−phase loop until the over current condition is removed or enable pin is toggled.

Remark: other regulation mode can be available for different applications. Please contact our ON Semiconductor representative for availability.

Adjustable Current−Limit Programming NCP383xMUAJxx Version

The R_{LIM} resistor connected between ILIM pin and GND determine the current limit threshold according to the electrical characteristic table.

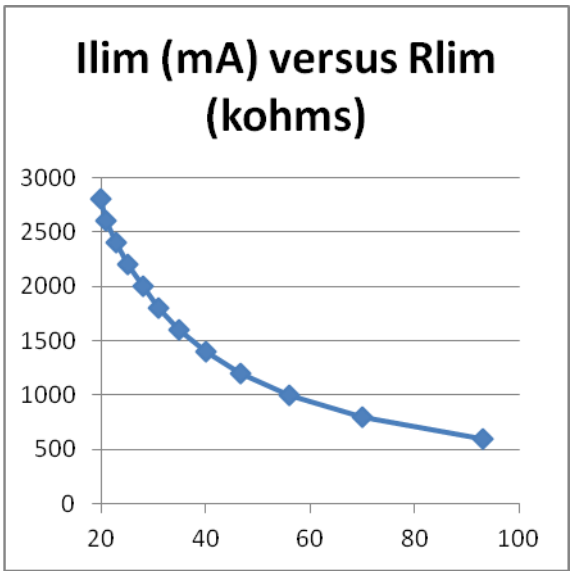


Figure 7. Typical Ilim Curve vs Rlim External Resistor

/FLAGx Indicators

The /FLAGx pin are an open−drain MOSFET asserted low during over current, reverse−voltage or over temperature conditions. When an over current or a reverse voltage fault is detected on the power path, /FLAGx pins are asserted low at the end of the associate deglitch time (see electrical characteristics). Due to this feature, the /FLAGx pins are not tied low during the charge of a heavy capacitive load or a voltage transient on output. Deglitch time is T_{FOCP} for over current fault and T_{FREV} for reverse voltage. The /FLAGx pins remain low until the fault is removed. Then, the /FLAG pins go high at the end of T_{FGL}

Undervoltage Lock−out

Due to a built−in under voltage lockout (UVLO) circuitry, the output remains disconnected from input until V_{IN} voltage is above V_{UVLO}. This circuit has a V_{HYST} hysteresis witch provides noise immunity to transient condition.

Thermal Sense

Thermal shutdown turns off the power MOSFET if the die temperature exceeds T_{SD}. A Hysteresis of T_{HYST} prevents the part from turning on until the die temperature cools at $T_{SD} - T_{HYST}$.

Enable Input

Enable pin must be driven by a logic signal (CMOS or TTL compatible) or connected to the GND or VIN. A logic low turns−on the device. A logic high on /ENX turns off device and reduce the current consumption down to I_{INOFF}.

Remark: Active high can be available for different applications. Please contact our ON Semiconductor representative for availability.

Blocking Control

The blocking control circuitry switches the bulk of the power MOS. When the part is off, the body diode limits the leakage current I_{REV} from OUTX to IN. In this mode, anode of the body diode is connected to IN pin and cathode is connected to OUTX pin. In operating condition, anode of the body diode is connected to OUTX pin and cathode is connected to IN pin preventing the discharge of the power supply.

APPLICATION INFORMATION

Power Dissipation

The device's junction temperature depends on different contributor factor such as board layout, ambient temperature, device environment, etc... Yet, the main contributor in term of junction temperature is the power dissipation of the power MOSFET. Assuming this, the power dissipation and the junction temperature in normal mode can be calculated with the following equations:

$$P_D = R_{DS(on)} \times \left(\left(I_{OUT1}\right)^2 + \left(I_{OUT}\right)^2 \right) \quad \text{(eq. 2)}$$

P_D = Power dissipation (W)
$R_{DS(on)}$ = Power MOSFET on resistance (Ω)
I_{OUTx} = Output current in channel X (A)

$$T_J = P_D \times R_{\theta JA} + T_A \quad \text{(eq. 3)}$$

T_J = Junction temperature (°C)
$R_{\theta JA}$ = Package thermal resistance (°C/W)
T_A = Ambient temperature (°C)

Power dissipation in regulation mode can be calculated by taking into account the drop $V_{IN} - V_{OUTX}$ link to the load by the following relation:

$$P_D \times \left(\left(V_{IN} - R_{LOAD1} \times I_{OCP}\right) + \left(V_{IN} - R_{LOAD2} \times I_{OCP}\right) \right) \times I_{OCP} \quad \text{(eq. 4)}$$

P_D = Power dissipation (W)
V_{IN} = Input Voltage (V)
R_{LOADX} = Load Resistance on channel X (Ω)
I_{OCP} = Output regulated current (A)

PCB Recommendations

The NCP383 integrates two up to 3 A rated NMOS FETs, and the PCB design rules must be respected to properly evacuate the heat out of the silicon. The DFN10 PAD1 must be connected to ground plane to increase the heat transfer if necessary. Of course, in any case, this pad must not connect to any other potential. By increasing PCB area, the $R_{\theta JA}$ of the package can be decreased, allowing higher current.

CIN / COUT1 / COUT2:
* AS CLOSE AS POSSIBLE TO NCP383
* DIRECTLY CONNECTED TO GND PLANE (LOW IMPEDANCE CONNECTION)
* TRY TO AVOID VIAS BETWEEN PIN AND CAPACITOR
* IF 120 μF COUT1 and COUT2 ARE LOCATED FAR AWAY FROM NCP383, TRY TO ADD EXTRA LOWER VALUE (~ 0.1 μF) CAPACITOR AS CLOSE AS POSSIBLE TO NCP383

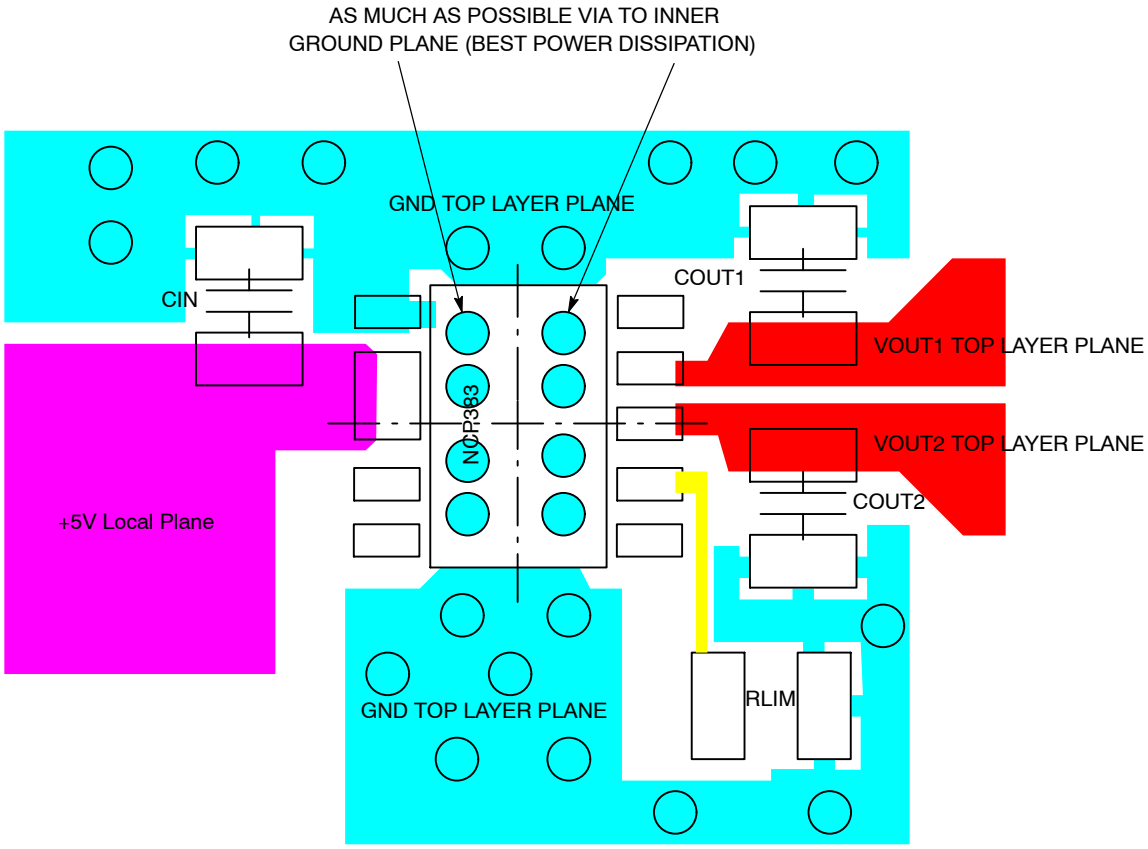
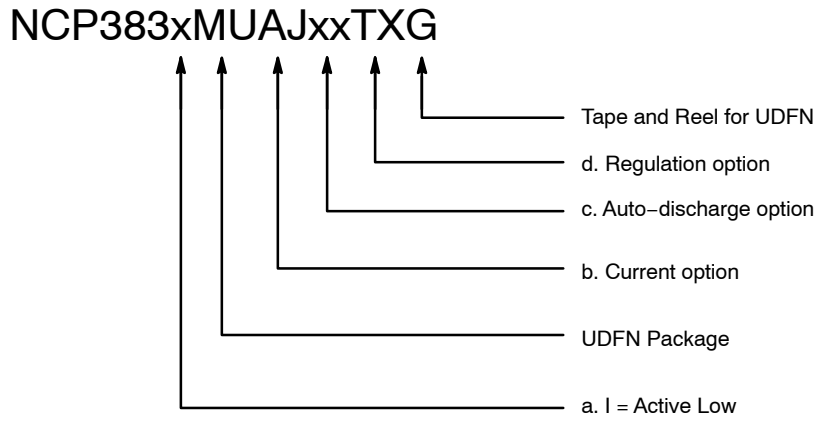


Figure 8. Layout Recommendations

ORDERING INFORMATION

Device	Package	Shipping†
NCP383LMUAJAATXG	UDFN10 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



Code	Contents
a	L: active low
b	AJ: adjustable current limit
c	A: No autodischarge output path
d	A: standard regulation (CC + TSD warning + timer)

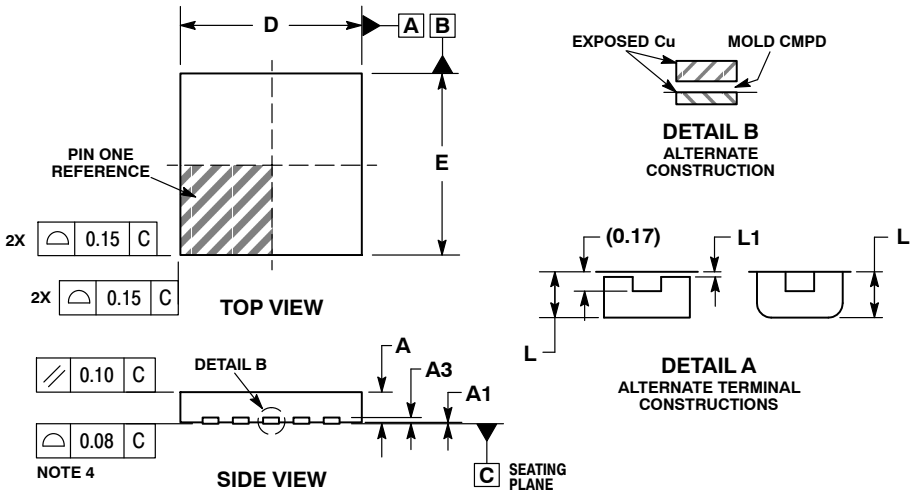
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

UDFN10 3x3, 0.5P (Leads 2 & 3 Tied)
CASE 517CC
ISSUE O

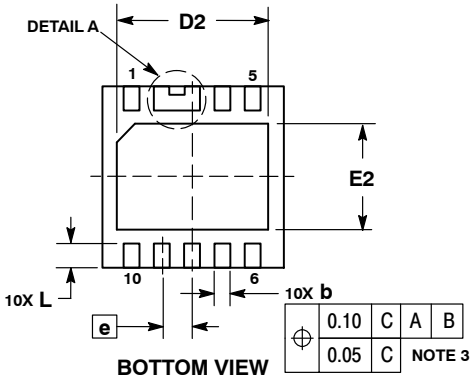
DATE 10 OCT 2011

SCALE 2:1

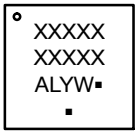


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	3.00 BSC	
D2	2.39	2.59
E	3.00 BSC	
E2	1.59	1.79
e	0.50 BSC	
L	0.35	0.45
L1	---	0.15



GENERIC MARKING DIAGRAM*

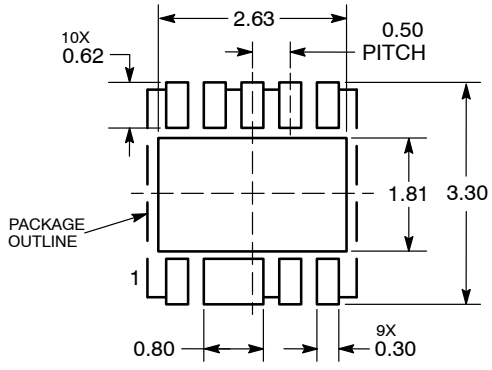


A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON59624E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	UDFN10 3X3, 0.5P (LEADS 2 & 3 TIED)	PAGE 1 OF 1

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

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For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales