# AK4633

## 16-Bit ΔΣ Mono CODEC with ALC & MIC/SPK-AMP

### GENERAL DESCRIPTION

The AK4633 is a 16-bit mono CODEC with Microphone-Amplifier and Speaker-Amplifier. Input circuits include a Microphone-Amplifier and an ALC (Automatic Level Control) circuit. Output circuits include a Speaker-Amplifier and Mono Line Output. The AK4633 suits a moving picture of Digital Still Camera and etc. This speaker-Amplifier supports a Piezo Speaker. The AK4633 is housed in a space-saving 24-pin QFN package.

### FEATURE

1. 16-Bit Delta-Sigma Mono CODEC
2. Recording Function
   - 1ch Mono Input
   - 1st MIC Amplifier: 0dB, 6dB, 10dB, 14dB, 17dB, 20dB, 26dB or 32dB
   - 2nd Amplifier with ALC: +36dB ~ -54dB, 0.375dB Step, Mute
   - ADC Performance (MIC-Amp= +20dB): S/(N+D): 84dB, DR, S/N: 85dB
   - Wind Noise Reduction
   - Notch Filter
3. Playback Function
   - Digital ALC (Automatic Level Control): +36dB ~ -54dB, 0.375dB Step, Mute
   - Mono Line Output Performance: S/(N+D): 85dB, S/N: 93dB
   - Mono Speaker-Amp
     - Speaker-Amp Performance: S/(N+D): 60dB (150mW@ 8Ω)
       Output Noise Level: -87dBV
     - BTL Output
     - Output Power: 400mW @ 8Ω
   - Beep Input
4. Power Management
5. Flexible PLL Mode:
   - Frequencies:
     11.2896MHz, 12MHz, 12.288MHz, 13.5MHz, 24MHz, 27MHz (MCKI pin)
     1fs (FCK pin)
     16fs, 32fs or 64fs (BICK pin)
6. EXT Mode:
   - Frequencies: 256fs, 512fs or 1024fs (MCKI pin)
7. Sampling Rate:
   - PLL Slave Mode (FCK pin) : 7.35kHz ~ 48kHz
   - PLL Slave Mode (BICK pin) : 7.35kHz ~ 48kHz
   - PLL Slave Mode (MCKI pin):
     8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
   - PLL Master Mode:
     8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
   - EXT Slave Mode/EXT Master Mode:
     7.35kHz~ 48kHz (256fs), 7.35kHz ~ 26kHz (512fs), 7.35kHz ~ 13kHz (1024fs)
8. Output Master Clock Frequency: 256fs
9. Serial μP Interface: 3-wire
10. Master / Slave Mode
11. Audio Interface Format: MSB First, 2's complement

- **ADC: DSP Mode, 16bit MSB justified, $I^2S$**
- **DAC: DSP Mode, 16bit MSB justified, 16bit LSB justified, $I^2S$**

**12. AK4633VN: Ta = -40 ~ 85°C**
**AK4633EN: Ta = -30 ~ 85°C**

**13. Power Supply**

- **AVDD: 2.2 ~ 3.6V (typ. 3.3V)**
- **DVDD: 1.6 ~ 3.6V (typ. 3.3V)**
- **SVDD: 2.2 ~ 4.0V (typ. 3.3V)**

**14. Power Supply Current: 12mA (All Power ON)**

**15. Package: 24-pin QFN(4mmx4mm)**

## ■ Block Diagram

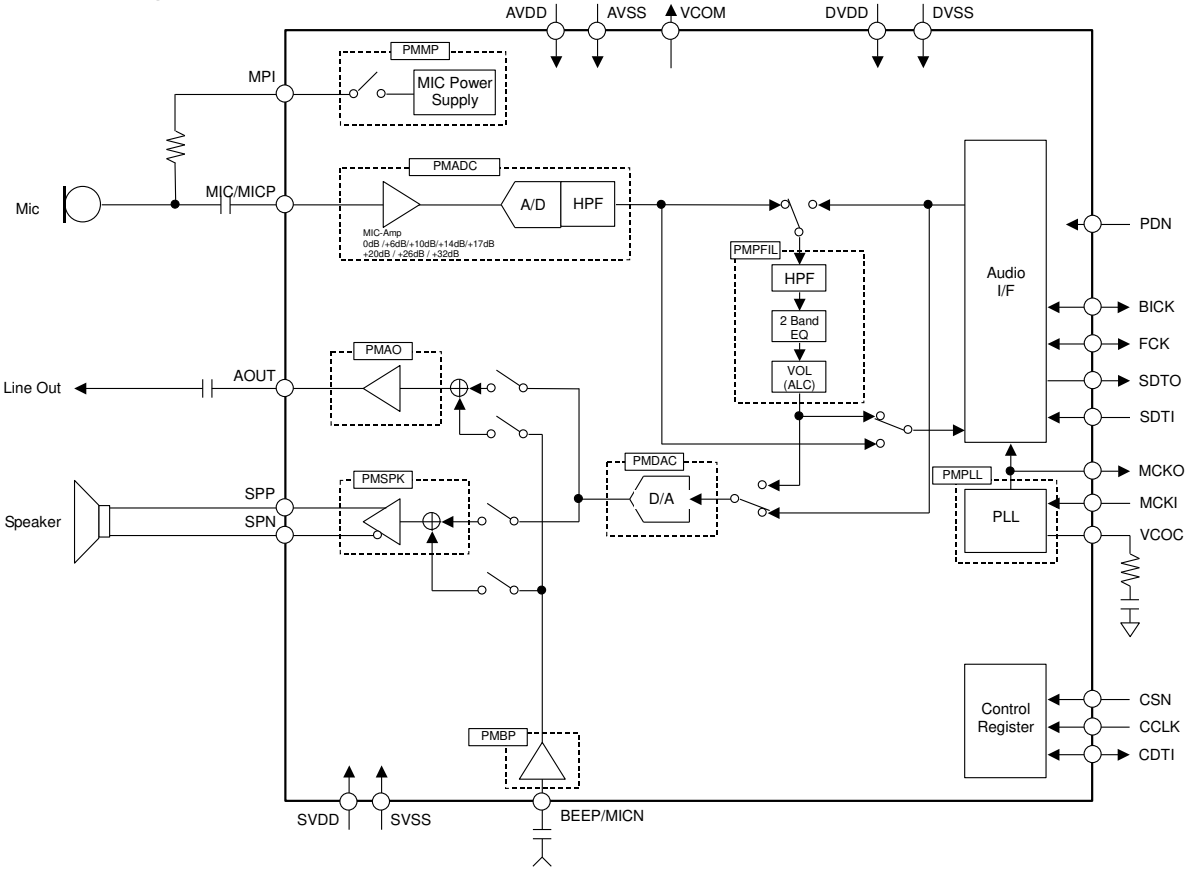
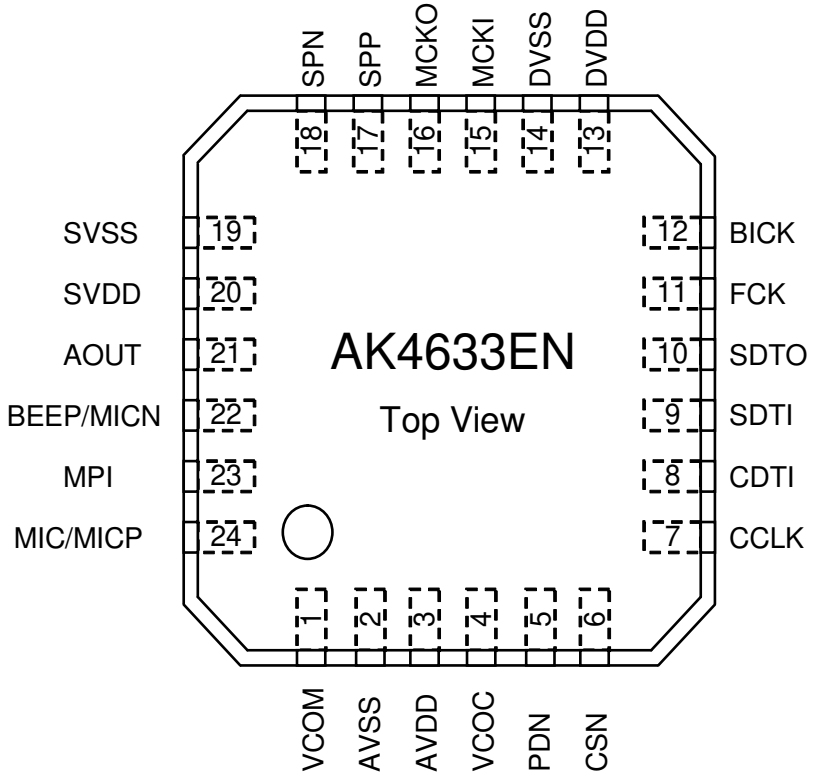



Figure 1. AK4633 Block Diagram

## ■ Ordering Guide

| | | |
|---|---|---|
| AK4633VN | –40 ~ +85°C | 24-pin QFN (0.5mm pitch) |
| AK4633EN | –30 ~ +85°C | 24-pin QFN (0.5mm pitch) |
| AKD4633 | Evaluation board for AK4633 | |

## ■ Pin Layout



## ■ Interchange with AK4631

### 1. Function

| Function | AK4631 | AK4633 |
|---|---|---|
| AVDD | 2.6V ~ 3.6V | 2.2V ~ 3.6V |
| DVDD | 2.6V ~ 3.6V | 1.6V ~ 3.6V |
| SVDD | 2.6V ~ 5.25V | 2.2V ~ 4.0V |
| MIC Input | Single-end | Single-end / differential |
| MIC Power Output Voltage | 0.75 x AVDD | 0.8 x AVDD |
| MIC-Amp | 0dB/+20dB/+26dB/+32dB | 0dB/+6dB/+10dB/+14dB<br>+17dB/+20dB/+26dB/+32dB |
| HPF for Wind Noise Reduction | No | Yes |
| Notch Filter | No | Yes |
| ALC for Input Signal | Analog ALC | Digital ALC (Note 1) |
| Input Volume | +27.5dB ~ -8dB, 0.5dB Step | +36dB ~ -54dB, 0.375dB Step<br>(Note 1) |
| ALC for Output Signal | Speaker-Amp block | Digital Block (Note 1) |
| Output Volume | +12dB ~ -115dB, 0.5dB Step | +36dB ~ -54dB, 0.375dB Step<br>(Note 1) |
| Maximum Output for SPK-Amp (using Piezo Speaker) | 8.5Vpp@SVDD=5V | 6.33Vpp@SVDD=3.8V |
| MCKI Pull-down Resistance | Yes | No (Delete MCKPD bit ) |
| Package | 28-pin QFN 5.2mm x 5.2mm<br>41-pin BGA 4.0mm x 4.0mm | 24-pin QFN 4.0mm x 4.0mm |

Note 1. ALC and Volume circuits are shared by input and output. Therefore, it is impossible to use ALC and Volume function at same time for both recording and playback mode.

## 2. Register Map

(1) AK4631

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 00H | Power Management 1 | 0 | PMVCM | PMBP | PMSPK | PMAO | PMDAC | PMMIC | PMADC |
| 01H | Power Management 2 | 0 | 0 | 0 | 0 | M/S | MCKPD | MCKO | PMPLL |
| 02H | Signal Select 1 | SPPS | BEEPS | ALC2S | DACA | DACM | MPWR | MICAD | MGAIN0 |
| 03H | Signal Select 2 | 0 | AOPSN | MGAIN1 | SPKG1 | SPKG0 | BEEPA | ALC1M | ALC1A |
| 04H | Mode Control 1 | PLL3 | PLL2 | PLL1 | PLL0 | BCKO1 | BCKO0 | DIF1 | DIF0 |
| 05H | Mode Control 2 | 0 | 0 | FS3 | MSBS | BCKP | FS2 | FS1 | FS0 |
| 06H | Timer Select | DVTM | ROTM | ZTM1 | ZTM0 | WTM1 | WTM0 | LTM1 | LTM0 |
| 07H | ALC Mode Control 1 | 0 | ALC2 | ALC1 | ZELM | LMAT1 | LMAT0 | RATT | LMTH |
| 08H | ALC Mode Control 2 | 0 | REF6 | REF5 | REF4 | REF3 | REF2 | REF1 | REF0 |
| 09H | Input PGA Control | 0 | IPGA6 | IPGA5 | IPGA4 | IPGA3 | IPGA2 | IPGA1 | IPGA0 |
| 0AH | Digital Volume Control | OVOL7 | OVOL6 | OVOL5 | OVOL4 | OVOL3 | OVOL2 | OVOL1 | OVOL0 |
| 0BH | ALC2 Mode Control | 0 | 0 | RFS5 | RFS4 | RFS3 | RFS2 | RFS1 | RFS0 |

(2) AK4633

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 00H | Power Management 1 | **PMPFIL** | PMVCM | PMBP | PMSPK | PMAO | PMDAC | 0 | PMADC |
| 01H | Power Management 2 | 0 | 0 | 0 | 0 | M/S | 0 | MCKO | PMPLL |
| 02H | Signal Select 1 | SPPSN | BEEPS | DACS | DACA | 0 | PMMP | MGAIN2 | MGAIN0 |
| 03H | Signal Select 2 | **PFSDO** | AOPS | MGAIN1 | SPKG1 | SPKG0 | BEEPA | PFDAC | ADCPF |
| 04H | Mode Control 1 | PLL3 | PLL2 | PLL1 | PLL0 | BCKO1 | BCKO0 | DIF1 | DIF0 |
| 05H | Mode Control 2 | ADRST | FCKO | FS3 | MSBS | BCKP | FS2 | FS1 | FS0 |
| 06H | Timer Select | 0 | 0 | ZTM1 | ZTM0 | WTM1 | WTM0 | RFST1 | RFST0 |
| 07H | ALC Mode Control 1 | 0 | ALC2 | ALC1 | ZELMN | LMAT1 | LMAT0 | RGAIN0 | LMTH0 |
| 08H | ALC Mode Control 2 | **IREF7** | IREF6 | IREF5 | IREF4 | IREF3 | IREF2 | IREF1 | IREF0 |
| 09H | Digital Volume Control | **IVOL7** | IVOL6 | IVOL5 | IVOL4 | IVOL3 | IVOL2 | IVOL1 | IVOL0 |
| 0AH | Digital Volume Control | OVOL7 | OVOL6 | OVOL5 | OVOL4 | OVOL3 | OVOL2 | OVOL1 | OVOL0 |
| 0BH | ALC Mode Control 3 | **RGAIN1** | **LMTH1** | OREF5 | OREF4 | OREF3 | OREF2 | OREF1 | OREF0 |
| 0DH | ALC LEVEL | **VOL7** | **VOL6** | **VOL5** | **VOL4** | **VOL3** | **VOL2** | **VOL1** | **VOL0** |
| 0EH | Signal Select 3 | **DATT1** | **DATT0** | **SMUTE** | **MDIF** | **EQ2** | **EQ1** | **HPF** | **HPFAD** |
| **10H - 1FH** | | **Digital Filter Setting** | | | | | | | |

hatching Register bits changed from the AK4631.
**Bold** Register bits added from the AK4631.

### 3. Register Setting

(1) When PLL reference clock is input from the FCK or BICK pin, the setting of FS3-0 bits is changed as shown in the following table.

| Mode | FS3 bit | FS2 bit | FS1 bit | FS0 bit | Sampling Frequency Range |
|---|---|---|---|---|---|
| 0 | 0 | 0 | Don't care | Don't care | 7.35kHz ≤ fs ≤ 12kHz |
| 1 | 0 | 1 | Don't care | Don't care | 12kHz < fs ≤ 24kHz |
| 2 | 1 | 0 | Don't care | Don't care | 24kHz < fs ≤ 48kHz |
| Others | Others | | | | N/A |

ALL of modes are changed from AK4631.

(2) In EXT Slave Mode, the setting of FS3-0 bits is changed as shown in the following table.

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| Mode | FS3-2 bits | FS1 bit | FS0 bit | MCKI Input Frequency | Sampling Frequency Range |
|---|---|---|---|---|---|
| 0 | Don't care | 0 | 0 | 256fs | 7.35kHz ≤ fs ≤ 48kHz |
| 1 | Don't care | 0 | 1 | 1024fs | 7.35kHz < fs ≤ 13kHz |
| 2 | Don't care | 1 | 0 | 512s | 7.35kHz < fs ≤ 26kHz |
| 3 | Don't care | 1 | 1 | 256fs | 7.35kHz ≤ fs ≤ 48kHz |

Hatching parts are the setting changed from AK4631.

## PIN / FUNCTION

| No. | Pin Name | I/O | Function |
|---|---|---|---|
| 1 | VCOM | O | Common Voltage Output Pin, 0.45 x AVDD<br>Bias voltage of ADC inputs and DAC outputs. |
| 2 | AVSS | - | Analog Ground Pin |
| 3 | AVDD | - | Analog Power Supply Pin |
| 4 | VCOC | O | Output Pin for Loop Filter of PLL Circuit<br>This pin must be connected to AVSS with one resistor and capacitor in series. |
| 5 | PDN | I | Power-Down Mode Pin<br>"H": Power up, "L": Power down reset and initialize the control register.<br>AK4633 must always be reset upon power-up. |
| 6 | CSN | I | Chip Select Pin |
| 7 | CCLK | I | Control Data Clock Pin |
| 8 | CDTI | I/O | Control Data Input Pin / Output pin |
| 9 | SDTI | I | Audio Serial Data Input Pin |
| 10 | SDTO | O | Audio Serial Data Output Pin |
| 11 | FCK | I/O | Frame Clock Pin |
| 12 | BICK | I/O | Audio Serial Data Clock Pin |
| 13 | DVDD | - | Digital Power Supply Pin |
| 14 | DVSS | - | Digital Ground Pin |
| 15 | MCKI | I | External Master Clock Input Pin |
| 16 | MCKO | O | Master Clock Output Pin |
| 17 | SPP | O | Speaker Amp Positive Output Pin |
| 18 | SPN | O | Speaker Amp Negative Output Pin |
| 19 | SVSS | - | Speaker Amp Ground Pin |
| 20 | SVDD | - | Speaker Amp Power Supply Pin |
| 21 | AOUT | O | Mono Line Output Pin |
| 22 | BEEP | I | Beep Signal Input Pin (MDIF bit = "0") |
| | MICN | I | Microphone Negative Input Pin for Differential Input (MDIF bit = "1") |
| 23 | MPI | O | MIC Power Supply Pin for Microphone |
| 24 | MIC | I | Microphone Input Pin for Single Ended input (MDIF bit = "0") |
| | MICP | I | Microphone Positive Input Pin for Differential Input (MDIF bit = "1") |

Note: All input pins except analog input pins (MIC/MICP and BEEP/MICN pins) must not be left floating.

## ■ Handling of Unused Pin

The unused I/O pins must be processed appropriately as below.

| Classification | Pin Name | Setting |
|---|---|---|
| Analog | MIC/MICP, BEEP/MICN, MPI, AOUT, SPP, SPN, VCOC | These pins must be open. |
| Digital | MCKI, SDTI | These pins must be connected to DVSS. |
| | FCK, BICK (Note) | These pins must be connected to DVSS, or be pulled-down/pulled-up by about 100kΩ resister . |
| | MCKO, SDTO | These pins should be open. |

(Note) When the AK4633 is used by the slave mode (M/Sbit="0"), these pins must be connected to DVSS. When the AK4633 is used by the master mode (M/Sbit="1"), these pins should be pulled-down or pulled-up by about 100kΩ resistor.

## ABSOLUATE MAXIMUM RATING

(AVSS=DVSS=SVSS=0V; Note 2)

| Parameter | | | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| Power Supplies: | Analog | | AVDD | –0.3 | 4.6 | V |
| | Digital | | DVDD | –0.3 | 4.6 | V |
| | Speaker-Amp | | SVDD | –0.3 | 4.6 | V |
| | \|AVSS – DVSS\| (Note 3) | | ΔGND1 | - | 0.3 | V |
| | \|AVSS – SVSS\| (Note 3) | | ΔGND2 | - | 0.3 | V |
| Input Current, Any Pin Except Supplies | | | IIN | - | ±10 | mA |
| Analog Input Voltage (Note 5) | | | VINA | –0.3 | AVDD+0.3 | V |
| Digital Input Voltage (Note 6) | | | VIND | –0.3 | DVDD+0.3 | V |
| Ambient Temperature (powered applied) | | AK4633VN | Ta | –40 | 85 | °C |
| | | AK4633EN | Ta | –30 | 85 | °C |
| Storage Temperature | | | Tstg | –65 | 150 | °C |
| Maximum Power Dissipation (Note 4) | | | Pd | - | 650 | mW |

Note 2. All voltages with respect to ground.
Note 3. AVSS, DVSS and SVSS must be connected to the same analog ground plane.
Note 4. In case that PCB wiring density is 100%. This power is the AK4633 internal dissipation that does not include power of externally connected speaker.
Note 5. BEEP/MICN, MIC/MICP pins
Note 6. PDN, CSN, CCLK, CDTI, SDTI, FCK, BICK, MCKI pins

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

## RECOMMENDED OPERATING CONDITIONS

(AVSS=DVSS=SVSS=0V; Note 2)

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Power Supplies | Analog | AVDD | 2.2 | 3.3 | 3.6 | V |
| (Note 7) | Digital | DVDD | 1.6 | 3.3 | 3.6 | V |
| | Speaker-Amp | SVDD | 2.2 | 3.3 | 4.0 | V |
| | Difference | DVDD – AVDD | - | - | 0.3 | V |
| | | DVDD – SVDD | - | - | 0.3 | V |
| | | AVDD – SVDD | - | - | 1.0 | V |

Note 2. All voltages with respect to ground.

Note 7. The power up sequence between AVDD, DVDD and SVDD is not critical. It is not permit to power DVDD off only when AVDD or SVDD is powered up. When the power supplies except DVDD are partially powered OFF, the AK4633 must be reset by bringing the PDN pin "L" after these power supplies are powered ON again. If AVDD is powered off when DVDD is powered up, the PMADC bit should be set to "0" before AVDD is powered off.

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

## ANALOG CHRACTERISTICS

(Ta=25°C; AVDD=DVDD=SVDD=3.3V; AVSS=DVSS=SVSS=0V; fs=8kHz, BICK=64fs; Signal Frequency=1kHz; 16bit Data; Measurement frequency=20Hz ~ 3.4kHz; EXT Slave Mode; unless otherwise specified)

| Parameter | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **MIC Amplifier :** MDIF bit = "0"; (Single-ended input) | | | | | |
| Input Resistance | | 20 | 30 | 40 | kΩ |
| Gain | (MGAIN2-0 bits = "000") | - | 0 | - | dB |
| | (MGAIN2-0 bits = "001") | - | 20 | - | dB |
| | (MGAIN2-0 bits = "010") | - | 26 | - | dB |
| | (MGAIN2-0 bits = "011") | - | 32 | - | dB |
| | (MGAIN2-0 bits = "100") | - | 6 | - | dB |
| | (MGAIN2-0 bits = "101") | - | 10 | - | dB |
| | (MGAIN2-0 bits = "110") | - | 14 | - | dB |
| | (MGAIN2-0 bits = "111") | - | 17 | - | dB |
| **MIC Amplifier :** MDIF bit = "1"; (Full-differential input) | | | | | |
| Input Voltage (Note 8) | (MGAIN2-0 bits = "001") | - | - | 0.228 | Vpp |
| | (MGAIN2-0 bits = "010") | - | - | 0.114 | Vpp |
| | (MGAIN2-0 bits = "011") | - | - | 0.057 | Vpp |
| | (MGAIN2-0 bits = "100") | - | - | 1.14 | Vpp |
| | (MGAIN2-0 bits = "101") | - | - | 0.721 | Vpp |
| | (MGAIN2-0 bits = "110") | - | - | 0.455 | Vpp |
| | (MGAIN2-0 bits = "111") | - | - | 0.322 | Vpp |
| **MIC Power Supply:** MPI pin | | | | | |
| Output Voltage (Note 9) | | 2.38 | 2.64 | 2.90 | V |
| Load Resistance | | 2 | - | - | kΩ |
| Load Capacitance | | - | - | 30 | pF |
| **ADC Analog Input Characteristics:** MIC → ADC, MIC Gain=20dB, IVOL=0dB, ALC1bit = "0" | | | | | |
| Resolution | | - | - | 16 | Bits |
| Input Voltage (MIC Gain=20dB,Note 10) | | 0.168 | 0.198 | 0.228 | Vpp |
| S/(N+D) (−1dBFS) (Note 11) | | 72 | 84 | - | dB |
| D-Range (−60dBFS) | | 75 | 85 | - | dB |
| S/N | | 75 | 85 | - | dB |
| **DAC Characteristics:** | | | | | |
| Resolution | | | | 16 | Bits |
| **Mono Line Output Characteristics:** AOUT pin, DAC → AOUT, $R_L$=10kΩ | | | | | |
| Output Voltage (Note 12) | | 1.78 | 1.98 | 2.18 | Vpp |
| S/(N+D) (0dBFS) (Note 11) | | 73 | 85 | - | dB |
| D-Range (-60dBFS) | | 83 | 93 | - | dB |
| S/N | | 83 | 93 | - | dB |
| Load Resistance | | 10 | - | - | kΩ |
| Load Capacitance | | - | - | 30 | pF |
| **Speaker-Amp Characteristics:** DAC → SPP/SPN pins, ALC2 bit = "0", $R_L$=8Ω, BTL, SVDD=3.3V | | | | | |
| Output Voltage | SPKG1-0 bits = "00" (-4.1dBFS) | 2.54 | 3.17 | 3.80 | Vpp |
| | SPKG1-0 bits = "01" (-4.1dBFS) | 3.20 | 4.00 | 4.80 | Vpp |
| S/(N+D) | As 150mW output power | 40 | 60 | - | dB |
| | As 400mW output power | - | 20 | - | dB |
| Output Noise Level | SPKG1-0 bits = "00" | - | -87 | - | dBV |
| | SPKG1-0 bits = "01" | -75 | -85 | - | dBV |
| | SPKG1-0 bits = "10" | - | -83 | - | dBV |
| Load Resistance | | 8 | - | - | Ω |
| Load Capacitance | | - | - | 30 | pF |

| Parameter | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Speaker-Amp Characteristics:** DAC → SPP/SPN pins, ALC2=OFF, $C_L$=3µF, $R_{serial}$=10Ω x 2, BTL, SVDD=3.8V | | | | | |
| Output Voltage | SPKG1-0 bits = "11" (-4.1dBFS) | - | 6.33 | - | Vpp |
| S/(N+D) (Note 13) | SPKG1-0 bits = "11" (-4.1dBFS) | - | 60 | - | dB |
| Output Noise Level (Note 13) SPKG1-0 bits = "11" | | - | -81 | - | dBV |
| Load Impedance (Note 14) | | 50 | - | - | Ω |
| Load Capacitance | | - | - | 3 | µF |
| **BEEP Input:** BEEP pin, External Input Resistance= 20kΩ | | | | | |
| Maximum Input Voltage (Note 15) | | - | 1.98 | - | Vpp |
| Output Voltage (Input Voltage=0.6Vpp) | | | | | |
| BEEP → SPP/SPN (SPKG1-0 bits = "00") | | 0.625 | 1.25 | 1.875 | Vpp |
| BEEP → AOUT | | 0.25 | 0.50 | 0.75 | Vpp |
| **Power Supplies** | | | | | |
| Power Up (PDN = "H") | | | | | |
| All Circuit Power-up: (Note 17) | | | | | |
| AVDD+DVDD | | | | | |
| | fs=8kHz | - | 8 | - | mA |
| | fs=48kHz | - | 11 | 17 | mA |
| SVDD: Speaker-Amp Normal Operation (SPPSN bit = "1", No Output) | | | | | |
| | SVDD=3.3V | - | 4 | 12 | mA |
| Power Down (PDN = "L") (Note 18) | | | | | |
| AVDD+DVDD+SVDD | | - | 1 | 100 | µA |

Note 8. It is a differential value of plus and minus input pin. Each input pins should be connected to the AC coupling capacitance serially. The differential input is not permission when MGAIN2-0 bits are "000". The Maximum input voltage of MICP and MICN pins are proportional to AVDD voltage. Vin= |(MICP) − (MICN)| = 0.069 x AVDD (max)@MGAIN2-0 bits = "001",
0.035 x AVDD (max)@MGAIN2-0 bits = "010", 0.017 x AVDD (max)@MGAIN2-0 bits = "011",
0.346 x AVDD (max)@MGAIN2-0 bits = "100", 0.218 x AVDD (max)@MGAIN2-0 bits = "101",
0.138 x AVDD (max)@MGAIN2-0 bits = "110", 0.098 x AVDD (max)@MGAIN2-0 bits = "111",
ADC function is not assumed for using the exceeded input voltage.

Note 9. Output Voltage is proportional to AVDD voltage. Vout = 0.8 x AVDD (typ).

Note 10. Input Voltage is proportional to AVDD voltage. Vin = 0.06 x AVDD (typ).

Note 11. When PLL reference clock is input to the FCK pin in PLL Slave Mode, S/(N+D):MIC→ADC is 75dB (typ) and S/(N+D):DAC→AOUT is 75dB(typ).

Note 12. Output Voltage is proportional to AVDD voltage. Vout = 0.6 x AVDD (typ).

Note 13. In case of measuring between SPP pin and SPN pin directly.

Note 14. Load impedance is total impedance of series resistance and piezo speaker impedance at 1kHz in Figure 41. Load capacitance is capacitance of piezo speaker. When piezo speaker is used, 10Ω or more series resistors should be connected at both SPP and SPN pins, respectively.

Note 15. The maximum input voltage of the BEEP is proportional to AVDD voltage and external input resistance (Rin). Vout = 0.6 x AVDD x Rin/20kΩ(max).

Note 16. Output Voltage is proportional to AVDD voltage. Vout = 0.6 x AVDD (typ).

Note 17. In case of PLL Master Mode (MCKI=12.288MHz) and PMMP = PMADC = PMDAC = PMPFIL = PMSPK = PMVCM = PMPLL = MCKO = PMAO = PMBP = PMMP = M/S ="1". In this case, the output current of MPI pin is 0mA.
When the AK4633 is EXT mode (PMPLL = MCKO = M/S = "0"), "AVDD+DVDD" is typically 6mA@fs=8kHz, 9mA@fs=48kHz.

Note 18. All digital inputs pins are fixed to DVDD or DVSS.

## FILTER CHRACTERISTICS

(Ta = 25°C; AVDD =2.2 ~ 3.6V, DVDD =1.6 ~ 3.6V, SVDD =2.2 ~ 4.0V; fs=8kHz)

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **ADC Digital Filter (Decimation LPF):** | | | | | | |
| Passband (Note 19) | ±0.16dB | PB | 0 | - | 3.0 | kHz |
| | −0.66dB | | - | 3.5 | - | kHz |
| | −1.1dB | | - | 3.6 | - | kHz |
| | −6.9dB | | - | 4.0 | - | kHz |
| Stopband (Note 19) | | SB | 4.7 | - | - | kHz |
| Passband Ripple | | PR | - | - | ±0.1 | dB |
| Stopband Attenuation | | SA | 73 | - | - | dB |
| Group Delay (Note 20) | | GD | - | 16 | - | 1/fs |
| Group Delay Distortion | | ΔGD | - | 0 | - | μs |
| **DAC Digital Filter (Decimation LPF):** | | | | | | |
| Passband (Note 19) | ±0.16dB | PB | 0 | - | 3.0 | |
| | −0.54dB | | - | 3.5 | - | |
| | −1.0dB | | - | 3.6 | - | |
| | −6.7dB | | - | 4.0 | - | |
| Stopband (Note 19) | | SB | 4.7 | - | - | kHz |
| Passband Ripple | | PR | - | - | ±0.1 | dB |
| Stopband Attenuation | | SA | 73 | - | - | dB |
| Group Delay (Note 20) | | GD | - | 16 | - | 1/fs |
| Group Delay Distortion | | ΔGD | - | 0 | - | μs |
| **DAC Digital Filter + Analog Filter:** | | | | | | |
| Frequency Response: 0 ~ 3.4kHz | | FR | - | ±1.0 | - | dB |

Note 19. The passband and stopband frequencies are proportional to fs (system sampling rate).
For example, ADC is PB=3.6kHz (@-1.0dB)= 0.45 x fs. A reference of frequency response is 1kHz.

Note 20. The calculated delay time caused by digital filtering. This time is from the input of analog signal to setting of the 16-bit data of a channel from the input register to the output register of the ADC.
For the DAC, this time is from setting the 16-bit data of a channel from the input register to the output of analog signal.
In case of selected the path through the programming filter (1st HPF + 2-band Equalizer + ALC), the Group Delay should be increased to 2/fs without the phase changing by IIR filter.

## DC CHRACTERISTICS

(Ta = 25°C; AVDD =2.2 ~ 3.6V, DVDD =1.6 ~ 3.6V, SVDD =2.2 ~ 4.0V)

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| High-Level Input Voltage | (DVDD ≥ 2.2V) | VIH | 70%DVDD | - | - | V |
| | (DVDD < 2.2V) | | 80%DVDD | - | - | V |
| Low-Level Input Voltage | (DVDD ≥ 2.2V) | VIL | - | - | 30%DVDD | V |
| | (DVDD < 2.2V) | | - | - | 20%DVDD | V |
| High-Level Output Voltage | (Iout=−80μA) | VOH | DVDD−0.4 | - | - | V |
| Low-Level Output Voltage | (Iout= 80μA) | VOL | - | - | 0.4 | V |
| Input Leakage Current | | Iin | - | - | ±10 | μA |

## SWITING CHARACTERISTICS

(Ta = 25°C; AVDD =2.2 ~ 3.6V, DVDD =1.6 ~ 3.6V, SVDD =2.2 ~ 4.0V; $C_L$=20pF)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **PLL Master Mode (PLL Reference Clock = MCKI pin) (Figure 2)** | | | | | |
| MCKI Input: Frequency | fCLK | 11.2896 | - | 27.0 | MHz |
| Pulse Width Low | tCLKL | 0.4/fCLK | - | - | ns |
| Pulse Width High | tCLKH | 0.4/fCLK | - | - | ns |
| MCKO Output: | | | | | |
| Frequency | fMCK | - | 256 x fFCK | - | kHz |
| Duty Cycle except fs=29.4kHz,32kHz | dMCK | 40 | 50 | 60 | % |
| fs=29.4kHz, 32kHz (Note 21) | dMCK | - | 33 | - | % |
| FCK Output: Frequency | fFCK | 8 | - | 48 | kHz |
| Pulse width High (DIF1-0 bits = "00" and FCKO bit = "1") | tFCKH | - | tBCK | - | ns |
| Duty Cycle (DIF1-0 bits ≠ "00" or FCKO bit = "0") | dFCK | - | 50 | - | % |
| BICK: Period (BCKO1-0 = "00") | tBCK | - | 1/16fFCK | - | ns |
| (BCKO1-0 = "01") | tBCK | - | 1/32fFCK | - | ns |
| (BCKO1-0 = "10") | tBCK | - | 1/64fFCK | - | ns |
| Duty Cycle | dBCK | - | 50 | - | % |
| Audio Interface Timing | | | | | |
| DSP Mode: (Figure 3, Figure 4) | | | | | |
| FCK "↑" to BICK "↑" (Note 22) | tDBF | 0.5 x tBCK -40 | 0.5 x tBCK | 0.5 x tBCK + 40 | ns |
| FCK "↑" to BICK "↓" (Note 23) | tDBF | 0.5 x tBCK -40 | 0.5 x tBCK | 0.5 x tBCK +40 | ns |
| BICK "↑" to SDTO (BCKP = "0") | tBSD | -70 | - | 70 | ns |
| BICK "↓" to SDTO (BCKP = "1") | tBSD | -70 | - | 70 | ns |
| SDTI Hold Time | tSDH | 50 | - | - | ns |
| SDTI Setup Time | tSDS | 50 | - | - | ns |
| Except DSP Mode: (Figure 5) | | | | | |
| BICK "↓" to FCK Edge | tBFCK | -40 | - | 40 | ns |
| FCK to SDTO (MSB) (Except $I^2S$ mode) | tFSD | -70 | - | 70 | ns |
| BICK "↓" to SDTO | tBSD | -70 | - | 70 | ns |
| SDTI Hold Time | tSDH | 50 | - | - | ns |
| SDTI Setup Time | tSDS | 50 | - | - | ns |

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **PLL Slave Mode (PLL Reference Clock: FCK pin) (Figure 6,Figure 7)** | | | | | |
| FCK: Frequency | fFCK | 7.35 | 8 | 48 | kHz |
| DSP Mode: Pulse Width High | tFCKH | tBCK-60 | - | 1/fFCK-tBCK | ns |
| Except DSP Mode: Duty Cycle | duty | 45 | - | 55 | % |
| BICK: Period | tBCK | 1/64fFCK | - | 1/16fFCK | ns |
| Pulse Width Low | tBCKL | 0.4 x tBCK | - | - | ns |
| Pulse Width High | tBCKH | 0.4 x tBCK | - | - | ns |
| **PLL Slave Mode (PLL Reference Clock: BICK pin) (Figure 6,Figure 7)** | | | | | |
| FCK: Frequency | fFCK | 7.35 | 8 | 48 | kHz |
| DSP Mode: Pulse width High | tFCKH | tBCK-60 | - | 1/fFCK-tBCK | ns |
| Except DSP Mode: Duty Cycle | duty | 45 | - | 55 | % |
| BICK: Period (PLL3-0 = "0001") | tBCK | - | 1/16fFCK | - | ns |
| (PLL3-0 = "0010") | tBCK | - | 1/32fFCK | - | ns |
| (PLL3-0 = "0011") | tBCK | - | 1/64fFCK | - | ns |
| Pulse Width Low | tBCKL | 0.4 x tBCK | - | - | ns |
| Pulse Width High | tBCKH | 0.4 x tBCK | - | - | ns |
| **PLL Slave Mode (PLL Reference Clock: MCKI pin) (Figure 8)** | | | | | |
| MCKI Input: Frequency | fCLK | 11.2896 | - | 27.0 | MHz |
| Pulse Width Low | fCLKL | 0.4/fCLK | - | - | ns |
| Pulse Width High | fCLKH | 0.4/fCLK | - | - | ns |
| MCKO Output: | | | | | |
| Frequency | fMCK | - | 256 x fFCK | - | kHz |
| Duty Cycle except fs=29.4kHz, 32kHz | dMCK | 40 | 50 | 60 | % |
| fs=29.4kHz, 32kHz (Note 21) | dMCK | - | 33 | - | % |
| FCK: Frequency | fFCK | 8 | - | 48 | kHz |
| DSP Mode: Pulse width High | tFCKH | tBCK-60 | - | 1/fFCK-tBFCK | ns |
| Except DSP Mode: Duty Cycle | duty | 45 | - | 55 | % |
| BICK: Period | tBCK | 1/64fFCK | - | 1/16fFCK | ns |
| Pulse Width Low | tBCKL | 0.4 x tBCK | - | - | ns |
| Pulse Width High | tBCKH | 0.4 x tBCK | - | - | ns |
| **Audio Interface Timing** | | | | | |
| DSP Mode: (Figure 9, Figure 10) | | | | | |
| FCK "↑" to BICK "↑" (Note 22) | tFCKB | 0.4 x tBCK | - | - | ns |
| FCK "↑" to BICK "↓" (Note 23) | tFCKB | 0.4 x tBCK | - | - | ns |
| BICK "↑" to FCK "↑" (Note 22) | tBFCK | 0.4 x tBCK | - | - | ns |
| BICK "↓" to FCK "↑" (Note 23) | tBFCK | 0.4 x tBCK | - | - | ns |
| BICK "↑" to SDTO (BCKP = "0") | tBSD | - | - | 80 | ns |
| BICK "↓" to SDTO (BCKP = "1") | tBSD | - | - | 80 | ns |
| SDTI Hold Time | tSDH | 50 | - | - | ns |
| SDTI Setup Time | tSDS | 50 | - | - | ns |
| Except DSP Mode: (Figure 12) | | | | | |
| FCK Edge to BICK "↑" (Note 24) | tFCKB | 50 | - | - | ns |
| BICK "↑" to FCK Edge (Note 24) | tBFCK | 50 | - | - | ns |
| FCK to SDTO (MSB) (Except $I^2S$ mode) | tFSD | - | - | 80 | ns |
| BICK "↓" to SDTO | tBSD | - | - | 80 | ns |
| SDTI Hold Time | tSDH | 50 | - | - | ns |
| SDTI Setup Time | tSDS | 50 | - | - | ns |

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **EXT Slave Mode (Figure 11)** | | | | | |
| MCKI Frequency: 256fs | fCLK | 1.8816 | 2.048 | 12.288 | MHz |
| 512fs | fCLK | 3.7632 | 4.096 | 13.312 | MHz |
| 1024fs | fCLK | 7.5264 | 8.192 | 13.312 | MHz |
| Pulse Width Low | tCLKL | 0.4/fCLK | - | - | ns |
| Pulse Width High | tCLKH | 0.4/fCLK | - | - | ns |
| FCK Frequency (MCKI = 256fs) | fFCK | 7.35 | 8 | 48 | kHz |
| (MCKI = 512fs) | fFCK | 7.35 | 8 | 26 | kHz |
| (MCKI = 1024fs) | fFCK | 7.35 | 8 | 13 | kHz |
| Duty Cycle | duty | 45 | - | 55 | % |
| BICK Period | tBCK | 312.5 | - | - | ns |
| BICK Pulse Width Low | tBCKL | 130 | - | - | ns |
| Pulse Width High | tBCKH | 130 | - | - | ns |
| Audio Interface Timing (Figure 12) | | | | | |
| FCK Edge to BICK "↑" (Note 24) | tFCKB | 50 | - | - | ns |
| BICK "↑" to FCK Edge (Note 24) | tBFCK | 50 | - | - | ns |
| FCK to SDTO (MSB) (Except $I^2S$ mode) | tFSD | - | - | 80 | ns |
| BICK "↓" to SDTO | tBSD | - | - | 80 | ns |
| SDTI Hold Time | tSDH | 50 | - | - | ns |
| SDTI Setup Time | tSDS | 50 | - | - | ns |

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **EXT Master Mode (Figure 2)** | | | | | |
| MCKI Frequency: 256fs | fCLK | 1.8816 | 2.048 | 12.288 | MHz |
| 512fs | fCLK | 3.7632 | 4.096 | 13.312 | MHz |
| 1024fs | fCLK | 7.5264 | 8.192 | 13.312 | MHz |
| Pulse Width Low | tCLKL | 0.4/fCLK | - | - | ns |
| Pulse Width High | tCLKH | 0.4/fCLK | - | - | ns |
| FCK Frequency (MCKI = 256fs) | fFCK | 7.35 | 8 | 48 | kHz |
| (MCKI = 512fs) | fFCK | 7.35 | 8 | 26 | kHz |
| (MCKI = 1024fs) | fFCK | 7.35 | 8 | 13 | kHz |
| Duty Cycle | dFCK | - | 50 | - | % |
| BICK: Period (BCKO1-0 bit= "00") | tBCK | - | 1/16fFCK | - | ns |
| (BCKO1-0 bit= "01") | tBCK | - | 1/32fFCK | - | ns |
| (BCKO1-0 bit= "10") | tBCK | - | 1/64fFCK | - | ns |
| Duty Cycle | dBCK | - | 50 | - | % |
| Audio Interface Timing | | | | | |
| DSP Mode: (Figure 3, Figure 4) | | | | | |
| FCK "↑" to BICK "↑" (Note 22) | tDBF | 0.5 x tBCK -40 | 0.5 x tBCK | 0.5 x tBCK + 40 | ns |
| FCK "↑" to BICK "↓" (Note 23) | tDBF | 0.5 x tBCK -40 | 0.5 x tBCK | 0.5 x tBCK +40 | ns |
| BICK "↑" to SDTO (BCKP bit= "0") | tBSD | -70 | - | 70 | ns |
| BICK "↓" to SDTO (BCKP bit= "1") | tBSD | -70 | - | 70 | ns |
| SDTI Hold Time | tSDH | 50 | - | - | ns |
| SDTI Setup Time | tSDS | 50 | - | - | ns |
| Except DSP Mode: (Figure 5) | | | | | |
| BICK "↓" to FCK Edge | tBFCK | -40 | - | 40 | ns |
| FCK to SDTO (MSB) | tFSD | -70 | - | 70 | ns |
| (Except $I^2S$ mode) | | | | | |
| BICK "↓" to SDTO | tBSD | -70 | - | 70 | ns |
| SDTI Hold Time | tSDH | 50 | - | - | ns |
| SDTI Setup Time | tSDS | 50 | - | - | ns |

Note 21. Duty Cycle = (the width of "L" ) / (the period of clock) x 100
Note 22. MSBS, BCKP bits = "00" or "11"
Note 23. MSBS, BCKP bits = "01" or "10"
Note 24. BICK rising edge must not occur at the same time as FCK edge.

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Control Interface Timing:** | | | | | |
| CCLK Period | tCCK | 200 | - | - | ns |
| CCLK Pulse Width Low | tCCKL | 80 | - | - | ns |
| Pulse Width High | tCCKH | 80 | - | - | ns |
| CDTI Setup Time | tCDS | 40 | - | - | ns |
| CDTI Hold Time | tCDH | 40 | - | - | ns |
| CSN "H" Time | tCSW | 150 | - | - | ns |
| CSN "↓" to CCLK "↑" | tCSS | 150 | - | - | ns |
| CCLK "↑" to CSN "↑" | tCSH | 50 | - | - | ns |
| CCLK "↓" to CDTI (at Read Command) | tDCD | - | - | 70 | ns |
| CSN "↑" to CDTI (Hi-Z) (at Read Command) | tCCZ | - | - | 70 | ns |
| **Reset Timing** | | | | | |
| PDN Pulse Width (Note 25) | tPD | 150 | - | - | ns |
| PMADC "↑" to SDTO valid (Note 26) | | | | | |
| ADRST bit = "0" | tPDV | - | 1059 | - | 1/fs |
| ADRST bit = "1" | tPDV | - | 291 | - | 1/fs |

Note 25. The AK4633 can be reset by the PDN pin = "L".
Note 26. This is the count of FCK "↑" from the PMADC bit = "1".

## ■ Timing Diagram

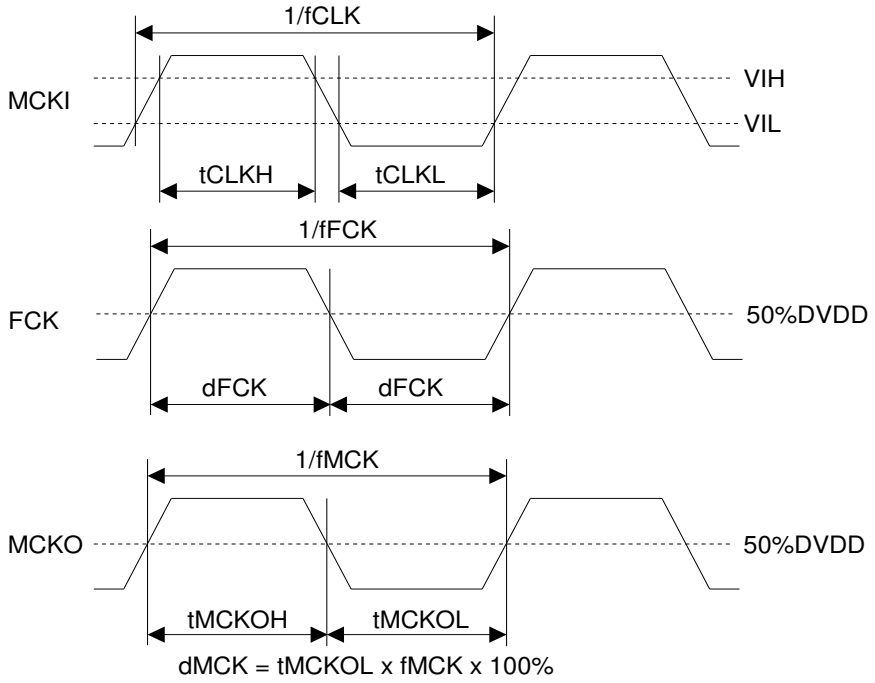



Figure 2. Clock Timing (PLL/EXT Master mode) (MCKO is not available at EXT Master Mode)

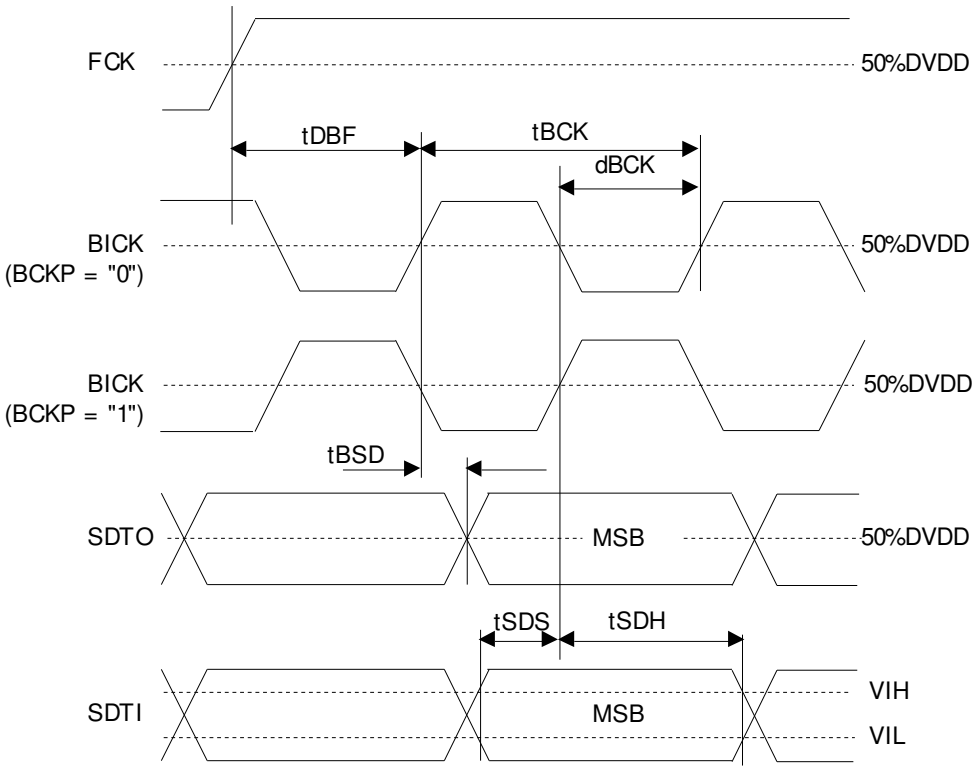



Figure 3. Audio Interface Timing (PLL/EXT Master mode & DSP mode: MSBS bit= “0”)

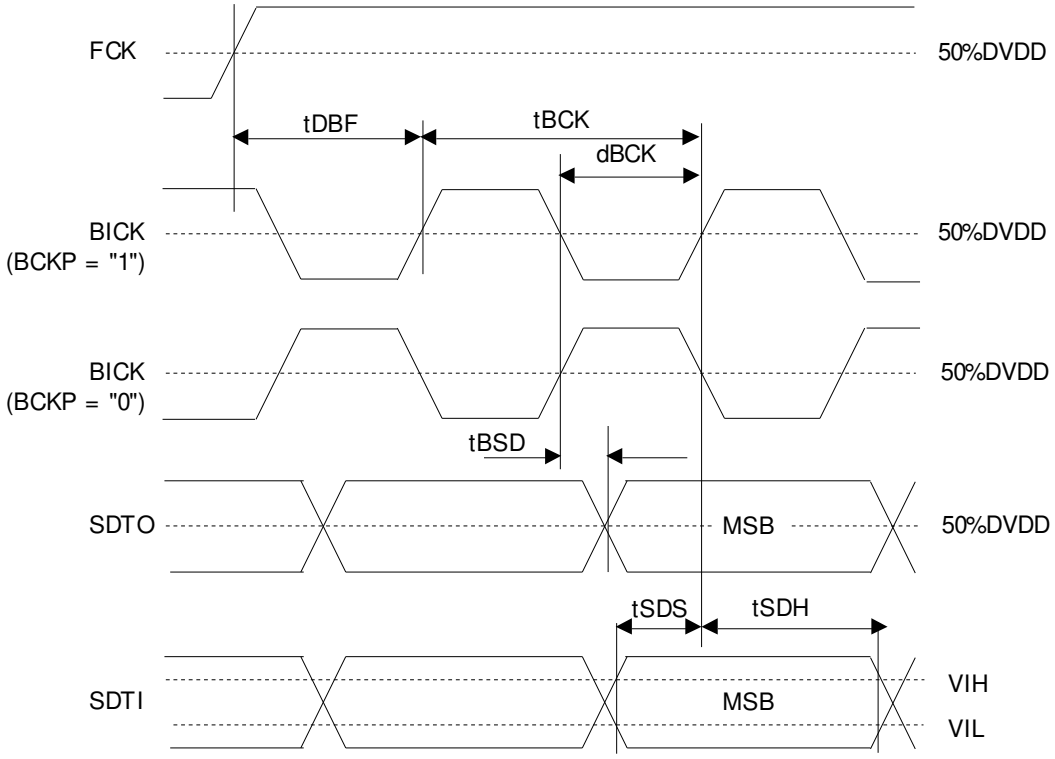



Figure 4. Audio Interface Timing (PLL/EXT Master mode & DSP mode: MSBS bit = "1")

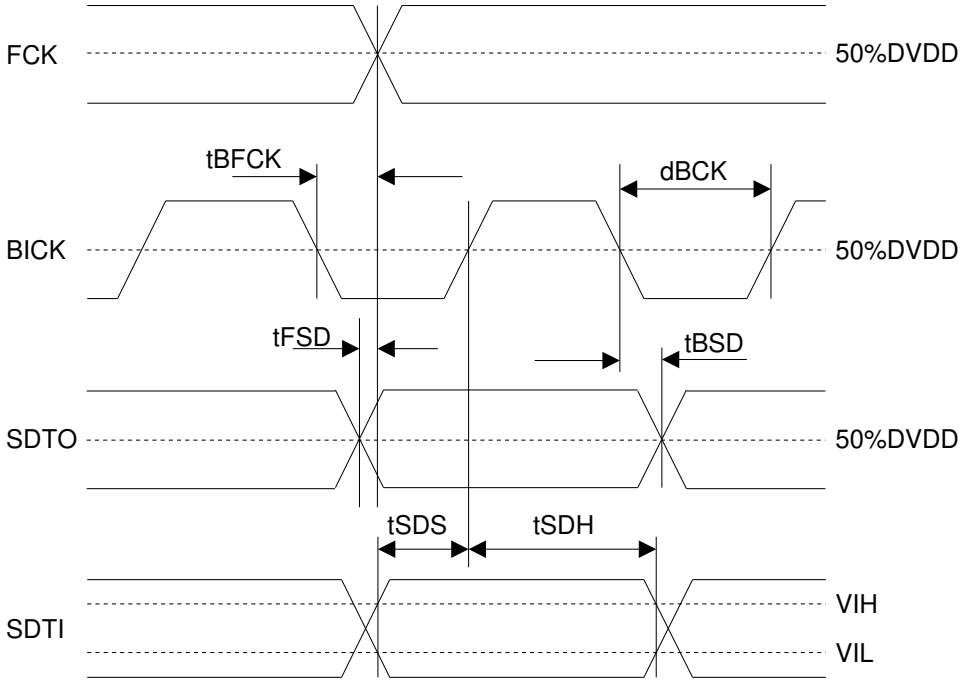



Figure 5. Audio Interface Timing (PLL/EXT Master mode & Except DSP mode)

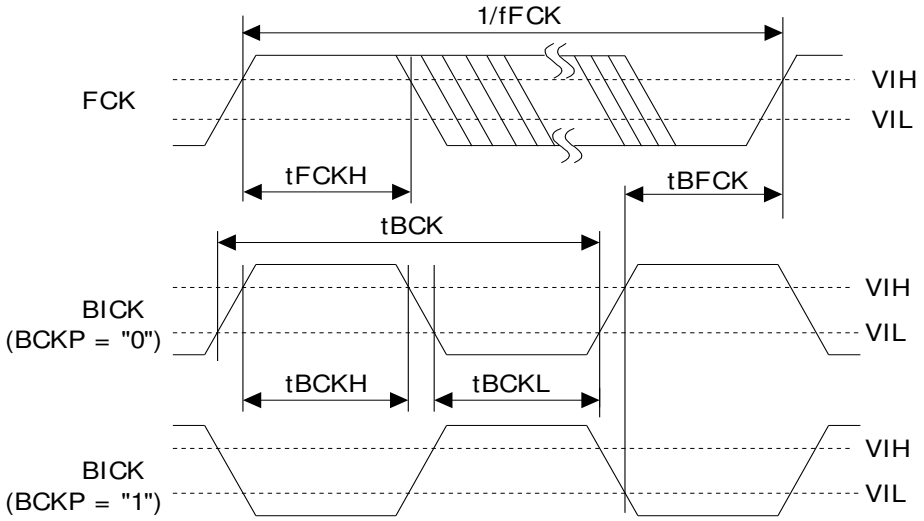



Figure 6. Clock Timing (PLL Slave mode**;** PLL Reference Clock = FCK or BICK pin & DSP mode; MSBS bit = "0")

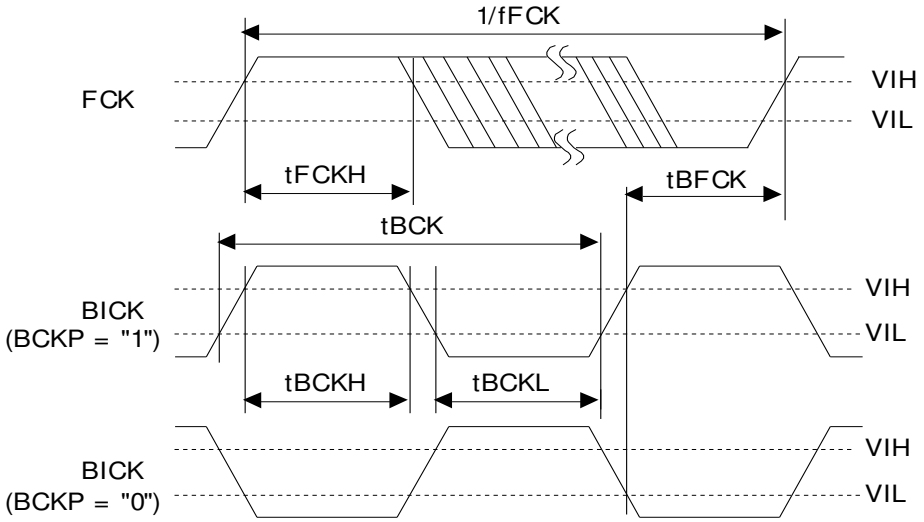



Figure 7. Clock Timing (PLL Slave mode; PLL Reference Clock = FCK or BICK pin & DSP mode; MSBS bit= "1")

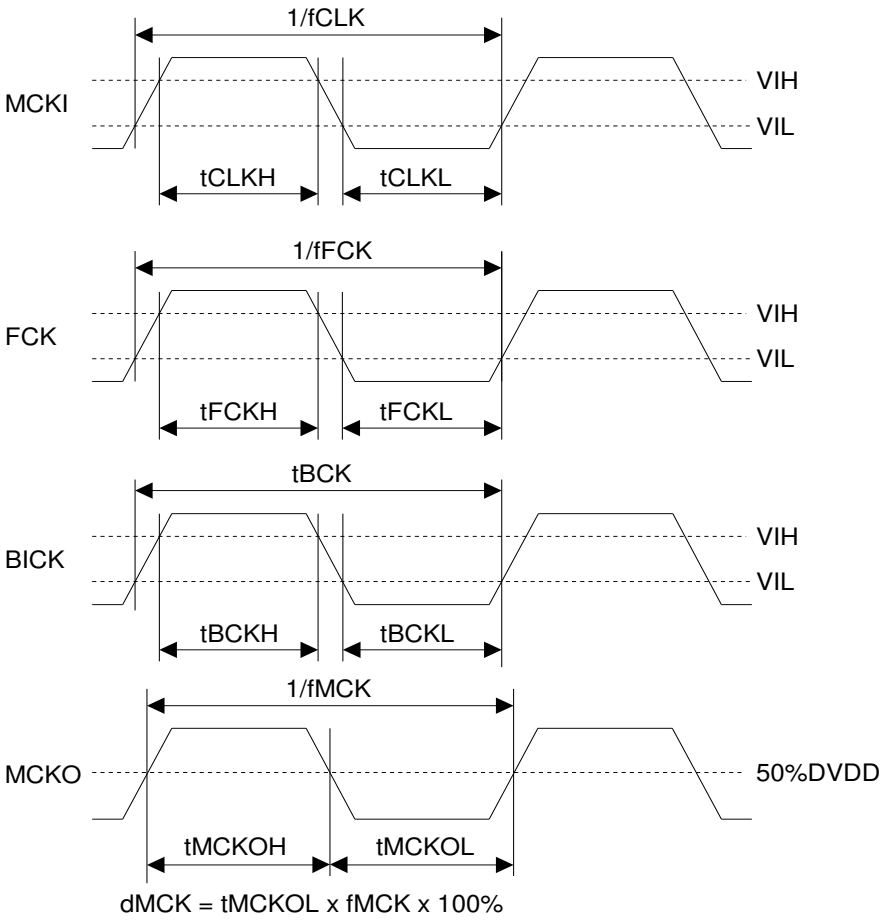



Figure 8. Clock Timing (PLL Slave mode; PLL Reference Clock = MCKI pin & Except DSP mode)

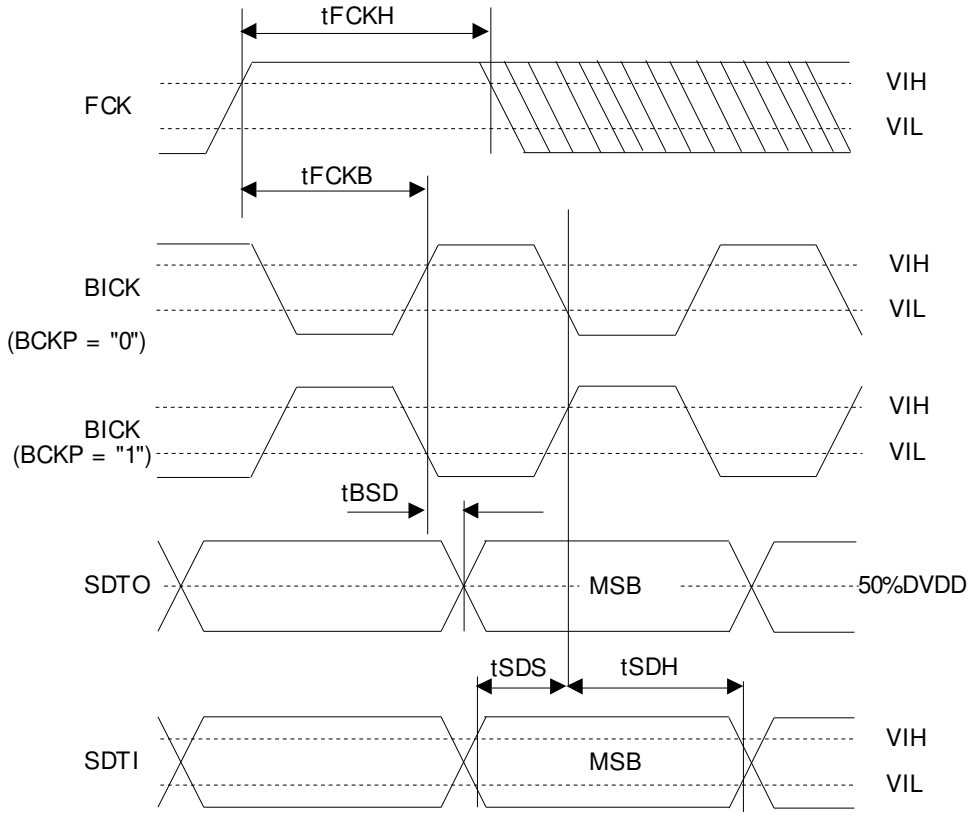



Figure 9. Audio Interface Timing (PLL Slave mode & DSP mode; MSBS bit= "0")

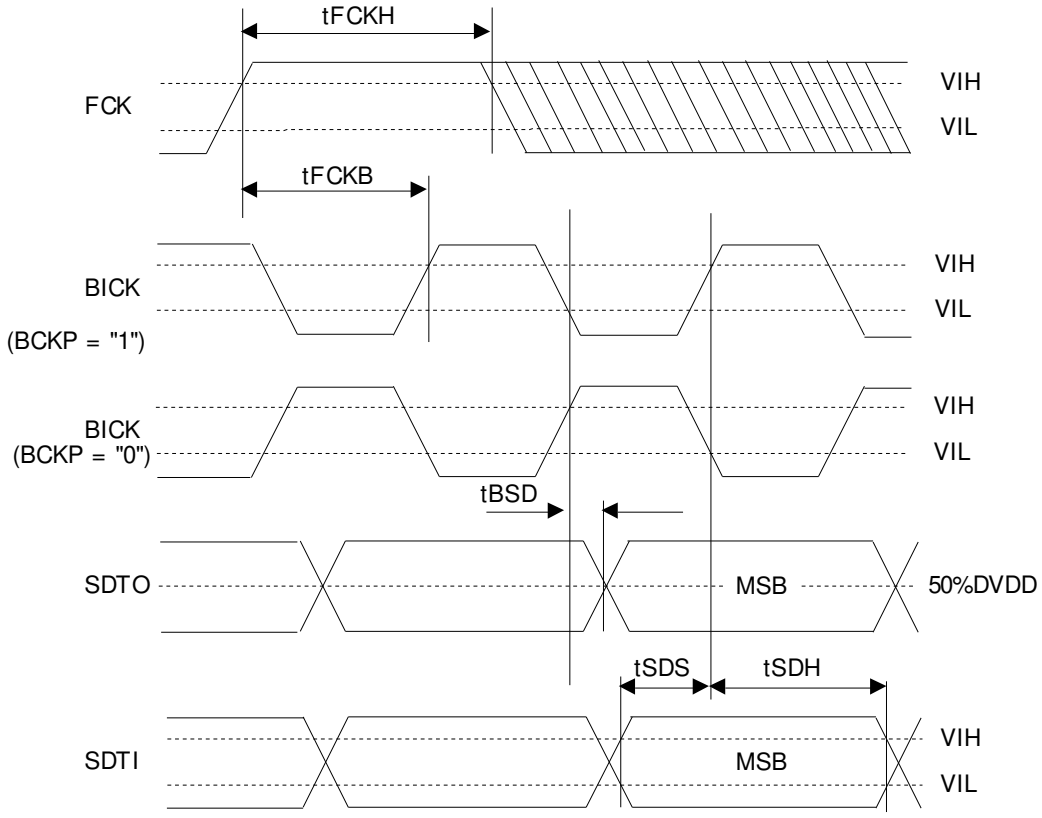



Figure 10. Audio Interface Timing (PLL Slave mode, DSP mode; MSBS bit= "1")

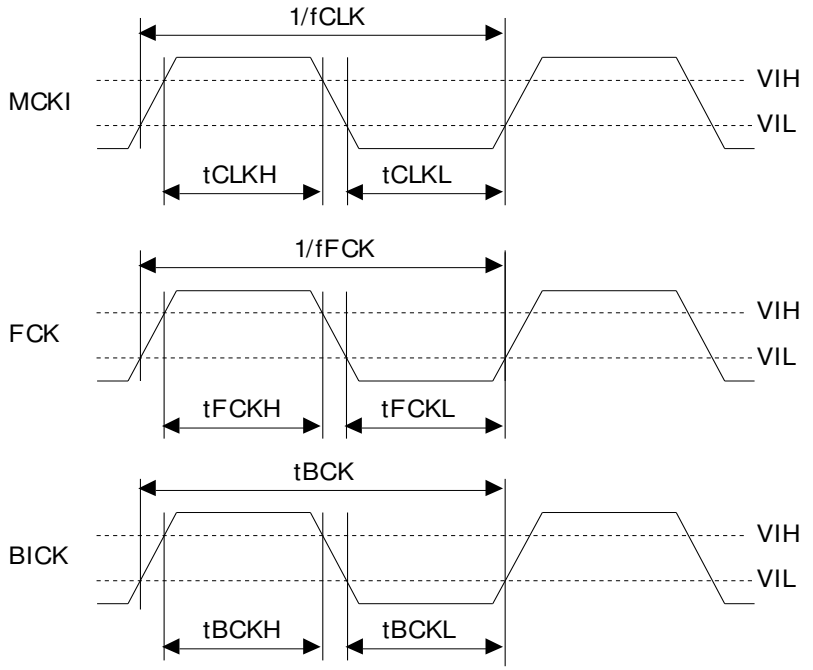



Figure 11. Clock Timing (EXT Slave mode)

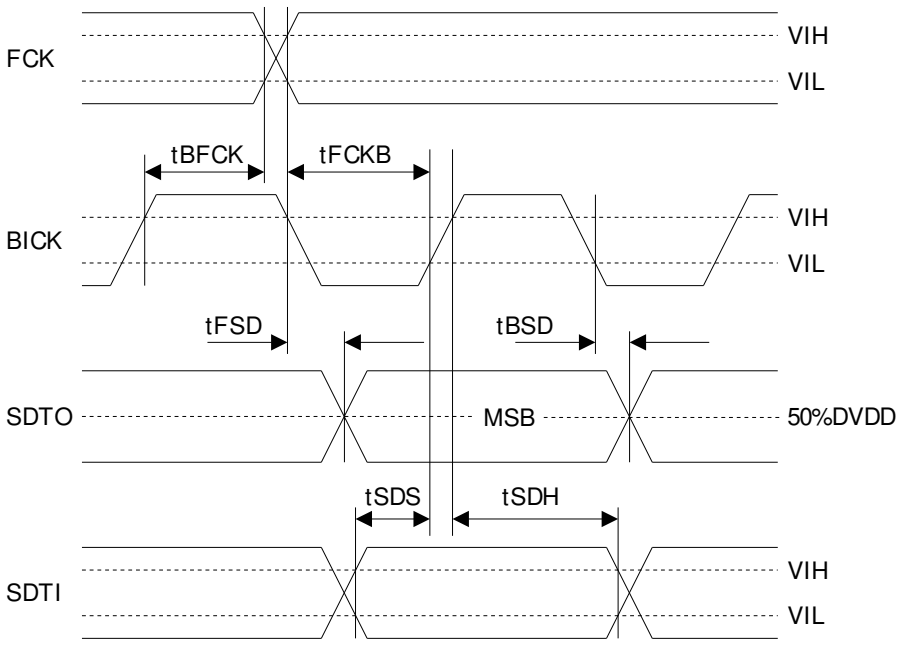



Figure 12. Audio Interface Timing (PLL, EXT Slave mode & Except DSP mode)

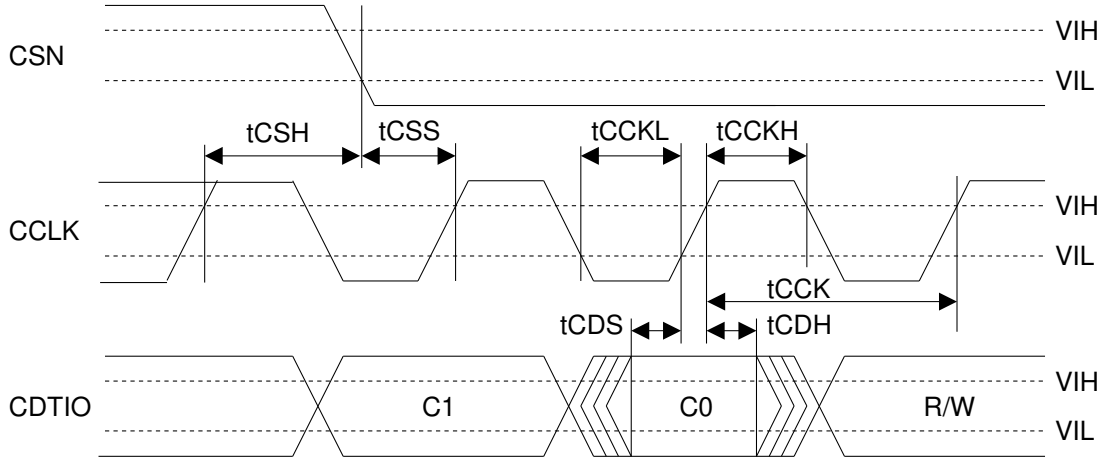



Figure 13. WRITE Command Input Timing

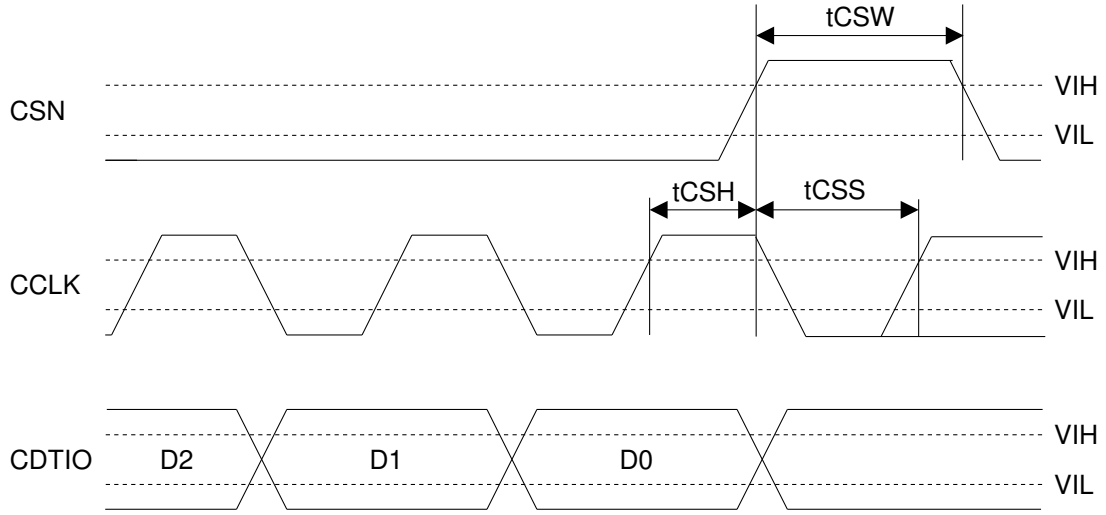



Figure 14. WRITE Data Input Timing

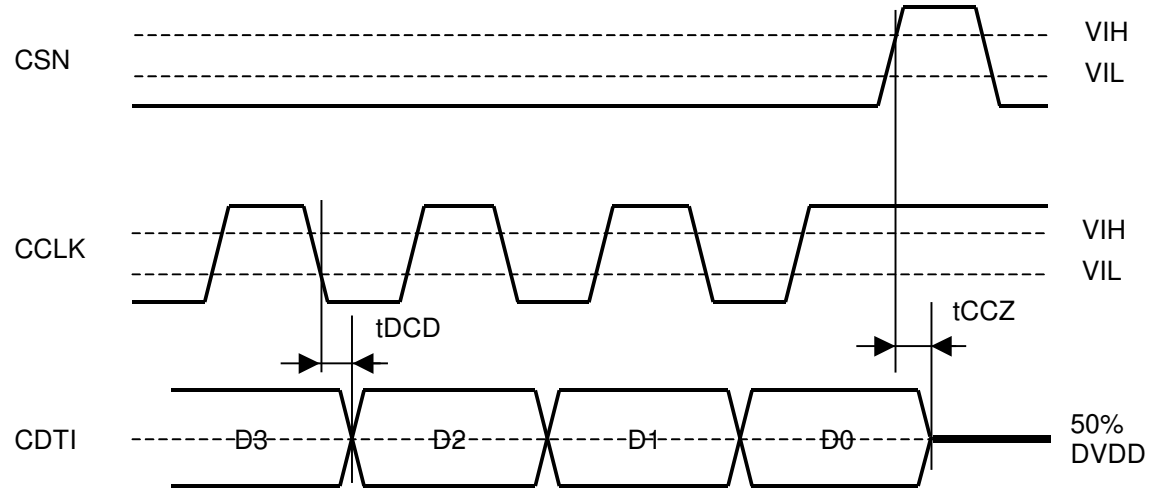



Figure 15 . Read Data Output Timing

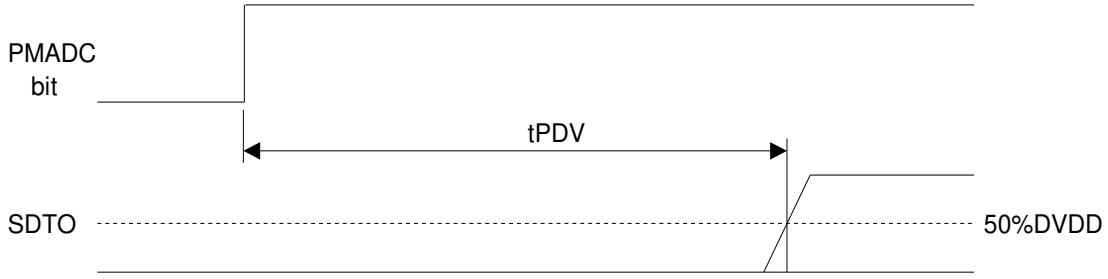



Figure 16. Power Down & Reset Timing 1

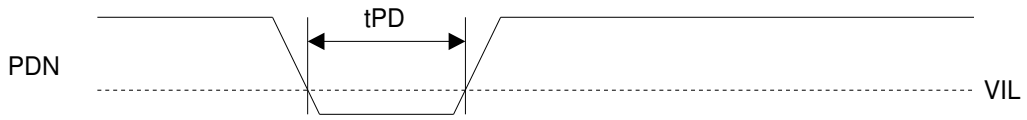



Figure 17. Power Down & Reset Timing 2

# OPERATION OVERVIEW

## ■ System Clock

There are the following four clock modes to interface with external devices (Table 1 and Table 2).

| Mode | PMPLL bit | M/S bit | PLL3-0 bit | Figure |
|---|---|---|---|---|
| PLL Master Mode | 1 | 1 | Table 4 | Figure 18 |
| PLL Slave Mode 1<br>(PLL Reference Clock: MCKI pin) | 1 | 0 | Table 4 | Figure 19 |
| PLL Slave Mode 2<br>(PLL Reference Clock: FCK or BICK pin) | 1 | 0 | Table 4 | Figure 20 |
| EXT Slave Mode | 0 | 0 | X | Figure 21 |
| EXT Master Mode | 0 | 1 | X | Figure 22 |

Table 1. Clock Mode Setting (X: Don't care)

| Mode | MCKO bit | MCKO pin | MCKI pin | BICK pin | FCK pin |
|---|---|---|---|---|---|
| PLL Master Mode | 0 | "L" Output | Master Clock Input for PLL (Note 27) | 16fs/32fs/64fs Output | 1fs Output |
| | 1 | 256fs Output | | | |
| PLL Slave Mode 1<br>(PLL Reference Clock: MCKI pin) | 0 | "L" Output | Master Clock Input for PLL (Note 27) | 16fs/32fs/64fs Input | 1fs Input |
| | 1 | 256fs Output | | | |
| PLL Slave Mode 2<br>(PLL Reference Clock: FCK or BICK pin) | 0 | "L" Output | GND | 16fs/32fs/64fs Input | 1fs Input |
| EXT Slave Mode | 0 | "L" Output | 256fs/ 512fs/ 1024fs Input | ≥ 32fs Input | 1fs Input |
| EXT Master Mode | 0 | "L" Output | 256fs/ 512fs/ 1024fs Input | 32fs/64fs Output | 1fs Output |

Note 27. 11.2896MHz/12MHz/12.288MHz/13.5MHz/24MHz/27MHz

Table 2. Clock pins state in Clock Modes

## ■ Master Mode/Slave Mode

The M/S bit selects either master or slave modes. M/S bit = "1" selects master mode and "0" selects slave mode. When the AK4633 is power-down mode (PDN pin = "L") and exits reset state, the AK4633 is in slave mode. After exiting reset state, the AK4633 becames master mode by changing M/S bit to "1".

When the AK4633 is used in master mode, FCK and BICK pins are a floating state until M/S bit becomes "1". FCK and BICK pins of the AK4633 should be pulled-down or pulled-up by a resistor about 100kΩ externally to avoid the floating state.

| M/S bit | Mode | |
|---|---|---|
| 0 | Slave Mode | (default) |
| 1 | Master Mode | |

Table 3. Select Master/Salve Mode

## ■ PLL Mode

When PMPLL bit is "1", a fully integrated analog phase locked loop (PLL) generates a clock that is selected by the PLL3-0 and FS3-0 bits. The PLL lock time is shown in Table 4, whenever the AK4633 is supplied to a stable clocks after PLL is powered-up (PMPLL bit = "0" → "1") or sampling frequency changes.

1) Setting of PLL Mode

| Mode | PLL3 bit | PLL2 bit | PLL1 bit | PLL0 bit | PLL Reference Clock Input Pin | Input Frequency | R and C of VCOC pin(Note 28) | | PLL Lock Time (max) | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | R[Ω] | C[F] | | |
| 0 | 0 | 0 | 0 | 0 | FCK pin | 1fs | 6.8k | 220n | 160ms | (default) |
| 1 | 0 | 0 | 0 | 1 | BICK pin | 16fs | 10k | 4.7n | 2ms | |
| 2 | 0 | 0 | 1 | 0 | BICK pin | 32fs | 10k | 4.7n | 2ms | |
| 3 | 0 | 0 | 1 | 1 | BICK pin | 64fs | 10k | 4.7n | 2ms | |
| 4 | 0 | 1 | 0 | 0 | MCKI pin | 11.2896MHz | 10k | 4.7n | 40ms | |
| 5 | 0 | 1 | 0 | 1 | MCKI pin | 12.288MHz | 10k | 4.7n | 40ms | |
| 6 | 0 | 1 | 1 | 0 | MCKI pin | 12MHz | 10k | 4.7n | 40ms | |
| 7 | 0 | 1 | 1 | 1 | MCKI pin | 24MHz | 10k | 4.7n | 40ms | |
| 12 | 1 | 1 | 0 | 0 | MCKI pin | 13.5MHz | 10k | 10n | 40ms | |
| 13 | 1 | 1 | 0 | 1 | MCKI pin | 27MHz | 10k | 10n | 40ms | |
| Others | Others | | | | N/A | | | | | |

Note 28. The tolerance of R is ±5%, C is ±30%.

Table 4. Setting of PLL Mode (*fs: Sampling Frequency)

2) Setting of sampling frequency in PLL Mode.
When PLL2 bit is "1" (PLL reference clock input is the MCKI pin), the sampling frequency is selected by FS2-0 bits as defined in Table 5.

| Mode | FS3 bit | FS2 bit | FS1 bit | FS0 bit | Sampling Frequency | |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 8kHz | (default) |
| 1 | 0 | 0 | 0 | 1 | 12kHz | |
| 2 | 0 | 0 | 1 | 0 | 16kHz | |
| 3 | 0 | 0 | 1 | 1 | 24kHz | |
| 4 | 0 | 1 | 0 | 0 | 7.35kHz | |
| 5 | 0 | 1 | 0 | 1 | 11.025kHz | |
| 6 | 0 | 1 | 1 | 0 | 14.7kHz | |
| 7 | 0 | 1 | 1 | 1 | 22.05kHz | |
| 10 | 1 | 0 | 1 | 0 | 32kHz | |
| 11 | 1 | 0 | 1 | 1 | 48kHz | |
| 14 | 1 | 1 | 1 | 0 | 29.4kHz | |
| 15 | 1 | 1 | 1 | 1 | 44.1kHz | |
| Others | Others | | | | N/A | |

Table 5. Setting of Sampling Frequency at PLL2 bit = "1" and PMPLL bit = "1"

When PLL2 bit is “0”(PLL reference clock input is FCK or BICK pin), the sampling frequency is selected by FS3-2 bits (Table 6).

| Mode | FS3 bit | FS2 bit | FS1 bit | FS0 bit | Sampling Frequency Range | |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | Don’t care | Don’t care | 7.35kHz ≤ fs ≤ 12kHz | (default) |
| 1 | 0 | 1 | Don’t care | Don’t care | 12kHz < fs ≤ 24kHz | |
| 2 | 1 | 0 | Don’t care | Don’t care | 24kHz < fs ≤ 48kHz | |
| Others | Others | | | | N/A | |

Table 6. Setting of Sampling Frequency at PLL2 bit = “0” and PMPLL bit = “1”

## ■ PLL Unlock State

1) PLL Master Mode (PMPLL bit = “1”, M/S bit = “1”)

In this mode, until PLL is locked after PMPLL bit = “0” → “1”, BICK and FCK pins output “L” and invalid frequency clock is output from the MCKO pin when MCKO bit is “1”. If MCKO bit is “0”, “L” is output from the MCKO pin. (Table 7)

In case that sampling frequency is changed, setting PMPLL bit to “0” could prevent unstable clocks, and BICK and FCK pins output “L”.

| PLL State | MCKO pin | | BICK pin | FCK pin |
|---|---|---|---|---|
| | MCKO bit = “0” | MCKO bit = “1” | | |
| After that PMPLL bit “0” → “1” | “L” Output | Invalid | “L” Output | “L” Output |
| PLL Unlock | “L” Output | Invalid | Invalid | Invalid |
| PLL Lock | “L” Output | 256fs Output | See Table 9 | 1fs Output |

Table 7. Clock Operation at PLL Master Mode (PMPLL bit = “1”, M/S bit = “1”)

2) PLL Slave Mode (PMPLL bit = “1”, M/S bit = “0”)

In this mode, an invalid clock is output from the MCKO pin after PMPLL bit = “0” → “1” or when sampling frequency is changed. After that, 256fs clock is output from the MCKO pin while PLL is locked. ADC and DAC output invalid data while the PLL is unlocked. For DAC, this output signal should be muted by writing “0” to DACA and DACM bits in Addr = 02H.

| PLL State | MCKO pin | |
|---|---|---|
| | MCKO bit = “0” | MCKO bit = “1” |
| After that PMPLL bit “0” → “1” | “L” Output | Invalid |
| PLL Unlock | “L” Output | Invalid |
| PLL Lock | “L” Output | 256fs Output |

Table 8. Clock Operation at PLL Slave Mode (PMPLL bit = “0”, M/S bit = “0”)

## ■ PLL Master Mode (PMPLL bit = “1”, M/S bit = “1”)

When an external clock (11.2896MHz, 12MHz , 12.288MHz, 13.5MHz, 24MHz or 27MHz) is input to the MCKI pin, the MCKO, BICK and FCK clocks are generated by an internal PLL circuit. The MCKO output frequency is fixed to 256fs, the output is enabled by MCKO bit. The BICK is selected among 16fs, 32fs or 64fs, by BCKO1-0 bits (Table 9).

In DSP mode, FCK output can select Duty 50% or High-output only during 1 BICK cycle (Note 10). Except DSP mode, FCKO bit should be set “0”.

When the BICK output frequency is 16fs, the audio interface format supports only Mode 0 (DSP Mode).

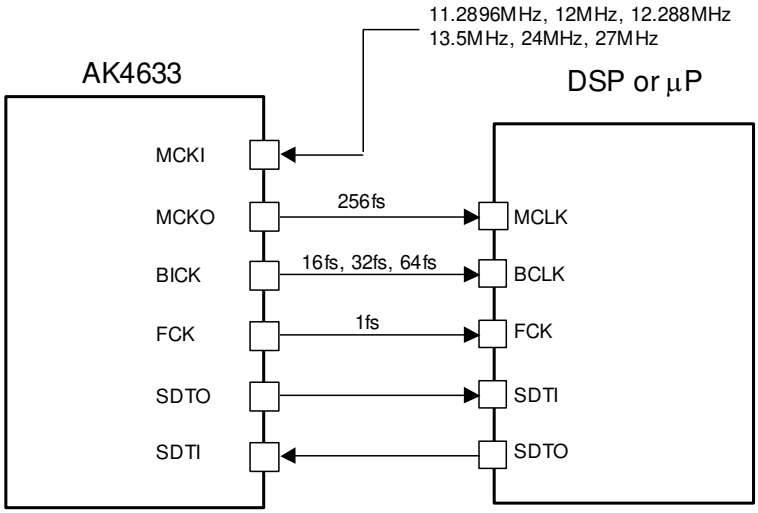



Figure 18. PLL Master Mode

| Mode | BCKO1 | BCKO0 | BICK Output Frequency | |
|---|---|---|---|---|
| 0 | 0 | 0 | 16fs | (default) |
| 1 | 0 | 1 | 32fs | |
| 2 | 1 | 0 | 64fs | |
| 3 | 1 | 1 | N/A | |

Table 9. BICK Output Frequency at PLL Master Mode

| Mode | FCKO | FCK Output | |
|---|---|---|---|
| 0 | 0 | Duty = 50% | (default) |
| 1 | 1 | High Width = 1/fBCK | |

fBCK is the output frequency of BICK

Table 10. FCK Output at PLL Master Mode and DSP Mode

## ■ PLL Slave Mode (PMPLL bit = “1”, M/S bit = “0”)

A reference clock of PLL is selected among the input clocks to MCKI, BICK or FCK pin. The required clock to the AK4633 is generated by an internal PLL circuit. Input frequency is selected by PLL3-0 bits. When the BICK input frequency is 16fs, the audio interface format supports only Mode 0(DSP Mode).

### a) PLL reference clock: MCKI pin

BICK and FCK inputs must be synchronized with MCKO output. The phase between MCKO and FCK dose not matter. Sampling frequency can be selected by FS3-0 bits (Table 5).

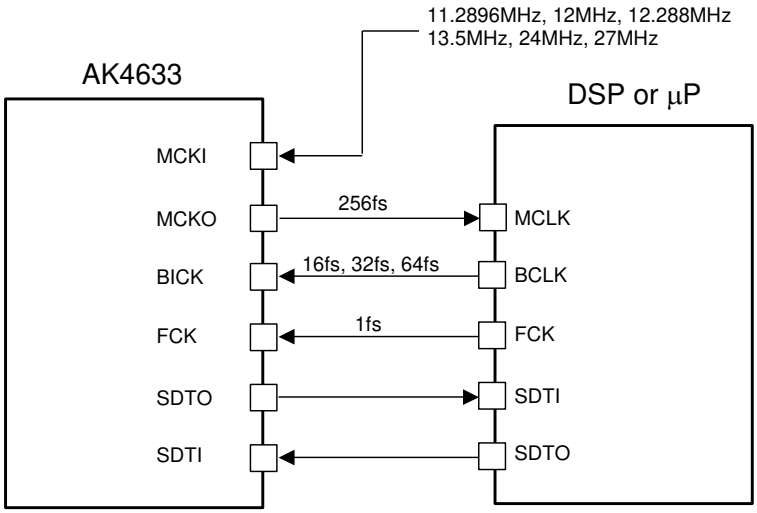



Figure 19. PLL Slave Mode1 (PLL Reference Clock: MCKI pin)

### b) PLL reference clock: BICK or FCK pin

In case of using BICK or FCK as PLL reference clock, the sampling frequency corresponds to 7.35kHz to 48kHz by FS3-0 bits (Table 6).

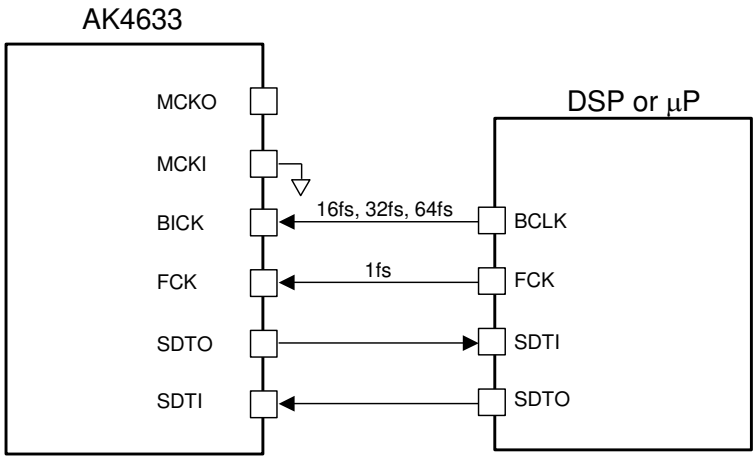



Figure 20. PLL Slave Mode 1 (PLL Reference Clock: FCK or BICK pin)

The external clocks (MCKI, BICK and FCK) should always be present whenever the ADC or DAC or Programmable Filter are in operation (PMADC bit = “1” or PMDAC bit = “1” or PMPFIL bit = “1”). If these clocks are not provided, the AK4633 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If the external clocks are not present, the ADC, DAC and Programmable Filter should be in the power-down mode (PMADC bit =PMDAC bit = PMPFIL bit = “0”).

## ■ EXT Slave Mode (PMPLL bit = "0", M/S bit = "0")

When PMPLL bit is "0" and M/S bit is "0", the AK4633 becomes EXT slave mode. Master clock is input from the MCKI pin, the internal PLL circuit is not operated. This mode is compatible with I/F of the normal audio CODEC. The clocks required to operate are MCKI (256fs, 512fs or 1024fs), BICK (≥32fs) and FCK (fs). The master clock (MCKI) should be synchronized with FCK. The phase between these clocks does not matter. The input frequency of MCKI is selected by FS3-0 bits (Table 11).

| Mode | FS3-2 bits | FS1 bit | FS0 bit | MCKI Input Frequency | Sampling Frequency Range | |
|---|---|---|---|---|---|---|
| 0 | Don't care | 0 | 0 | 256fs | 7.35kHz ≤ fs ≤ 48kHz | (default) |
| 1 | Don't care | 0 | 1 | 1024fs | 7.35kHz < fs ≤ 13kHz | |
| 2 | Don't care | 1 | 0 | 512s | 7.35kHz < fs ≤ 26kHz | |
| 3 | Don't care | 1 | 1 | 256fs | 7.35kHz < fs ≤ 48kHz | |

Table 11. Setting MCKI Frequency at EXT Slave Mode (PMPLL bit = "0", M/S bit = "0")

**External Slave Mode does not support Mode 0 (DSP Mode) of Audio Interface Format.**

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. The out-of-band noise can be reduced by using higher frequency of the master clock. The S/N of the DAC output through AOUT amp at fs=8kHz is shown in Table 12.

| MCKI | S/N (fs=8kHz, 20kHzLPF + A-weighted) |
|---|---|
| 256fs | 84dB |
| 512fs | 92dB |
| 1024fs | 92dB |

Table 12. Relationship between MCKI and S/N of AOUT

The external clocks (MCKI, BICK and FCK) should always be present whenever the ADC or DAC or Programmable Filter are in operation (PMADC bit = "1" or PMDAC bit = "1" or PMPFIL bit = "1"). If these clocks are not provided, the AK4633 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If the external clocks are not present, the ADC, DAC and Programmable Filter should be in the power-down mode (PMADC bit =PMDAC bit = PMPFIL bit = "0").

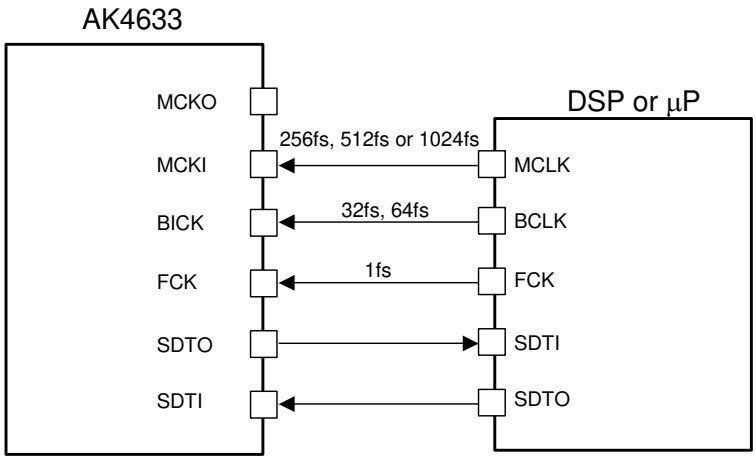



Figure 21. EXT Slave Mode

## ■ EXT Master Mode (PMPLL bit = "0", M/S bit = "1")

When PMPLL bit is "0" and M/S bit is "1", the AK4633 becomes clock master mode(EXT Master Mode). Master clock is input from MCKI pin, the internal PLL circuit is not operated. The clock required to operate is MCKI (256fs, 512fs or 1024fs). The input frequency of MCKI is selected by FS3-0 bits (Table 11). The output frequency of BICK is selected to 32fs or 64fs by setting BCKO1-0 bit (Table 14). FCK bit should be set to "0".

| Mode | FS3-2 bits | FS1 bit | FS0 bit | MCKI Input Frequency | Sampling Frequency Range | |
|---|---|---|---|---|---|---|
| 0 | Don't care | 0 | 0 | 256fs | 7.35kHz ≤ fs ≤ 48kHz | (default) |
| 1 | Don't care | 0 | 1 | 1024fs | 7.35kHz < fs ≤ 13kHz | |
| 2 | Don't care | 1 | 0 | 512s | 7.35kHz < fs ≤ 26kHz | |
| 3 | Don't care | 1 | 1 | 256fs | 7.35kHz < fs ≤ 48kHz | |

Table 13. Setting MCKI Frequency at EXT Slave Mode (PMPLL bit = "0", M/S bit = "1")

**External Master Mode does not support Mode 0 (DSP Mode) of Audio Interface Format.**

MCKI should always be present whenever the ADC or DAC or Programmable Filter is in operation (PMADC bit = "1" or PMDAC bit = "1" or PMPFIL bit = "1"). If MCKI is not provided, the AK4633 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If MCKI is not present, the ADC, DAC and Programmable Filter should be in the power-down mode (PMADC bit =PMDAC bit = PMPFIL bit = "0").

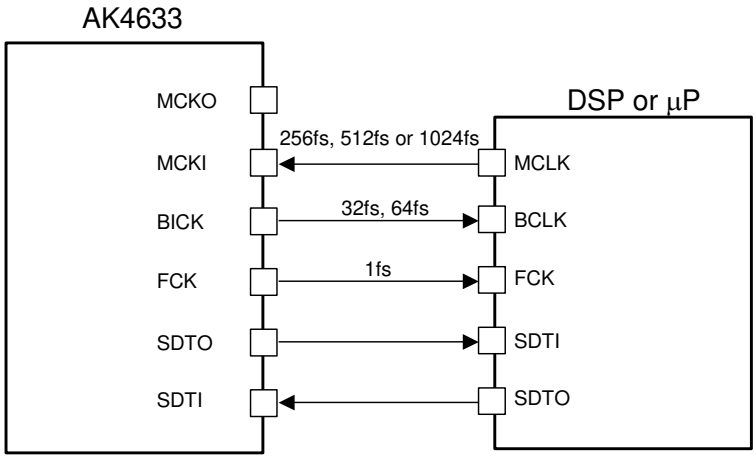



Figure 22. EXT Master Mode

| Mode | BCKO1 | BCKO0 | BICK Output Frequency | |
|---|---|---|---|---|
| 0 | 0 | 0 | N/A | (default) |
| 1 | 0 | 1 | 32fs | |
| 2 | 1 | 0 | 64fs | |
| 3 | 1 | 1 | N/A | |

Table 14. BICK Output Frequency at EXT Master Mode

## ■ Audio Interface Format

Four types of data formats are available and are selected by setting the DIF1-0 bits (Table 15). In all modes, the serial data is MSB first, 2's complement format. Audio interface formats can be used in both master and slave modes. FCK and BICK are output from the AK4633 in master mode, but must be input to the AK4633 in slave mode.

In Mode 1-3, the SDTO is clocked out on the falling edge of BICK and the SDTI is latched on the rising edge.

| Mode | DIF1 | DIF0 | SDTO (ADC) | SDTI (DAC) | BICK | Figure | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | DSP Mode | DSP Mode | ≥ 16fs | Table 16 | |
| 1 | 0 | 1 | MSB justified | LSB justified | ≥ 32fs | Figure 23 | |
| 2 | 1 | 0 | MSB justified | MSB justified | ≥ 32fs | Figure 24 | (default) |
| 3 | 1 | 1 | $I^2S$ compatible | $I^2S$ compatible | ≥ 32fs | Figure 25 | |

Table 15. Audio Interface Format

In Mode0 (DSP mode), the audio I/F timing is changed by BCKP and MSBS bits.

When BCKP bit is "0", SDTO data is output by rising edge of BICK, SDTI data is latched on a falling edge of BICK.
When BCKP bit is "1", SDTO data is output by falling edge of BICK, SDTI data is latched on a rising edge of BICK.

MSB data position of SDTO and SDTI can be shifted by MSBS bit. The shifted period is a half of BICK.

| MSBS bit | BCKP bit | Audio Interface Format | |
|---|---|---|---|
| 0 | 0 | Figure 26 | (default) |
| 0 | 1 | Figure 27 | |
| 1 | 0 | Figure 28 | |
| 1 | 1 | Figure 29 | |

Table 16. Audio Interface Format in Mode 0

If 16-bit data that ADC outputs is converted to 8-bit data by removing LSB 8-bit, "−1" at 16bit data is converted to "−1" at 8-bit data. And when the DAC playbacks this 8-bit data, "−1" at 8-bit data will be converted to "−256" at 16-bit data and this is a large offset. This offset can be removed by adding the offset of "128" to 16-bit data before converting to 8-bit data.

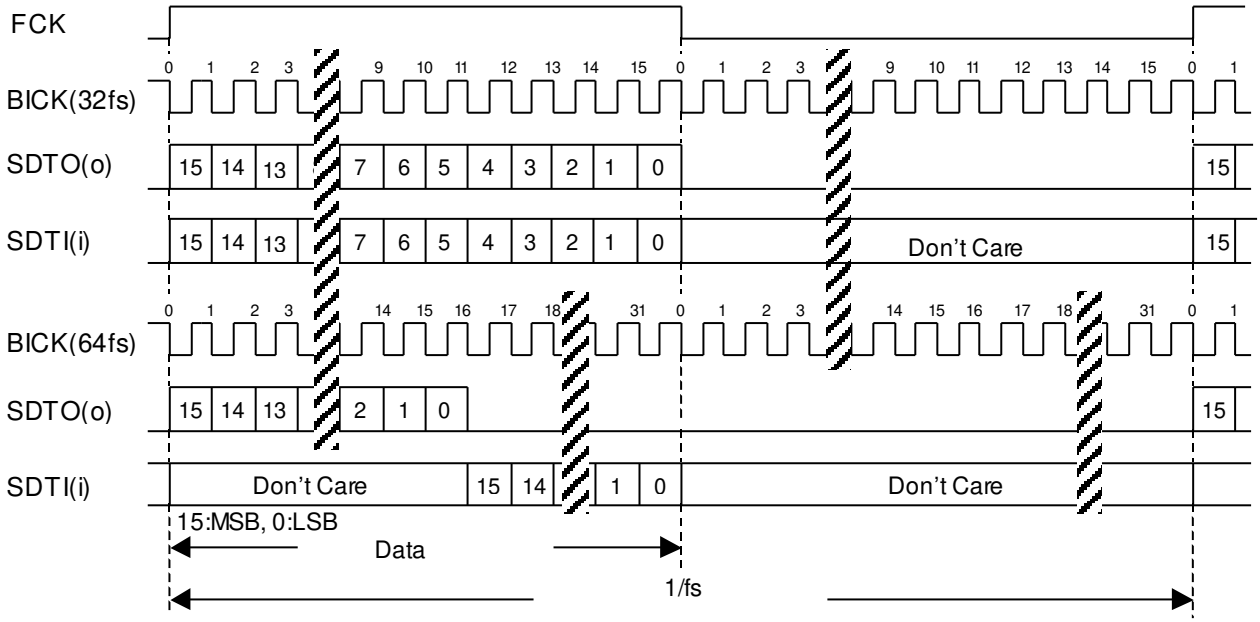



Figure 23. Mode 1 Timing

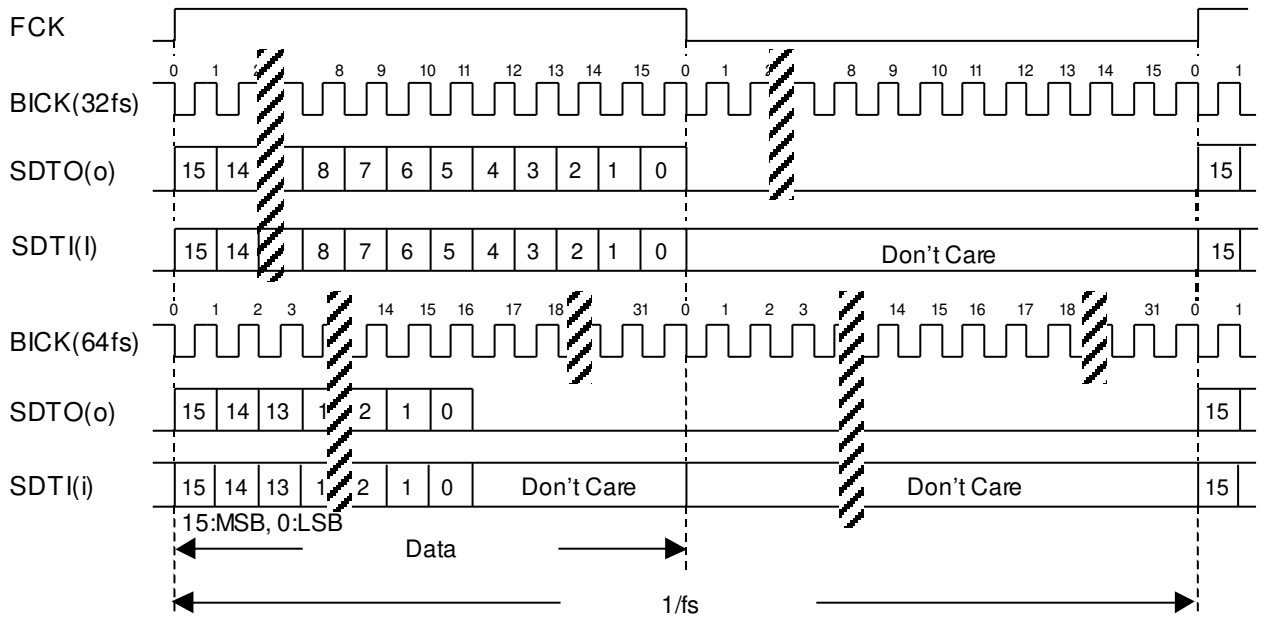



Figure 24. Mode 2 Timing

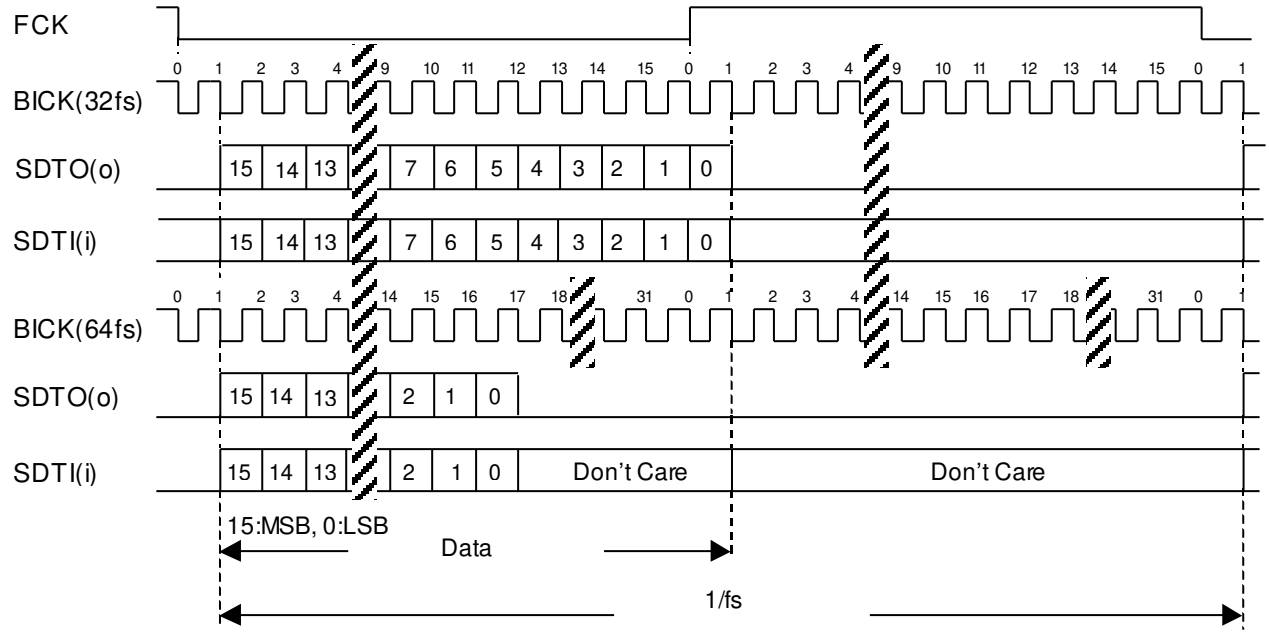



Figure 25. Mode 3 Timing

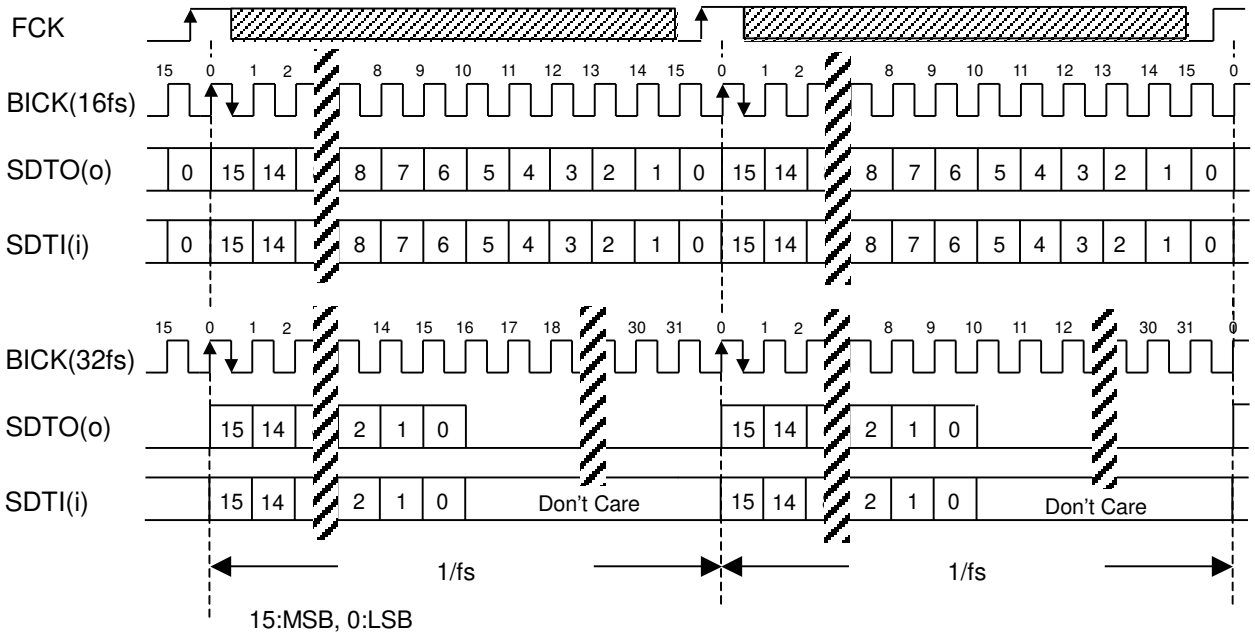



Figure 26. Mode 0 Timing (BCKP bit= "0", MSBS bit= "0")

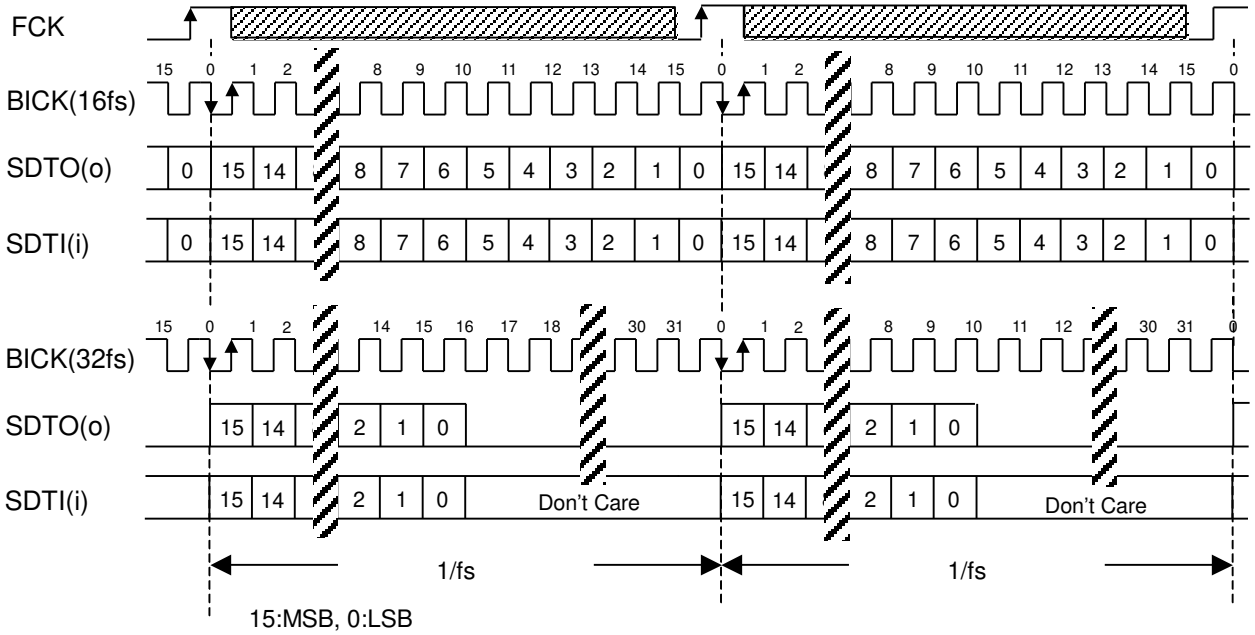



Figure 27. Mode 0 Timing (BCKP bit= "1", MSBS bit= "0")

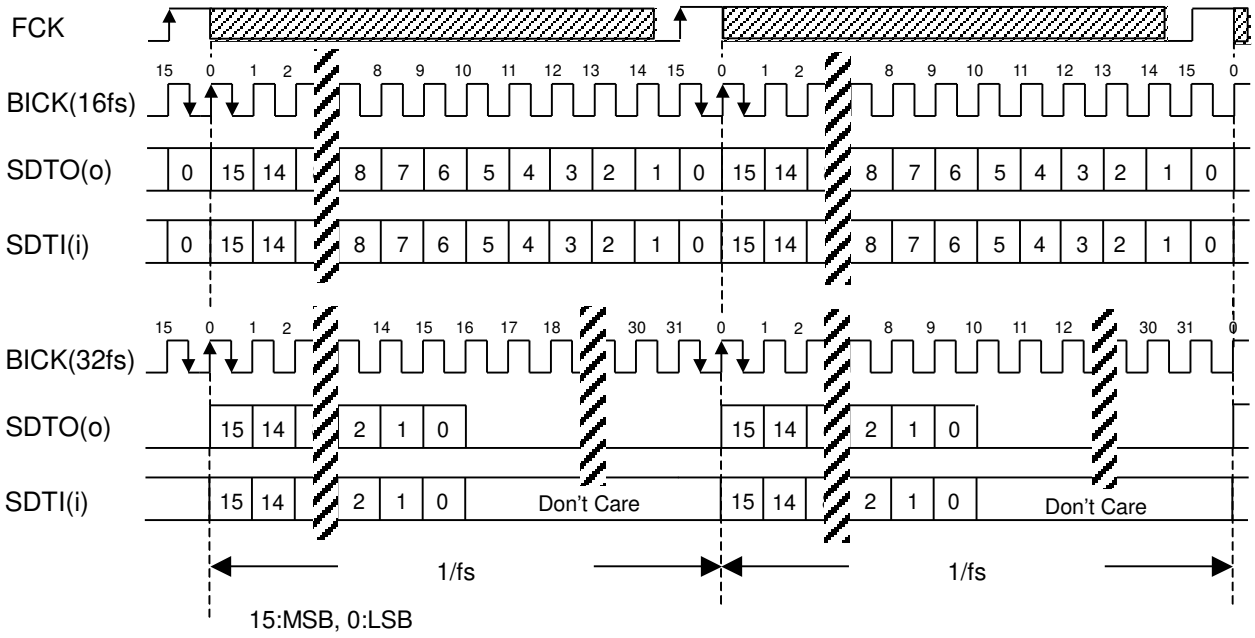



Figure 28. Mode 0 Timing (BCKP bit= "0", MSBS bit= "1")

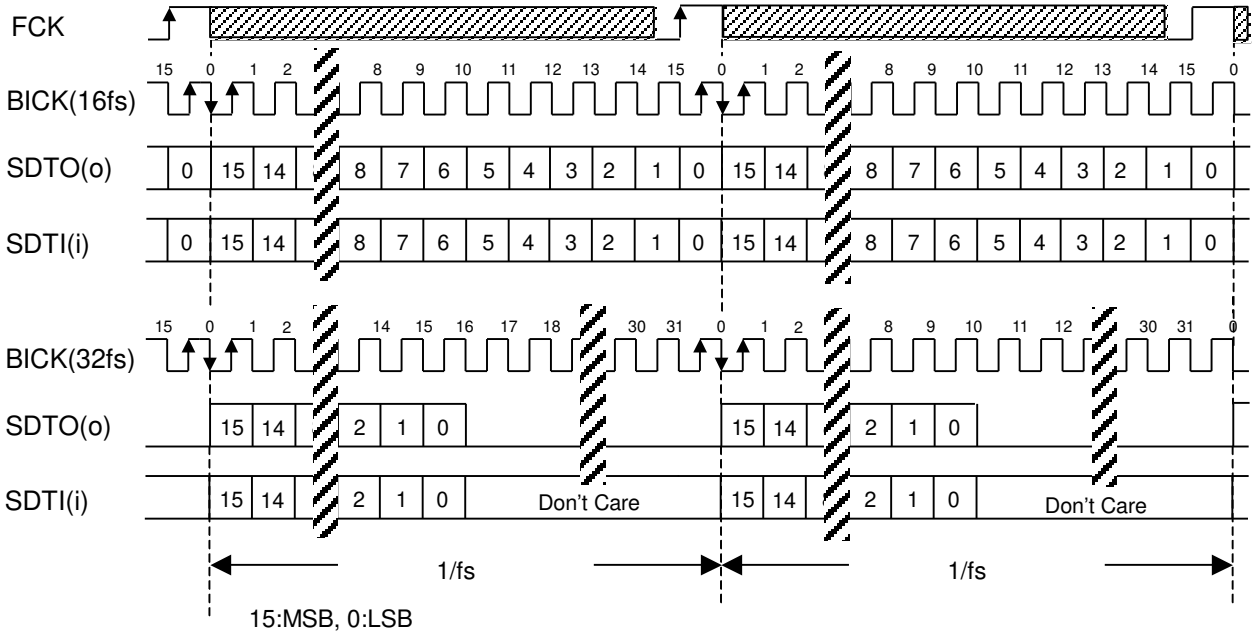



Figure 29. Mode 0 Timing (BCKP bit= "1", MSBS bit= "1")

## ■ System Reset

Upon power-up, reset the AK4633 by bringing the PDN pin = "L". This ensures that all internal registers reset to their initial values.

The ADC enters an initialization cycle when the PMADC bit is changed from "0" to "1". The initialization cycle time is selected by ADRST bit (Table 17). During the initialization cycle, the ADC digital data outputs of both channels are forced to a 2's complement, "0". The ADC output reflects the analog input signal after the initialization cycle is completed. The DAC does not require an initialization cycle.

(Note) The initial data of ADC has the offset data that depends on the condition of the microphone and the cut-off frequency of HPF. When Off-set becomes a problem, lengthen initialization time of ADC by ADRST bit = "0" or do not use initial output data of ADC.

| ADRST bit | Init Cycle | | | |
|---|---|---|---|---|
| | Cycle | fs = 8kHz | fs = 16kHz | fs = 48kHz |
| 0 | 1059/fs | 132.4ms | 66.2ms | 22.1ms |
| 1 | 291/fs | 36.4ms | 18.2ms | 6.1ms |

Table 17. Initialization cycle of ADC

## ■ MIC Gain Amplifier

The AK4633 has a Gain Amplifier for Microphone input. This gain is selected by MGAIN2-0 bits. The typical input impedance is 30kΩ.

| MGAIN2 bit | MGAIN1 bit | MGAIN0 bit | Input Gain | |
|---|---|---|---|---|
| 0 | 0 | 0 | 0dB | |
| 0 | 0 | 1 | +20dB | (default) |
| 0 | 1 | 0 | +26dB | |
| 0 | 1 | 1 | +32dB | |
| 1 | 0 | 0 | +6dB | |
| 1 | 0 | 1 | +10dB | |
| 1 | 1 | 0 | +14dB | |
| 1 | 1 | 1 | +17dB | |

Table 18. Input Gain

## ■ MIC Power

The MPI pin supplies power for the Microphone. This output voltage scales with 0.8 x AVDD (typ) and the load resistance is minimum 2kΩ. Do not connect any capacitor directly to the MPI pin

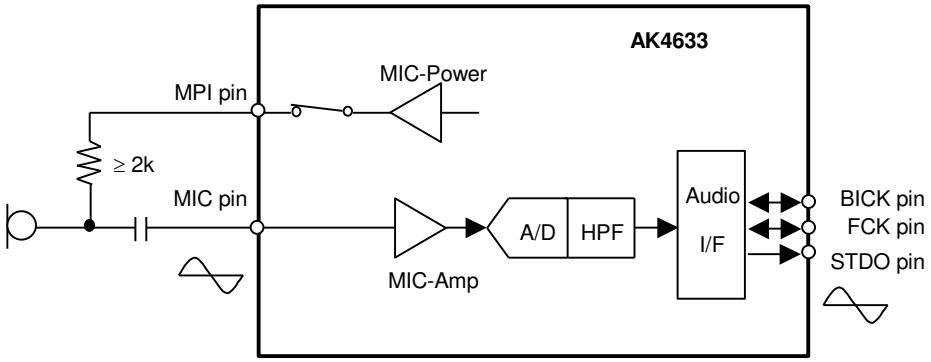



Figure 30. MIC Block Circuit

## ■ MIC Differential Input

The MIC input becomes an differential input when MDIF bit is "1". The input pins are MICN and MICP pins. At this time, the MICP pin can not be used for an BEEP input. When MDIF bit is "1", the PMBP, BEEPA and BEEPS bits should be set to "0".

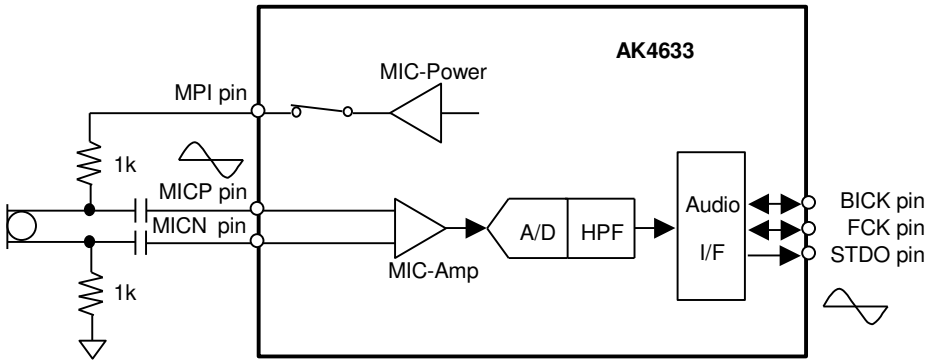
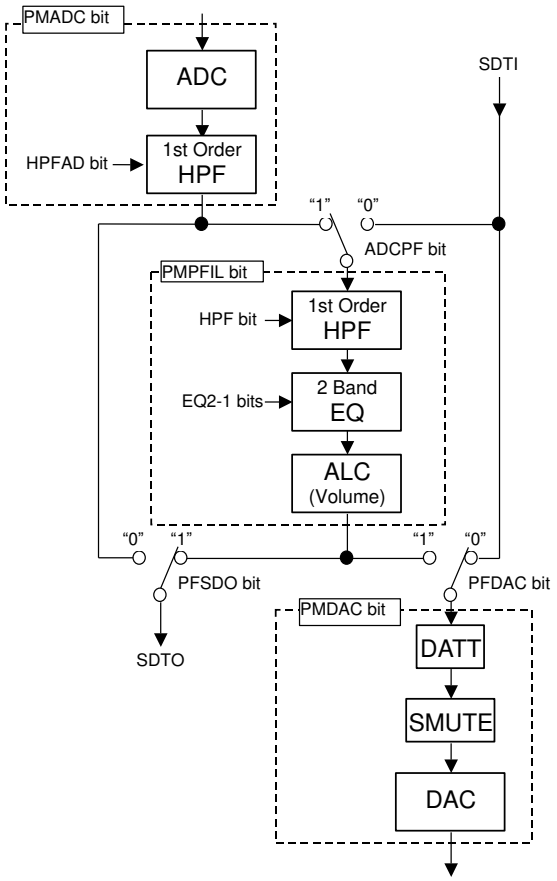



Figure 31. MIC Differential Input Circuit

## ■ Digital Block

Digital Block is composed as shown in Figure 32. The recording and playback signal paths are selected by ADCPF bit, PFDAC bit and PFSDO bit (Figure 32~ Figure 35, Table 19)




(1) ADC: Include the Digital Filter(LPF) for ADC as shown in "FILTER CHRACTERISTICS".
(2) DAC: Include the Digital Filter(LPF) for DAC as shown in "FILTER CHRACTERISTICS".
(3) HPF: High Pass Filter. Enable to use for a Wind-Noise Reduction Filter. (See "Programmable Filter")
(4) EQ: using for an Equalizer or Notch Filter. (See "Programmable Filter")
(5) Volume: Digital Volume with ALC function. (See "Digital Volume" or "ALC")
(6) DATT: 4 steps Digital Volume for playback path.( See "Output Digital Volume2")
(7) SMUTE: Soft mute.

Figure 32. Digital block path

| Mode | ADCPF bit | PFDAC bit | PFSDO bit | Figure |
|---|---|---|---|---|
| Recoding Main Mode | 1 | 0 | 1 | Figure 33 |
| Playback Main Mode | 0 | 1 | 0 | Figure 34 |
| Loop Back Mode | 1 | 1 | 1 | Figure 35 |

Table 19. Recode/Playback Mode

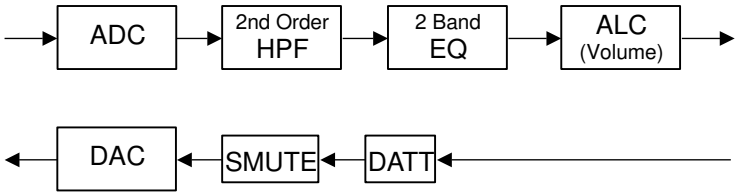



Figure 33. The path at ADCPF bit = "1", PFDAC bit = "0" and PFSDO bit = "1" (default)

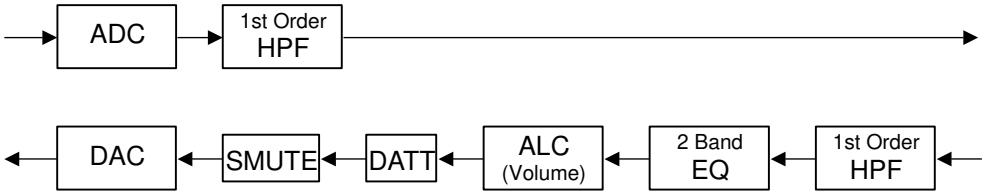



Figure 34. The path at ADCPF bit = "0", PFDAC bit = "1" and PFSDO bit = "0"

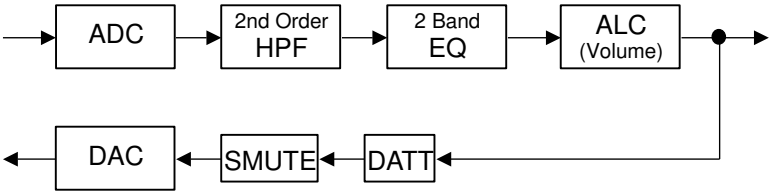



Figure 35. The path at ADCPF bit = "1", PFDAC bit = "1" and PFSDO bit = "1"

## ■ Digital Programmable Filter

The AK4633 have 2steps of 1st order HPF and 2 band Equalizer for recording and playback path (Figure 32).

(1) High Pass Filter (HPF)

Normally, this HPF is used for a Wind-Noise Reduction Filter. This is composed with 2 steps of 1st order HPF. The coefficient of both HPF is same and should be set by F1A13-0 bits and F1B13-0 bits. The HPF of ADC could be ON/OFF by HPFAD bit, and the HPF before 2 band EQ could be ON/Off by setting HPF bit. When the HPF is OFF, the audio data passes this block by 0dB . The coefficient should be set when HPFAD bit = HPF bit = "0" or PMADC bit = PMPFIL bit = "0". After changing the coefficient, the HPF starts with 3/fs (max) delay time after (HPFAD bit and PMADC bit) or (HPF bit and PMPFIL bit) are set to "1". The waiting time is not necessity for setting HPFAD bit, HPF bit, PMADC bit and PMPFIL bit to "1" after setting the coefficient.

fs: Sampling frequency
fc: Cut-off frequency

Register setting (Note 29)
HPF: F1A[13:0] bits =A, F1B[13:0] bits =B
(MSB=F1A13, F1B13; LSB=F1A0, F1B0)

$$A = \frac{1}{1 + \tan(\pi fc/fs)}, \quad B = \frac{1 - \tan(\pi fc/fs)}{1 + \tan(\pi fc/fs)}$$

The cut-off frequency should be set as below.
fc/fs ≥ 0.0001 (fc min = 1.6Hz at 16kHz)

(2) 2 band Equalizer

This could be used as Equalizer or notch filter. 2 band Equalizer (EQ1 and EQ2) are ON/OFF independently by EQ1 bit and EQ2 bit. When Equalizer is OFF, the audio data passes this block by 0dB. The coefficient of EQ1 should be set by E1A15-0 bits, E1B15-0 bits and E1C15-0 bits, the coefficient of EQ2 should be set by E2A15-0 bits, E2B15-0 bits and E2C15-0 bits. The EQ1 coefficient should be set when EQ1 bit = "0" or PMPFIL bit = "0", the EQ2 coefficient should be set when EQ2 bit = "0" or PMPFIL bit = "0". After changing the coefficient, the Equalizer starts with 3/fs (max) delay time after (EQ1 bit and PMPFIL bit) or (EQ2 bit and PMPFIL bit) are set to "1". The waiting time is not necessity for setting EQ1 bit, EQ2 bit and PMPFIL bit to "1" after setting the coefficient.

fs: Sampling frequency
fo: Center frequency
fb: Band width of 3dB gain difference from center frequency
K : Gain ( -1 ≤ K <∟ 3 )

Register setting(Note 29)
EQ1: E1A[15:0] bits =A, E1B[15:0] bits =B, E1C[15:0] bits =C
EQ2: E2A[15:0] bits =A, E2B[15:0] bits =B, E2C[15:0] bits =C
(MSB=E1A15, E1B15, E1C15, E2A15, E2B15, E2C15 ; LSB= E1A0, E1B0, E1C0, E2A0, E2B0, E2C0)

$$A = K \times \frac{\tan(\pi fb/fs)}{1 + \tan(\pi fb/fs)}, \quad B = \cos(2\pi\, fo/fs) \times \frac{2}{1 + \tan(\pi fb/fs)}, \quad C = -\frac{1 - \tan(\pi fb/fs)}{1 + \tan(\pi fb/fs)}$$

The center frequency should be set as below.
fo/fs <∟ 0.497

When the gain of K is set to "-1", these Equalizers work as a notch filter. If the difference between two center frequencies of these notch filters is small, the center frequency will differ from the frequency that is calculated by the above equation. The difference between the actual two center frequencies is smaller that the difference between the two calculated center frequencies. It is required to adjust the center frequencies when these are calculated. The frequency response can be confirmed by the control soft that is attached in an evaluation board kit. If the two center frequencies are near, the actual center frequencies should be confirmed by this software.

e.g.) Sampling frequency = 44.1kHz, the center frequencies of 2 band notch fitters are 6000Hz and 6500Hz, and the band width is 200Hz.

When the coefficients that are calculated by fo = 6000Hz and 6500Hz is used, the actual center frequencies are 6017Hz and 6476Hz. When the coefficients that are calculated by fo = 5984Hz and 6522Hz is used, the actual center frequencies are 6000Hz and 6500Hz.

Note 29. [changing real number to binary number for the filter coefficient setting upon is as below]

X=( the real filter coefficient setting upon) x $2^{13}$

Round off the X value to the decimal point and change it to binary number.
The MSB bit of each filter coefficient setting register is a sign bit.

## ■ Input Digital volume (Manual mode)

When ADCPF bit = "1" and ALC1 bit = "0", ALC block becomes an input digital volume (manual mode). The digital volume's gain is set by IVOL7-0 bits as shown in Table 20. The IVOL7-0 bits value are reflected to this input volume at zero cross or zero cross time out. The zero crossing timeout period is set by ZTM1-0 bits.

| IVOL7-0bits | GAIN(0dB) | Step | |
|---|---|---|---|
| F1H | +36.0 | 0.375dB | |
| F0H | +35.625 | | |
| EFH | +35.25 | | |
| : | : | | |
| 92H | +0.375 | | |
| 91H | 0.0 | | (default) |
| 90H | -0.375 | | |
| : | : | | |
| 2H | -53.625 | | |
| 1H | -54.0 | | |
| 0H | MUTE | | |

Table 20. Input Digital Volume Setting

When writing to the IVOL7-0 bits continually, the control register should be written in an interval more than zero crossing timeout. If not, a zero crossing counter is reset each time and the volume will not be changed. However, it could be ignored when writing a same register value as the last time. At this time, a zero crossing counter is not reset, so can be written in an interval less than zero crossing timeout.

## ■ Output Digital volume (Manual mode)

When ADCPF bit = "0" and ALC2 bit = "0", ALC block become an output digital volume (manual mode). The digital volume's gain is set by OVOL7-0 bits as shown in Table 21. The OVOL7-0 bits value are reflected to this output volume at zero cross or zero cross time out. The zero crossing timeout period is set by ZTM1-0 bits.

| OVOL7-0bits | GAIN(0dB) | Step | |
|---|---|---|---|
| F1H | +36.0 | 0.375dB | |
| F0H | +35.625 | | |
| EFH | +35.25 | | |
| : | : | | |
| 92H | +0.375 | | |
| 91H | 0.0 | | (default) |
| 90H | -0.375 | | |
| : | : | | |
| 2H | -53.625 | | |
| 1H | -54.0 | | |
| 0H | MUTE | | |

Table 21. Output Digital Volume Setting

When writing to the OVOL7-0 bits continually, the control register should be written by an interval more than zero crossing timeout. If not, a zero crossing counter is reset each time and the volume will not be changed. However, it could be ignored when writing a same register value as the last time. At this time, a zero crossing counter is not reset, so it can be written by an interval less than zero crossing timeout.

## ■ Output Digital Volume2

AK4633 has 4 steps output volume in addition to the volume setting by OVOL7-0 bits. This volume is set by DATT1-0 bits as shown in Table 22.

| DATT1-0bits | GAIN(0dB) | Step | |
|---|---|---|---|
| 0H | 0.0 | 6.0dB | (default) |
| 1H | -6.0 | | |
| 2H | -12.0 | | |
| 3H | -18.1 | | |

Table 22. Output Digital Volume2 Setting

## ■ ALC Operation

The ALC (Automatic Level Control) is operated by ALC block. When ADCPF bit = "1", ALC operation is enable for recording path. When ADCPF bit = "0", ALC operation is enable for playback path. ON/OFF of the ALC operation for recording is controlled by ALC1 bit and the ON/OFF of ALC operation for playback is controlled by ALC2 bit.

1. ALC Limiter Operation

When the ALC limiter is enabled, and output exceeds the ALC limiter detection level (Table 23), the volume value is attenuated by the amount defined by LMAT1-0 bits (Table 24) automatically.

When the ZELMN bit = "0"(zero crossing detection valid), the VOL value is changed by ALC limiter operation at the zero crossing point or zero crossing timeout. Zero crossing timeout period is set by ZTM1-0 bit that is in common with ALC recovery zero crossing timeout period's setting (Table 25).

When the ZELMN bit = "1" (zero crossing detection invalid), VOL value has been changed immediately (period: 1/fs) by ALC limiter operation. The attenuation for limiter operation is fixed to 1 step and not controlled by setting LMAT1-0 bits.

After finishing the attenuation operation, if ALC bit does not change to "0", the operation repeats when the output signal level exceeds the ALC limiter detection level.

| LMTH1 | LMTH0 | ALC Limiter Detection Level | ALC Recovery Waiting Counter Reset Level | |
|---|---|---|---|---|
| 0 | 0 | ALC Output ≥ –2.5dBFS | –2.5dBFS > ALC Output ≥ –4.1dBFS | |
| 0 | 1 | ALC Output ≥ –4.1dBFS | –4.1dBFS > ALC Output ≥ –6.0dBFS | (default) |
| 1 | 0 | ALC Output ≥ –6.0dBFS | –6.0dBFS > ALC Output ≥ –8.5dBFS | |
| 1 | 1 | ALC Output ≥ –8.5dBFS | –8.5dBFS > ALC Output ≥ –12dBFS | |

Table 23. ALC Limiter Detection Level / Recovery Waiting Counter Reset Level

| LMAT1 | LMAT0 | ALC1 Limiter ATT Step | | | | |
|---|---|---|---|---|---|---|
| | | ALC1 Output ≥ LMTH | ALC1 Output ≥ FS | ALC1 Output ≥ FS + 6dB | ALC1 Output ≥ FS + 12dB | |
| 0 | 0 | 1 | 1 | 1 | 1 | (default) |
| 0 | 1 | 2 | 2 | 2 | 2 | |
| 1 | 0 | 2 | 4 | 4 | 8 | |
| 1 | 1 | 1 | 2 | 4 | 8 | |

Table 24. ALC Limiter ATT Step Setting

| ZTM1 | ZTM0 | | Zero Crossing Timeout Period | | | |
|---|---|---|---|---|---|---|
| | | | 8kHz | 16kHz | 44.1kHz | |
| 0 | 0 | 128/fs | 16ms | 8ms | 2.9ms | (default) |
| 0 | 1 | 256/fs | 32ms | 16ms | 5.8ms | |
| 1 | 0 | 512/fs | 64ms | 32ms | 11.6ms | |
| 1 | 1 | 1024/fs | 128ms | 64ms | 23.2ms | |

Table 25. ALC Zero Crossing Timeout Period Setting

2. ALC Recovery Operation

The ALC recovery operation waits for the WTM1-0 bits (Table 26) to be set after completing the ALC limiter operation. If the input signal does not exceed "ALC recovery waiting counter reset level" (Table 23) during the wait time, the ALC recovery operation is executed. The VOL value is automatically incremented by RGAIN1-0 bits (Table 27) up to the set reference level (Table 28, Table 29) with zero crossing detection which timeout period is set by ZTM1-0 bits (Table 25). The ALC recovery operation is executed in a period set by WTM1-0 bits.

For example, when the current VOL value is 30H and RGAIN1-0 bits are set to "01"(2 steps), VOL is changed to 32H by the auto limiter operation and then the input signal level is gained by 0.75dB (=0.375dB x 2). When the VOL value exceeds the reference level (IREF7-0 or OREF5-0), the VOL values are not increased.

When
"ALC recovery waiting counter reset level (LMTH1-0) ≤ Output Signal < ALC limiter detection level (LMTH1-0)" during the ALC recovery operation, the waiting timer of ALC recovery operation is reset. When
"ALC recovery waiting counter reset level (LMTH1-0) > Output Signal",
the waiting timer of ALC recovery operation starts.

The ALC operation corresponds to the impulse noise. When the impulse noise is input, the ALC recovery operation becomes faster than a normal recovery operation. When large noise is input to microphone instantaneously, the quality of small level in the large noise can be improved by this fast recovery operation. The speed of first recovery operation is set by RFST1-0 bits (Table 30).

| WTM1 | WTM0 | | ALC Recovery Operation Waiting Period | | | |
|---|---|---|---|---|---|---|
| | | | 8kHz | 16kHz | 44.1kHz | |
| 0 | 0 | 128/fs | 16ms | 8ms | 2.9ms | (default) |
| 0 | 1 | 256/fs | 32ms | 16ms | 5.8ms | |
| 1 | 0 | 512/fs | 64ms | 32ms | 11.6ms | |
| 1 | 1 | 1024/fs | 128ms | 64ms | 23.2ms | |

Table 26. ALC Recovery Operation Waiting Period

| RGAIN1 | RGAIN0 | GAIN STEP | | |
|---|---|---|---|---|
| 0 | 0 | 1 | 0.375dB | (default) |
| 0 | 1 | 2 | 0.750dB | |
| 1 | 0 | 3 | 1.125dB | |
| 1 | 1 | 4 | 1.500dB | |

Table 27. ALC Recovery GAIN Step

| IREF7-0bits | GAIN(0dB) | Step | |
|---|---|---|---|
| F1H | +36.0 | 0.375dB | (default) |
| F0H | +35.625 | | |
| EFH | +35.25 | | |
| : | : | | |
| C5H | +19.5 | | |
| : | : | | |
| 92H | +0.375 | | |
| 91H | 0.0 | | |
| 90H | -0.375 | | |
| : | : | | |
| 2H | -53.625 | | |
| 1H | -54.0 | | |
| 0H | MUTE | | |

Table 28. Reference Level at ALC Recovery operation for recoding

| OREF5-0bits | GAIN(0dB) | Step | |
|---|---|---|---|
| 3CH | +36.0 | 1.5dB | (default) |
| 3BH | +34.5 | | |
| 3AH | +33.0 | | |
| : | : | | |
| 28H | +6.0 | | |
| : | : | | |
| 25H | +1.5 | | |
| 24H | 0.0 | | |
| 23H | -1.5 | | |
| : | : | | |
| 2H | -51.0 | | |
| 1H | -52.5 | | |
| 0H | -54.0 | | |

Table 29. Reference Level at ALC Recovery operation for playback

| RFST1 bit | RFST0 bit | Recovery Speed | |
|---|---|---|---|
| 0 | 0 | 4 times | (default) |
| 0 | 1 | 8 times | |
| 1 | 0 | 16times | |
| 1 | 1 | N/A | |

Table 30. First Recovery Speed Setting

3. The Volume at the ALC Operation

The current volume value at the ALC operation is reflected by VOL7-0 bits. It is enable to check the current volume value with reading the register value of VOL7-0 bits.

| VOL7-0bits | GAIN(0dB) |
|---|---|
| 0EH | +36.0 |
| 0FH | +35.625 |
| 10H | +35.25 |
| : | : |
| 3AH | +19.5 |
| : | : |
| 6DH | +0.375 |
| 6EH | 0.0 |
| 6FH | -0.375 |
| : | : |
| FDH | -53.625 |
| FEH | -54.0 |
| FFH | MUTE |

Table 31. Value of VOL7-0 bits

4. Example of the ALC Operation for Recording Operation

Table 32 shows the examples of the ALC setting for a microphone recording.

| Register Name | Comment | fs=8kHz | | fs=16kHz | |
|---|---|---|---|---|---|
| | | Data | Operation | Data | Operation |
| LMTH | Limiter detection Level | 01 | –4.1dBFS | 01 | –4.1dBFS |
| ZELM | Limiter zero crossing detection | 0 | Enable | 0 | Enable |
| ZTM1-0 | Zero crossing timeout period | 00 | 16ms | 01 | 16ms |
| WTM1-0 | Recovery waiting period<br>*WTM1-0 bits should be the same data as ZTM1-0 bits | 00 | 16ms | 01 | 16ms |
| IREF7-0 | Maximum gain at recovery operation | C5H | 19.5dB | C5H | 19.5dB |
| IVOL7-0 | Gain of IVOL | C5H | 19.5dB | C5H | 19.5dB |
| LMAT1-0 | Limiter ATT step | 11 | 1/2/4/8 step | 11 | 1/2/4/8 step |
| RGAIN1-0 | Recovery GAIN step | 00 | 1 step | 00 | 1 step |
| ALC | ALC enable | 1 | Enable | 1 | Enable |
| FRSL1-0 | Speed of Fast Recovery | 00 | 4 times | 10 | 4times |

Table 32. Example of the ALC Setting (Recording)

5. Example of the ALC Operation for Playback Operation

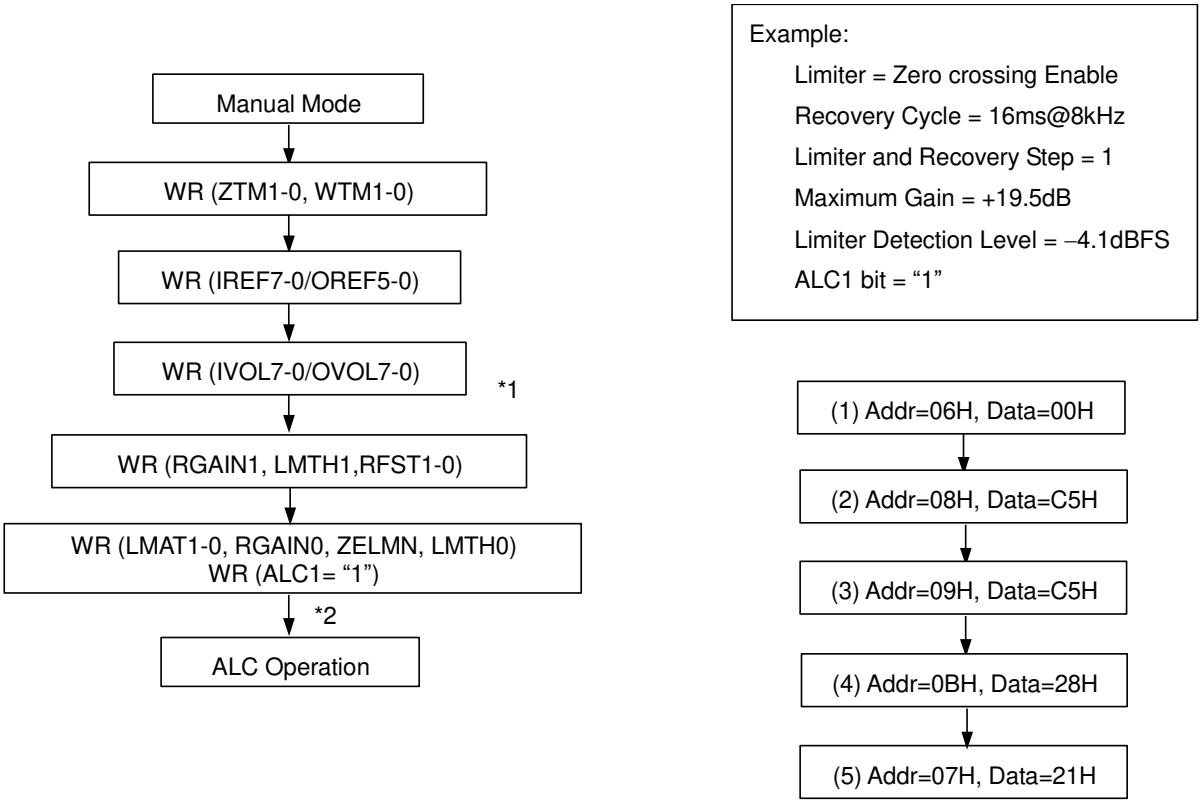
Table 33 shows the examples of the ALC setting for playback operation.

| Register Name | Comment | fs=8kHz | | fs=16kHz | |
|---|---|---|---|---|---|
| | | Data | Operation | Data | Operation |
| LMTH | Limiter detection Level | 01 | –4.1dBFS | 01 | –4.1dBFS |
| ZELM | Limiter zero crossing detection | 0 | Enable | 0 | Enable |
| ZTM1-0 | Zero crossing timeout period | 00 | 16ms | 01 | 16ms |
| WTM1-0 | Recovery waiting period<br>*WTM1-0 bits should be the same data as ZTM1-0 bits | 00 | 16ms | 01 | 16ms |
| OREF5-0 | Maximum gain at recovery operation | 28 | +6dB | 28 | +6dB |
| OVOL7-0 | Gain of IVOL | 91 | 0dB | 91 | 0dB |
| LMAT1-0 | Limiter ATT step | 11 | 1/2/4/8 step | 11 | 1/2/4/8 step |
| RGAIN1-0 | Recovery GAIN step | 00 | 1 step | 00 | 1 step |
| ALC | ALC enable | 1 | Enable | 1 | Enable |
| FRSL1-0 | Speed of Fast Recovery | 00 | 4 times | 00 | 4 times |

Table 33. Example of the ALC Setting (Playback)

The following registers should not be changed during ALC operation. These bits should be changed after ALC operation is finished by ALC1 = ALC2 bits ="0" or PMPFIL bit = "0".

- **LMTH, LMAT1-0, WTM1-0, ZTM1-0, RGAIN1-0, IREF7-0/OREF7-0, ZELM, RFST1-0**




Note : WR : Write

*1: The value of volume at starting should be the same or smaller than REF's.

*2: When setting ALC1 bit or ALC2 bit to "0", the operation is shifted to manual mode after passing the zero crossing time set by ZTM1-0 bits.

Figure 36. Registers set-up sequence at ALC operation

## ■ SOFTMUTE

Soft mute operation is performed in the digital input domain. When the SMUTE bit goes to "1", the input signal is attenuated by –∞ ("0") during the cycle of 245/fs (31msec@fs=8kHz). When the SMUTE bit is returned to "0", the mute is cancelled and the input attenuation gradually changes to 0dB during the cycle of 245/fs (31msec@fs=8kHz). If the soft mute is cancelled within the cycle of 245/fs (31msec@fs=8kHz), the attenuation is discontinued and it is returned to 0dB. The soft mute for Playback operation is effective for changing the signal source without stopping the signal transmission.

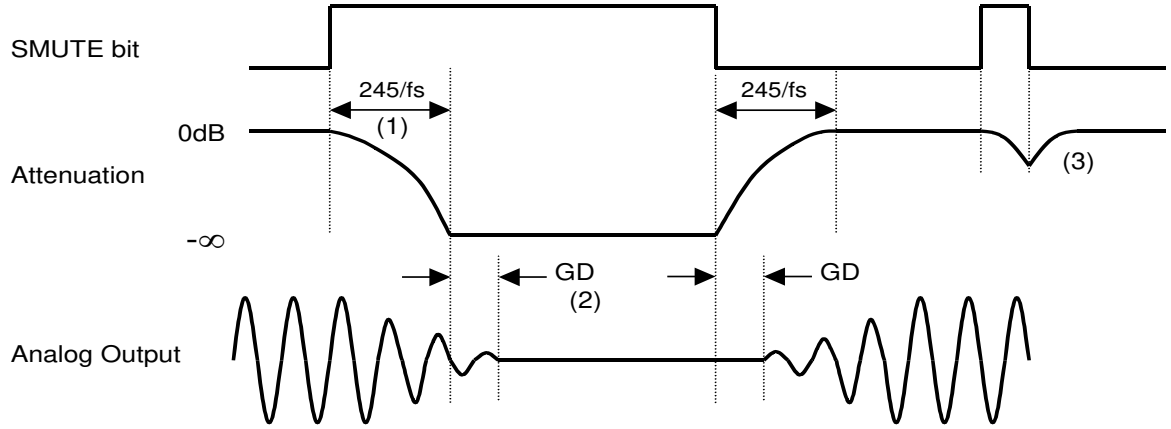



Figure 37. Soft Mute Function

(1) The input signal is attenuated by –∞ ("0") during the cycle of 245/fs (31msec@fs=8kHz).
(2) Analog output corresponding to digital input has group delay (GD).
(3) If the soft mute is cancelled within the cycle of 245/fs (31msec@fs=8kHz), the attenuation is discounted and returned to 0dB within the same cycle.

## ■ BEEP Input

When the PMBP bit is set to "1", the beep input is powered-up. When the BEEPS bit is set to "1", the input signal from the BEEP pin is output to Speaker-Amp. When the BEEPA bit is set to "1", the input signal from the BEEP pin is output to the mono line output amplifier. The external resister Ri adjusts the signal level of BEEP input. Table 34 shows the typical gain example at $R_i$ = 20kΩ. This gain is in inverse proportion to $R_i$. It should be set MDIF bit to "0" expect PMBP bit = BEEPA bit = BEEPS bit = "0".

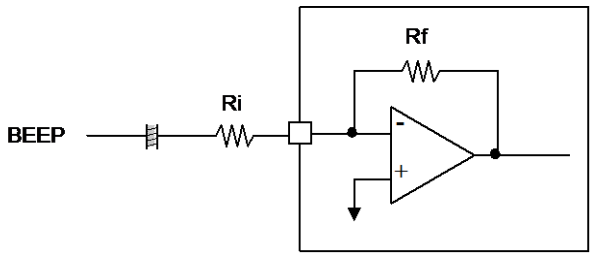



Figure 38. Block Diagram of BEEP pin

| SPKG1-0 bits | BEEP → SPP/SPN Gain | BEEP → AOUT Gain |
|---|---|---|
| 00 | +8dB | 0dB |
| 01 | +10dB | 0dB |
| 10 | +12dB | 0dB |
| 11 | +14dB | 0dB |

Table 34. BEEP Input Gain at $R_i$ = 20kΩ

## ■ Mono Line Output (AOUT pin)

A signal of DAC is output from the AOUT pin. When the DACA bit is "0", this output is OFF. The load resistance is 10kΩ(min). When PMAO bit is "0" and AOPS bit is "0", the mono line output enters power-down and is pulled down by 100Ω(typ). When ADPS bit is "1", the mono line output enters power-save mode. If PMAO bit is controlled at AOPS bit = "1", POP noise will be reduced at power-up and down. Then, this line should be pulled down by 20kΩ of resister after C-coupling shown in Figure 39. This rising and falling time is max 300 ms at C=1.0μF . When PMAO bit is "1" and AOPS bit is "0", the mono line output enters power-up state.

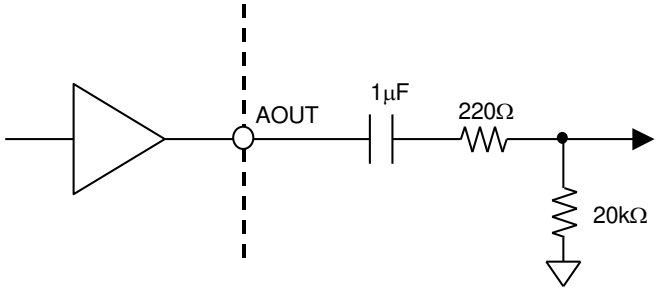
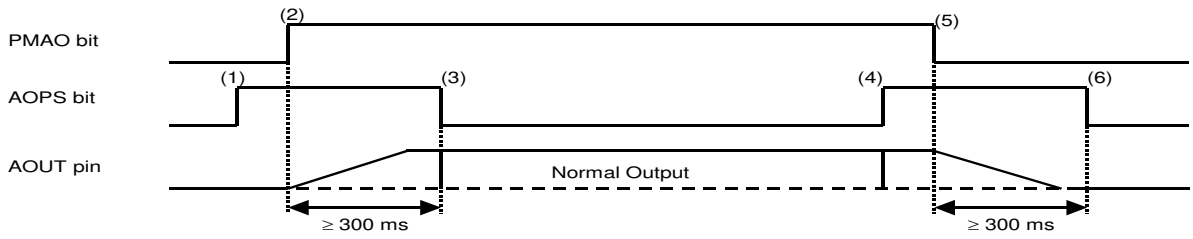



Figure 39. AOUT external circuit in case of using POP Reduction function

### AOUT Control Sequence in case of using POP Reduction Circuit




(1) Set AOPS bit = "1". Mono line output enters the power-save mode.
(2) Set PMAO bit = "1". Mono line output exits the power-down mode.
AOUT pin rises up to VCOM voltage. Rise time is 200ms (max 300ms) at C=1μF.
(3) Set AOPS bit = "0" after AOUT pin rises up. Mono line output exits the power-save mode.
Mono line output is enabled.
(4) Set AOPS bit = "1". Mono line output enters power-save mode.
(5) Set PMAO bit = "1". Mono line output enters power-down mode.
AOUT pin falls down to AVSS. Fall time is 200ms (max 300ms) at C=1μF.
(6) Set AOPS bit = "0" after AOUT pin falls down. Mono line output exits the power-save mode.

Figure 40. Mono Line Output Control Sequence in case of using POP Reduction function

## ■ Speaker Output

The power supply voltage for Speaker-Amp SVDD can be set in the range of 2.2V to 4.0V. However, SVDD should be set in the range of 2.6V to 3.6V, when 8Ω dynamic speaker is connected. If SVDD is more than 3.6V when 8Ω dynamic speaker is connected to the AK4633, the output of Speaker-Amp should be restricted in consideration of maximum power dissipation.

The output signal from DAC is input to the Speaker-amp. This Speaker-amp is a mono output controlled by BTL and the gain of Speaker-Amp is set by SPKG1-0 bits. The output voltage depends on AVDD and SPKG1-0 bits.

| SPKG1-0 bits | SPK-AMP Output Level[Vpp]<br>DAC =-4.1dBFS (Note 30) | Gain<br>(Note 31) |
|---|---|---|
| 00 | 3.17 | 0dB |
| 01 | 4.00 | +2dB |
| 10 | 5.03 | +4dB |
| 11 | 6.33 | +6dB |

Note 30. AVDD=3.3V. The output level is proportional to AVDD.
Note 31. The Gain with a reference of SPKG1-0 bits = "00".
Note 32. The setting of SPKG1-0 bits = "01" is recommend when 8Ω dynamic speaker is connected.
The SPK-Amp Power is 250mW at 8Ω Load Resistance and 4.0Vpp output level.

Table 35. SPK-Amp Output Voltage and Gain

<Caution for using Piezo Speaker>

When a piezo speaker is used, resistances more than 10Ω should be connected between SPP/SPN pins and speaker in series respectively as shown in Figure 41. Zener diodes should be connected between speaker and GND as shown in Figure 41, in order to protect SPK-Amp of the AK4633 from the power that the piezo speaker outputs when the speaker is pressured. Zener diodes of the following Zener voltage should be used.

92% of SVDD ≤ Zener voltage of Zener diodo(ZD of Figure 41) ≤ SVDD+0.3V
Ex) In case of SVDD = 3.8V: 3.5V ≤ ZD ≤ 4.1V

For example, Zener diode which Zener voltage is 3.9V(Min 3.7V, Max 4.1V) can be used.

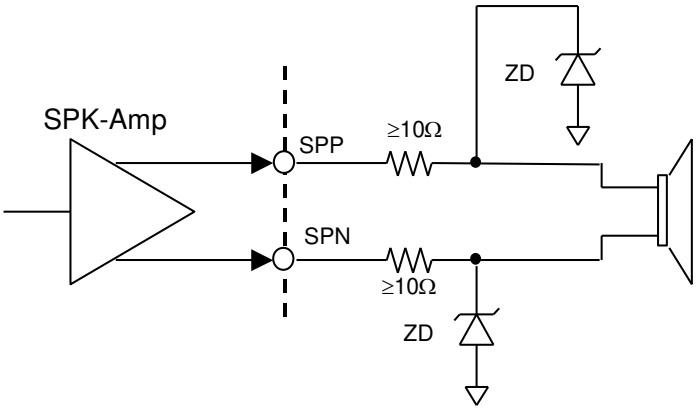


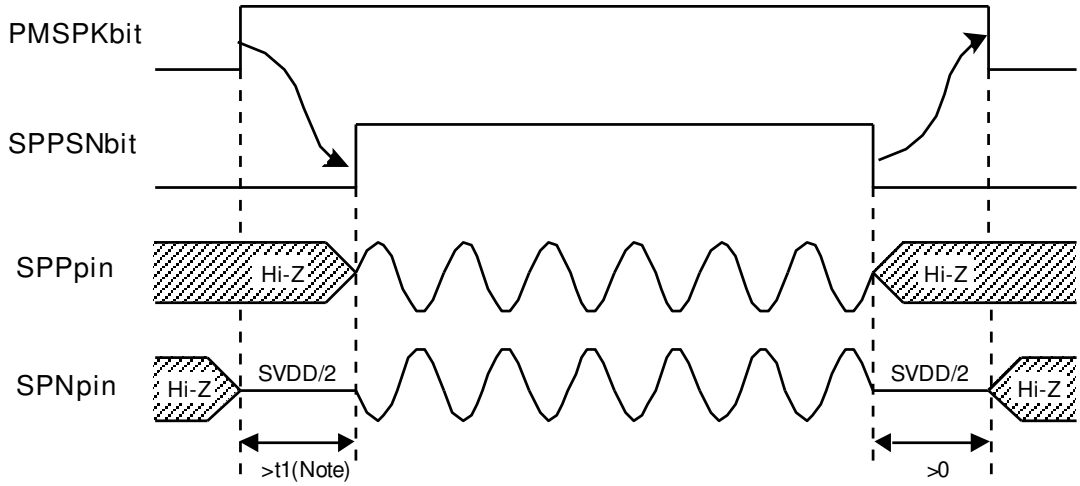

Figure 41. Circuit of Speaker Output (using a piezo speaker)

<Control Sequence of Speaker Amp>

Speaker-Amp can be powered-up/down by controlling the PMSPK bit. When the PMSPK bit is "0", the SPP and SPN pins are placed in a Hi-Z state.

When the PMSPK bit is "1" and SPPSN bit is "0", the Speaker-amp enters power-save-mode. In this mode, the SPP pin is placed in a Hi-Z state and the SPN pin goes to SVDD/2 voltage.

When the PMSPK bit is "1" and the PDN pin is controlled from "L" to "H", the SPP and SPN pins rise up from power-save-mode. In this mode, the SPP pin is placed in a Hi-Z state and the SPN pin goes to SVDD/2 voltage. Because the SPP and SPN pins rise up at power-save-mode, this mode can reduce pop noise. When the AK4633 is powered-down, pop noise can be also reduced by first entering power-save-mode.



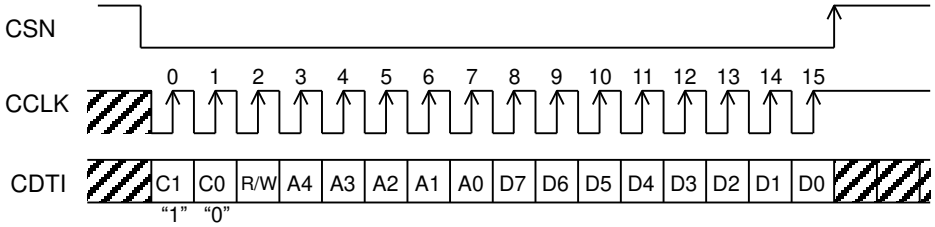

(Note)
SPPSN bit should be set to "1" at more than 1ms after PMSPK bit is set to "1". When BEEP Input Amp and Speaker Amp are powered-up at the same time, SPPSN bit should be set to "1" after BEEP Input become stable. When the resistance and capacitance of BEEP pin are R=20kΩ and C=0.1μF, 10ms(=5τ) is required for BEEP Input to become stable.

Figure 42. Power-up/Power-down Timing for Speaker-Amp

## ■ Serial Control Interface

Internal registers may be written and read by 3-wire µP interface pins (CSN, CCLK and CDTI). The data on this interface consists of a 2-bit Chip address (2bits, fixed to "10"), Read/Write, Register address (MSB first, 5bits) and Control data (MSB first, 8bits). Address and data is clocked in on the rising edge of CCLK and data is clocked out on the falling edge. Data writing is available on the rising edge of CSN. When reading the data, the CDTI pin becomes output mode on the falling edge of 8th CCLK and outputs D7-D0. The output finishes on the rising edge of CSN. The CDTI pin is placed in a Hi-Z state except outputting data at read operation mode. The clock speed of CCLK is 5MHz (max). The value of internal registers is initialized at the PDN pin = "L".

Note 33. Data reading is available for the address 00H~0BH and 0DH~0FH. When reading the address 0CH and 10H ~ 1FH, the register values are invalid.




C1-C0: Chip Address (C1 = "1", C0 = "0"); Fixed to "10"
R/W: READ/WRITE ("1": WRITE, "0": READ)
A4-A0: Register Address
D7-D0: Control data

Figure 43. Serial Control I/F Timing

## ■ Register Map

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 00H | Power Management 1 | PMPFIL | PMVCM | PMBP | PMSPK | PMAO | PMDAC | 0 | PMADC |
| 01H | Power Management 2 | 0 | 0 | 0 | 0 | M/S | 0 | MCKO | PMPLL |
| 02H | Signal Select 1 | SPPSN | BEEPS | DACS | DACA | 0 | PMMP | MGAIN2 | MGAIN0 |
| 03H | Signal Select 2 | PFSDO | AOPS | MGAIN1 | SPKG1 | SPKG0 | BEEPA | PFDAC | ADCPF |
| 04H | Mode Control 1 | PLL3 | PLL2 | PLL1 | PLL0 | BCKO1 | BCKO0 | DIF1 | DIF0 |
| 05H | Mode Control 2 | ADRST | FCKO | FS3 | MSBS | BCKP | FS2 | FS1 | FS0 |
| 06H | Timer Select | 0 | 0 | ZTM1 | ZTM0 | WTM1 | WTM0 | RFST1 | RFST0 |
| 07H | ALC Mode Control 1 | 0 | ALC2 | ALC1 | ZELMN | LMAT1 | LMAT0 | RGAIN0 | LMTH0 |
| 08H | ALC Mode Control 2 | IREF7 | IREF6 | IREF5 | IREF4 | IREF3 | IREF2 | IREF1 | IREF0 |
| 09H | Digital Volume Control | IVOL7 | IVOL6 | IVOL5 | IVOL4 | IVOL3 | IVOL2 | IVOL1 | IVOL0 |
| 0AH | Digital Volume Control | OVOL7 | OVOL6 | OVOL5 | OVOL4 | OVOL3 | OVOL2 | OVOL1 | OVOL0 |
| 0BH | ALC Mode Control 3 | RGAIN1 | LMTH1 | OREF5 | OREF4 | OREF3 | OREF2 | OREF1 | OREF0 |
| 0CH | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0DH | ALC LEVEL | VOL7 | VOL6 | VOL5 | VOL4 | VOL3 | VOL2 | VOL1 | VOL0 |
| 0EH | Signal Select 3 | DATT1 | DATT0 | SMUTE | MDIF | EQ2 | EQ1 | HPF | HPFAD |
| 0FH | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 10H | E1 Co-efficient 0 | E1A7 | E1A6 | E1A5 | E1A4 | E1A3 | E1A2 | E1A1 | E1A0 |
| 11H | E1 Co-efficient 1 | E1A15 | E1A14 | E1A13 | E1A12 | E1A11 | E1A10 | E1A9 | E1A8 |
| 12H | E1 Co-efficient 2 | E1B7 | E1B6 | E1B5 | E1B4 | E1B3 | E1B2 | E1B1 | E1B0 |
| 13H | E1 Co-efficient 3 | E1B15 | E1B14 | E1B13 | E1B12 | E1B11 | E1B10 | E1B9 | E1B8 |
| 14H | E1 Co-efficient 4 | E1C7 | E1C6 | E1C5 | E1C4 | E1C3 | E1C2 | E1C1 | E1C0 |
| 15H | E1 Co-efficient 5 | E1C15 | E1C14 | E1C13 | E1C12 | E1C11 | E1C10 | E1C9 | E1C8 |
| 16H | E2 Co-efficient 0 | E2A7 | E2A6 | E2A5 | E2A4 | E2A3 | E2A2 | E2A1 | E2A0 |
| 17H | E2 Co-efficient 1 | E2A15 | E2A14 | E2A13 | E2A12 | E2A11 | E2A10 | E2A9 | E2A8 |
| 18H | E2 Co-efficient 2 | E2B7 | E2B6 | E2B5 | E2B4 | E2B3 | E2B2 | E2B1 | E2B0 |
| 19H | E2 Co-efficient 3 | E2B15 | E2B14 | E2B13 | E2B12 | E2B11 | E2B10 | E2B9 | E2B8 |
| 1AH | E2 Co-efficient 4 | E2C7 | E2C6 | E2C5 | E2C4 | E2C3 | E2C2 | E2C1 | E2C0 |
| 1BH | E2 Co-efficient 5 | E2C15 | E2C14 | E2C13 | E2C12 | E2C11 | E2C10 | E2C9 | E2C8 |
| 1CH | HPF Co-efficient 0 | F1A7 | F1A6 | F1A5 | F1A4 | F1A3 | F1A2 | F1A1 | F1A0 |
| 1DH | HPF Co-efficient 1 | 0 | 0 | F1A13 | F1A12 | F1A11 | F1A10 | F1A9 | F1A8 |
| 1EH | HPF Co-efficient 2 | F1B7 | F1B6 | F1B5 | F1B4 | F1B3 | F1B2 | F1B1 | F1B0 |
| 1FH | HPF Co-efficient 3 | 0 | 0 | F1B13 | F1B12 | F1B11 | F1B10 | F1B9 | F1B8 |

PDN pin = "L" resets the registers to their default values.

Note 34. Unused bits must contain a "0" value.
Note 35. When reading address 0CH and 10H to 1FH, the values are invalid.
Note 36. Address 0DH is a read only register. Writing access to 0DH does not effect the operation.

## ■ Register Definitions

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 00H | Power Management 1 | PMPFIL | PMVCM | PMBP | PMSPK | PMAO | PMDAC | 0 | PMADC |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PMADC: ADC Block Power Control
0: Power down (default)
1: Power up
When the PMADC bit changes from "0" to "1", the initialization cycle (1059/fs=133ms@8kHz when ADRST bit = "0") starts. After initializing, digital data of the ADC is output.

PMDAC: DAC Block Power Control
0: Power down (default)
1: Power up

PMAO: Mono Line Out Power Control
0: Power down (default)
1: Power up

PMSPK: Speaker Block Power Control
0: Power down (default)
1: Power up

PMBP: BEEP In Power Control
0: Power down (default)
1: Power up
Even if PMBP bit is "0", the path is still connected between BEEP and AOUT/SPK-Amp. BEEPS and BEEPA bits should be set to "0" to disconnect these paths.

PMVCM: VCOM Block Power Control
0: Power down (default)
1: Power up

PMPFIL: Programmable Filter Block(HPF/2 Band EQ/ALC) Control
0: Power down (default)
1: Power up

Each block can be powered-down respectively by writing "0" to each bit. When the PDN pin is "L", all blocks are powered-down.

When PMPLL and MCKO bits and all bits in 00H address are "0", all blocks are powered-down. The registers remain unchanged.

When any of the blocks are powered-up, the PMVCM bit must be set to "1". PMVCM bit can be "0" when PMPLL and MCKO bits and all bits in 00H address are "0".

When BEEP signal is output from Speaker-Amp (Signal path: BEEP pin → SPP/SPN pins) or Mono Lineout-Amp (Signal path: BEEP pin → AOUT pin) only, the clocks may not be present. When ADC, DAC, ALC1 or ALC2 is in operation, the clocks must always be present.

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 01H | Power Management 2 | 0 | 0 | 0 | 0 | M/S | 0 | MCKO | PMPLL |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PMPLL: PLL Block Power Control
0: PLL is Power down and External is selected. (default)
1: PLL is Power up and PLL Mode is selected.

MCKO: Master Clock Output Enable
0: "L" Output (default)
1: 256fs Output

M/S: Master/Slave Mode Select
0: Slave Mode (default)
1: Master Mode

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 02H | Signal Select 1 | SPPSN | BEEPS | DACS | DACA | 0 | PMMP | MGAIN2 | MGAIN0 |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

MGAIN2, MGAIN0: MIC-Amp Gain Control (Table 18)
MGAIN1 bit is D5 bit of 03H. Default: "001H" (+20.0dB)

PMMP: Power Supply Control for Microphone
0: OFF (default)
1: ON
When PMADC bit is "1", PMMP bit is enabled.

DACA: Switch Control from DAC to Mono Line Output
0: OFF (default)
1: ON
When PMAO bit is "1", DACA bit is enabled. When PMAO bit is "0", the AOUT pin outputs AVSS.

DACS: Switch Control from DAC to Speaker-Amp
0: OFF (default)
1: ON
When DACS bit is "1", DAC output signal is input to Speaker-Amp.

BEEPS: Switch Control from BEEP pin to Speaker-Amp
0: OFF (default)
1: ON
When BEEPS bit is "1", BEEP signal is input to Speaker-Amp.

SPPSN: Speaker-Amp Power-Save Mode
0: Power-Save Mode (default)
1: Normal Operation
When SPPSN bit is "0", Speaker-Amp is in power-save mode. In this mode, the SPP pin goes to Hi-Z and the SPN pin outputs SVDD/2 voltage. When PMSPK bit = "1", SPPSN bit is enabled. After the PDN pin is set to "H", Speaker-Amp is in power-down mode since PMSPK bit is "0".

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 03H | Signal Select 2 | PFSDO | AOPS | MGAIN1 | SPKG1 | SPKG0 | BEEPA | PFDAC | ADCPF |
| Default | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

ADCPF: Select the input signal to Programmable Filter/ALC
0: SDTI
1: Output from ADC (default)

PFDAC: Select the input signal to DAC
0: SDTI (default)
1: Output from programmable Filter/ALC

BEEPA: Switch Control from beep signal to mono line output amp
0: OFF (default)
1: ON
When PMAO bit is "1", BEEPA bit is enabled. When PMAO bit is "0", the AOUT pin go to AVSS.

SPKG1-0: Select Speaker-Amp Output Gain (Table 35)
Default: "00"

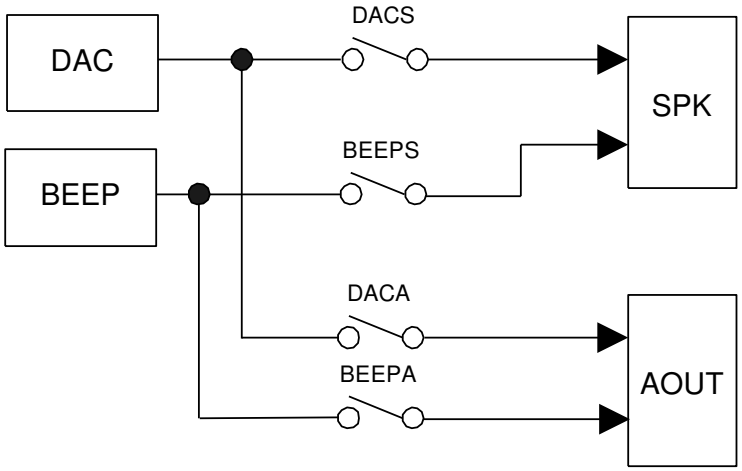



Figure 44. Speaker and Mono Lineout-Amps switch control

MGAIN1: MIC-Amp Gain Control (Table 18)
MGAIN2, MGAIN0 bit is D1, D2 bit of 02H. Default: "001H" (+20.0dB)

AOPS: Mono Line Output Power-Save Mode
0: Normal Operation (default)
1: Power Save Mode
Power-save mode is enable when AOPS bit = "1". POP noise at power-up/down can be reduced by changing at AOPS bit = "1" (Figure 40).

PFSDO : Select the output signal from SDTO
0: Output from ADC (+ 1st HPF)
1: Output from Programmable Filter/ALC (default)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 04H | Mode Control 1 | PLL3 | PLL2 | PLL1 | PLL0 | BCKO1 | BCKO0 | DIF1 | DIF0 |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

DIF1-0: Audio Interface Format (Table 15)
Default: "10" (MSB justified)

BCKO1-0: Select BICK output frequency at Master Mode (Table 9)
Default: "00" (16fs)

PLL3-0: Select input frequency at PLL mode (Table 4)
Default: "0000" (FCK pin)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 05H | Mode Control 2 | ADRST | FCKO | FS3 | MSBS | BCKP | FS2 | FS1 | FS0 |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

FS3-0: Setting of Sampling Frequency (Table 5 and Table 6) and MCKI Frequency (Table 11)
These bits select sampling frequency at PLL mode and MCKI frequency at EXT mode.
Default: "0000"

BCKP, MSBS: "00" (default) (Table 16)

FCKO: Select FCK output frequency at Master Mode (Table 10)
"0" (default)

ADRST: Select ADC initialization cycle
0: 1059/fs (default)
1: 291/fs

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 06H | Timer Select | 0 | 0 | ZTM1 | ZTM0 | WTM1 | WTM0 | RFST1 | RFST0 |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

WTM1-0: ALC1 Recovery Waiting Period (Table 26)
A period of recovery operation when any limiter operation does not occur during ALC1 operation
Default is "00".

ZTM1-0: ALC1 Zero crossing timeout Period (Table 25)
When the IPGA perform zero crossing or timeout, the IPGA value is changed by the μP WRITE operation, ALC1 recovery operation. Default is "00".

FRSL1-0: ALC First recovery Speed (Table 30)
Default: "00" (4times)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 07H | ALC Mode Control 1 | 0 | ALC2 | ALC1 | ZELMN | LMAT1 | LMAT0 | RGAIN0 | LMTH0 |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

LMTH1-0: ALC Limiter Detection Level / Recovery Waiting Counter Reset Level (Table 23)
LMTH1 bit is D6 bit of 0BH. Default: "01".

RGAIN1-0: ALC Recovery Gain Step (Table 27)
RGAIN1 bit is D7 bit of 0BH. Default: "00"

LMAT1-0: ALC Limiter ATT Step (Table 24)
Default: "00"

ZELMN: Enable zero crossing detection at ALC Limiter operation
0: Enable (default)
1: Disable

ALC1: ALC Enable for Recording
0: Recording ALC Disable (default)
1: Recording ALC Enable

ALC2: ALC Enable for Playback
0: Playback ALC Disable (default)
1: Playback ALC Enable

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 08H | ALC Mode Control 2 | IREF7 | IREF6 | IREF5 | IREF4 | IREF3 | IREF2 | IREF1 | IREF0 |
| Default | | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |

IREF7-0: Reference value at Recording ALC Recovery Operation. 0.375dB step, 242 Level (Table 28)
Default: "C5H" (+19.5dB)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 09H | Input Digital Volume Control | IVOL7 | IVOL6 | IVOL5 | IVOL4 | IVOL3 | IVOL2 | IVOL1 | IVOL0 |
| Default | | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

IVOL7-0: Input Digital Volume; 0.375dB step, 242 Level (Table 20)
Default: "91H" (0.0dB)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0AH | Digital Volume Control | OVOL7 | OVOL6 | OVOL5 | OVOL4 | OVOL3 | OVOL2 | OVOL1 | OVOL0 |
| Default | | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

OVOL7-0: Output Digital Volume; 0.375dB step, 242 Level (Table 21)
Default: "91H" (0.0dB)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0BH | ALC Mode Control 3 | RGAIN1 | LMTH1 | OREF5 | OREF4 | OREF3 | OREF2 | OREF1 | OREF0 |
| Default | | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |

OREF5-0: Reference value at Playback ALC Recovery Operation. 0.375dB step, 50 Level (Table 29)
Default: "28H" (+6.0dB)

RGAIN1-0: ALC Recovery Gain Step (Table 27)
RGAIN1 bit is D1 bit of 07H. Default: "00"

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0DH | Input Digital Volume Control | VOL7 | VOL6 | VOL5 | VOL4 | VOL3 | VOL2 | VOL1 | VOL0 |
| Default | | - | - | - | - | - | - | - | - |

VOL7-0: Current ALC volume value; 0.375dB step, 242 Level. Read operation only (Table31)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0EH | Mode Control 3 | DATT1 | DATT0 | SMUTE | MDIF | EQ2 | EQ1 | HPF | HPFAD |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

HPFAD: HPF after ADC Enable
0: Disable
1: Enable (default)
When HPFAD bit = "0", HPFAD block is through (0dB).

HPF: HPF Enable in Filter block that PMPFIL bit is controlled.
0: Disable
1: Enable (default)
When HPF bit = "0", HPF block is through (0dB).

EQ1: Equalizer1(EQ1) Enable
0: Disable (default)
1: Enable
When EQ1 bit is "1", the settings of E1A15-0, E1B15-0 and E1C15-0 bits are enabled. When EQ1 bit is "0", EQ1 block is through (0dB).

EQ2: Equalizer2(EQ2) Enable
0: Disable (default)
1: Enable
When EQ2 bit is "1", the settings of E2A15-0, E2B15-0 and E2C15-0 bits are enabled. When EQ2 bit is "0", EQ2 block is through (0dB).

SMUTE: soft mute control
0: Normal Operation (default)
1: DAC outputs soft-muted

MDIF: MIC Input Type Select
0: Single-ended input (MIC pin Input: Default)
1: Full-differential input (MIC pin and BEEP/MICP pin Input)
When MDIF bit = "1", it must be set PMBP bit = BEEPA bit = BEEPS bit = "0".

DATT1-0: Output Digital Volume2; 6dB step, 4 Level (Table 22)
Default: "00H" (0.0dB)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 10H | E1 Co-efficient 0 | E1A7 | E1A6 | E1A5 | E1A4 | E1A3 | E1A2 | E1A1 | E1A0 |
| 11H | E1 Co-efficient 1 | E1A15 | E1A14 | E1A13 | E1A12 | E1A11 | E1A10 | E1A9 | E1A8 |
| 12H | E1 Co-efficient 2 | E1B7 | E1B6 | E1B5 | E1B4 | E1B3 | E1B2 | E1B1 | E1B0 |
| 13H | E1 Co-efficient 3 | E1B15 | E1B14 | E1B13 | E1B12 | E1B11 | E1B10 | E1B9 | E1B8 |
| 14H | E1 Co-efficient 4 | E1C7 | E1C6 | E1C5 | E1C4 | E1C3 | E1C2 | E1C1 | E1C0 |
| 15H | E1 Co-efficient 5 | E1C15 | E1C14 | E1C13 | E1C12 | E1C11 | E1C10 | E1C9 | E1C8 |
| 16H | E2 Co-efficient 0 | E2A7 | E2A6 | E2A5 | E2A4 | E2A3 | E2A2 | E2A1 | E2A0 |
| 17H | E2 Co-efficient 1 | E2A15 | E2A14 | E2A13 | E2A12 | E2A11 | E2A10 | E2A9 | E2A8 |
| 18H | E2 Co-efficient 2 | E2B7 | E2B6 | E2B5 | E2B4 | E2B3 | E2B2 | E2B1 | E2B0 |
| 19H | E2 Co-efficient 3 | E2B15 | E2B14 | E2B13 | E2B12 | E2B11 | E2B10 | E2B9 | E2B8 |
| 1AH | E2 Co-efficient 4 | E2C7 | E2C6 | E2C5 | E2C4 | E2C3 | E2C2 | E2C1 | E2C0 |
| 1BH | E2 Co-efficient 5 | E2C15 | E2C14 | E2C13 | E2C12 | E2C11 | E2C10 | E2C9 | E2C8 |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

E1A15-0, E1B15-0, E1C15-0: Coefficient for Equalizer 1(16bit x3)
Default: “0000H”

E2A15-0, E2B15-0, E2C15-0: Coefficient for Equalizer 2 (16bit x3)
Default: “0000H”

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 1CH | HPF Co-efficient 0 | F1A7 | F1A6 | F1A5 | F1A4 | F1A3 | F1A2 | F1A1 | F1A0 |
| Default | | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 1DH | HPF Co-efficient 1 | 0 | 0 | F1A13 | F1A12 | F1A11 | F1A10 | F1A9 | F1A8 |
| Default | | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 1EH | HPF Co-efficient 2 | F1B7 | F1B6 | F1B5 | F1B4 | F1B3 | F1B2 | F1B1 | F1B0 |
| Default | | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 1FH | HPF Co-efficient 3 | 0 | 0 | F1B13 | F1B12 | F1B11 | F1B10 | F1B9 | F1B8 |
| Default | | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |

F1A13-0, F1B13-0: FIL1 (Wind-noise Reduction Filter) Coefficient Setting Enable (14bit x 2)
Default: F1A13-0 bits = 0x1F16, F1B13-0 bits = 0x1E2B
fc = 75Hz@fs=8kHz, 150Hz@fs=16kHz

## SYSTEM DESIGN

Figure 45 shows the system connection diagram for the AK4633. An evaluation board [AKD4633] is available which demonstrates the optimum layout, power supply arrangements and measurement results.

**Single Ended input**

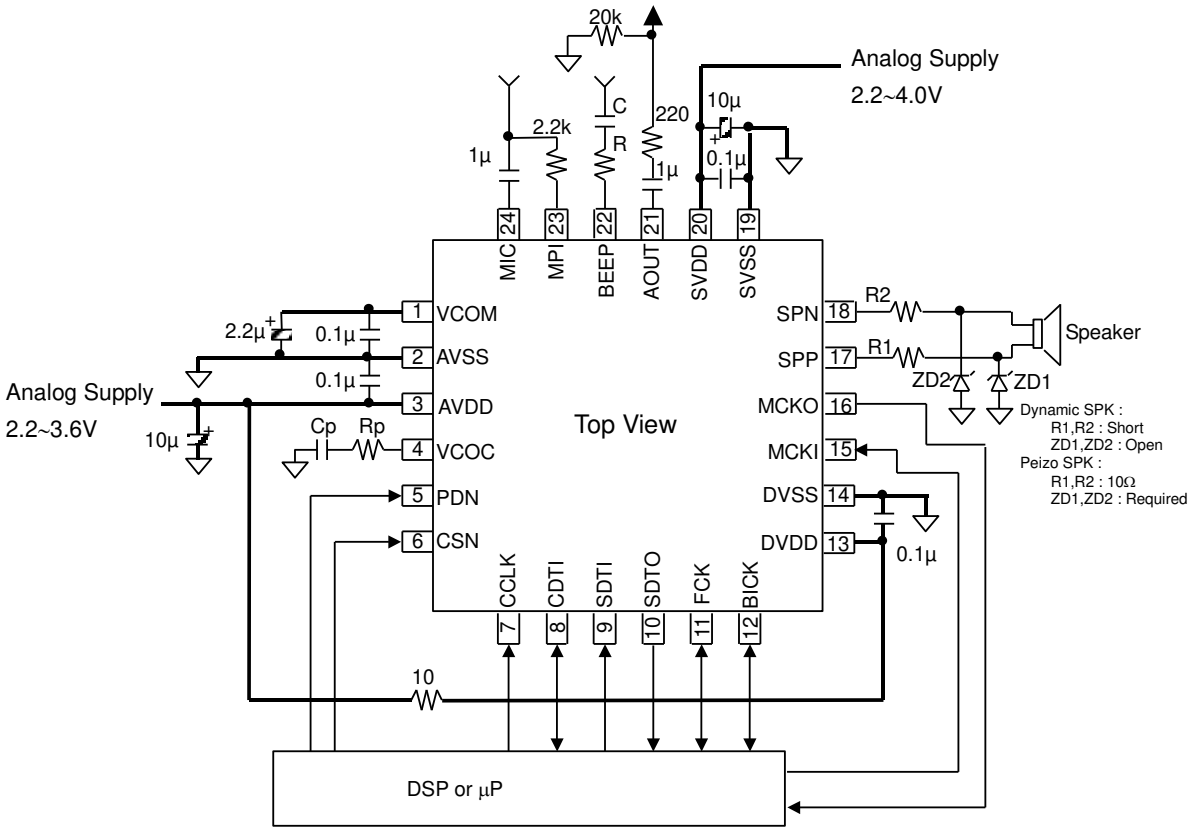



Figure 45. Typical Connection Diagram

**Differential Input**

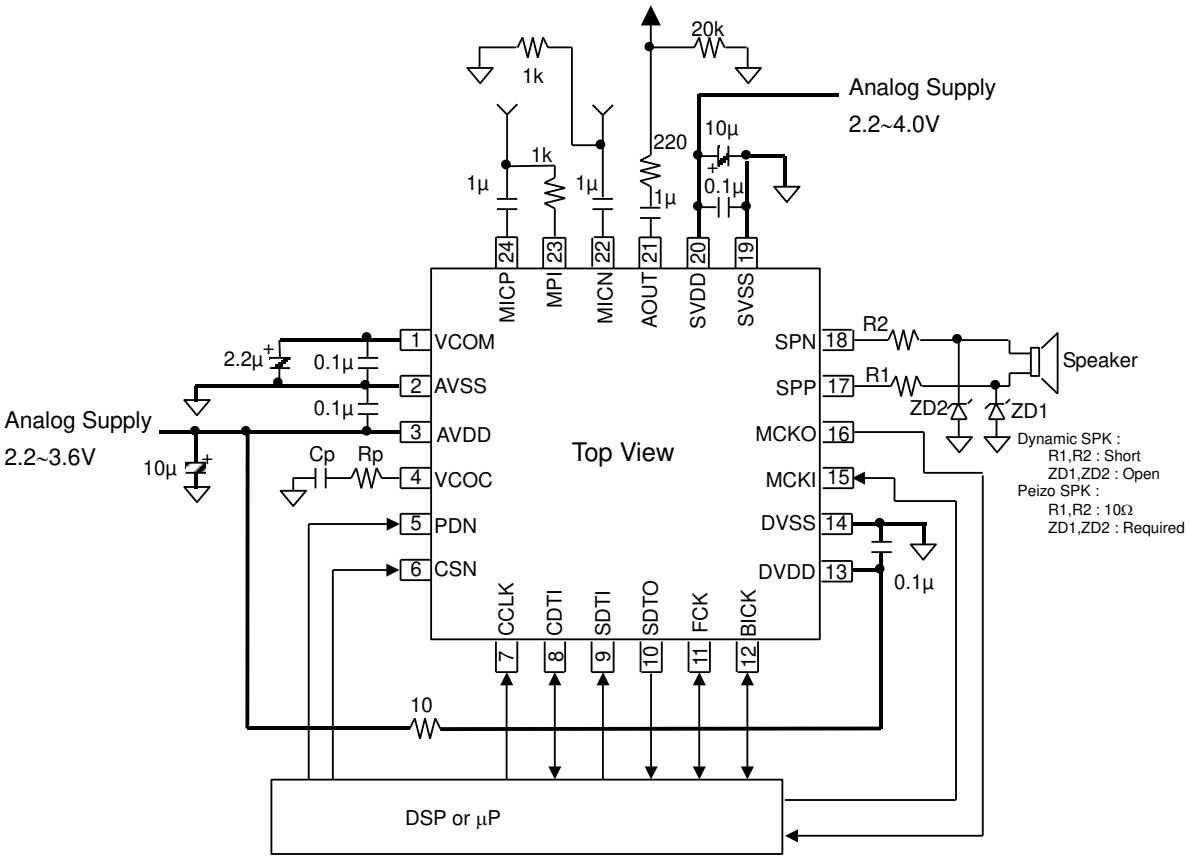



Figure 46. Typical Connection Diagram

Note:
- AVSS, DVSS and SVSS of the AK4633 should be distributed separately from the ground of external controllers.
- If AVDD and DVDD are separated, DVDD should be set from 1.6V to 3.6V.
- All digital input pins should not be left floating.
- When the AK4633 is EXT mode (PMPLL bit = "0"), a resistor and capacitor of the VCOC pin are not needed.
- When the AK4633 is PLL mode (PMPLL bit = "1"), a resistor and capacitor of the VCOC pin are shown in Table 36.

| Mode | PLL3 bit | PLL2 bit | PLL1 bit | PLL0 bit | PLL Reference Clock Input Pin | Input Frequency | Rp and Cp of VCOC pin | | PLL Lock Time (max) | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Rp[Ω] | Cp[F] | | |
| 0 | 0 | 0 | 0 | 0 | FCK pin | 1fs | 6.8k | 220n | 160ms | (default) |
| 1 | 0 | 0 | 0 | 1 | BICK pin | 16fs | 10k | 4.7n | 2ms | |
| 2 | 0 | 0 | 1 | 0 | BICK pin | 32fs | 10k | 4.7n | 2ms | |
| 3 | 0 | 0 | 1 | 1 | BICK pin | 64fs | 10k | 4.7n | 2ms | |
| 4 | 0 | 1 | 0 | 0 | MCKI pin | 11.2896MHz | 10k | 4.7n | 40ms | |
| 5 | 0 | 1 | 0 | 1 | MCKI pin | 12.288MHz | 10k | 4.7n | 40ms | |
| 6 | 0 | 1 | 1 | 0 | MCKI pin | 12MHz | 10k | 4.7n | 40ms | |
| 7 | 0 | 1 | 1 | 1 | MCKI pin | 24MHz | 10k | 4.7n | 40ms | |
| 12 | 1 | 1 | 0 | 0 | MCKI pin | 13.5MHz | 10k | 10n | 40ms | |
| 13 | 1 | 1 | 0 | 1 | MCKI pin | 27MHz | 10k | 10n | 40ms | |
| Others | Others | | | | N/A | | | | | |

Table 36. Setting of PLL Mode (*fs: Sampling Frequency)

## 1. Grounding and Power Supply Decoupling

The AK4633 requires careful attention to power supply and grounding arrangements. AVDD, DVDD and SVDD are usually supplied from the system's analog supply. If AVDD, DVDD and SVDD are supplied separately, the correct power up sequence should be observed. AVSS, DVSS and SVSS of the AK4633 should be connected to the analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4633 as possible, with the small value ceramic capacitor being the nearest.

## 2. Voltage Reference

VCOM is a signal ground of this chip. A 2.2μF electrolytic capacitor in parallel with a 0.1μF ceramic capacitor attached to the VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK4633.

## 3. Analog Inputs

The Mic and Beep inputs are single-ended. The input signal range scales with nominally at 0.06 x AVDD Vpp for the Mic input and 0.6 x AVDD Vpp for the Beep input, centered around the internal common voltage (approx. 0.45 x AVDD). Usually the input signal is AC coupled using a capacitor. The cut-off frequency is $fc = 1/(2\pi RC)$. The AK4633 can accept input voltages from AVSS to AVDD.

## 4. Analog Outputs

The input data format for the DAC is 2's complement. The output voltage is a positive full scale for 7FFFH(@16bit) and a negative full scale for 8000H(@16bit). Mono output from the MOUT pin and Mono Line Output from the AOUT pin are centered at 0.45 x AVDD (typ). The Speaker-Amp output is centered at SVDD/2.

## CONTROL SEQUENCE

### ■ Clock Set up

When ADC, DAC and Programmable Filter are used, the clocks must be supplied.

1. In case of PLL Master Mode

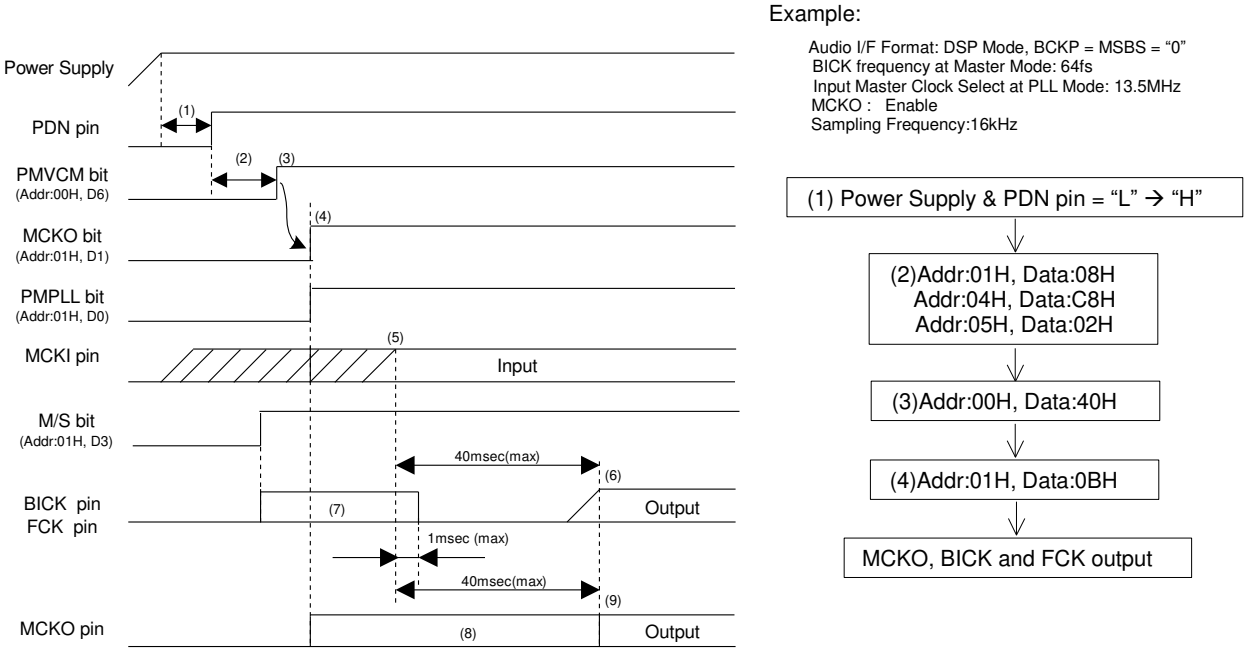



Figure 47. Clock Set Up Sequence (1)

<Example>

(1) After Power Up: PDN pin = "L" → "H"
"L" time (1) of 150ns or more is needed to reset the AK4633.

(2) DIF1-0, PLL3-0, FS3-0, BCKO1-0, MSBS, BCKP and M/S bits should be set during this period.

(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered-up before the other block operates.

(4) In case of using MCKO output: MCKO bit = "1"
In case of not using MCKO output: MCKO bit = "0"

(5) PLL lock time is 40ms(max) after PMPLL bit changes from "0" to "1" and MCKI is supplied from an external source.

(6) The AK4633 starts to output the FCK and BICK clocks after the PLL becomes stable. The normal operation of the block which a clock is necessary for becomes possible.

(7) The invalid frequencies are output from FCK and BICK pins during this period.

(8) The invalid frequency is output from the MCKO pin during this period.

(9) The normal clock is output from the MCKO pin after the PLL is locked.

2. When the external clock (FCK or BICK pin) is used in PLL Slave mode.

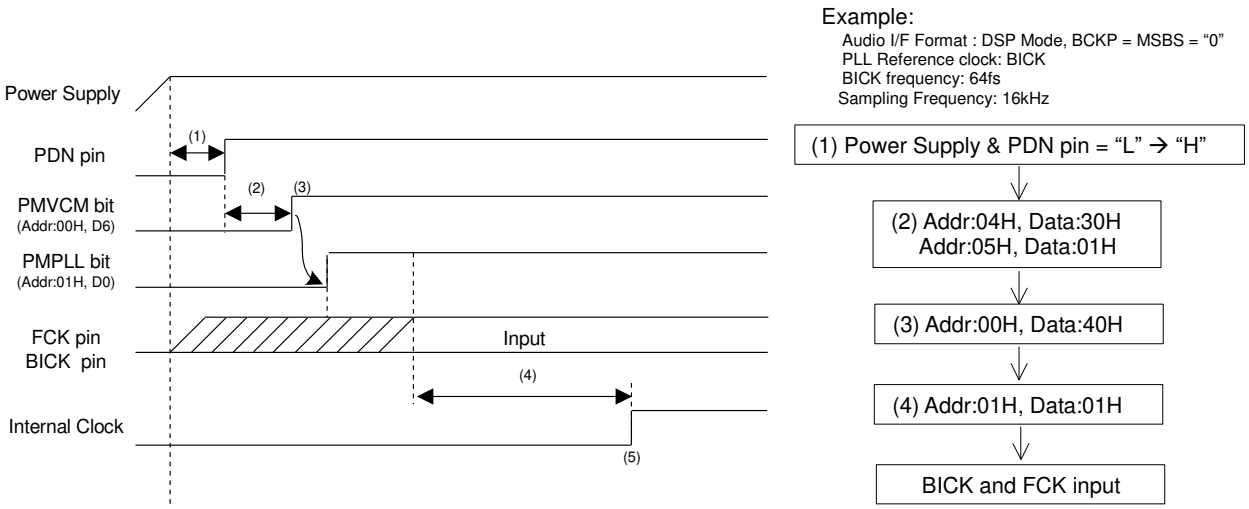



Figure 48. Clock Set Up Sequence (2)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time (1) of 150ns or more is needed to reset the AK4633.

(2) DIF1-0, FS3-0, PLL3-0, MSBS and BCKP bits should be set during this period.

(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.

(4) PLL starts after the PMPLL bit changes from "0" to "1" and PLL reference clocks (FCK or BICK pin) are supplied. PLL lock time is 160ms(max) when PLL reference clock is FCK, and PLL lock time is 2ms(max) when PLL reference clock is BICK.

(5) Normal operation starts after the PLL is locked.

3. When the external clock (MCKI pin) is used in PLL Slave mode.

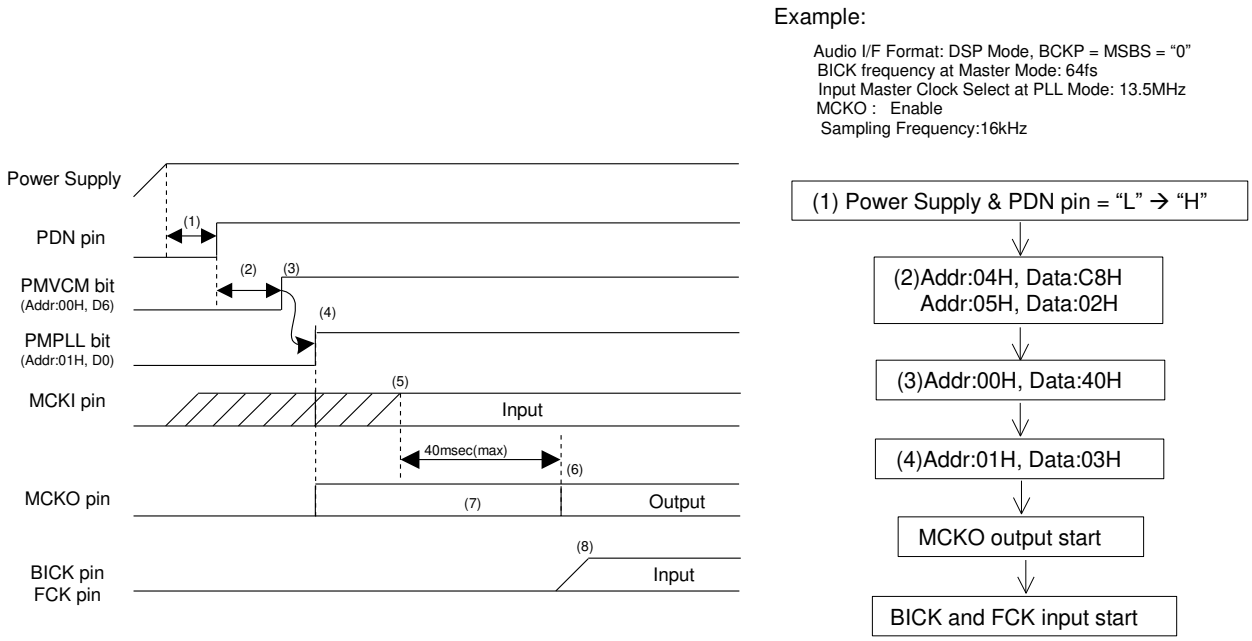



Figure 49. Clock Set Up Sequence (3)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time (1) of 150ns or more is needed to reset the AK4633.

(2) DIF1-0, PLL3-0, FS3-0, BCKO1-0, MSBS, BCKP and M/S bits should be set during this period.

(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.

(4) PLL Power Up: PMPLL bit "0" → "1"

(5) PLL lock time is 40ms(max) after the PMPLL bit changes from "0" to "1" and PLL reference clock (MCKI pin) is supplied.

(6) The normal clock is output from the MCKO pin after PLL is locked.

(7) The invalid frequency is output from the MCKO pin during this period.

(8) BICK and FCK clocks should be synchronized with MCKO clock.

4. EXT Slave Mode

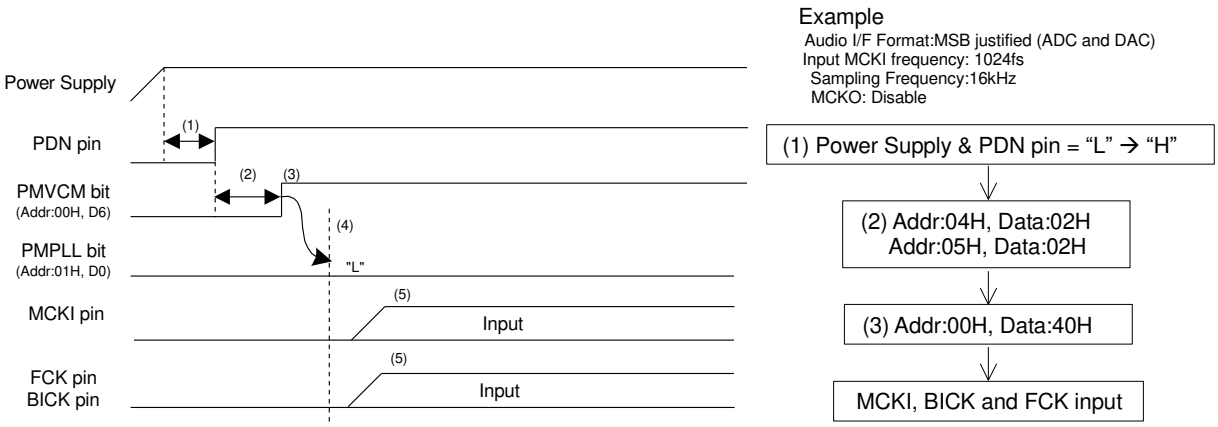



Figure 50. Clock Set Up Sequence (4)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time (1) of 150ns or more is needed to reset the AK4633.

(2) DIF1-0 and FS1-0 bits should be set during this period.

(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.

(4) Power down PLL: PMPLL bit = "0"

(5) Normal operation starts after the MCKI, FCK and BICK are supplied.

## ■ MIC Input Recording

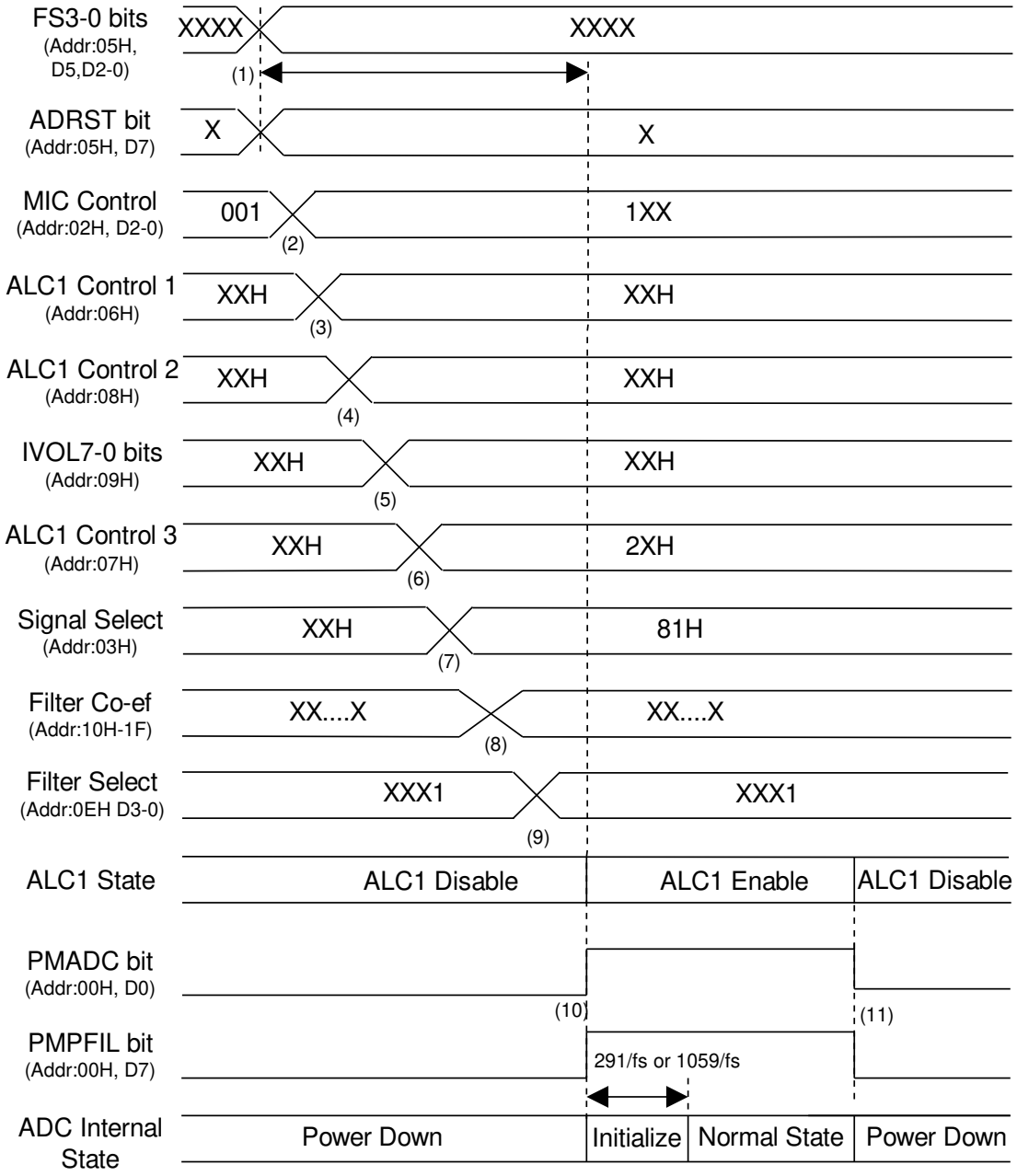



Figure 51. MIC Input Recording Sequence

Example:

PLL Master Mode
Audio I/F Format:DSP Mode, BCKP=MSBS="0"
Sampling Frequency: 16kHz
Pre MIC AMP:+20dB
MIC Power On
ADC Initialize time : 291/fs
ALC1 setting:Refer to Table 32
HPFAD, HPF : ON (fc=150Hz)
2 band EQ : OFF

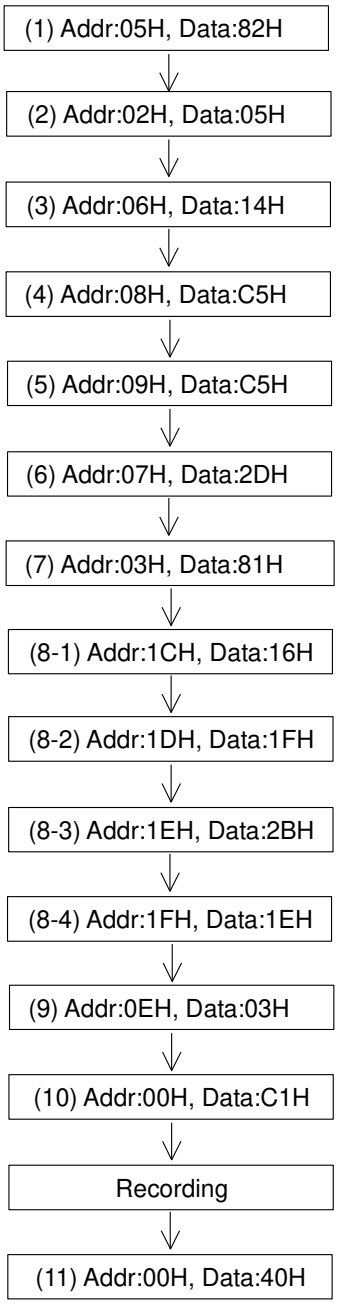



Figure 52. MIC Input Recording Sequence Example

<Example>

This sequence is an example of ALC1 setting at fs=16kHz. If the parameter of the ALC1 is changed, please refer to "Table 32. Example of the ALC Setting (Recording)"

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS3-0 bit) and ADC initialization cycle. When the AK4633 is PLL mode, Programmable Filter and ADC should be powered-up in consideration of PLL lock time after a sampling frequency is changed.
(2) Set up MIC input (Addr: 02H)
(3) Set up Timer Select for ALC1 (Addr: 06H)
(4) Set up REF value for ALC1 (Addr: 08H)
(5) Set up IVOL value at start ALC1 (Addr: 09H)
(6) Set up LMTH0, RGAIN0, LMAT1-0, ZELM and ALC1 bits (Addr: 07H)
(7) Set up path of programmable filter: PFSDO bit = ADCPF bit = "1"
(8) Set up coefficient of programmable filter (HPF/EQ): Addr: 10H ~ 1FH
(9) Set up ON/OFF of programmable filter (HPF/EQ)
HPFAD bit should be set to "1".
(10) Power Up programmable filter and ADC: PMPFIL bit = PMADC bit = "0" → "1"
The initialization cycle time of ADC is 1059/fs=66ms@fs=16kHz when ADRST bit = "0",
and 291/fs=18ms@fs=16kHz when ADRST bit = "1". The ALC1 starts at IVOL value set by (5).
(11) Power Down programmable filter and ADC: PMPFIL bit = PMADC bit = "1" → "0"

## ■ Speaker-amp Output

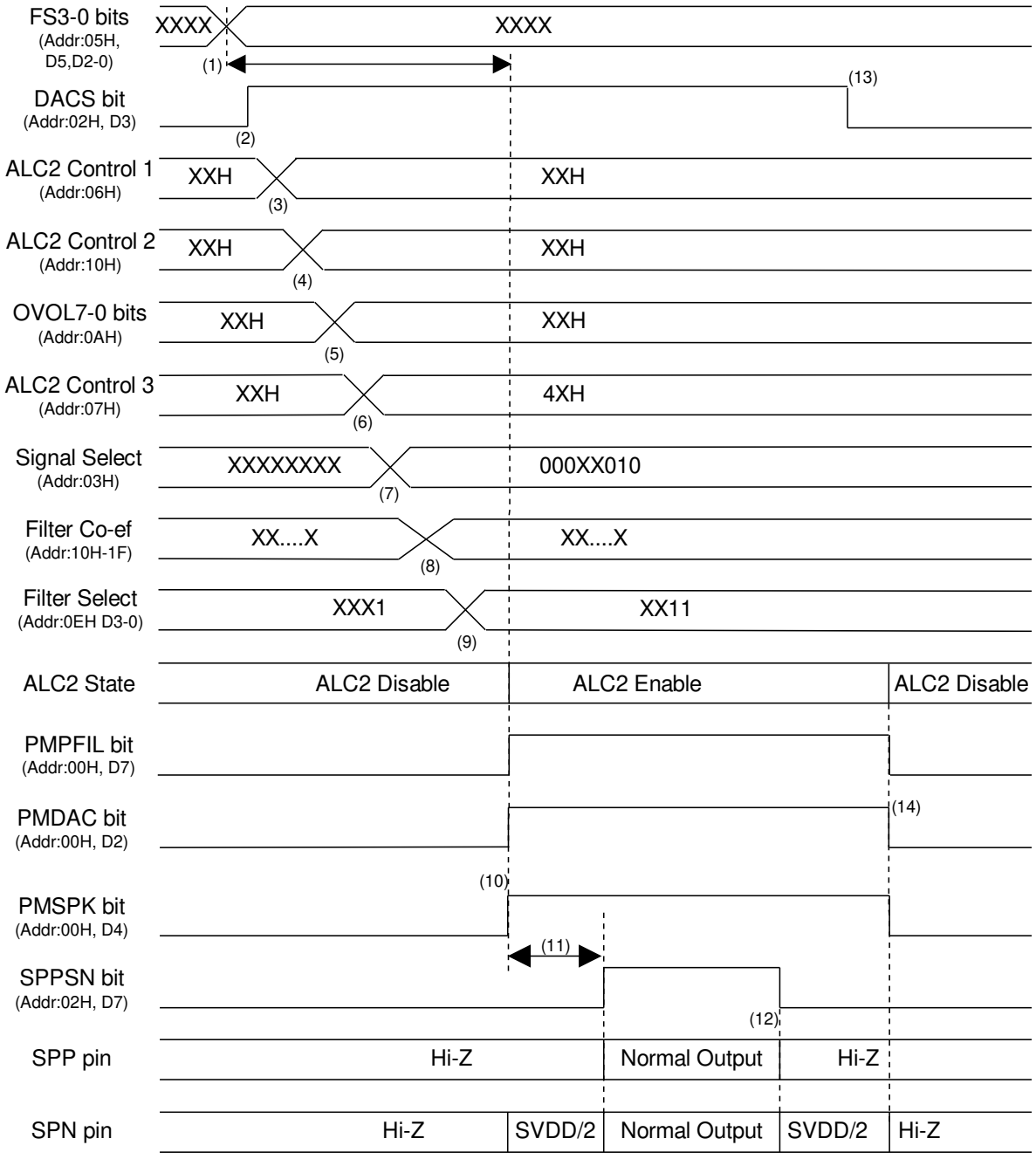



Figure 53. Speaker-Amp Output Sequence

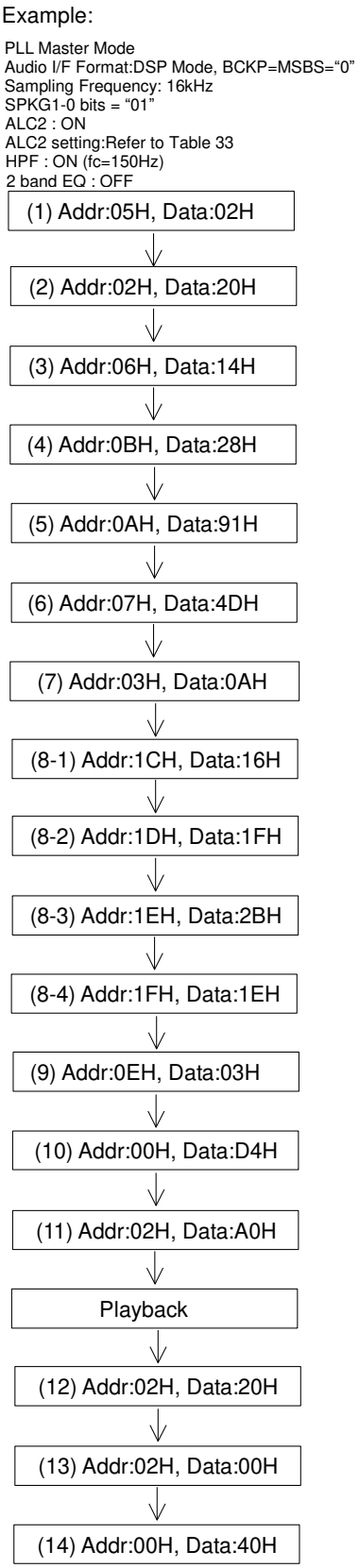



Figure 54. Speaker-Amp Output Sequence Example

<Example>

This sequence is an example of ALC2 setting at fs=16kHz. If the parameter of the ALC2 is changed, please refer to "Table 33. Example of the ALC Setting (Playback)".

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS3-0 bits). When the AK4633 is PLL mode, DAC and Speaker-Amp should be powered-up in consideration of PLL lock time after a sampling frequency is changed.
(2) Set up the path of "DAC → SPK-Amp": DACS bit: "0" → "1"
(3) Set up the ALC2 Timer (Addr: 06H)
(4) Set up the REF value of ALC2 (Addr: 08H)
(5) Set up OVOL value at start ALC2 (Addr: 10H), RGAIN1 and LMTH1
(6) Set up LMTH0, RGAIN0, LMAT1-0, ZELM and ALC2 bits (Addr: 07H)
(7) Set up path of programmable filter and SPK-Amp gain:
PFDAC bit = "1", ADCPF bit = "0", SPKG1-0 bits = "XX"
(8) Set up coefficient of programmable filter (HPF/EQ): Addr: 10H ~ 1FH
(9) Set up ON/OFF of programmable filter (HPF/EQ)
HPF bit is recommended to "1".
(10) Power Up DAC, SPK and programmable filter:
PMDAC bit = PMSPK bit = PMPFIL bit = "0" → "1"
(11) Exit Speaker power-save-mode: SPPSN bit = "0" → "1"
SPPSN bit should be set to "1" at more than 1ms after PMSPK bit is set to "1".
(12) Enter Speaker power-save-mode: SPPSN bit = "1" → "0"
(13) Disable the path of "DAC → SPK-Amp": DACS bit = "1" → "0"
(14) Power Down DAC, Speaker and programmable filter: PMDAC bit = PMSPK bit = PMPFIL bit = "1" → "0"

## ■ BEEP Signal Output from Speaker-Amp

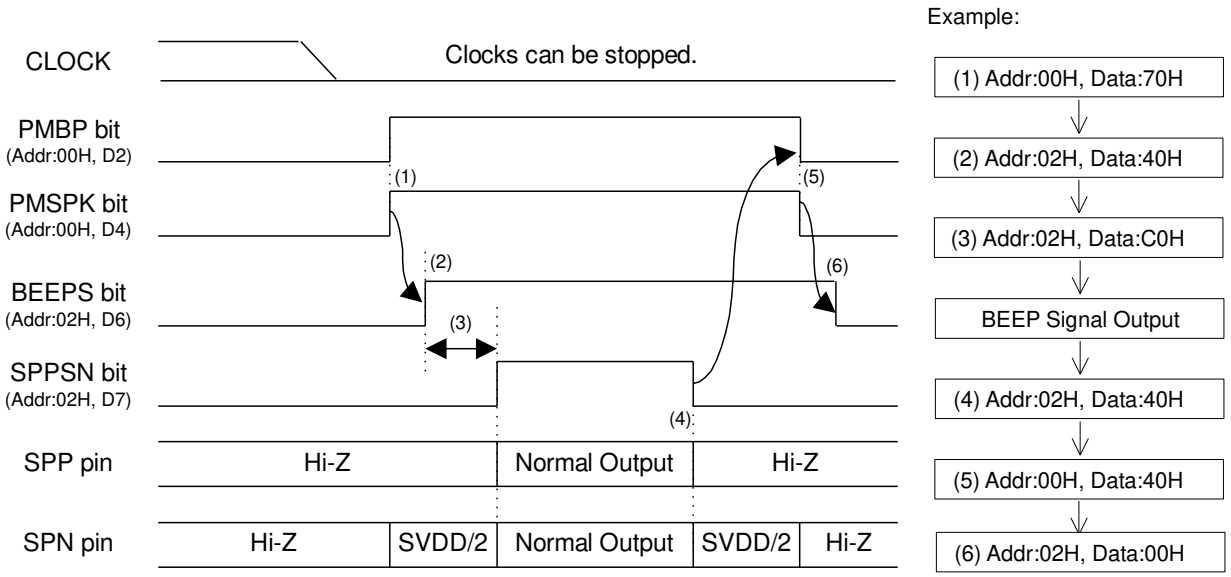



Figure 55. "BEEP-Amp → Speaker-Amp" Output Sequence

<Example>

The clock is not needed to supply when only BEEP-Amp and Speaker-Amp are operating.

(1) Power Up BEEP-Amp and Speaker-Amp: PMBP bit = PMSPK bit = "0" → "1"
(2) Enable the path of "BEEP → SPK-Amp": BEEPS bit = "0" → "1"
(3) Exit the power-save-mode of Speaker-Amp: SPPSN bit = "0" → "1"
"(4)" time depends on the time constant of external resistor and capacitor connected to BEEP pin. If Speaker-Amp output is enabled before input of BEEP-Amp becomes stable, pop noise may occur.
e.g. R=20k, C=0.1μF: Recommended wait time is more than 5τ = 10ms.
(4) Enter the power-save-mode of Speaker-Amp: SPPSN bit = "1" → "0"
(5) Power Down BEEP-Amp and Speaker-Amp: PMBP bit = PMSPK bit = "1" → "0"
(6) Disable the path of "BEEP → SPK-Amp": BEEPS bit = "1" → "0"

## ■ Mono Lineout

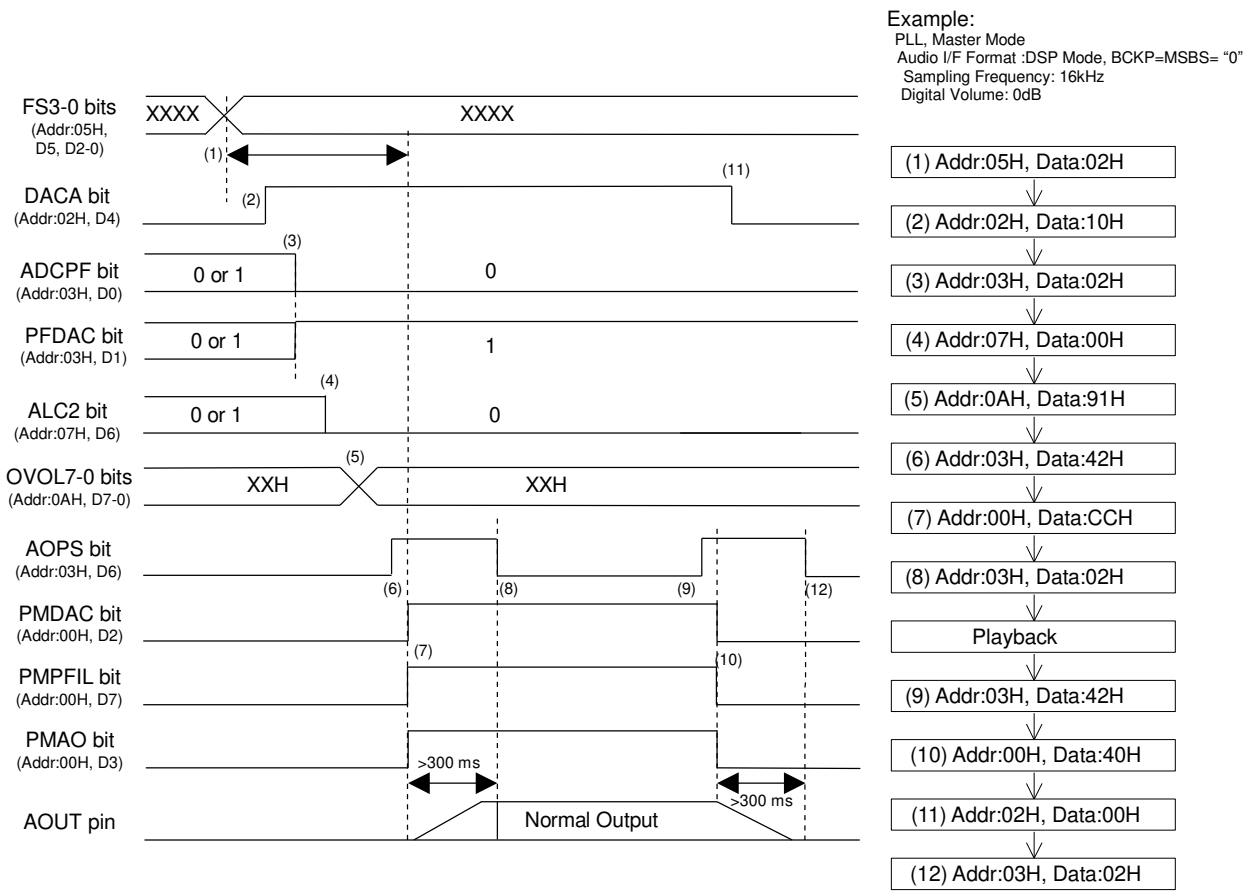



Figure 56. Mono Lineout Sequence

<Example>

This sequence is an example of Digital Output Volume at manual mode.

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS3-0 bits).
DAC should be powered-up in consideration of PLL lock time.

(2) Set up the path of "DAC → Mono Line Amp": DACA bit: "0" → "1"

(3) Set up the path: ADCPF bit = "0", PFDAC bit = "1"

(4) Disable ALC2: ALC2 bit = "0"

(5) Set up the digital volume (Addr: 0AH)

(6) Enter the power-save-mode of AOUT: AOPS bit: "0" → "1"

(7) Power Up DAC, programming filter and mono lineout.
PMDAC bit = PMPFIL bit = PMAO bit = "0" → "1"
The AOUT pin powers up at rising edge. The rise time is 300ms(max) when C = 1μF.

(8) Exit the power-save-mode of AOUT: AOPS bit: "1" → "0"
The setting should be done after the AOUT pin rises up. After the setting, the signal is output from the AOUT pin.

(9) Enter the power-save-mode of AOUT: AOPS bit: "0" → "1"

(10) Power Down DAC, programmable filter and mono lineout.
PMDAC bit = PMPFIL bit = PMAO bit = "1" → "0"
The AOUT pin powers up at falling edge. The fall time is 300ms(max) when C = 1μF.

(11) Disable the path of "DAC → Mono Line Amp": DACA bit: "1" → "0"

(12) Exit the power-save-mode of AOUT: AOPS bit: "1" → "0"
The setting should be down after the AOUT pin falls down.

## ■ Stop of Clock

Master clock can be stopped when ADC, DAC and programmable filters are not in operation.

1. PLL Master Mode

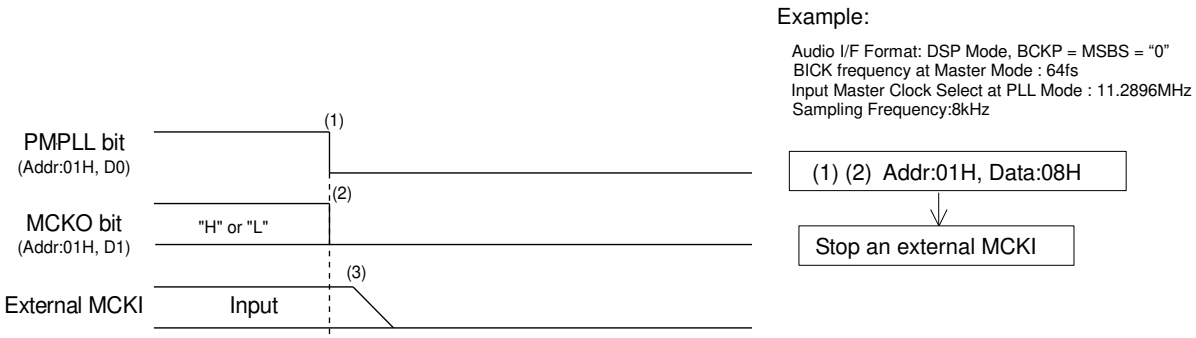



Figure 57. Clock Stopping Sequence (1)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
(2) Stop MCKO clock: MCKO bit = "1" → "0"
(3) Stop an external master clock.

2. PLL Slave Mode (FCK or BICK pins)

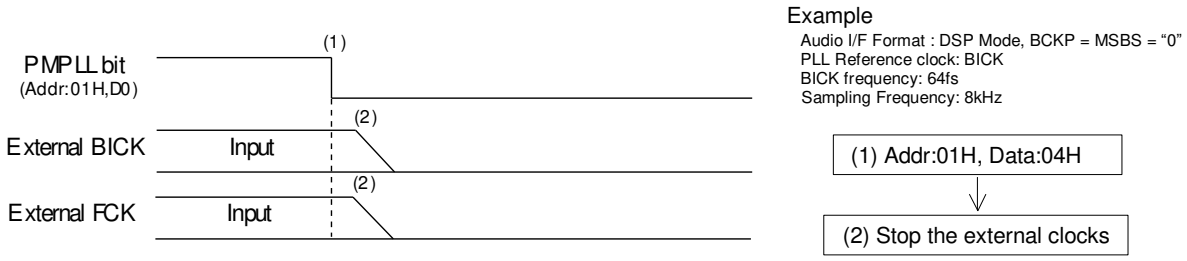



Figure 58. Clock Stopping Sequence (2)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
(2) Stop the external BICK and FCK clocks.

3. PLL Slave Mode (MCKI pin)

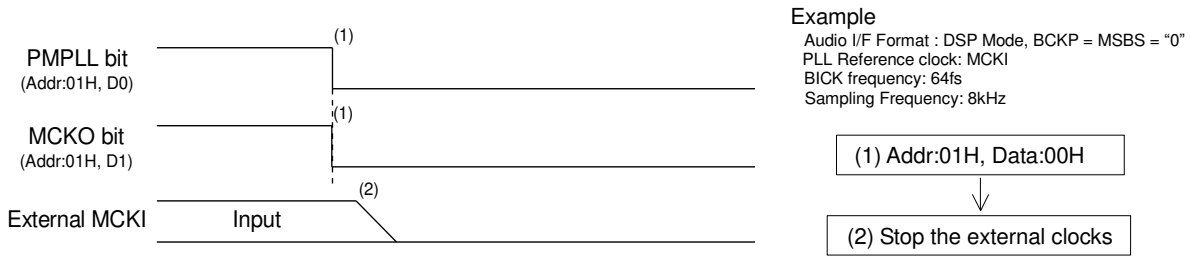



Figure 59. Clock Stopping Sequence (3)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
Stop MCKO output: MCKO bit = "1" → "0"
(2) Stop the external master clock.

4. EXT Slave Mode

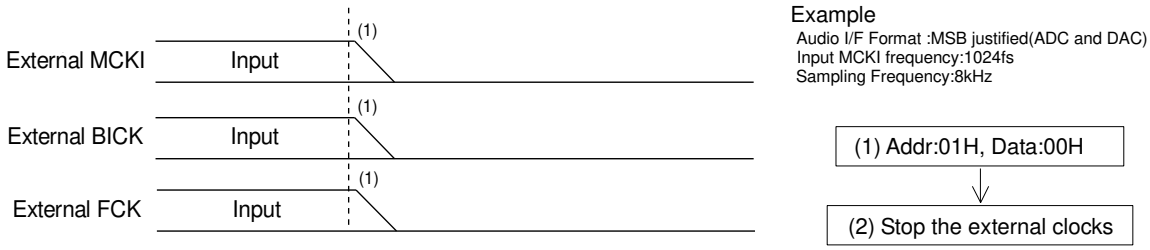



Figure 60. Clock Stopping Sequence (4)

<Example>
(1) Stop the external MCKI, BICK and FCK clocks.

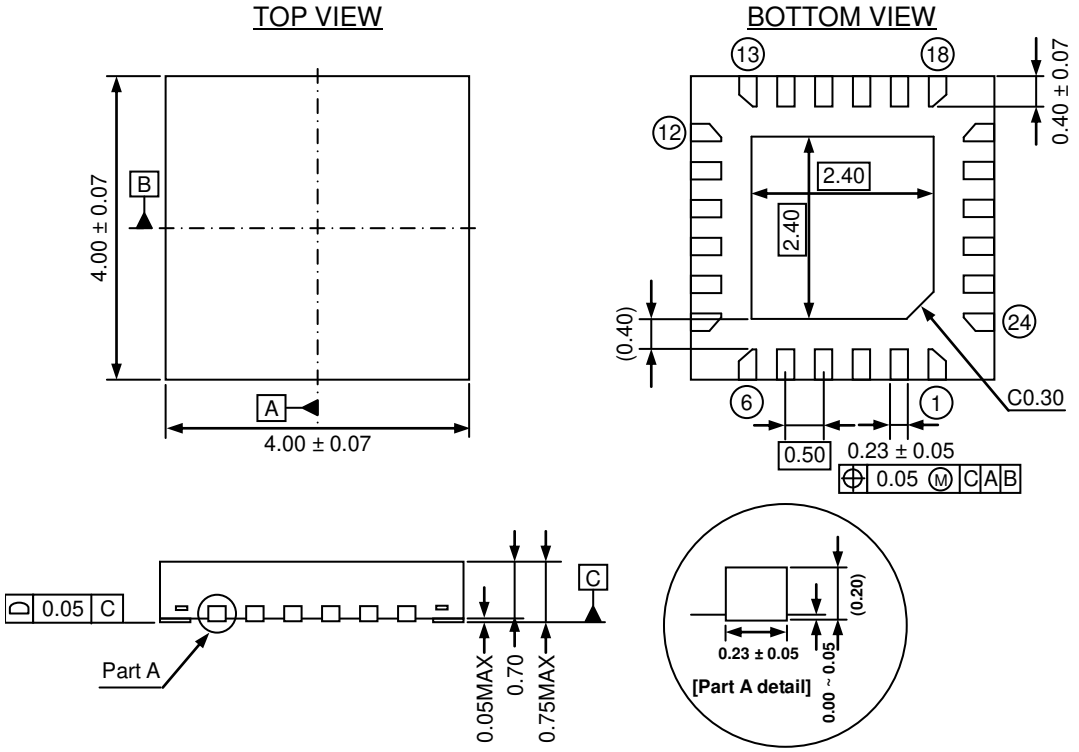
## ■ Power Down

VCOM should be powered-down after the master clock is stopped if clocks are supplied when all blocks except for VCOM are powered-down. The AK4633 is also powered-down by the PDN pin = "L". In this case, the registers are initialized.

## PACKAGE

### ■ Outline Dimensions

24pin QFN (Unit: mm)

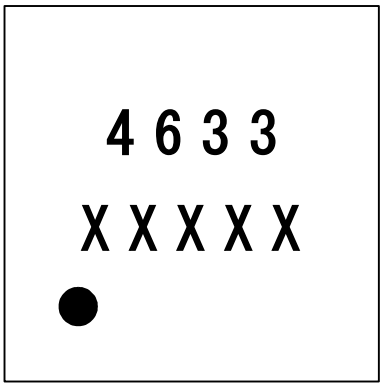



Note) The exposed pad on the bottom surface of the package must be open or connected to GND.

### ■ Material & Lead finish

Package molding compound: Epoxy Resin, Halogen (bromine and chlorine) free
Lead frame material: Cu Alloy
Pin surface treatment: Solder (Pb free) plate

## MARKING




XXXXX: Date code (5 digit)
Pin #1 indication

## REVISION HISTORY

| Date (YY/MM/DD) | Revision | Reason | Page | Contents |
|---|---|---|---|---|
| 05/12/26 | 00 | First Edition | | |
| 06/04/28 | 03 | Error Correct | 40 | Table 19 : PDSDO bit → PFSDO bit |
| | | Error Correct | 41 | 2 Band Equalizer : The Coefficient of C is corrected.<br><br>[Before correct]<br>$C = \frac{1 - \tan(\pi fb/fs)}{1 + \tan(\pi fb/fs)}$<br><br>[After correct]<br>$C = -\frac{1 - \tan(\pi fb/fs)}{1 + \tan(\pi fb/fs)}$ |
| | | Add Explanation | 42 | 2 Band Equalizer : The note is added when these equalizer are used as notch filters |
| | | Add Explanation | 53, 75 | Speaker-Amp Control Sequence<br>The wait time from PMSPK bit = "1" to SPPSN bit is "1" is added. |
| | | Error Correct | 54 | Serial control interface<br>Bit6 in Figure 43 : A2 → A1 |
| 09/01/05 | 04 | Product Addition | 2, 3, 8 | The AK4633EN was added.<br>(1) Ambient Temperature<br>AK4633VN: –40 ~ +85ºC<br>AK4633EN: –30 ~ +85ºC |
| 09/01/05 | 04 | Error Correct | 28 | ■ PLL Unlock State<br>Table 7: The BICK and FCK pin states were changed.<br>Table 8: PMPLL bit = "1" → "0" |
| | | | 50 | ■ BEEP Input<br>In the last sentence, the MDIF bit value was changed.<br>MDIF bit to "1" → MDIF bit to "0" |
| | | | 61 | EQ1: Equalizer1 (EQ1) Enable<br>EQA15-0 → E1A15-0<br>EQB15-0 → E1B15-0<br>EQC15-0 → E1C15-0<br><br>EQ2: Equalizer1 (EQ2) Enable<br>EQA15-0 → E2A15-0<br>EQB15-0 → E2B15-0<br>EQC15-0 → E2C15-0 |
| 10/04/14 | 05 | Specification Addition | 09 | RECOMMENDED OPERATING CONDITIONS<br>AVDD – SVDD was added: 1.0V (max) |
| 15/10/30 | 06 | Specification Change | 80, 81 | PACKAGE, MARKING.<br>Package dimension and Marking were changed. |

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