MP44018A

CrM/DCM Multi-Mode PFC Controller with Enhanced Light-Load Efficiency

DESCRIPTION

The MP44018A is a CrM/DCM multi-mode PFC controller that provides simple and high-performance active power factor correction using minimal external components.

The MP44018A features a very low supply current. This allows the device to achieve low standby power loss, and the typical no load power is below 30mW.

The switching frequency is reduced by dead time extension technology under light-load conditions, which improves light-load efficiency. The MP44018A also achieves lower THD due to variable-on-time control in discontinuous conduction mode (DCM) when compared to conventional constant-on-time (COT) control.

Multi-protection functionality largely enhances the safety and reliability of the system. The MP44018A feature over-voltage protection (OVP), over-current limit (OCL), over-current protection (OCP), under-voltage protection (UVP), brown-in (BI) and brownout (BO), static OVP, VCC under-voltage lockout (UVLO), and over-temperature protection (OTP).

MP44018A is available in SOIC-8 package.

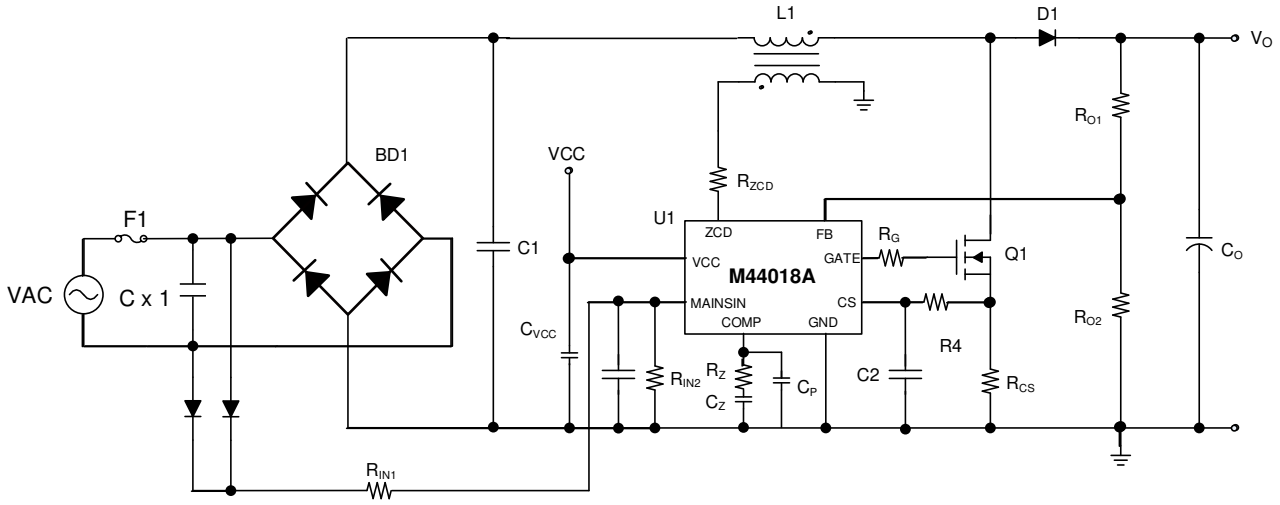
FEATURES

- Valley Turn-On for Minimum Switching Loss
- Frequency Reduction to Reduce Switching Loss Under Light-Load Conditions
- Low Supply Current in Burst Mode
- Soft-On/Off Burst for Low Audible Noise
- Mains Compensation
- Improved THD
- Under-Voltage Protection (UVP)
- Over-Current Limit (OCL)
- Over-Current Protection (OCP)
- Over-Voltage Protection (OVP)
- Brown-In (BI) and Brownout (BO)
- Over-Temperature Protection (OTP)
- Open/Short Pin Protection
- Soft Start-Up
- Enhanced Dynamic Response
- Available in an SOIC-8 Package

APPLICATIONS

- LCD and OLED TVs
- Desktop PCs and Servers
- High-Power Supply for Lighting
- AC/DC Adapters, Open-Frame SMPS
- Video Game Consoles

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP44018-AGS	SOIC-8	*See Below*	2

*For Tape & Reel, add suffix –Z (e.g. MP44018-AGS–Z).

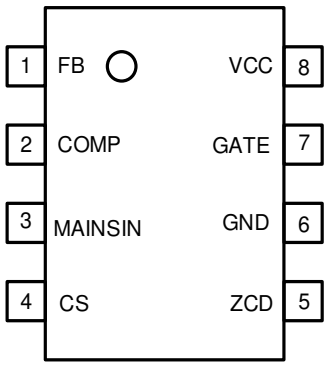
TOP MARKING

M44018-A
LLLLLLLL
MPSYWW

M44018-A: Part number
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

PACKAGE REFERENCE

TOP VIEW



SOIC-8

PIN FUNCTIONS

Pin #	Name	Description
1	FB	**Output voltage sense.** This pin senses the output voltage through a resistor divider, and compares the sensed voltage to the reference voltage (V_R) (typically 2.5V). This allows the output voltage to be regulated. FB also integrates under-voltage protection (UVP) and over-voltage protection (OVP), described below: UVP: Pull the FB pin below 0.36V for a blanking time (t_{BL_UVP}) of 55µs to shut down the IC, or pull COMP down for the IC to enter low-supply current mode. OVP: If FB exceeds V_{FB_OVP} (typically 2.7V) for a blanking time (t_{BL_OVP}) of 22µs, the IC stops switching. It resumes switching when FB drops back to 2.62V.
2	COMP	**Error amplifier output.** The compensation network is connected between this pin and GND. If the internal COMP voltage (V_{COMPI}) drops below V_{COMPI_BOFF} (typically 60mV), switching stops are five soft-off pulses. As V_{COMPI} ramps up to V_{COMPI_BON} (typically 120mV), switching resumes after five soft-on pulses.
3	MAINSIN	**Mains voltage sense.** MAINSIN is connected to the AC with a two-diode rectifier, or connected just after the rectifier bridge. The rectifier voltage is scaled down by a resistor divider to MAINSIN. The voltage on MAINSIN provides brown-in and brownout functions, and provides feed-forward compensation for the COMP voltage. If MAINSIN's peak voltage exceeds V_{MAINS_BI} (typically 1V), the device starts to switch with COMP soft start-up. If MAINSIN's peak voltage remains below V_{MAINS_BO} (typically 0.9V) for t_{BO} (typically 50ms), a brownout condition is confirmed. The PFC stops switching, and COMP is pulled down to zero.
4	CS	**Current sense.** The CS pin provides monitoring for over-current protection (OCP) and over-current limiting (OCL). A lead-edge blanking time ensures that the CS pin does not mistrigger OCP or OCL. OCL: If CS exceeds V_{OCL} (typically 0.5V) with an LEB time (t_{OCL_LEB}) of 300ns, the IC stops switching. OCL is cycle-by- cycle current limited. OCP: If the CS voltage exceeds V_{OCP} (typically 0.75V) in two consecutive 180µs restart switching cycles, the OCP flag is triggered, and the IC stops switching. OCP is reset by an auto-recovery timer (t_{OCP_R}) of 80ms, or by a brown-in, brownout, or VCC under-voltage lockout (UVLO) event.
5	ZCD	**Zero-current detection through auxiliary winding.** A leading-edge blanking time (t_{ZCD_LEB}) of 0.3µs is inserted to filter out the noise ringing on ZCD after the gate turns off. The positive voltage on ZCD must exceed V_{ZCD_H} (typically 0.75V), then drop below V_{ZCD_L} (typically 0.25V) for the next stoke. The valley switch must wait for the end of the minimum period limitation time or dead time extension control. The restart timer generates a signal to turn on the MOSFET when ZCD is not detected for t_{ZCD_TO} (typically 180µs) after it switches off.
6	GND	**Ground.**
7	GATE	**Gate driver output.** The high output current of the gate driver can drive the low-cost power MOSFET. If GATE is supplied with a high V_{CC}, the high-level voltage of GATE is clamped to 13V.
8	VCC	**Supply voltage.** VCC supplies power to the IC's signal path and the gate driver. Connect a bypass capacitor from VCC to ground to reduce noise.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{CC}) ..... -0.3V to +35V
FB, COMP, MAINSIN, CS..... -0.3V to +6V
GATE..... -0.3V to +14V
ZCD ..... -0.5V to +8V
ZCD current ..... -10mA to +10mA
Continuous power dissipation (T_A = 25°C) (2)
SOIC-8 .....1.4W
Junction temperature..... 150°C
Lead temperature (solder) .....260°C
Storage temperature.....-55°C to +150°C

ESD Ratings

Human body model (HBM) .....±2kV
Charged device model (CDM)..... ±2kV

Recommended Operating Conditions (3)

Supply voltage (V_{CC})..... 12V to 32V
MAINSIN..... 0V to 4V
Maximum junction temp (T_J) .....125°C

Thermal Resistance (4)	θ_{JA}	θ_{JC}	
SOIC-8	90	45	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS (5)

V_{CC} = 20V, T_A = T_J= -40°C to +125°C, min and max values are guaranteed by characterization. Typical values are tested under 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage (VCC)						
Turn-on threshold	V_{CC_ON}		10.2	10.7	11.2	V
Turn-off threshold	V_{CC_OFF}		8.1	8.5	9.1	V
Hysteresis	V_{CC_HYS}		1.8	2.1	2.4	V
Supply Current						
Start-up current	$I_{STARTUP}$	V_{CC} = 9.5V		25	40	µA
Quiescent current	I_Q	No switch		0.18	0.25	mA
Operating current	I_{CC}	f_{SW} = 70kHz, C_{LOAD} = 1nF		2.1	3	mA
Mains Voltage Sensing (MAINSIN)						
Brown-in voltage	V_{MAINS_BI}		0.95	1	1.05	V
Brownout voltage	V_{MAINS_BO}		0.85	0.9	0.95	V
Brownout comparator hysteresis	$V_{BO(HYS)}$		0.05	0.1	0.14	V
Brownout timer	t_{BO}			50		ms
Protection current for MAINSIN open	$I_{MAINSIN\_BIAS}$			20		nA
Error Amplifier						
Reference voltage	V_R		2.463	2.5	2.538	V
Transconductance	G_{M1}	V_{FB} = 2.45V	80	105	125	uS
	G_{M2}	V_{FB} = 2.2V to 2.3V	160	280	400	uS
	G_{M3}	V_{FB} = 2.65V to 2.75V	660	780	940	uS
Source current	$I_{SOURCE1(COMP)}$	V_{FB} = V_R - 0.3V	40	70	100	µA
	$I_{SOURCE2(COMP)}$	V_{FB} = V_R - 0.05V	3	5	7	µA
Sink current	$I_{SINK1(COMP)}$	V_{FB} = V_R + 0.05V	-2.5	-4.5	-6.5	µA
	$I_{SINK2(COMP)}$	V_{FB} = V_R + 0.15V	-25	-50	-75	µA
Feedback Inverter Pin (FB)						
UVP stop threshold	V_{FB_UVP}		0.35	0.4	0.45	V
UVP hysteresis	$V_{FB\_UVP\_HYS}$			0.04		V
UVP blanking time	t_{BL_UVP}		35	55	75	µs
FB start G_{M3} (5)	V_{FB_SGM3}		2.56	2.6	2.64	V
FB start G_{M2} (5)	V_{FB_SGM2}		2.36	2.4	2.44	V
OVP trigger threshold	V_{FB_OVP}		2.66	2.7	2.73	V
OVP hysteresis	$V_{FB\_OVP\_HYS}$			0.08		V
OVP blanking time	t_{BL_OVP}		15	22	32	µs
Protection current for FB open	I_{FB_BIAS}	V_{FB} = 2V		20		nA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{CC} = 20V, T_A = T_J = -40°C to +125°C, min and max values are guaranteed by characterization, typical values are tested under 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Current Sense (CS)						
Protection current for CS open	I_{CS_BIAS}			-220		nA
Over-current limit threshold	V_{OCL}		460	500	530	mV
LEB time for OCL	t_{OCL_LEB}			300		ns
Driver delay time	t_{CS_DELAY}			100		ns
Over-current protection threshold	V_{OCP}		600	750	1000	mV
Voltage difference between OCP and OCL	V_{OCP_OCL}		100	200	500	mV
LEB time for OCP	t_{OCP_LEB}			250		ns
OCP recovery time	t_{OCP_R}			80		ms
Zero-Current Detection (ZCD)						
Protection current for ZCD open	I_{ZCD_BIAS}			5		nA
Upper clamp voltage	V_{ZCD_CLAMP}	I_{ZCD} = 3mA	7.2	7.8		V
Zero-current sensing threshold	V_{ZCD_H}	V_{ZCD} rising	0.6	0.75	0.9	V
	V_{ZCD_L}	V_{ZCD} falling	0.2	0.25	0.3	V
Turn-on delay after ZCD detected	t_{ZCD_DELAY}			150		ns
ZCD timer-out time	t_{ZCD_TO}		130	180	250	µs
ZCD leading-edge blanking time (5)	t_{ZCD_LEB}			0.3		µs
Minimum off time	t_{OFF_MINI}		1	1.4	1.9	µs
Error Amplifier Output (COMP)						
Comp voltage at max on time (5)	V_{COMP_H}			3.8		V
Comp voltage at zero on time (5)	V_{COMP_L}			0.8		V
Internal COMP voltage transient CrM to DCM (5)	V_{COMPI_C2D}			0.38		V
Internal COMP voltage to enter burst off (6)	V_{COMPI_BOFF}		30	60	90	mV
Internal COMP voltage to enter burst on	V_{COMPI_BON}		95	120	150	mV
Burst hysteresis	V_{BURST_HYS}		30	60	95	mV
Soft-off burst pulses counter (5)	$N_{SOFTOFF}$			5		
Soft-on burst pulses counter (5)	N_{SOFTON}			5		
Maximum dead time	t_{DEAD_MAX}		19	22	29	µs

ELECTRICAL CHARACTERISTICS *(continued)*

V_{CC} = 20V, T_A = T_J = -40°C to +125°C, min and max values are guaranteed by characterization, typical values are tested under 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Mains Compensation						
On time	t_{ON_LL}	VCOMP = 3.8V, MAINSIN = 1.0V	20	24	29	µs
	t_{ON_HL}	VCOMP = 3.8V, MAINSIN = 3.38V	1.6	2.1	2.8	µs
Gate Driver (GATE)						
Drop voltage	R_{OH}	$I_{GDSOURCE}$ = 20mA		10	16	Ω
	R_{OL}	I_{GDSINK} = 20mA		2.5	6	Ω
Voltage falling time	t_F			20		ns
Voltage rising time	t_R			120		ns
Max output drive voltage	V_{GATE_MAX}		11.5	13	15	V
Source current capability (5)	I_{GATE_SOURCE}			-600		mA
Sink current capability (5)	I_{GATE_SINK}			1		A
UVLO saturation voltage	$V_{SATURATION}$	V_{CC} = 0V to V_{CC_ON}, I_{GATE_SINK} = 10mA			1.5	V
Internal OTP						
OTP trig level (5)	T_{OTP}			150		°C
OTP hysteresis (5)	T_{OTP_HYS}			40		°C

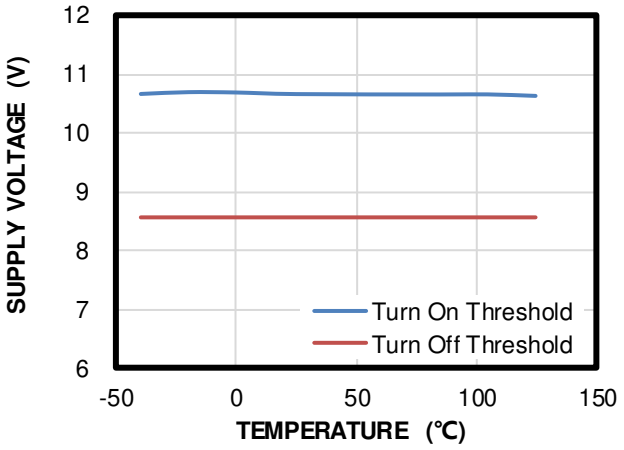
Notes:

5) Guaranteed by design.
6) V_{COMPI} = (V_{COMP} - V_{COMP_L}) / 3

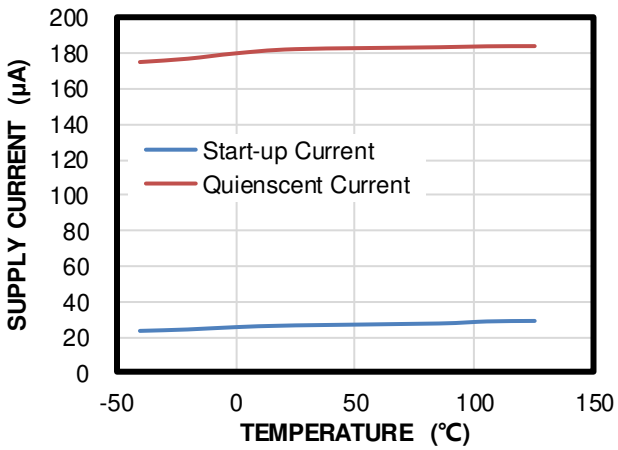
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 85V_{AC} to 265V_{AC}, V_{OUT} = 400V, T_A = 25°C, unless otherwise noted.

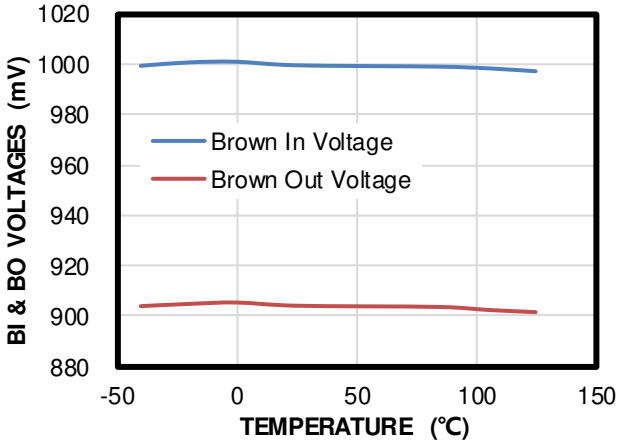
Supply Voltage vs. T_J



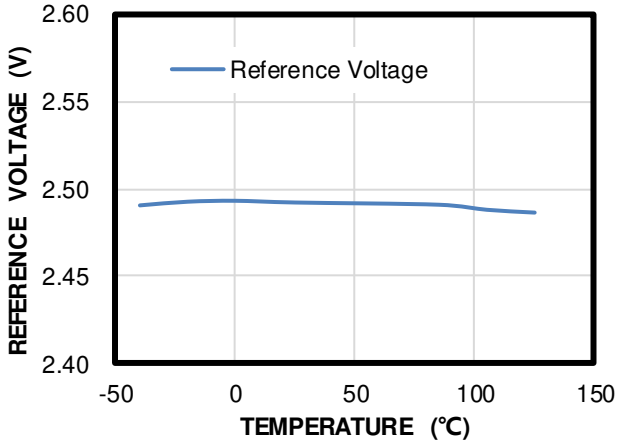
Supply Current vs. T_J



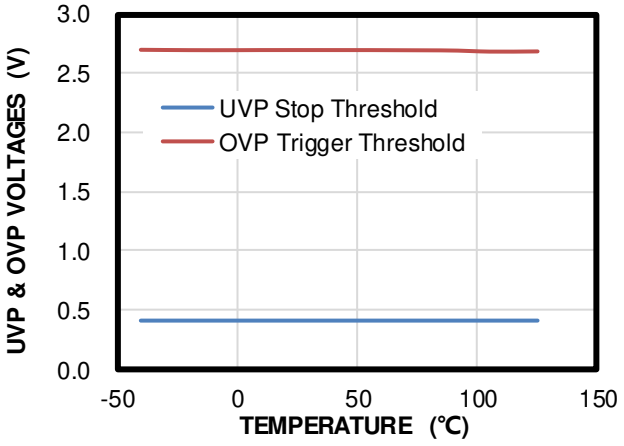
Brown-In and Brownout Voltages vs. T_J



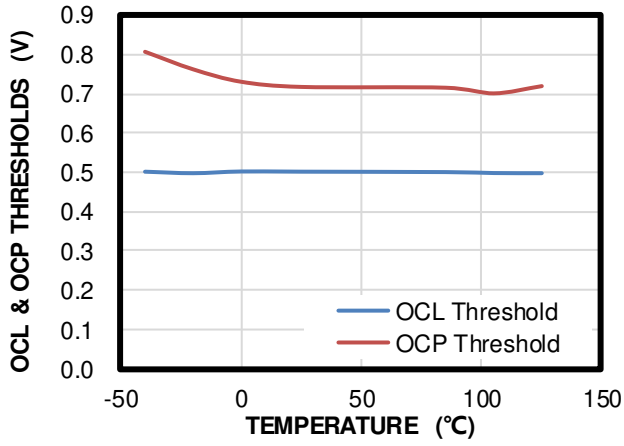
Reference Voltage vs. T_J



UVP and OVP Voltages vs. T_J



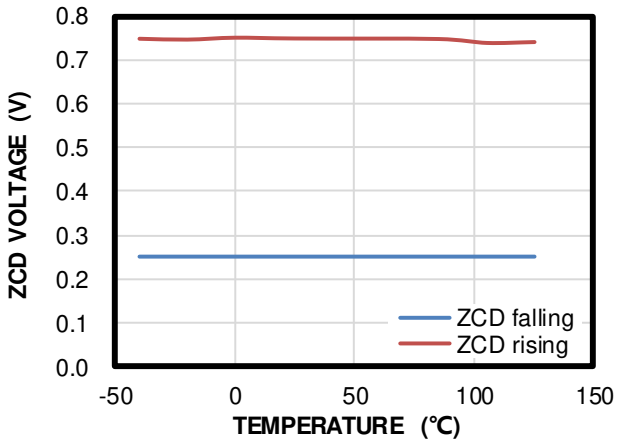
OCL and OCP Thresholds vs. T_J



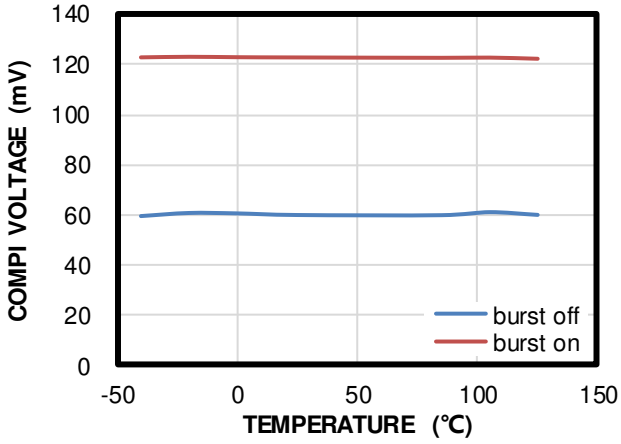
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 85V_{AC} to 265V_{AC}, V_{OUT} = 400V, T_A = 25°C, unless otherwise noted.

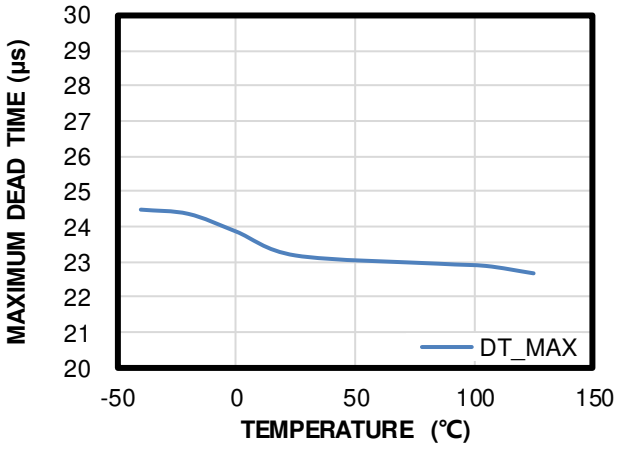
Zero-Current Detection Threshold vs. T_J



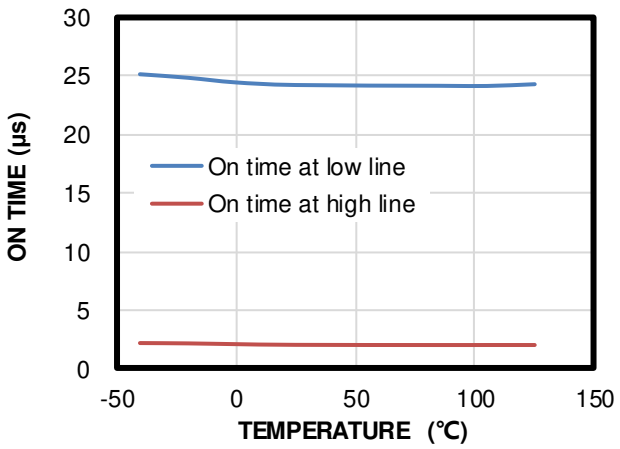
COMPI Voltage to Enter Burst On and Off vs. T_J



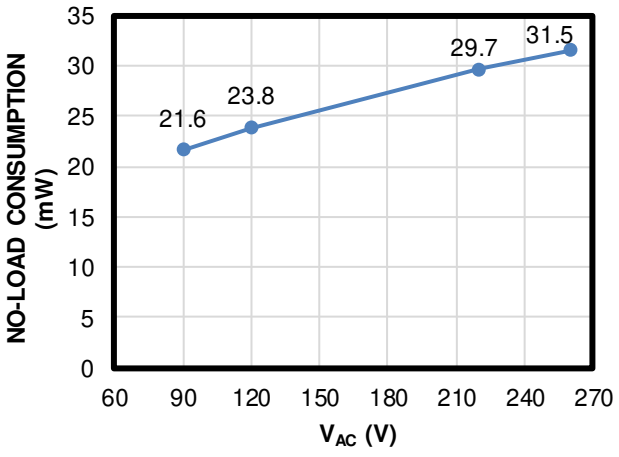
Maximum Dead Time vs. T_J



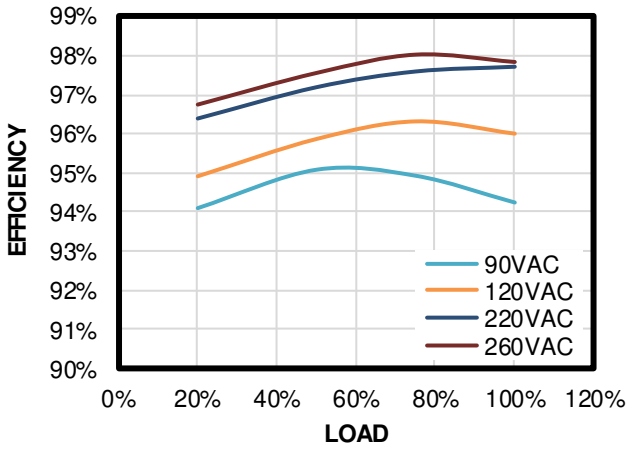
On Time at Low and High Line vs. T_J



No-Load Consumption



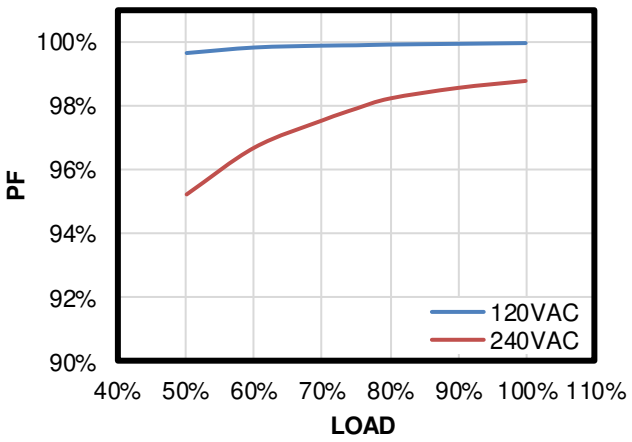
Efficiency



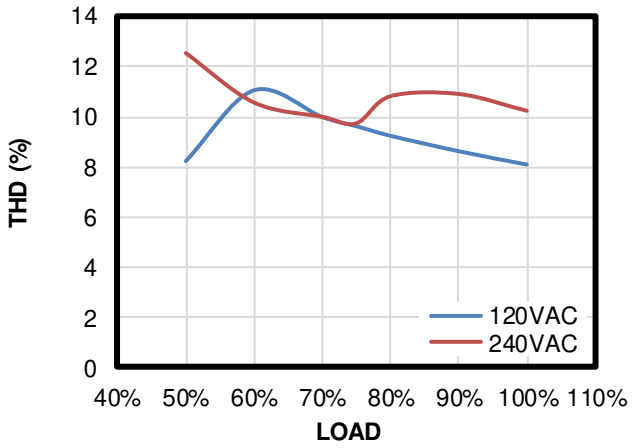
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 85V_{AC} to 265V_{AC}, V_{OUT} = 400V, T_A = 25°C, unless otherwise noted.

Power Factor

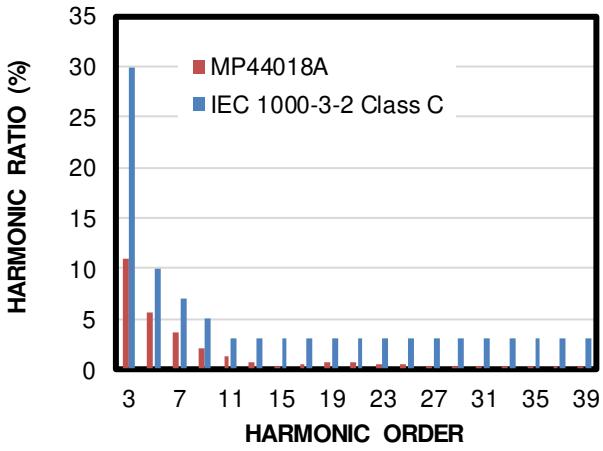


THD



Harmonics

V_{IN} = 230V_{AC}, P_{OUT} = 240W

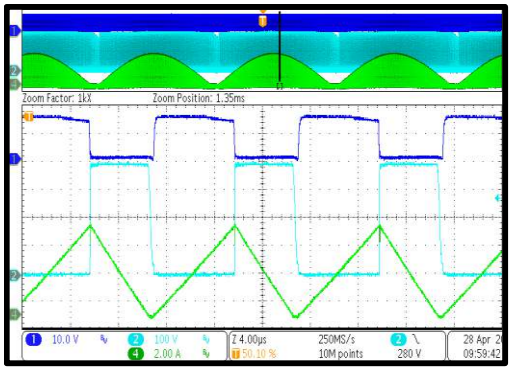


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 85V_{AC} to 265V_{AC}, V_{OUT} = 400V, T_A = 25°C, unless otherwise noted.

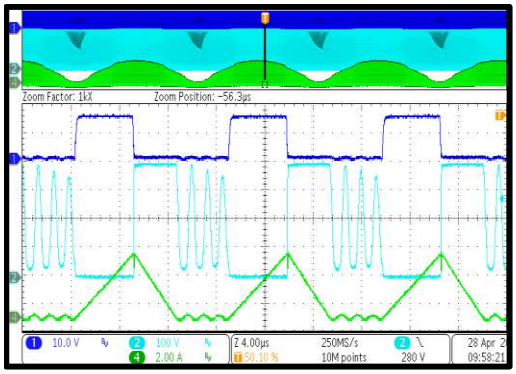
Steady State

V_{IN} = 120V_{AC}, P_{OUT} = 240W



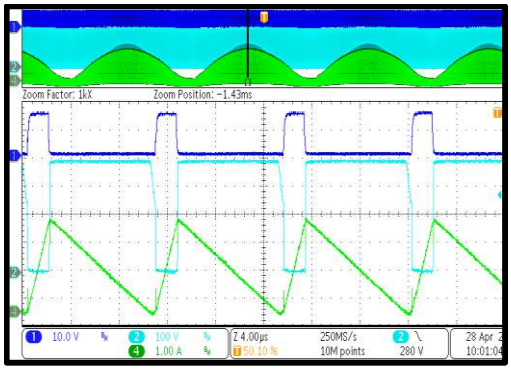
Steady State

V_{IN} = 120V_{AC}, P_{OUT} = 120W



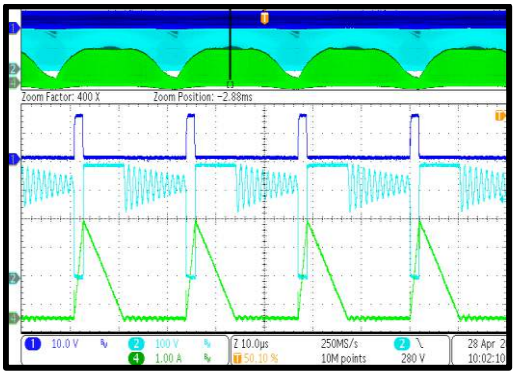
Steady State

V_{IN} = 230V_{AC}, P_{OUT} = 240W



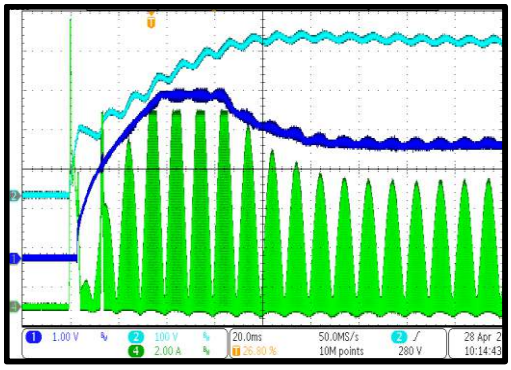
Steady State

V_{IN} = 230V_{AC}, P_{OUT} = 120W



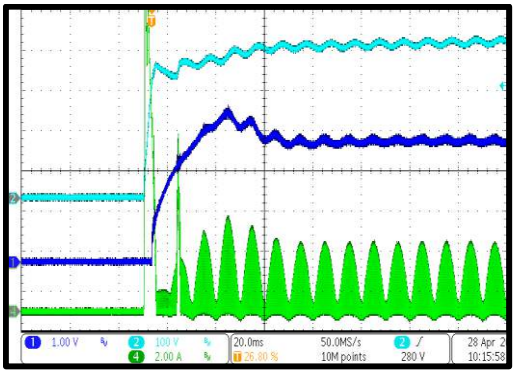
Start-Up

V_{IN} = 120V_{AC}, P_{OUT} = 240W



Start-Up

V_{IN} = 230V_{AC}, P_{OUT} = 240W

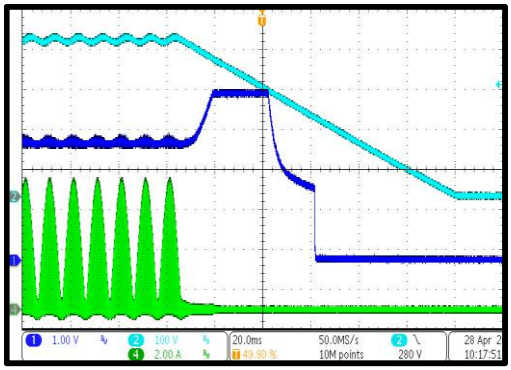


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 85V_{AC} to 265V_{AC}, V_{OUT} = 400V, T_A = 25°C, unless otherwise noted.

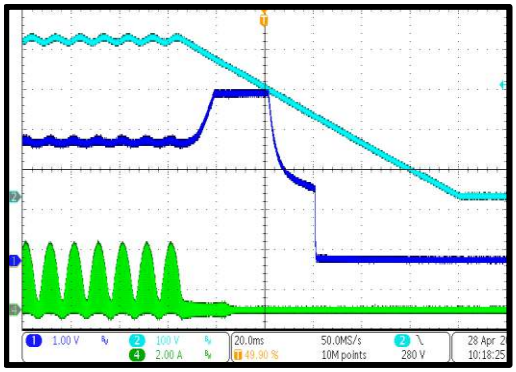
Shutdown

V_{IN} = 120V_{AC}, P_{OUT} = 240W



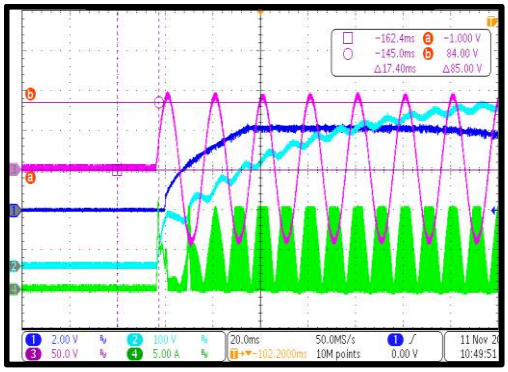
Shutdown

V_{IN} = 230V_{AC}, P_{OUT} = 240W



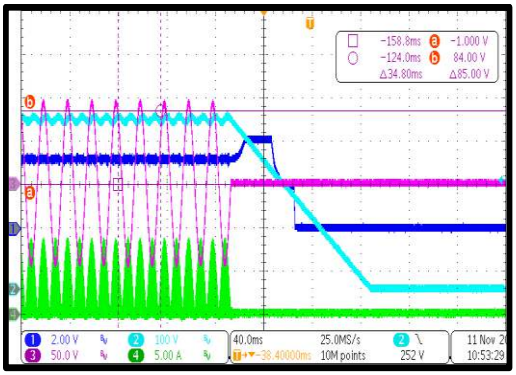
Brown-In

P_{OUT} = 240W



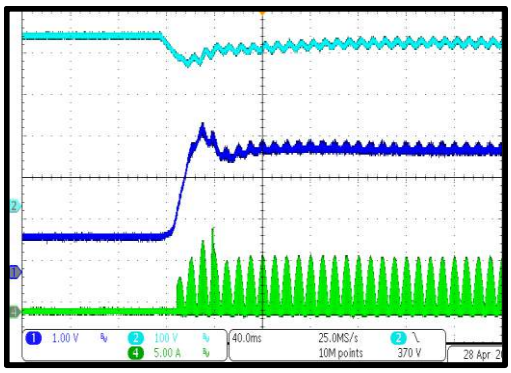
Brownout

P_{OUT} = 240W



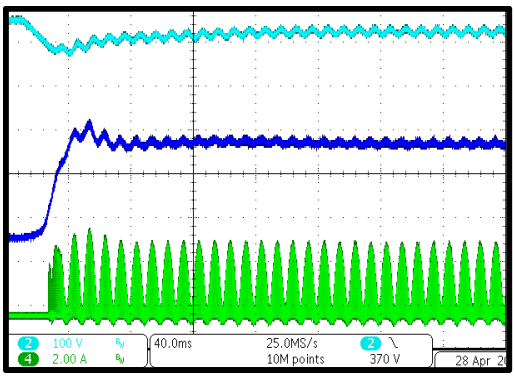
Load Transient

V_{IN} = 120V_{AC}, 0W to 240W



Load Transient

V_{IN} = 230V_{AC}, 0W to 240W



FUNCTIONAL BLOCK DIAGRAM

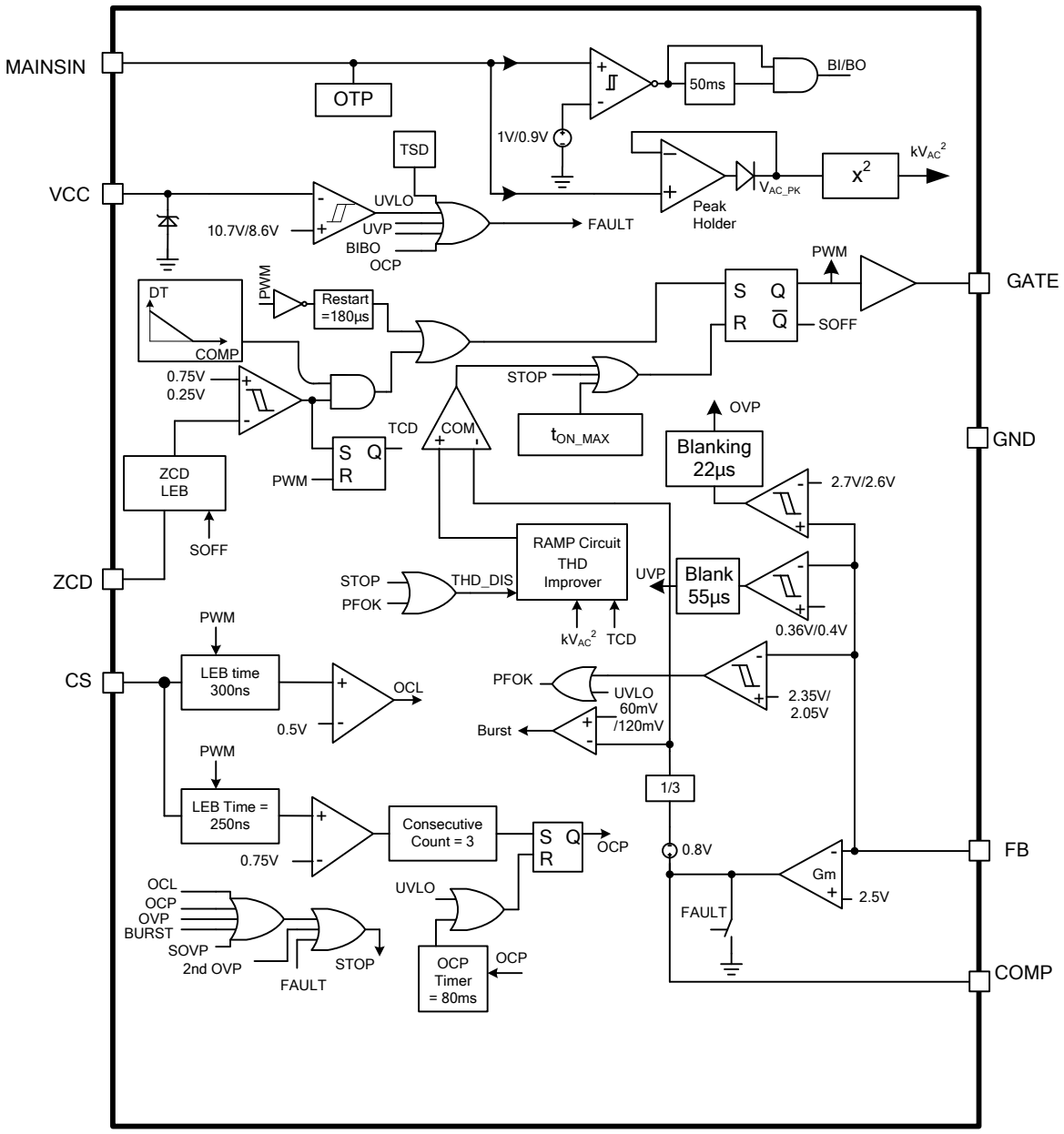


Figure 1: Functional Block Diagram

OPERATION

The MP44018A is designed to provide simple, high-performance active power factor correction (PFC) using minimal external components. CrM/DCM multi-mode allows the MP44018A to operate in transition mode at heavy load. Multi-mode allows the device to then convert seamlessly into discontinuous conduction mode (DCM) at light loads, which maximizes operating efficiency.

The MP44018A features a very low supply current, which meets typical standby power requirements. The no-load power is usually below 30mW.

Start-Up and Brown-In

Figure 2 shows the typical start-up timing diagram.

As V_{CC} gradually builds up and reaches V_{CC_ON} (typically 10.7V) at time t1, the IC is enabled. Then the IC starts to sense the brown-in condition through MAINSIN. When the sampled peak voltage exceeds V_{MAINS_BI} (typically 1V), it starts to switch at time t2. The MP44018A implements a COMP soft start-up, and the bus voltage achieves its regulation voltage at t3.

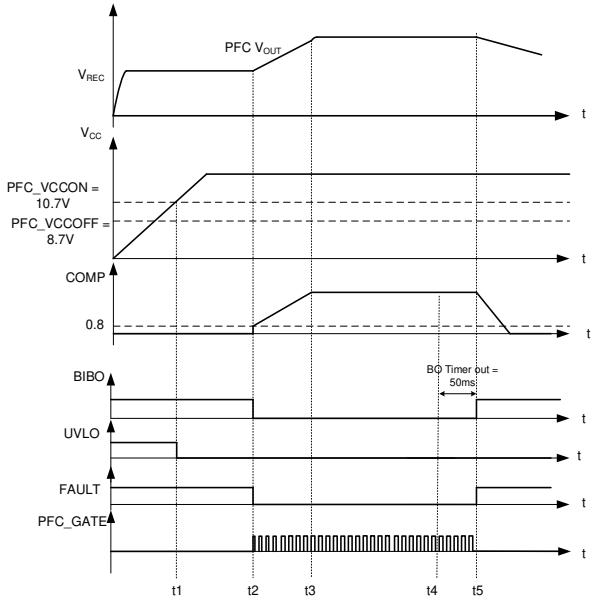


Figure 2: Start-Up and Brown-In/Brownout

Brownout Function

The AC peak voltage is continuously sensed by MAINSIN. Because the AC peak voltage falls below V_{MAINS_BO} (typically 0.9V) at t4, the device continues switching until the brownout timer (typically 50ms) ends at t5. Then the IC confirms the brownout condition.

At this point, the PFC stops switching and COMP is pulled down to zero. The device restarts with a COMP soft start if the peak MAINSIN voltage exceeds V_{MAINS_BI} (typically 1V).

Enhanced Dynamic Response

The boost PFC output voltage is sensed on FB, and is compared with the internal reference V_R (typically 2.5V) (see Figure 13 on page 19). R_{O1} is recommended to be 10MΩ to minimize power consumption. R_{O2} can be calculated with Equation (1):

$$R_{O2} = \frac{R_{O1} \times V_R}{V_O - V_R} \quad (1)$$

The voltage compensation tank is connected from COMP to GND. Proportional integral (PI) control with a high-frequency pole is typically used for compensation.

Figure 3 shows a nonlinear G_M, which achieves both good loop regulation in steady state and enhanced dynamic response during load transient. If the output voltage is detected with an undershoot of 4%, the gain increases to four times the normal gain. A higher gain can pull up COMP quickly and reduce the voltage drop during load step.

If the output voltage is above or below the normal voltage with an overshoot of 4%, the gain increases to eight times the normal gain. This ensures that COMP is quickly pulled down to avoid triggering over-voltage protection (OVP).

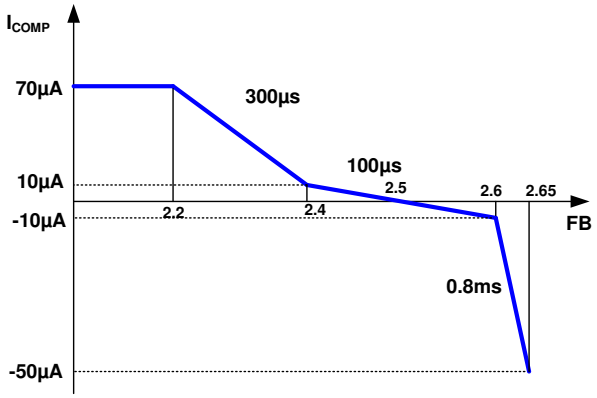


Figure 3: Nonlinear G_M

Valley Switching

To minimize the switching loss, the MP44018A always achieves valley switching through zero-current detection (ZCD) under any condition, regardless of whether the device is operating in DCM or critical conduction mode (CrM). Figure 4 shows the internal functional block and its peripheral circuitry.

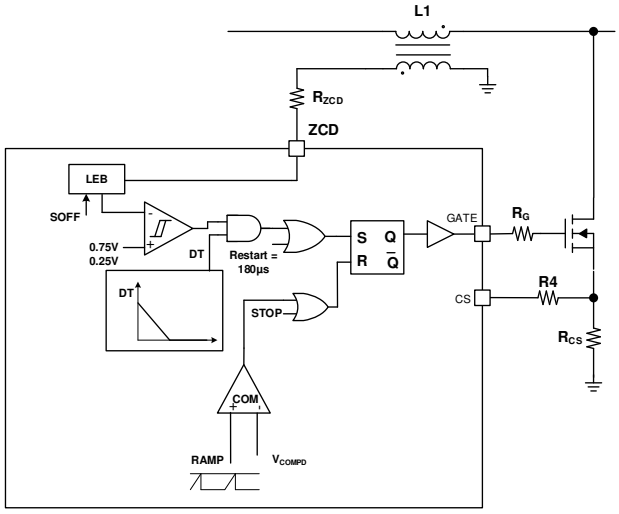


Figure 4: ZCD Functional Block

A leading-edge blanking time (t_{ZCD_LEB}) of about 0.3µs is inserted to filter out the noise on ZCD right after the gate turns off.

The positive voltage on ZCD must exceed V_{ZCD_H} (typically 0.75V), then drop below V_{ZCD_L} (typically 0.25V) for the next trigger condition. In addition to waiting for a ZCD trigger condition, the actual turn-on action should wait for the end of the dead time extension (DTE) signal (see the Frequency Reduction Function section below). As soon as the DTE signal ends and the ZCD trigger condition is fulfilled, the controller switches on the MOSFET after a delay time (t_{ZCD_DELAY}) of 150ns at the minimum drain source voltage (see Figure 5).

The turn ratio of the auxiliary winding is determined by a sufficient positive voltage, estimated with Equation (2):

$$n < \frac{V_O - \sqrt{2}V_{AC}}{0.75} \quad (2)$$

Where V_{AC} is the maximum RMS input voltage.

R_{ZCD} can be calculated with Equation (3):

$$R_{ZCD} > \frac{V_O}{N \times I_{ZCD\_MAX}} \quad (3)$$

A restart timer (t_{ZCD_TO}) of 180µs generates a signal to turn on the MOSFET after it switches off. This also allows the MOSFET to turn on during the start-up period, since no valley signal can be detected on ZCD.

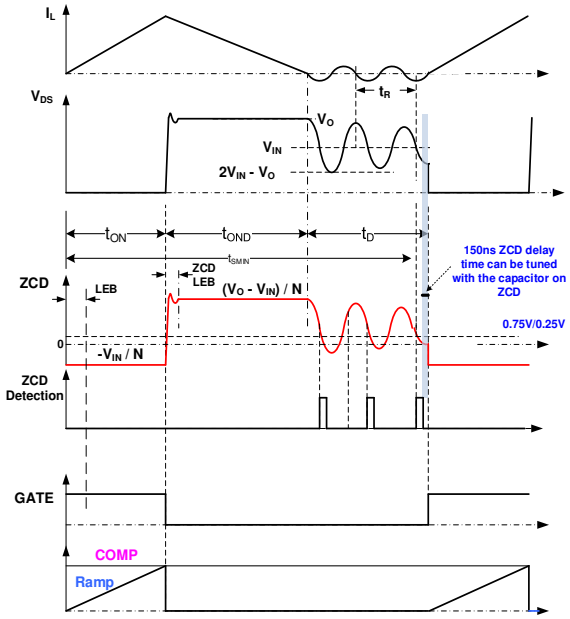


Figure 5: ZCD Timing Diagram

Frequency Reduction Function

The MP44018A reduces the switching frequency with DTE technology under light loads. The MP44018A works in CrM under heavy loads. In CrM, the PFC's frequency increases as the load reduces, which means the switching loss becomes dominant. The MP44018A gradually inserts a dead time (t_D) as the load becomes lighter.

Figure 6 shows how the dead time is extended when the COMP voltage drops.

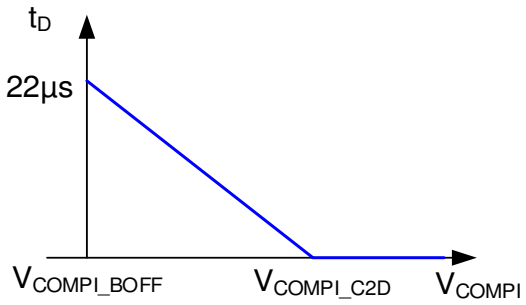


Figure 6: Dead Time Extension

The maximum dead time (t_{DEAD_MAX}) is 23µs, when COMP reaches its minimum voltage and linearly reaches zero as the internal COMP (V_{COMPI}) approaches the threshold V_{COMP_C2D} (typically 0.38V).

With this control scheme, the system alternates between CrM and DCM smoothly as the load is gradually reduced. This means the switching frequency is automatically reduced for maximum efficiency as shown in figure 7 and figure 8.

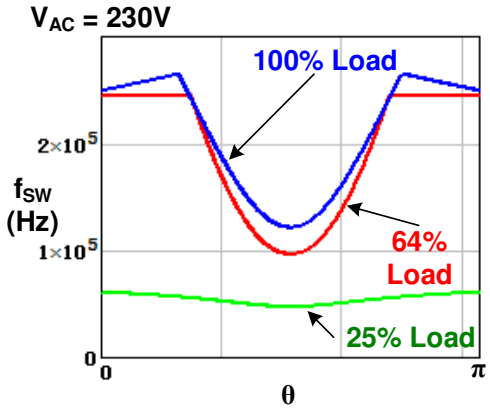


Figure 7: Switching Frequency in a Line Cycle

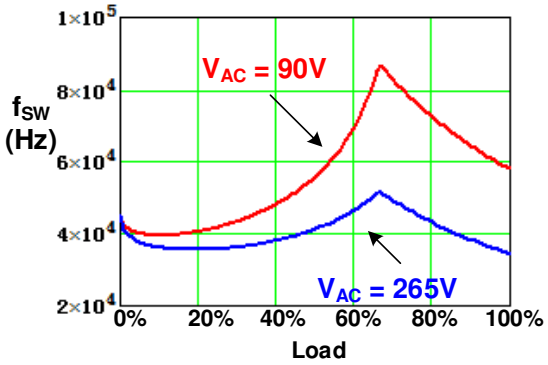


Figure 8: Switching Frequency vs. Load

Burst Mode Operation

Figure 9 shows a burst mode control diagram.

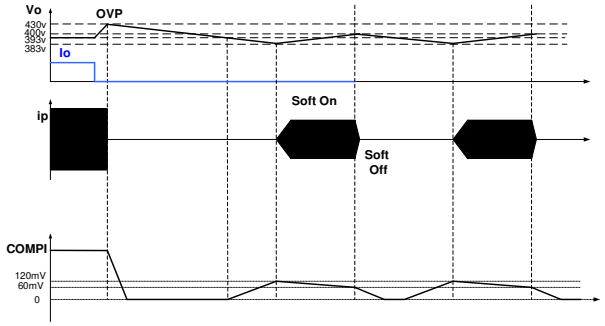


Figure 9: Burst Mode Control

Based on how the COMP voltage indicates load information, the controller enters DCM. It enters burst mode at certain loads to improve light-load efficiency and standby power loss. As the load decreases, COMP gradually drops. When V_{COMPI} drops below V_{COMPI_BOFF} (typically 60mV), switching stops with five soft-off pulses. As V_{COMPI} ramps up to V_{COMPI_BON} (typically 120mV), switching resumes with five soft-on pulses. This soft-on/off control avoids abrupt inductor current changes, and attenuates the acoustic noise accordingly.

During the burst-off period, the IC shuts down most of internal block and ensures that the supply current is below I_Q (typically 180µA).

Improved THD

Under heavy loads, the MP44018A works in CrM. The average input current in one cycle can be estimated with Equation (4):

$$I_{IN}(\theta) = \frac{v_{AC}(\theta)}{2L} \times t_{ON}(\theta) = \frac{v_{AC}(\theta)}{R_{EQ1}} \quad (4)$$

Where V_{AC} is the RMS of the line voltage, calculated with Equation (5):

$$v_{AC}(\theta) = \sqrt{2} V_{AC} \sin(\theta) \quad (5)$$

And R_{EQ1} is the equivalent input resistor, which can be can be calculated with Equation (6):

$$R_{EQ1} = \frac{2L}{t_{ON}(\theta)} \quad (6)$$

Where t_{ON} (θ) is the on time.

Since t_{ON} (θ) is generated by an internal ramp current compared to the COMP voltage, t_{ON} (θ) stays constant in one AC line cycle. R_{EQ} behaves like a resistant load. This means the input average current is proportional to V_{AC} (θ).

Along with reducing the load, the MP44018A gradually works from CrM to DCM to reduce the switching loss in light-load.

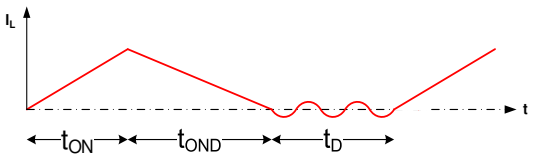


Figure 10: DCM Operation

The average input current in one cycle can be estimated with Equation (7):

$$I_{IN}(\theta)=\frac{v_{AC}(\theta)}{2L}\times t_{ON}(\theta)\times D_C(\theta)=\frac{v_{AC}(\theta)}{R_{EQ2}} \quad (7)$$

Where R_{EQ2} can be estimated with Equation (8):

$$R_{EQ2}=\frac{2L}{t_{ON}(\theta)\times D_C(\theta)} \quad (8)$$

And D_C can be estimated with Equation (9):

$$D_C(\theta)=\frac{t_{ON}+t_{OND}}{t_{ON}+t_{OND}+t_D} \quad (9)$$

A dedicated variable-on-time control circuit is integrated, and t_{ON} can be calculated with Equation (10):

$$t_{ON}(\theta)=\frac{\varepsilon}{D_C(\theta)} \quad (10)$$

Where ε is a constant defined by the internal parameters. R_{EQ2} can also be calculated with Equation (11):

$$R_{EQ2}=\frac{2L}{\varepsilon} \quad (11)$$

R_{EQ2} also behaves like a resistant load, and the input average current is proportional to V_{AC} (θ).

Mains Compensation

The input power for the boost PFC converter can be estimated with Equation (12):

$$P_{IN}=\frac{V_{AC}^{\ 2}}{2L}\times t_{ON} \quad (12)$$

This means the AC transient response is suboptimal due to the square of the mains input voltage.

The COMP voltage (V_{COMP}) can be estimated with Equation (13):

$$V_{COMP}\sim\frac{1}{V_{AC}^{\ 2}} \quad (13)$$

V_{COMP} varies between low-line and high-line. For general design, the burst mode load is determined by V_{COMP}. In high-line, the converter easily enters burst mode in heavy load condition. The audible noise comes out accordingly.

To compensate for the mains input voltage influence, the MP44018A contains a square of V_{AC} compensation circuits. The AC peak voltage is sensed at MAINSIN, and is fed to the generation of internal ramp current.

The internal COMP voltage can be estimated with Equation (14):

$$V_{COMPI}=4\times L\times P_{IN}\frac{K_{MAIN}^{\ 2}}{K_{RAMP}} \quad (14)$$

Where K_{MAIN} is the voltage divider ratio of MAINSIN, and K_{RAMP} is equal to t_{ON_LL} (typically 24μs/V).

Figure 11 shows t_{ON}.

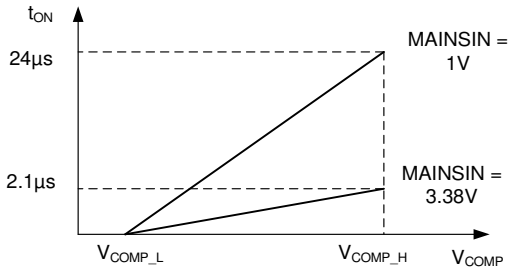


Figure 11: t_{ON} vs. COMP

Over-Current Limit (OCL)

Figure 12 shows the block diagram of over-current limit (OCL) and over-current protection (OCP). The current is sensed by the CS pin. It can limit the current cycle by cycle when CS exceeds V_{OCL} (0.5V). An LEB time (t_{OCL_LEB}) of 300ns is applied during OCL to avoid mistriggering the OCL due to a spike current raised by discharging the drain-source capacitor of the MOSFET.

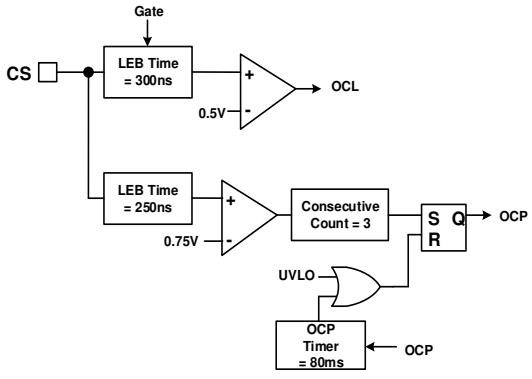


Figure 12: OCL and OCP

Over-Current Protection (OCP)

A second OCP is also integrated in CS with a shorter LEB time (t_{OCP_LEB}) of 250ns. If the CS voltage exceeds V_{OCP} (typically 0.75V) in two consecutive 180µs restart switching cycles, the OCP flag is triggered and the IC stops switching. OCP is reset by an auto-recovery timer (t_{OCP_R}) of 80ms, or brown-in, brownout, or V_{CC} UVLO. OCP only protects from big faults, such as an inductor short or a bypass diode short.

Under-Voltage Protection (UVP) and Over-Voltage Protection (OVP)

The scaled-down voltage is connected to FB, which is the input of the under-voltage protection (UVP) and over-voltage protection (OVP) comparators, as well as the error amplifier.

Figure 13 shows that if the FB voltage exceeds the OVP trigger threshold (typically 2.7V), the OVP comparator shuts down the output of the gate drive circuit after a blanking time (t_{BL_OVP}) of 22µs. Switching resumes when FB drops to 2.62V.

The UVP comparator shuts down operation if FB drops below 0.36V for a blanking time (t_{BL_UVP}) of 55µs. The UVP comparator's hysteresis is 40mV. COMP is discharged to zero, and the device's supply current is reduced to a minimum when UVP is triggered.

The UVP function can disable switching when FB is open, or the FB feedback loop is open.

The UVP and OVP comparators value are set as below:

- OVP: 108% of V_R. Normal operation resumes at 104% of V_R.
- UVP: 12% of V_R. Normal operation resumes at 16% of V_R.

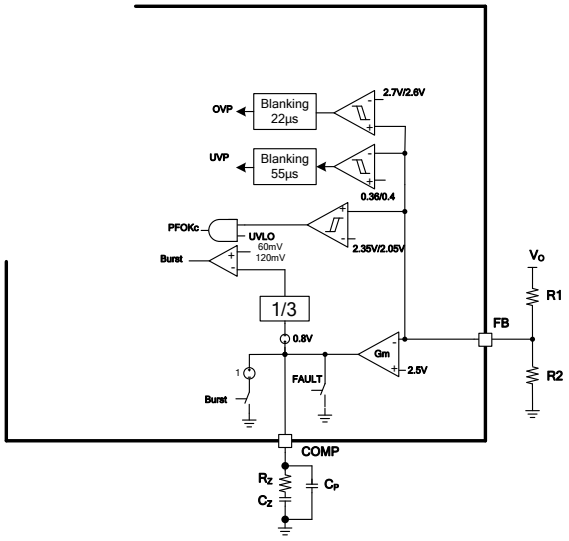


Figure 13: FB Function Block

Gate Driver

The IC includes a push-pull gate driver that can directly drive the MOSFET. The peak source current is 600mA, and the peak sink current capability is 1A.

APPLICATION INFORMATION

Design Requirements

Table 1 lists recommended design requirements.

Table 1: Recommended Designs

Parameter	Symbol	Value
Input AC RMS voltage	V_{AC}	85V_{AC} to 265V_{AC}
Input AC voltage frequency	f_{LINE}	47Hz to 63Hz
Output voltage	V_O	400V
Output voltage ripple	V_{O_RIPPLE}	⩽3% V_O
Output voltage OVP threshold	ΔOVP	40V
Output power	P_O	240W
Efficiency	η	⩾93%

Power Stage Design

Selecting the Bridge

The diode bridge should withstand the maximum reverse input AC voltage and the maximum input current. When selecting a diode bridge, consider the maximum instantaneous voltage (the peak voltage of the line voltage), and the maximum input RMS current (the input RMS current at low-line). In addition, package size and thermal performance should also be considered. To handle the line frequency current, use a standard low-cost diode bridge with slow recovery.

In this case, the maximum input RMS current can be calculated with Equation (15):

$$I_{AC\_MAX} = \frac{P_O}{\eta_{MIN} \times V_{AC\_MIN}} = 3.04(A) \quad (15)$$

The maximum instantaneous voltage can be estimated with Equation (16):

$$V_{IN\_MAX} = \sqrt{2} \times V_{AC\_MAX} = 375(V) \quad (16)$$

A standard 600V/8A bridge can be selected to provide enough margin.

Selecting the Input Capacitor

The input capacitor before the boost inductor is used to provide a bypass path for the high switching frequency current, and to minimize fluctuation on the rectified sinusoidal input voltage. In general, a voltage drop up to 10% on the input capacitor may be expected. The worst-case scenario occurs when the input voltage is below its minimum threshold voltage due to a large current ripple.

The input capacitor (C_{IN}) can be calculated with Equation (17):

$$C_{IN} = \frac{I_{AC\_MAX}}{2\pi \times f_{SW} \times r \times V_{AC\_MIN}} \quad (17)$$

Where *r* is the coefficient (0.01 to 0.1), and f_{SW} is the switching frequency at the peak of the minimum input AC voltage.

Select a capacitor with good high-frequency performance, such as a film capacitor. Assume a minimum f_{SW} (e.g. 40kHz) and set coefficient *r* to be 0.05. The input capacitance can be calculated with Equation (18):

$$C_{IN} = \frac{I_{AC\_MAX}}{2\pi \times f_{SW} \times r \times V_{AC\_MIN}} = 2.85\mu F \quad (18)$$

Two 1μF film capacitors with a 450V voltage rating are recommended as the input capacitors because they provide high-frequency energy during the switching cycle.

Boost Inductor Design

The boost inductance value (L_{MAX}), which is required to ensure that the maximum load can be delivered from the minimum input voltage, can be estimated with Equation (19):

$$L_{MAX} = \frac{V^2_{AC\_MIN} \times \eta \times t_{ON\_MAX}}{2 \times P_O} \quad (19)$$

The boost inductance value should be below L_{MAX}. A normal inductance is recommended to use 60%-70% ratio of L_{MAX} to avoid t_{ON} being close to t_{ON_MAX}.

If ratio is selected as 60%, the actual inductance of this case is,

$$L_{ACTUAL} = \frac{V^2_{AC\_MIN} \times \eta \times t_{ON\_MAX} \times Ratio}{2 \times P_O} = 182\mu H \quad (20)$$

The boost inductance value should exceed L_{MIN}. To avoiding triggering over-current protection (OCP) when triggering the over-current limit (OCL), there is a delay time (t_{CS_DELAY}) of 100ns, as well as a MOSFET turn-off delay.

The minimum boost inductance can be estimated with Equation (21):

$$L_{MIN} = \frac{\sqrt{2}V_{AC\_MAX} \times 300ns}{V_{OCP\_OCL}} \times R_{CS} = 37.5\mu H \quad (21)$$

Selecting the Boost MOSFET

The voltage rating of the MOSFET is determined by the output voltage, over-voltage protection (OVP) threshold, plus some margin, such that $V_{DS} > V_O + \Delta V_{OVP}$. The current rating of the MOSFET is determined by the RMS value of the current flowing through the MOSFET.

V_{DS} can be calculated with Equation (22):

$$V_{DS} > V_O + \Delta V_{OVP} = 440V \quad (22)$$

The RMS current of MOSFET can be estimated with Equation (23):

$$I_{QRMS} = 2\sqrt{2} \times I_{AC\_MAX} \times \sqrt{\frac{1}{6} - \frac{4\sqrt{2}}{9\pi} \times \frac{V_{AC\_MIN}}{V_O}} = 3A \quad (23)$$

In addition, the MOSFET pulsed-drain current should exceed the peak inductor current, calculated with Equation (24):

$$I_{D\_PULSE} > I_{LPK\_MAX} = 2\sqrt{2} \times I_{AC\_MAX} = 8.6A \quad (24)$$

Selecting the Boost Diode

The boost diode should have the same voltage rating as the boost MOSFET.

The average current of output diode is the same as the output current of PFC regulator, calculated with Equation (25):

$$I_{DAVG} = I_O = 0.6A \quad (25)$$

To estimate the power consumption of the diode, the RMS current can be calculated with Equation (26):

$$I_{DRMS} = 2\sqrt{2} \times I_{AC\_MAX} \times \sqrt{\frac{4\sqrt{2}}{9\pi} \times \frac{V_{AC\_MIN}}{V_O}} = 1.82A \quad (26)$$

The boost diode must have average and RMS current ratings that exceed I_{DAVG} and I_{DRMS}, respectively.

Diodes are available with a range of different speed/recovery charges. Fast diodes typically have higher conduction loss but lower switching loss. Slow diodes typically have lower conduction loss but higher switching loss. Maximum efficiency is achieved when the diode speed rating matches the application. In this case, a boost diode with a fast recovery is recommended.

Selecting the Output Capacitor

Consider the following when selecting an output capacitor: the output voltage ripple (V_{O_RIPPLE}), ripple current rating, and hold-up time.

The output ripple is a function of the effective series resistance (ESR) of the capacitor, the output voltage, and the line frequency (f_{LINE}). The output ripple can be estimated with Equation (27):

$$V_{O\_RIPPLE} = 2x\frac{P_O}{V_O}x\sqrt{\frac{1}{(2\pi \times 2f_{LINE}xC_O)^2} + ESR^2} \quad (27)$$

In this case, the calculated ripple with the selected capacitor should be below 3% of the output voltage, and the ESR of the output capacitor is assumed to be 1Ω. C_O can be calculated with Equation (28):

$$C_O \geq \frac{1}{2\pi x 2f_{LINE}\sqrt{\left(\frac{3\% \times V_O^2}{2xP_O}\right)^2 - ESR^2}} = 160\mu F \quad (28)$$

To ensure that the error amplifier's nonlinear gain is not activated by the extremes of the output voltage ripple, the output voltage ripple amplitude should satisfy the condition calculated with Equation (29):

$$\frac{V_{O\_RIPPLE}}{V_O} \leq \frac{2x100mV}{V_R} = 8\% \quad (29)$$

The maximum RMS ripple current flowing in the output capacitor can be estimated with Equation (30):

$$I_{O\_RIPPLE\_MAX} = \sqrt{I_{DRMS}^2 - \left(\frac{P_O}{V_O}\right)^2} = 1.72A \quad (30)$$

This current flowing into the output capacitor is made up of a switching frequency component (50Hz) and a twice line frequency ripple component (100kHz), calculated with Equation (31) and Equation (32), respectively:

$$I_{O\_RIPPLE\_50Hz} = \frac{1}{\sqrt{2}}x\frac{P_O}{V_O} = 0.424A \quad (31)$$

$$I_{O\_RIPPLE\_100KHz} = \sqrt{I_{DRMS}^2 - \frac{3}{2}x\left(\frac{P_O}{V_O}\right)^2} = 1.67A \quad (32)$$

The capacitor should be chosen so that the hold-up time satisfies the relationship calculated with Equation (33):

$$C_O = \frac{2 \cdot P_O \times t_{HOLDUP}}{\eta \times \left(V_O^2 - V_{O\_HOLDUP}^2\right)} \quad (33)$$

Where V_O is the minimum output voltage under all normal operating conditions, and V_{O_HOLDUP} is the required minimum operating output voltage to supply the downstream DC/DC converter when the line voltage is shut down. The maximum voltage at the output is a combination of the output voltage, output voltage ripple, and OVP threshold. Therefore, the voltage rating of the capacitor must be greater than this maximum output voltage at the worst case.

In this example design, an aluminum electrolytic capacitor with specification of 450V/180µF is recommended.

Control Circuit Design

The VCC Pin

If an external VCC power supply is not used, a simple approach to handling start-up is to use a start-up resistor connected to the input AC voltage. As the VCC capacitor's charge rises above the turn-on threshold through the start-up resistor, the IC begins to work.

The MP44018A needs a minimum 40µA start-up current when VCC is 9.5V. The start-up resistance can be calculated with Equation (34):

$$R_{STARTUP} \leq \frac{\sqrt{2} \times V_{AC\_MIN} - 9.5}{I_{STARTUP}} = 2.9M\Omega \quad (34)$$

Since the start-up resistor causes a voltage drop between the input AC voltage and the supply voltage of the chip, use a resistor with higher resistance to minimize the power consumption.

The FB Pin

V_O can be set by using the appropriate FB resistors. Output voltage regulation accuracy degrades with higher-value resistors due to the effect of the FB bias current. Ensure that the FB bias current degrades the output voltage regulation less than 1%, by calculating the upper voltage divider resistor value with Equation (35):

$$R_{O\_UPPER} \leq 1\% \times \frac{V_O}{I_{O\_BIAS}} = 40M\Omega \quad (35)$$

Considering the power consumption, it is recommended to use three 3.3MΩ resistors in series for the FB upper voltage divider resistor.

The lower voltage divider resistor value can be calculated with Equation (36):

$$R_{O\_LOWER} = \frac{V_R}{V_O - V_R} \times R_{O\_UPPER} = 62.3k\Omega \quad (36)$$

The MAINSIN Pin

The MAINSIN voltage range related to V_{AC} range is between 1V and 3.38V. In this case, an $85V_{AC}$ voltage can be set as the brown-in voltage. The MAINSIN voltage divider can be calculated with Equation (37):

$$\frac{R_{I\_LOWER}}{R_{I\_LOWER} + R_{I\_UPPER}} = \frac{V_{MAINS\_BI}}{V_{AC\_MIN}} = \frac{1}{120} \quad (37)$$

Considering the power consumption, a higher-value resistor is recommended. In this case, three 3.3MΩ resistors in series is recommended for the MAINSIN upper voltage divider resistor.

The lower voltage divider resistor value can be calculated with Equation (38):

$$R_{I\_LOWER} = \frac{R_{I\_UPPER}}{120 - 1} = 83.2k\Omega \quad (38)$$

The CS Pin

CS is used for OCP and OCL. The current flowing through the MOSFET should be below the OCL threshold. The CS resistor value can be estimated with Equation (39):

$$R_{CS} \leq \frac{V_{OCL}}{2\sqrt{2} \times I_{AC\_MAX}} = 58m\Omega \quad (39)$$

In this case, two 100mΩ resistors in parallel are recommended (specifically, two 2512 SMT resistors).

To enhance the ability of anti-interference, a 1kΩ resistor is connected in series to CS. To pass the surge test, a 100pF capacitor must be connected from CS to GND.

The ZCD Pin

The ZCD resistor connects the ZCD of the chip to the auxiliary winding. The main purpose of the resistor is to avoid excessive current on ZCD. Therefore, a minimum ZCD resistor is required to ensure that the current flowing through ZCD is below the ZCD maximum current under the maximum auxiliary winding voltage. The ZCD current can be calculated with Equation (40):

$$I_{ZCD} = \frac{V_{AUX\_MAX} - V_{ZCD\_CLAMP}}{R_{ZCD}} \leq 10mA \quad (40)$$

Where V_{AUX_MAX} is the maximum voltage on the

auxiliary winding (V_O / N), N is the ratio of winding, and V_{ZCD_CLAMP} is the upper clamp voltage of the ZCD pin.

In addition, the auxiliary winding voltage cannot be so low such that it triggers the zero-current sense threshold, which controls the gate of MOSFET to turn off. This threshold can be calculated with Equation (41):

$$V_{AUX\_MIN} = \frac{V_O - \sqrt{2} \times V_{AC\_MAX}}{N} \geq 0.75V \quad (41)$$

Where N can be estimated with Equation (42):

$$N \leq \frac{V_O - \sqrt{2} \times V_{AC\_MAX}}{0.75} = 34 \quad (42)$$

Considering the design of the boost inductor, 26:3 is selected as the winding ratio. Then R_{ZCD} can be calculated with Equation (43):

$$R_{ZCD} \geq \frac{V_{AUX\_MAX} - V_{ZCD\_CLAMP}}{10mA} = 3.8k\Omega \quad (43)$$

R_{ZCD} is recommended to be 33kΩ.

The COMP Pin

Based on the small signal modeling, the control to output voltage transfer function (resistive load) can be estimated with Equation (44):

$$G_{VC}(s) = \frac{K_{RAMP}}{3 \times K_{MAIN}^2} \times \frac{1}{2V_O C_O L} \times \frac{1}{\frac{2}{R_O C_O} + s} \quad (44)$$

Where K_{MAIN} is the MAINSIN voltage divider ratio, and K_{RAMP} is equal to t_{ON_LL}.

In this case, G_{VC} is calculated with Equation (45):

$$G_{VC}(s) = \frac{4706.67}{s + 16.67} \quad (45)$$

In addition, the voltage error amplifier is a transconductance amplifier. The voltage compensation tank is connected from COMP to GND. A Type-II compensation network is recommended.

The transfer function of the transconductance amplifier can be calculated with Equation (46):

$$G_{EA}(s) = K_{FB} \times G_{M1} \times \frac{1}{C_P s} \times \frac{\frac{1}{C_Z R_Z} + s}{\frac{C_Z + C_P}{C_Z C_P R_Z} + s} \quad (46)$$

Where K_{FB} is the FB voltage divider ratio, and G_{M1} is the transconductance value when FB is about equal to V_R (about 104μs).

Then the open voltage loop transfer function can be calculated with Equation (47):

$$G(s) = G_{VC}(s) \times G_{EA}(s) \quad (47)$$

In this case, to design a high-stability voltage loop, 12Hz is recommended as a suitable crossover frequency, and the phase margin must exceed 45°. 5Hz is the recommended zero value, and 50Hz is designed as the pole with high frequency.

The value of the compensation network can be calculated with Equation (48):

$$R_Z = \frac{1}{K_{FB} \times G_{M1}} \times 10^{\frac{-\Phi_{VC}(12)}{20}} = 28.5k\Omega \quad (48)$$

Where C_Z can be estimated with Equation (49):

$$C_Z = \frac{1}{2\pi \times 5 \times R_Z} = 1.1\mu F \quad (49)$$

And C_P can be estimated with Equation (50):

$$C_P = \frac{1}{2\pi \times 50 \times R_Z} = 0.1\mu F \quad (50)$$

R_Z = 30kΩ, C_Z = 1μF, and C_P = 220pF are the recommended values of the compensation network.

PCB Layout Guidelines

PCB layout is a critical factor for stable operation and EMI performance. The device can malfunction due to noise coupling. For the best results, refer to Figure 14 and follow the guidelines below:

1. Make power loop 1 and power loop 2 as small as possible.
2. Do not place the IC in power loop 1 or power loop 2.
3. Make the areas of high dV/dt junctions (e.g. the drain of the external primary MOSFET) as small as possible. Place the IC and control circuits far away from these areas.
4. Separate the reference ground of the IC and control signals circuit from the ground of the power loop. Then connect this signal ground to the ground of the output capacitor with a single-point junction.
5. Connect the VCC-GND capacitor close to IC.
6. Connect the FB-GND capacitor close to IC.
7. Connect the MAINS-GND capacitor close to IC. Ensure that the CS wiring does not cross MAINSIN. Otherwise, the CS noise may couple to MAINSIN and impact peak voltage sensing.
8. If the PFC stage is connected to a cascade DC/DC stage, separate both GNDs with an output capacitor, so that GND noises do not interfere with one another.

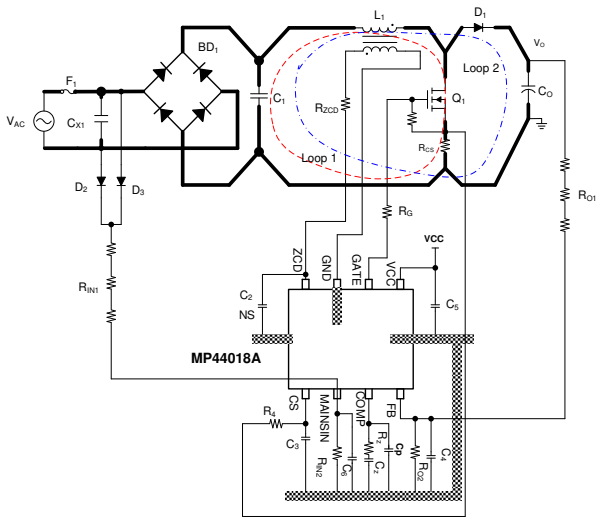


Figure 14: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

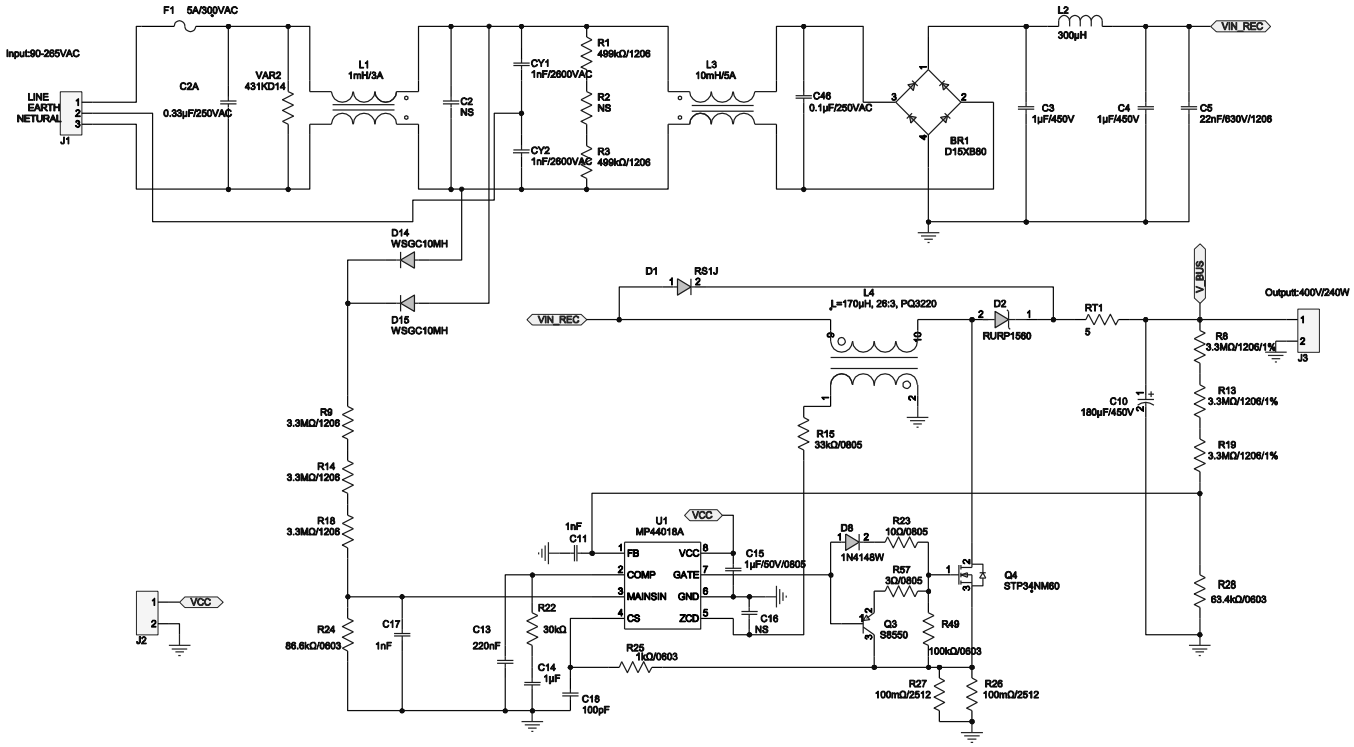


Figure 15: MP44018A Typical Application Circuit

CONTROL FLOWCHARTS

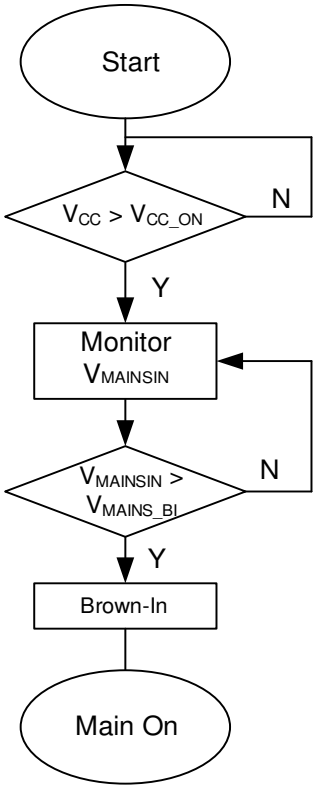


Figure 16: Start-Up Flowchart

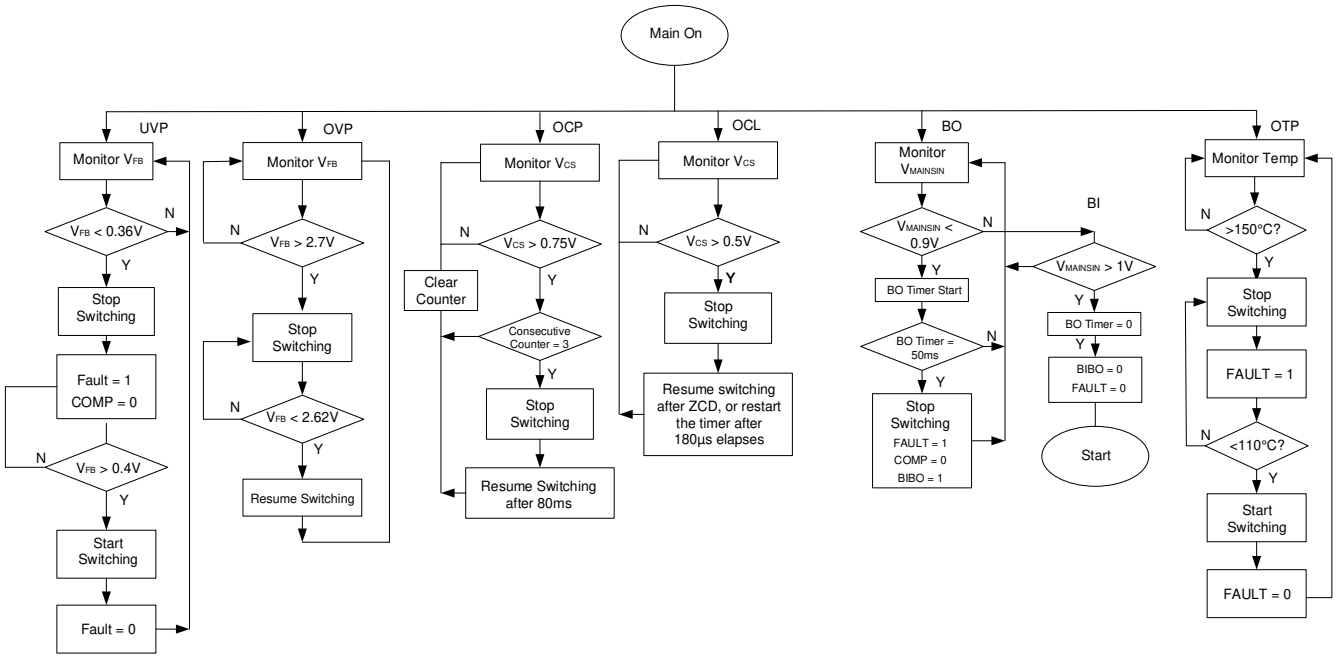
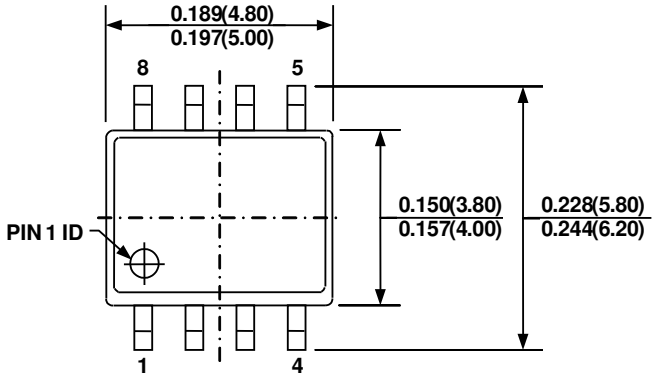


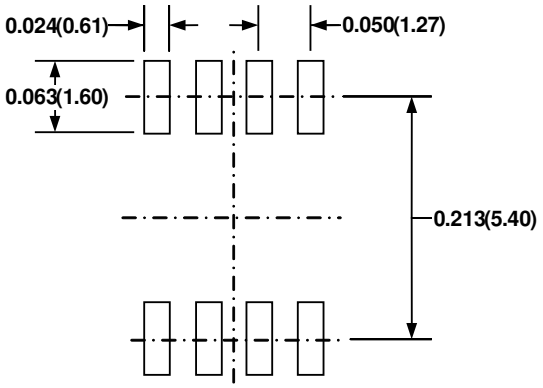
Figure: 17: Control Flowchart

PACKAGE INFORMATION

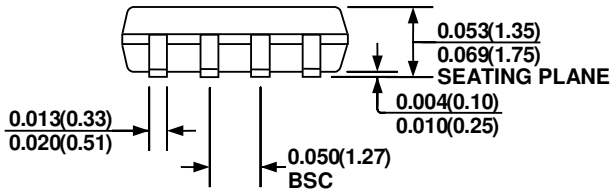
SOIC-8



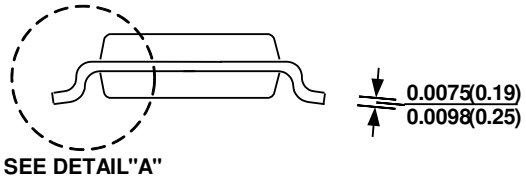
TOP VIEW



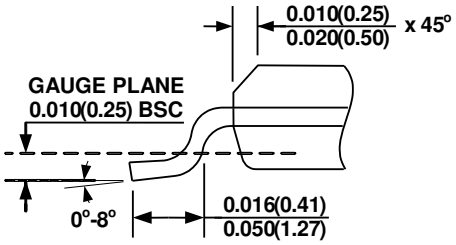
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

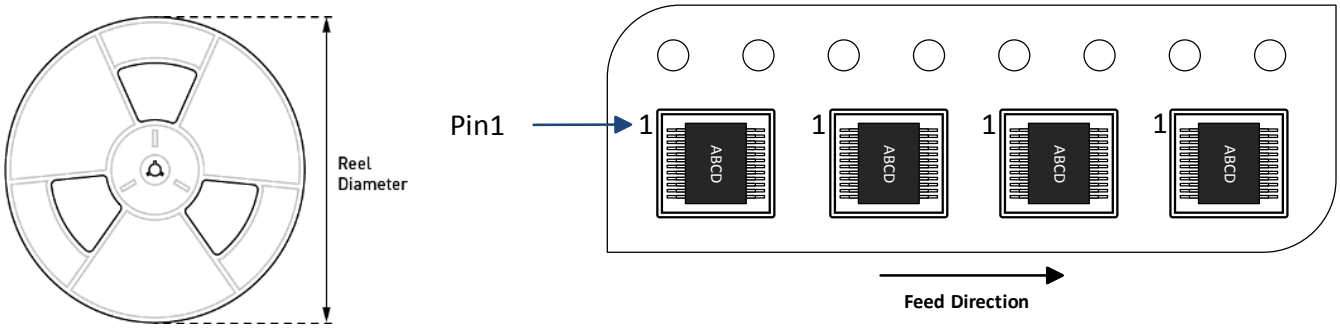


DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA
6) DRAWING IS NOT TO SCALE

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP44018-AGS–Z	SOIC-8	2500	100	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	8/11/2020	Initial Release	-
1.01	11/10/2020	Updated figure 2, steady state to VIN=120VAC, Pout=120w; Updated figure 4, steady state to VIN=230VAC, Pout=120w,	P12
		Updated Brown in /brown out waveform	P13