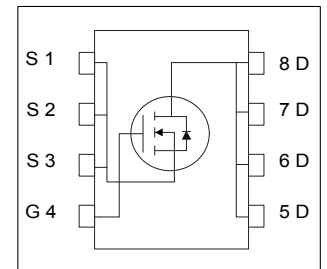
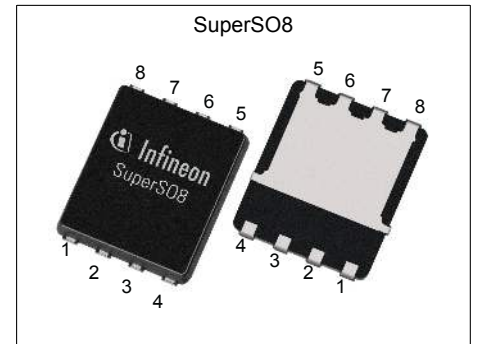


# MOSFET

## OptiMOS™3 Power-Transistor, 40 V

### Features

- Fast switching MOSFET for SMPS
- Optimized technology for DC/DC converters
- Qualified according to JEDEC<sup>1)</sup> for target applications
- N-channel; Logic level
- Excellent gate charge x RDS(on) product (FOM)
- Very low on-resistance RDS(on)
- Superior thermal resistance
- 100% Avalanche tested
- Pb-free plating; RoHS compliant
- Halogen-free according to IEC61249-2-21



RoHS

**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	40	V
$R_{DS(on),max}$	1.8	mΩ
$I_D$	209	A

Type / Ordering Code	Package	Marking	Related Links
BSC018N04LS G	PG-TDSON-8	018N04LS	-

<sup>1)</sup> J-STD20 and JESD22

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**1 Maximum ratings**  
 at  $T_A=25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	209	A	$V_{GS}=10\text{ V}$ , $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_C=100\text{ °C}$ $V_{GS}=4.5\text{ V}$ , $T_C=25\text{ °C}$ $V_{GS}=4.5\text{ V}$ , $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_A=25\text{ °C}$ , $R_{thJA}=50\text{ K/W}^2)$
		-	-	132		
		-	-	180		
		-	-	114		
		-	-	30		
Pulsed drain current <sup>3)</sup>	$I_{D,pulse}$	-	-	836	A	$T_C=25\text{ °C}$
Avalanche current, single pulse <sup>4)</sup>	$I_{AS}$	-	-	50	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	295	mJ	$I_D=50\text{ A}$ , $R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	125	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$ , $R_{thJA}=50\text{ K/W}^2)$
		-	-	2.5		
Operating and storage temperature	$T_j, T_{stg}$	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

**2 Thermal characteristics**

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	$R_{thJC}$	-	-	1	K/W	-
Thermal resistance, junction - case, top	$R_{thJC}$	-	-	18	K/W	-
Device on PCB, 6 cm <sup>2</sup> cooling area <sup>2)</sup>	$R_{thJA}$	-	-	50	K/W	-

<sup>1)</sup> Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature at 25°C. For higher case temperature please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

<sup>3)</sup> See figure 3 for more detailed information

<sup>4)</sup> See figure 13 for more detailed information

### 3 Electrical characteristics

at  $T_j=25\text{ °C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	1.2	-	2	V	$V_{DS}=V_{GS}$ , $I_D=85\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.1 10	1 100	$\mu\text{A}$	$V_{DS}=40\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$ $V_{DS}=40\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ °C}$
Gate-source leakage current	$I_{GSS}$	-	10	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	2.0 1.5	2.5 1.8	m $\Omega$	$V_{GS}=4.5\text{ V}$ , $I_D=50\text{ A}$ $V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$
Gate resistance	$R_G$	-	1.3	-	$\Omega$	-
Transconductance	$g_{fs}$	90	180	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$ , $I_D=50\text{ A}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance <sup>1)</sup>	$C_{iss}$	-	8900	12000	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=20\text{ V}$ , $f=1\text{ MHz}$
Output capacitance <sup>1)</sup>	$C_{oss}$	-	1800	2400	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=20\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance	$C_{rss}$	-	100	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=20\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	13	-	ns	$V_{DD}=20\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=30\text{ A}$ , $R_G=1.6\text{ }\Omega$
Rise time	$t_r$	-	7.4	-	ns	$V_{DD}=20\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=30\text{ A}$ , $R_G=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	55	-	ns	$V_{DD}=20\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=30\text{ A}$ , $R_G=1.6\text{ }\Omega$
Fall time	$t_f$	-	9.0	-	ns	$V_{DD}=20\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=30\text{ A}$ , $R_G=1.6\text{ }\Omega$

**Table 6 Gate charge characteristics<sup>2)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	26	-	nC	$V_{DD}=20\text{ V}$ , $I_D=30\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	14	-	nC	$V_{DD}=20\text{ V}$ , $I_D=30\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	$Q_{gd}$	-	11	-	nC	$V_{DD}=20\text{ V}$ , $I_D=30\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	$Q_{sw}$	-	23	-	nC	$V_{DD}=20\text{ V}$ , $I_D=30\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total <sup>1)</sup>	$Q_g$	-	113	150	nC	$V_{DD}=20\text{ V}$ , $I_D=30\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	2.9	-	V	$V_{DD}=20\text{ V}$ , $I_D=30\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total <sup>1)</sup>	$Q_g$	-	54	72	nC	$V_{DD}=20\text{ V}$ , $I_D=30\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	106	-	nC	$V_{DS}=0.1\text{ V}$ , $V_{GS}=0\text{ to }10\text{ V}$
Output charge	$Q_{oss}$	-	69	-	nC	$V_{DD}=20\text{ V}$ , $V_{GS}=0\text{ V}$

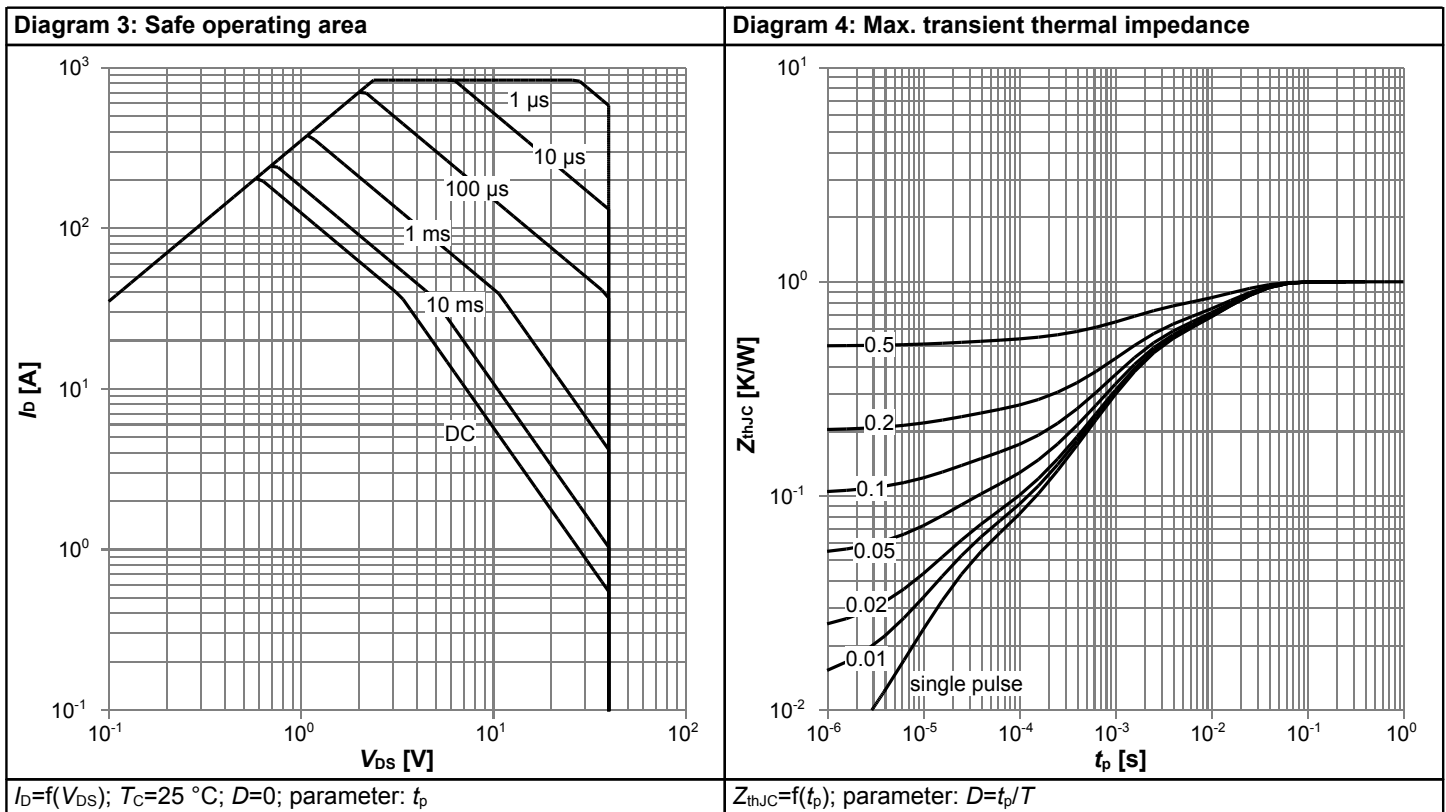
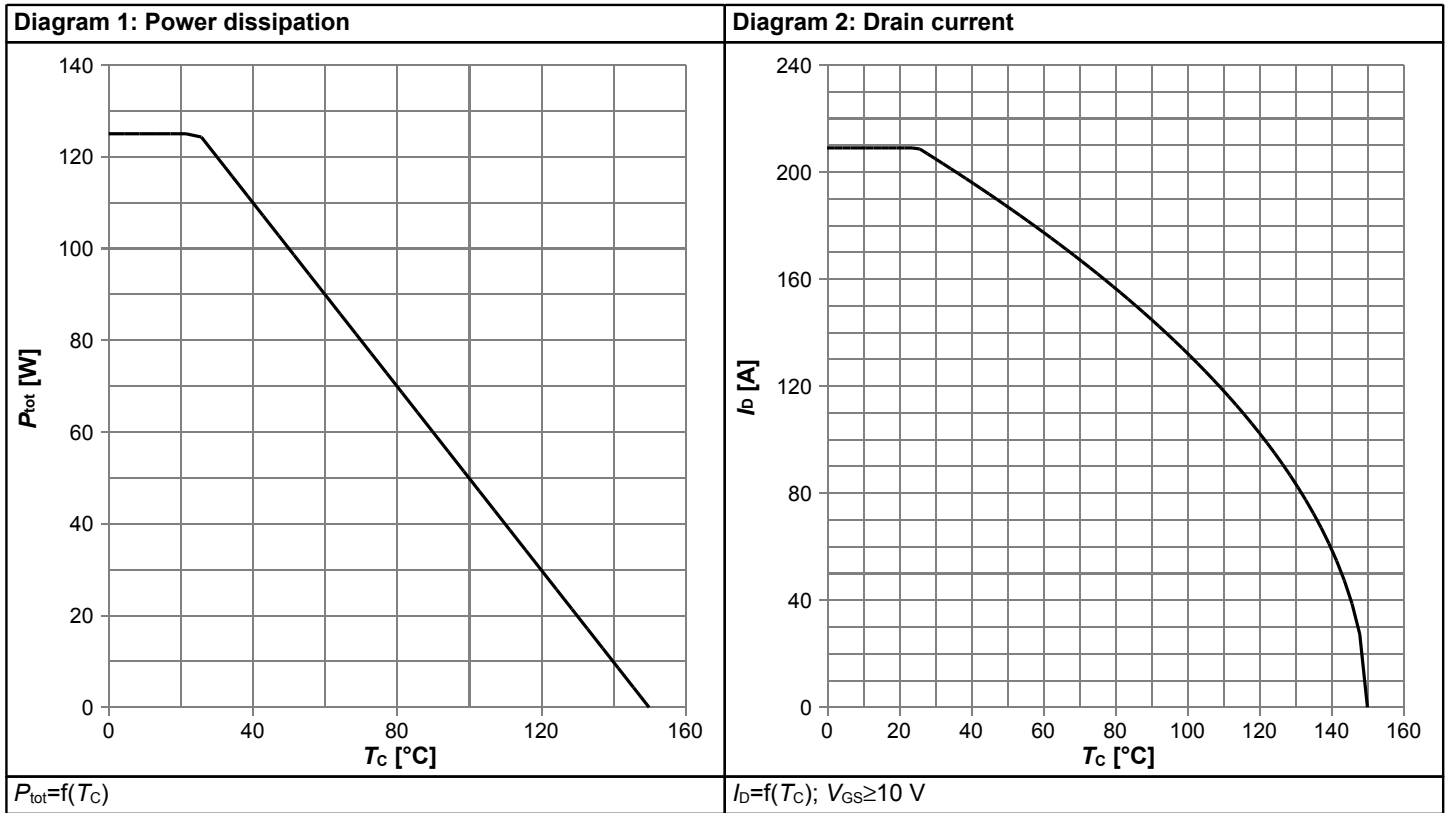
<sup>1)</sup> Defined by design. Not subject to production test

<sup>2)</sup> See "Gate charge waveforms" for parameter definition

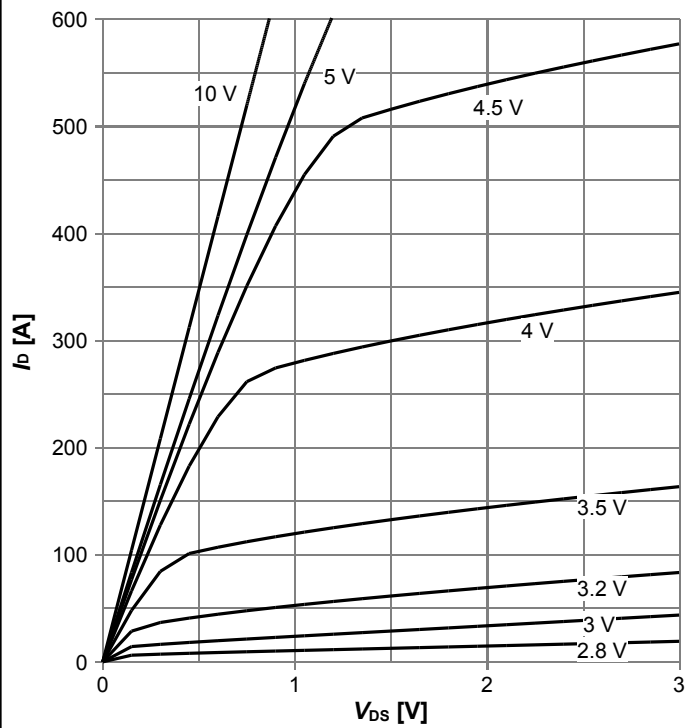
**Table 7 Reverse diode**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	104	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	836	A	$T_C=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	0.81	1.2	V	$V_{GS}=0\text{ V}, I_F=50\text{ A}, T_j=25\text{ °C}$
Reverse recovery charge	$Q_{rr}$	-	125	-	nC	$V_R=20\text{ V}, I_F=I_S, di_F/dt=400\text{ A}/\mu\text{s}$

## 4 Electrical characteristics diagrams

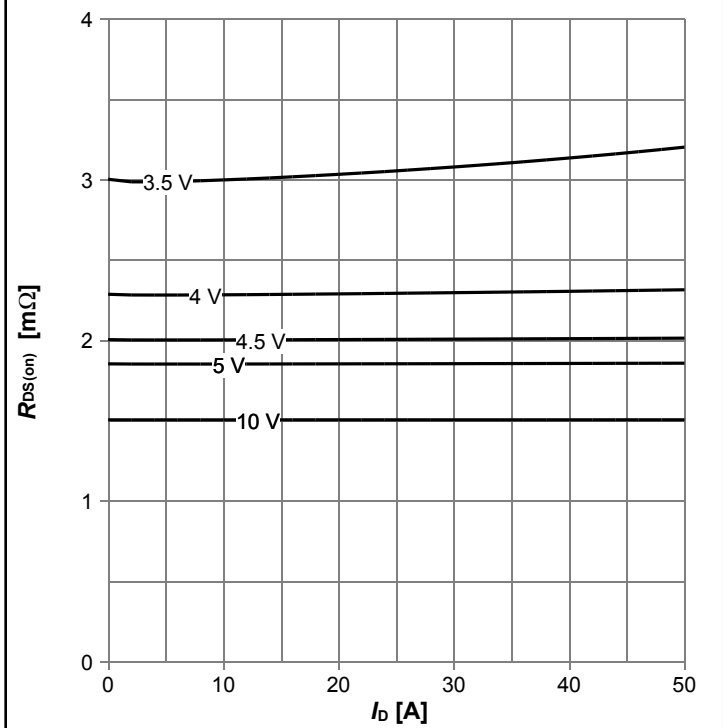


**Diagram 5: Typ. output characteristics**



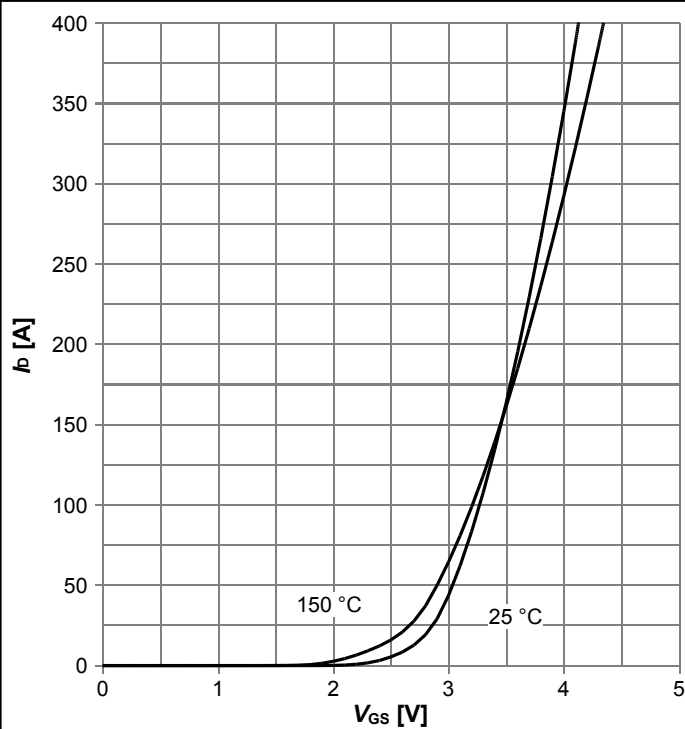
$I_D = f(V_{DS}); T_j = 25\text{ °C};$  parameter:  $V_{GS}$

**Diagram 6: Typ. drain-source on resistance**



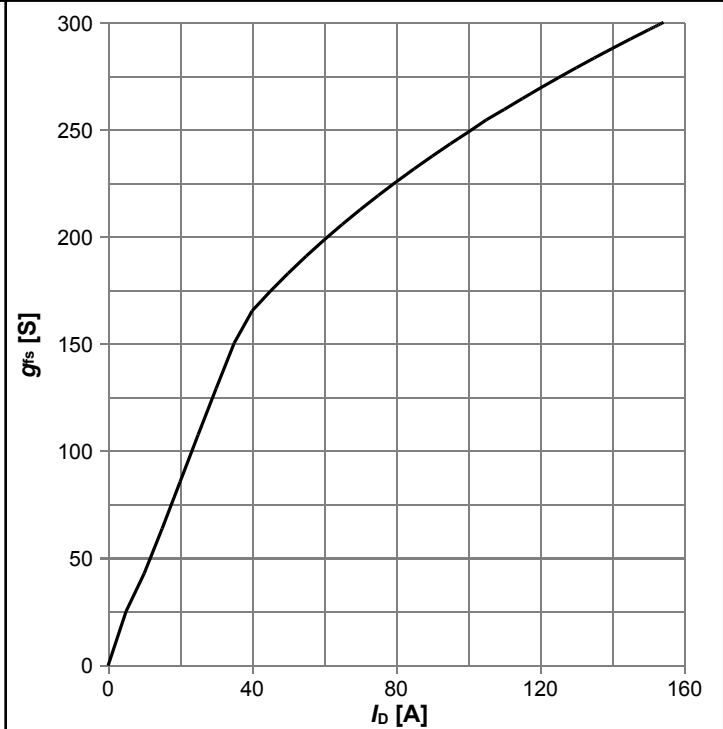
$R_{DS(on)} = f(I_D); T_j = 25\text{ °C};$  parameter:  $V_{GS}$

**Diagram 7: Typ. transfer characteristics**



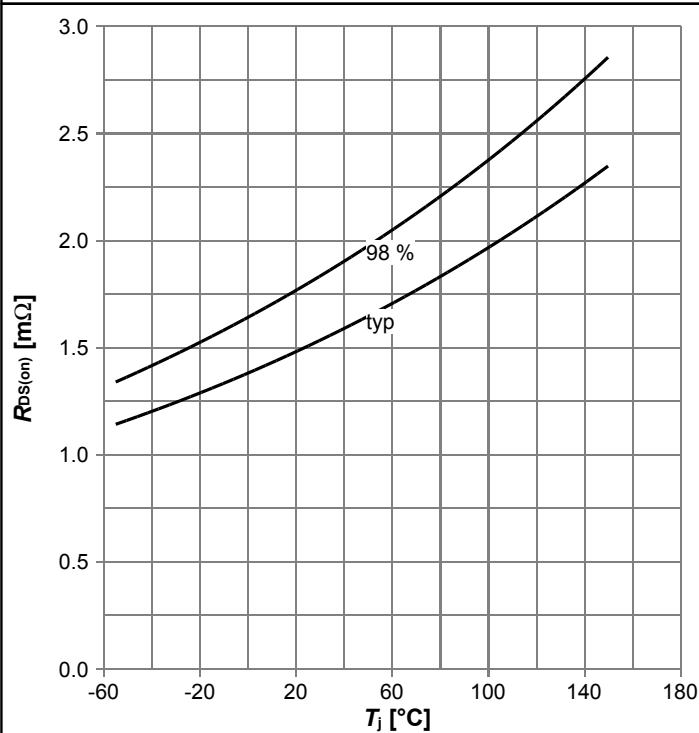
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max};$  parameter:  $T_j$

**Diagram 8: Typ. forward transconductance**



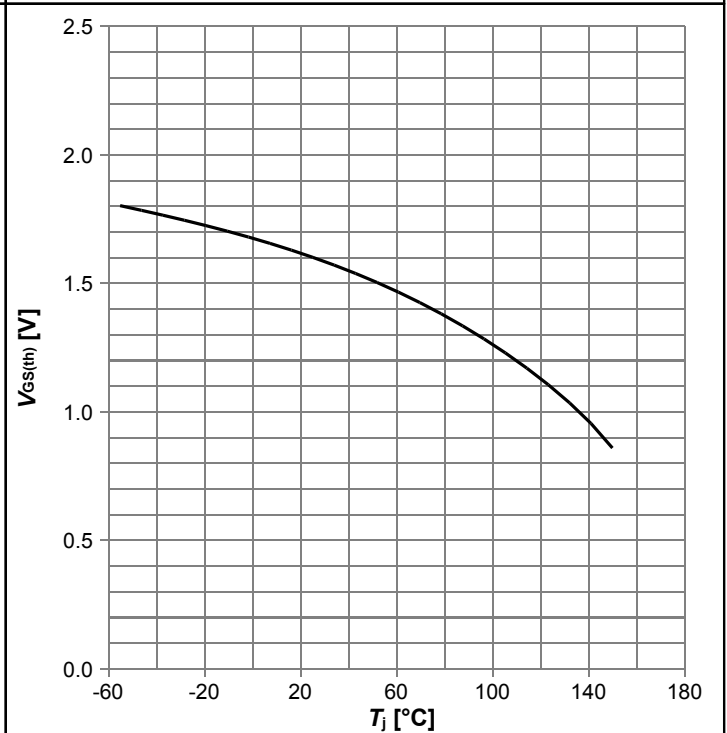
$g_{fs} = f(I_D); T_j = 25\text{ °C}$

Diagram 9: Drain-source on-state resistance



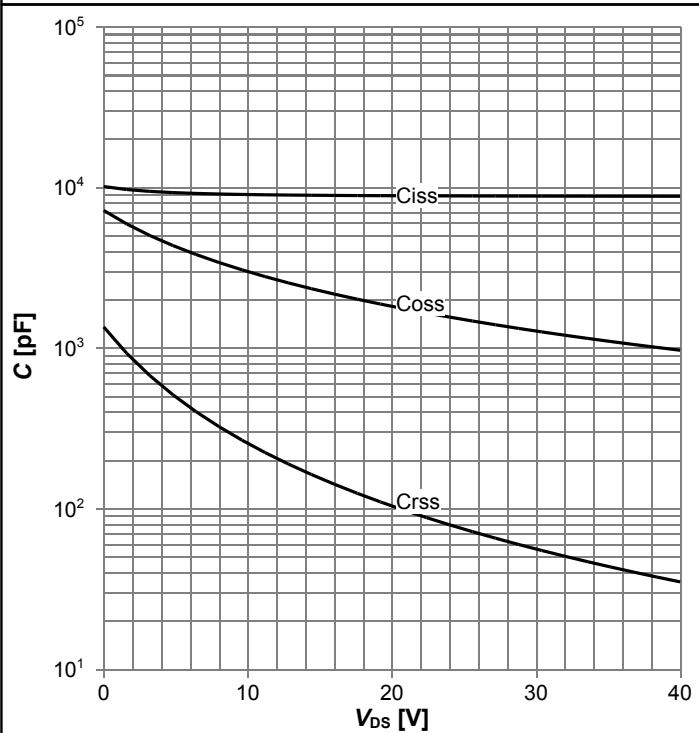
$R_{DS(on)}=f(T_j)$ ;  $I_D=50$  A;  $V_{GS}=10$  V

Diagram 10: Typ. gate threshold voltage



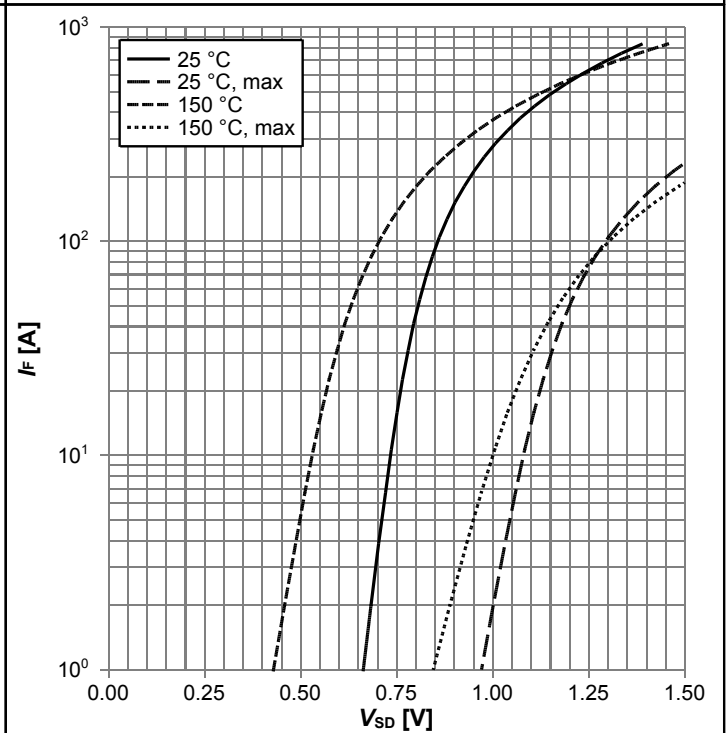
$V_{GS(th)}=f(T_j)$ ;  $V_{GS}=V_{DS}$ ;  $I_D=85$   $\mu$ A

Diagram 11: Typ. capacitances



$C=f(V_{DS})$ ;  $V_{GS}=0$  V;  $f=1$  MHz

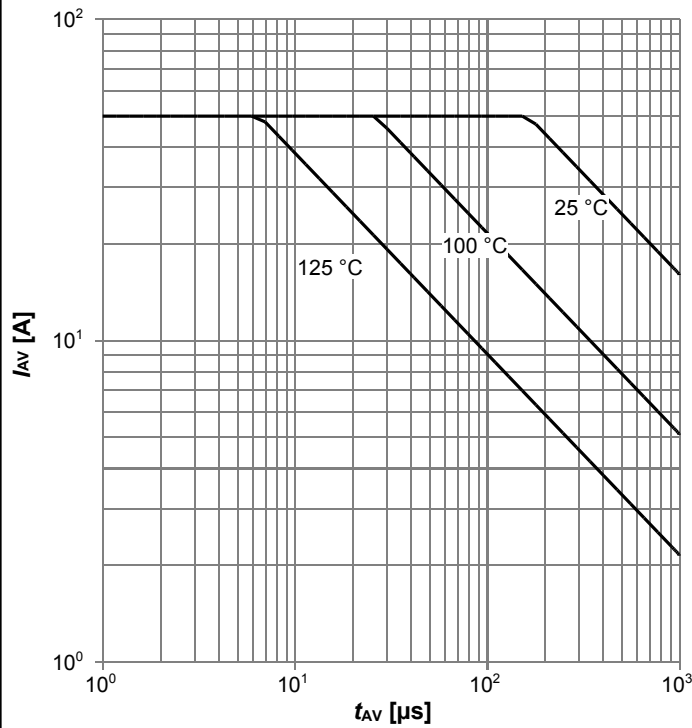
Diagram 12: Forward characteristics of reverse diode



$I_F=f(V_{SD})$ ; parameter:  $T_j$

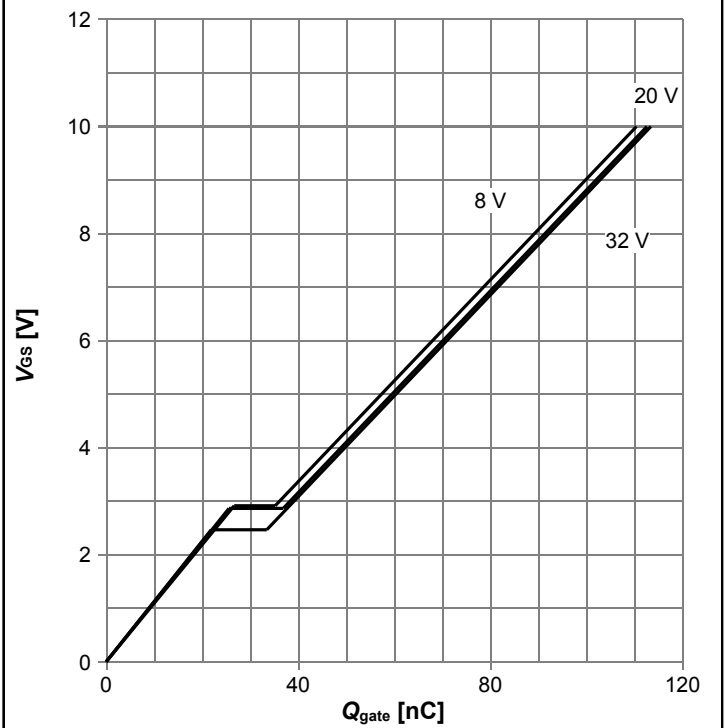


Diagram 13: Avalanche characteristics



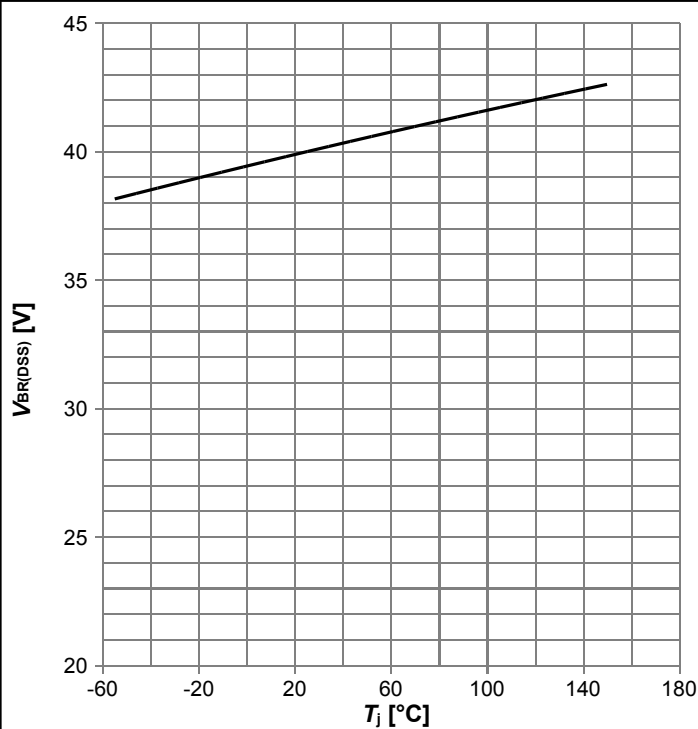
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$ ; parameter:  $T_{j(start)}$

Diagram 14: Typ. gate charge



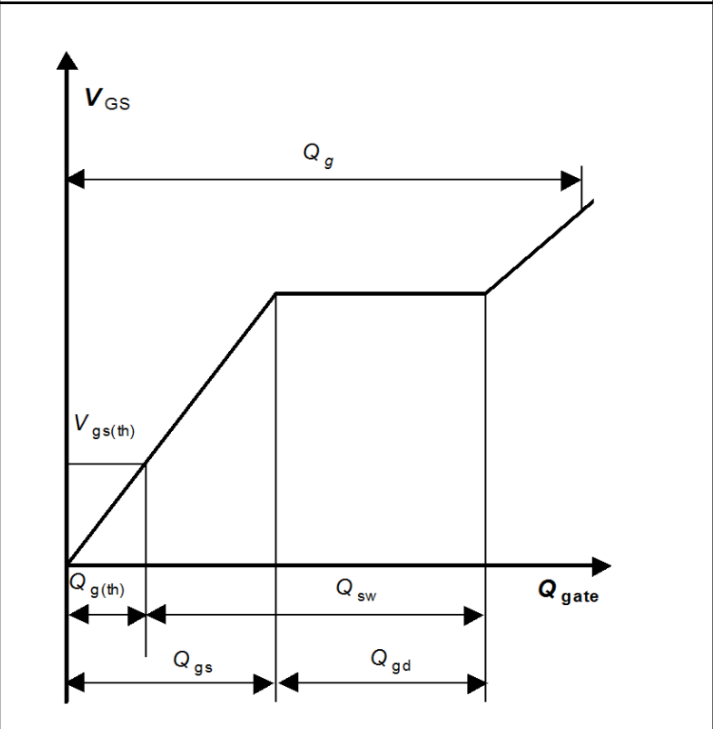
$V_{GS}=f(Q_{gate}); I_D=30 \text{ A pulsed}$ ; parameter:  $V_{DD}$

Diagram 15: Drain-source breakdown voltage

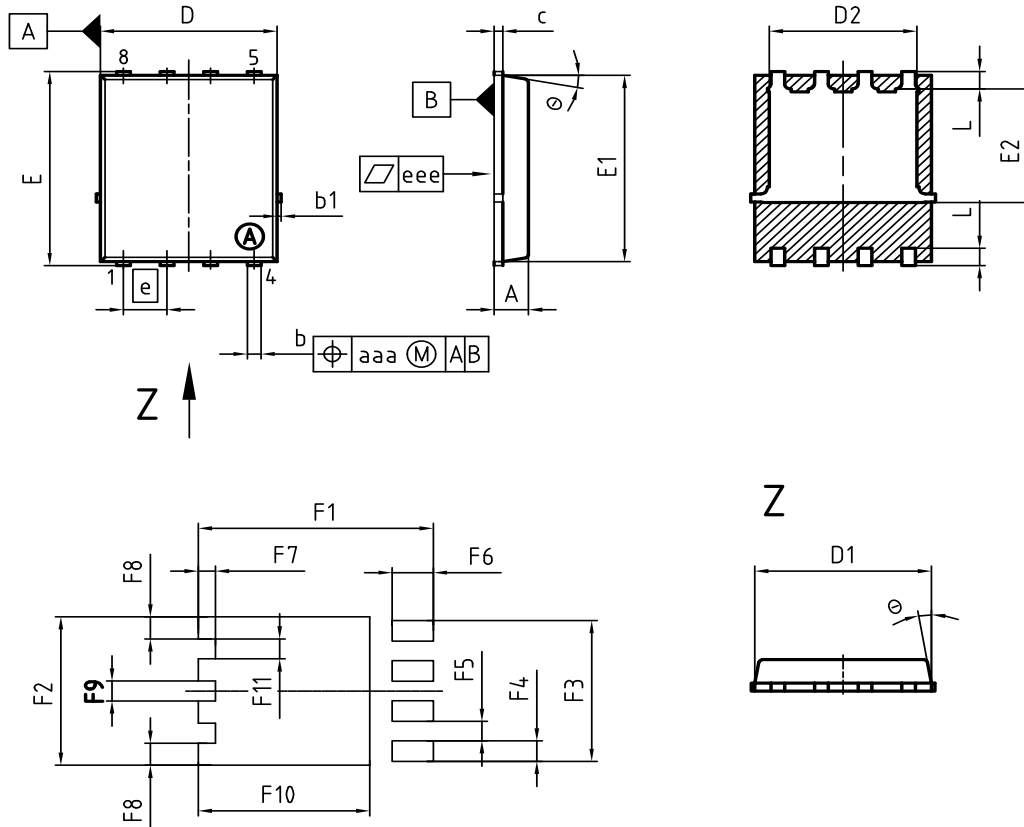


$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Diagram Gate charge waveforms



## 5 Package Outlines

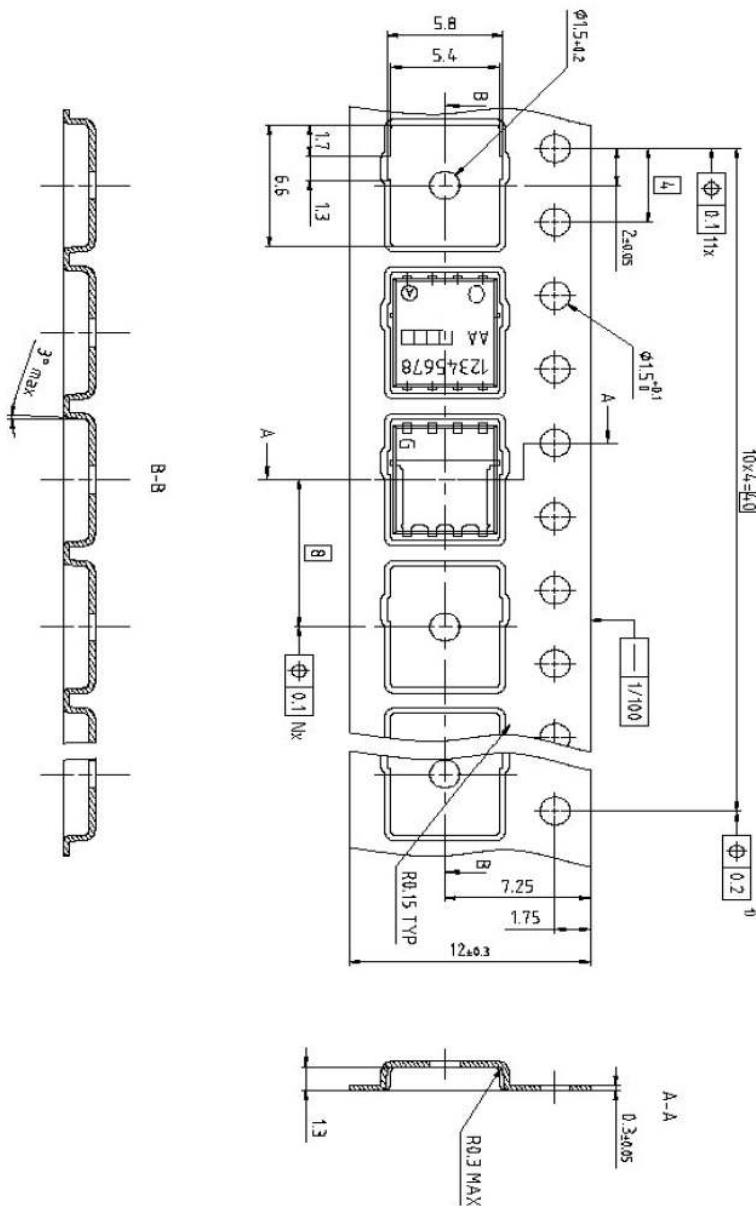


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.34	0.54	0.013	0.021
b1	0.02	0.22	0.001	0.008
c	0.15	0.35	0.006	0.014
D=D1	4.95	5.35	0.195	0.211
D2	4.20	4.40	0.165	0.173
E	5.95	6.35	0.234	0.250
E1	5.70	6.10	0.224	0.240
E2	3.40	3.80	0.134	0.150
e	1.27		0.050	
N	8		8	
L	0.45	0.65	0.018	0.026
theta	8.5°	11.5°	8.5°	11.5°
aaa	0.25		0.010	
eee	0.05		0.002	
F1	6.75	6.95	0.266	0.274
F2	4.60	4.80	0.181	0.189
F3	4.36	4.56	0.172	0.180
F4	0.55	0.75	0.022	0.030
F5	0.52	0.72	0.020	0.028
F6	1.10	1.30	0.043	0.051
F7	0.40	0.60	0.016	0.024
F8	0.60	0.80	0.024	0.031
F9	0.53	0.73	0.021	0.029
F10	4.90	5.10	0.193	0.201
F11	0.53	0.73	0.021	0.029

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Figure 1 Outline PG-TDSON-8, dimensions in mm/inches

**OptiMOS™3 Power-Transistor, 40 V**  
**BSC018N04LS G**



**Figure 2 Outline Tape (PG-TDSON-8), dimensions in mm**

## Revision History

BSC018N04LS G

**Revision: 2020-08-14, Rev. 2.1**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
1.4	2020-07-23	Release of preliminary datasheet
2.1	2020-08-14	Update current rating and footnotes

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