

DM74LS165 8-Bit Parallel In/Serial Output Shift Registers

General Description

This device is an 8-bit serial shift register which shifts data in the direction of Q_A toward Q_H when clocked. Parallel-in access is made available by eight individual direct data inputs, which are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit.

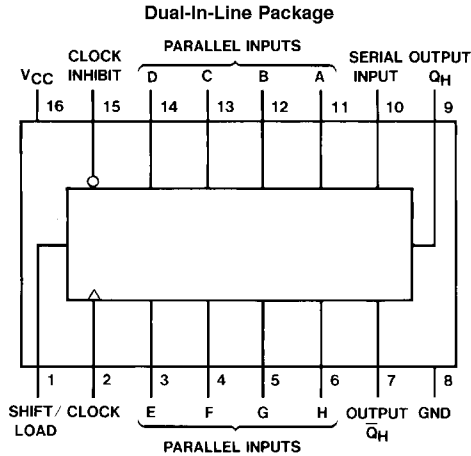
Clocking is accomplished through a 2-input NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel

loading is inhibited as long as the load input is high. Data at the parallel inputs are loaded directly into the register on a high-to-low transition of the shift/load input, regardless of the logic levels on the clock, clock inhibit, or serial inputs.

Features

- Complementary outputs
- Direct overriding (data) inputs
- Gated clock inputs
- Parallel-to-serial data conversion
- Typical frequency 35 MHz
- Typical power dissipation 105 mW

Connection Diagram



Order Number DM54LS165J, DM54LS165W, DM74LS165WM or DM74LS165N
See Package Number J16A, M16B, N16E or W16A

Function Table

Shift/ Load	Clock Inhibit	Inputs			Internal Outputs		Output Q_H
		Clock	Serial	Parallel	Q_A	Q_B	
				A...H			
L	X	X	X	a...h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = High Level (steady state), L = Low Level (steady state)

X = Don't Care (any input, including transitions)

↑ = Transition from low-to-high level

a...h = The level of steady-state input at inputs A through H, respectively.

Q_{A0} , Q_{B0} , Q_{H0} = The level of Q_A , Q_B , or Q_H , respectively, before the indicated steady-state input conditions were established.

Q_{An} , Q_{Gn} = The level of Q_A or Q_G , respectively, before the most recent ↑ transition of the clock.

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V	DM54LS	-55°C to +125°C
Input Voltage	7V	DM74LS	0°C to +70°C
Operating Free Air Temperature Range		Storage Temperature Range	-65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM54LS165			DM74LS165			Units
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			2			V
V _{IL}	Low Level Input Voltage			0.7			0.8	V
I _{OH}	High Level Output Current			-0.4			-0.4	mA
I _{OL}	Low Level Output Current			4			8	mA
f _{CLK}	Clock Frequency (Note 2)			30	0		25	MHz
f _{CLK}	Clock Frequency (Note 3)				0		20	MHz
t _w	Pulse Width (Note 3)	Clock	18		25			ns
		Load	15		15			
t _{SU}	Setup Time (Note 7)	Parallel	10		10			ns
		Serial	10		20			
		Enable	10		30			
		Shift	10		45			
t _H	Hold Time (Note 7)	5			0			ns
T _A	Free Air Operating Temperature	-55		125	0		70	°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 4)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = -18 mA			-1.5	V
V _{OH}	High Level Output Voltage	V _{CC} = Min, I _{OH} = Max	DM54	2.5		V
		V _{IL} = Max, V _{IH} = Min	DM74	2.7	3.4	
V _{OL}	Low Level Output Voltage	V _{CC} = Min, I _{OL} = Max			0.4	V
		V _{IL} = Max, V _{IH} = Min	DM74		0.35	
		I _{OL} = 4 mA, V _{CC} = Min			0.25	0.4
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 7V (DM74)	Shift/Load		0.3	mA
		V _I = 10V (DM54)	Others		0.1	
I _{IH}	High Level Input Current	V _{CC} = Max	Shift/Load		60	μA
		V _I = 2.7V	Others		20	
I _{IL}	Low Level Input Current	V _{CC} = Max	Shift/Load		-1.2	mA
		V _I = 0.4V	Others		-0.4	
I _{OS}	Short Circuit Output Current	V _{CC} = Max	DM54	-20	-100	mA
		(Note 5)	DM74	-20	-100	
I _{CC}	Supply Current	V _{CC} = Max (Note 6)		21	36	mA

Note 2: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V

Note 3: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V

Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: With all outputs open, clock inhibit and shift/load at 4.5V, and a clock pulse applied to the CLOCK input, I_{CC} is measured first with the parallel inputs at 4.5V, then again grounded.

Electrical Characteristics (Continued)

Note 7: $T_A = 25^\circ\text{C}$ and $V_{CC} = 5\text{V}$.

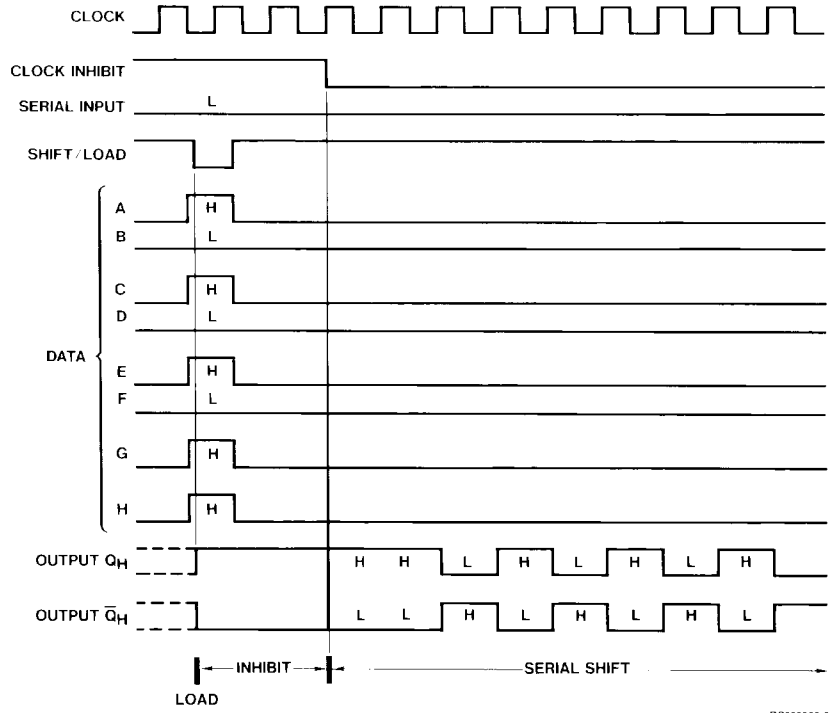
Switching Characteristics

at $V_{CC} = 5\text{V}$ and $T_A = 25^\circ\text{C}$

Symbol	Parameter	From (Input) To (Output)	DM54LS		DM74LS		DM74LS		Units
			$C_L = 15\text{ pF}$		$C_L = 15\text{ pF}$		$R_L = 2\text{ k}\Omega$ $C_L = 50\text{ pF}$		
			Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Load to Any Q		30		35		37	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Load to Any Q		30		35		42	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q		30		40		42	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q		30		40		47	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	H to Q_H		20		25		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	H to Q_H		30		30		37	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	H to \bar{Q}_H		30		30		32	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	H to \bar{Q}_H		25		25		32	ns

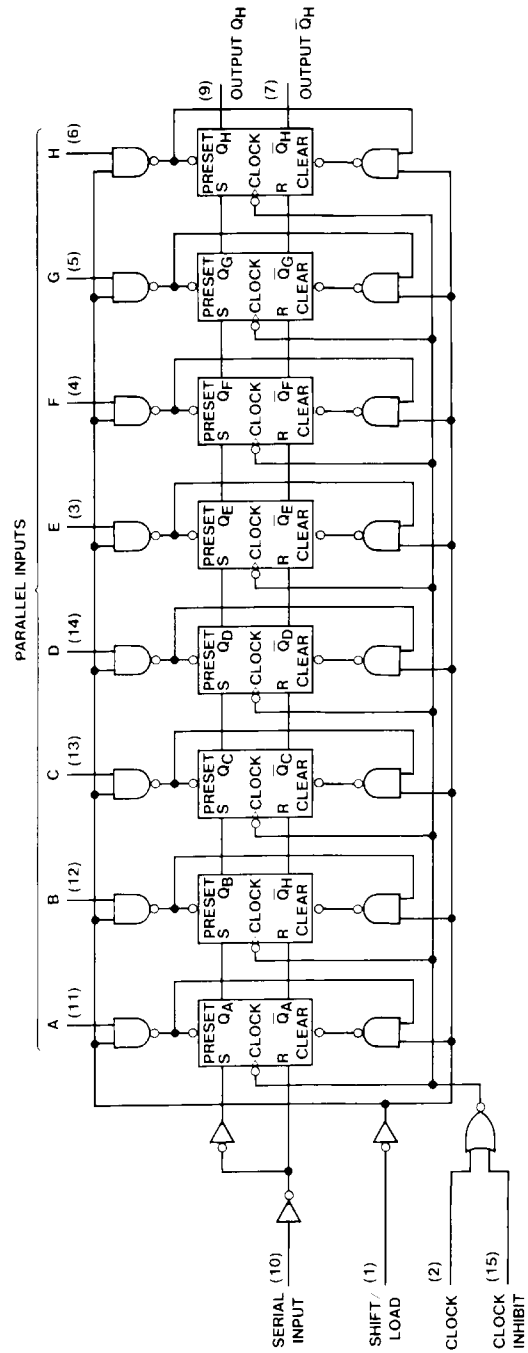
Timing Diagram

Typical Shift, Load, and Inhibit Sequences

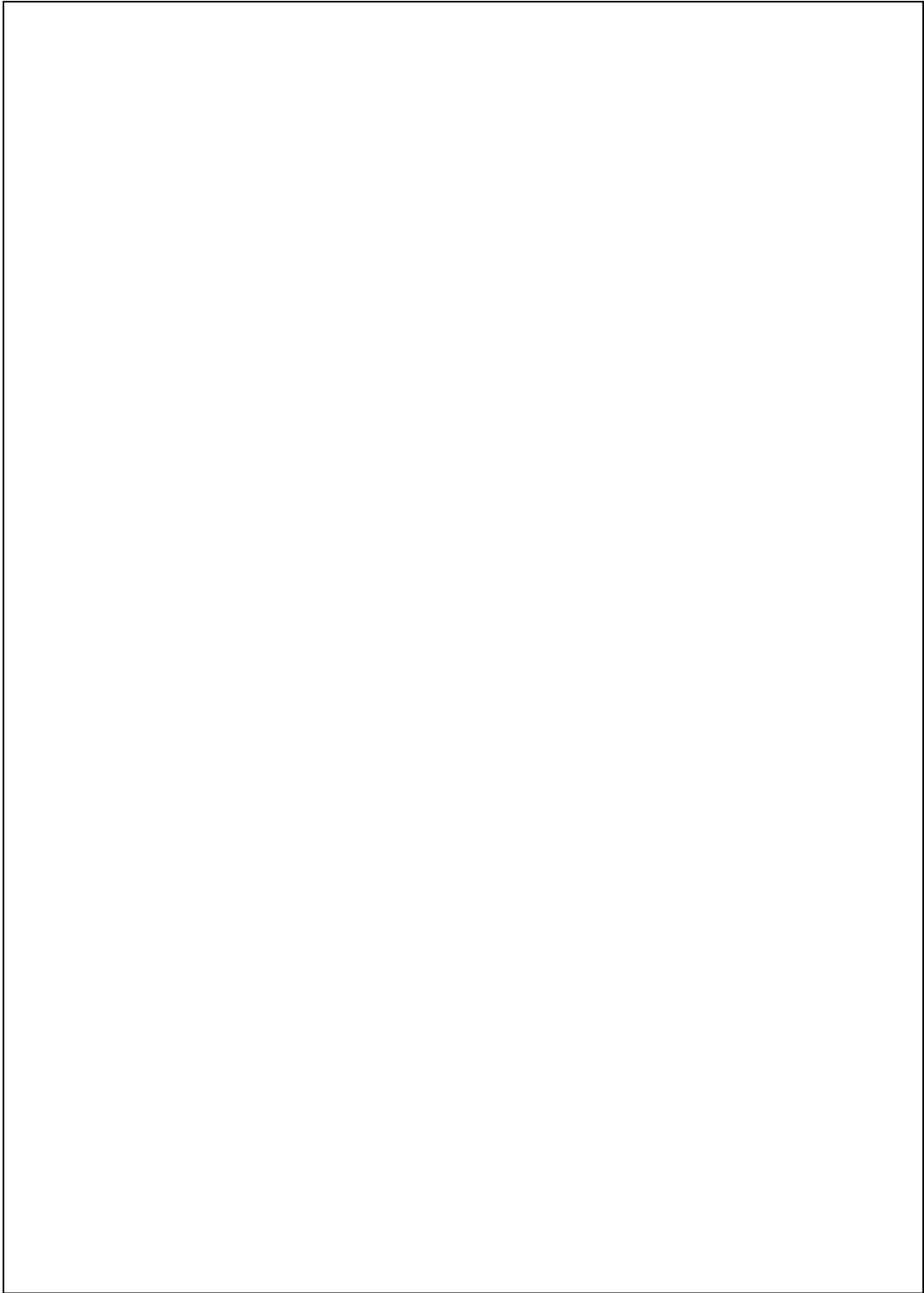


DS006399-3

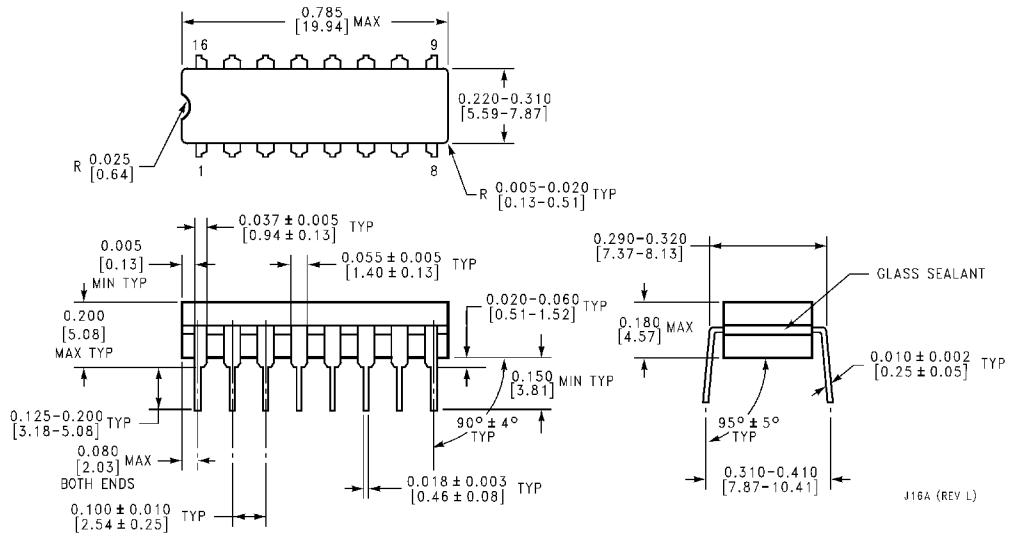
Logic Diagram



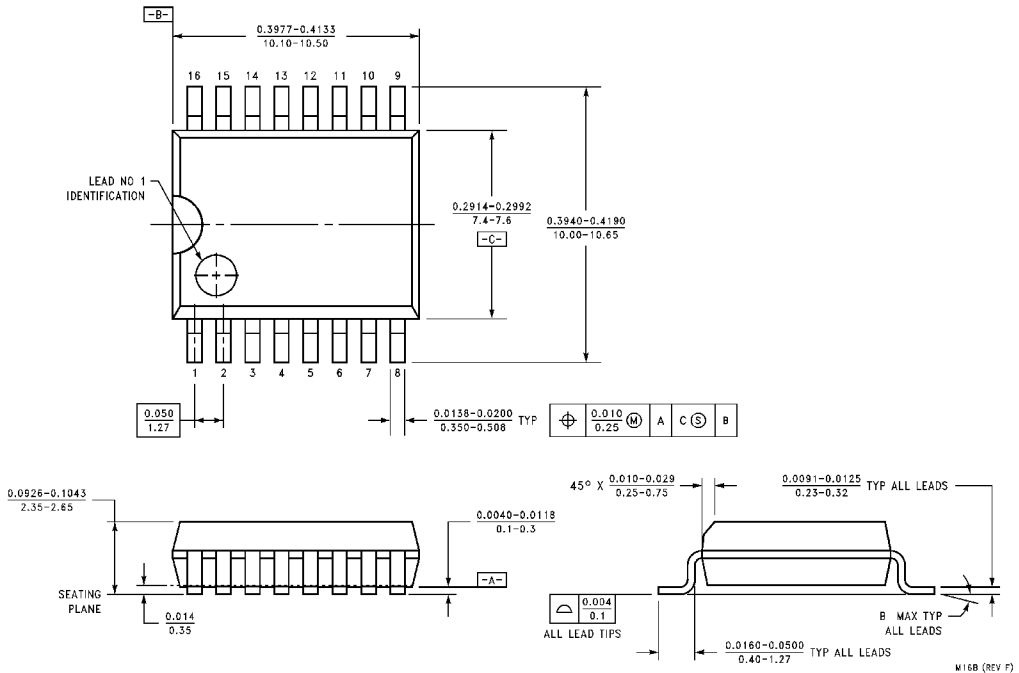
DSM6392



Physical Dimensions inches (millimeters) unless otherwise noted

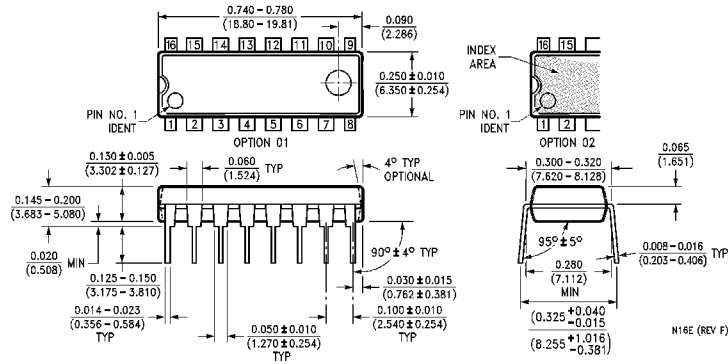


16-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS165J
Package Number J16A

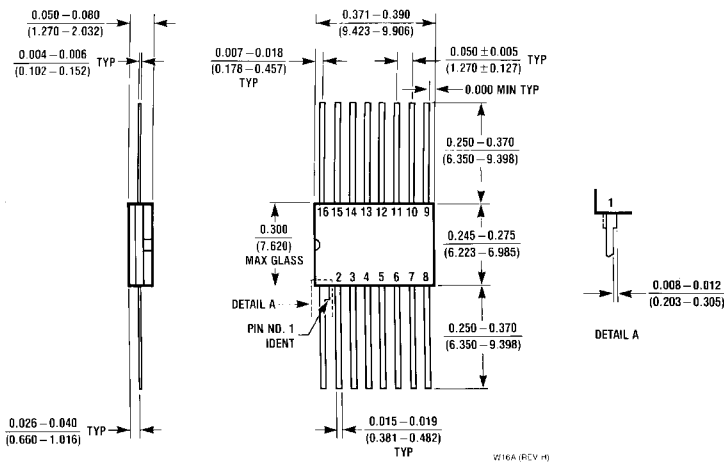


16-Lead Wide Small Outline Molded Package (M)
Order Number DM74LS165WM
Package Number M16B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS165N
Package Number N16E



16-Lead Ceramic Flat Package (W)
Order Number DM54LS165W
Package Number W16A

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Fairchild Semiconductor
Corporation
Americas
Customer Response Center
Tel: 1-888-522-5372

www.fairchildsemi.com

Fairchild Semiconductor
Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 8 141-35-0
English Tel: +44 (0) 1 793-85-68-56
Italy Tel: +39 (0) 2 57 5631

Fairchild Semiconductor
Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: +852 2737-7200
Fax: +852 2314-0061

National Semiconductor
Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179