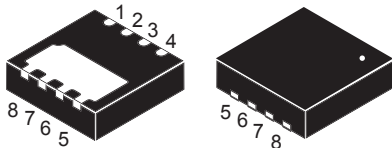
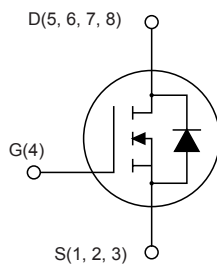


## N-channel 600 V, 1.5 $\Omega$ typ., 2.2 A MDmesh II Power MOSFET in a PowerFLAT 3.3x3.3 HV package


**PowerFLAT 3.3x3.3 HV**


AM15810v1



### Features

Order code	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$
STL3NM60N	600 V	1.8 $\Omega$	2.2 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

#### Product status link

[STL3NM60N](#)

#### Product summary

<b>Order code</b>	STL3NM60N
<b>Marking</b>	3NM60
<b>Package</b>	PowerFLAT 3.3x3.3 HV
<b>Packing</b>	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	600	V
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	2.2	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	1.7	
	Drain current (continuous) at $T_A = 25\text{ }^\circ\text{C}$	0.65	
	Drain current (continuous) at $T_A = 100\text{ }^\circ\text{C}$	0.5	
$I_{DM}^{(1)}$	Drain current pulsed	2.6	A
$P_{TOT}$	Total power dissipation at $T_A = 25\text{ }^\circ\text{C}$	2	W
	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	22	W
$I_{AS}$	Avalanche current, repetitive or non-repetitive (pulse width limited by $T_J$ max)	1	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AS}$ , $V_{DD} = 50\text{ V}$ )	119	mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$T_J$	Operating junction temperature range	-55 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature range		$^\circ\text{C}$

1. Pulse width is limited by safe operating area.

2.  $I_{SD} \leq 2.2\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DS}(\text{peak}) \leq V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance, junction-to-case	5.6	$^\circ\text{C}/\text{W}$
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient	62.5	$^\circ\text{C}/\text{W}$

1. When mounted on an 1-inch<sup>2</sup> FR-4, 2 Oz copper board,  $t < 10\text{ s}$ .

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified.

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	600			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$ , $T_C = 125\text{ °C}^{(1)}$			100	
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 1\text{ A}$		1.5	1.8	$\Omega$

1. Defined by design, not subject to production test.

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 50\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	188	-	pF
$C_{oss}$	Output capacitance		-	13	-	pF
$C_{rSS}$	Reverse transfer capacitance		-	1.1	-	pF
$C_{oss\ eq.}^{(1)}$	Equivalent capacitance energy related	$V_{DS} = 0\text{ to }480\text{ V}$ , $V_{GS} = 0\text{ V}$	-	100	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	6	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}$ , $I_D = 2.2\text{ A}$	-	9.5	-	nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 0\text{ to }10\text{ V}$	-	1.6	-	nC
$Q_{gd}$	Gate-drain charge	(see Figure 14. Test circuit for gate charge behavior)	-	5.3	-	nC

1.  $C_{oss\ eq.}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 1.1\text{ A}$ ,	-	8.6	-	ns
$t_r$	Rise time	$R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	6.2	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	20.8	-	ns
$t_f$	Fall time		-	20	-	ns

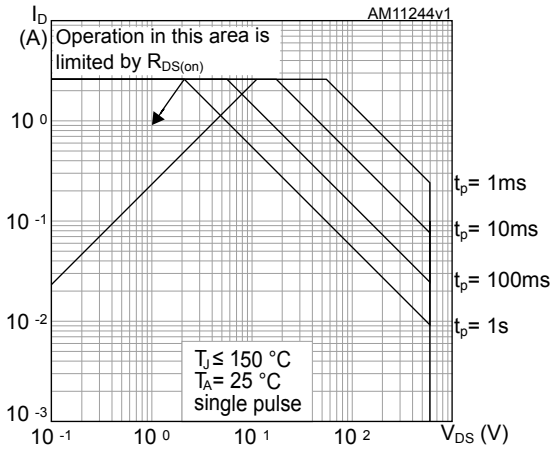
**Table 6. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		2.2	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		2.6	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 2.2 \text{ A}, V_{GS} = 0 \text{ V}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 2.2 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s},$	-	168		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60 \text{ V}$	-	672		nC
$I_{RRM}$	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	8		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 2.2 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s},$	-	2.3		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60 \text{ V}, T_J = 150 \text{ }^\circ\text{C}$	-	913		nC
$I_{RRM}$	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	9		A

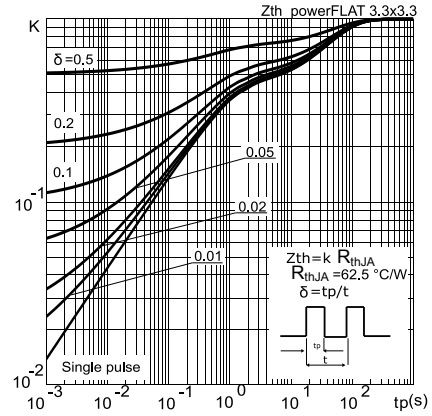
1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

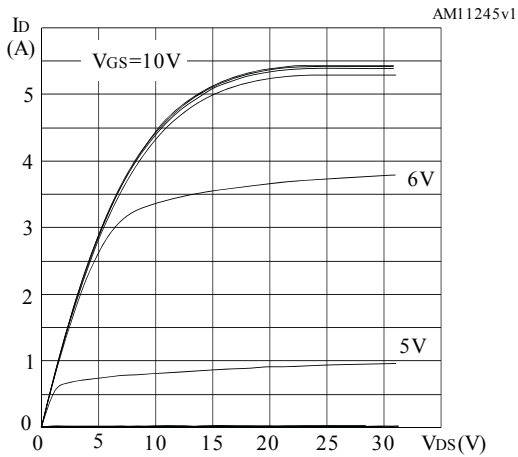
**Figure 1. Safe operating area**



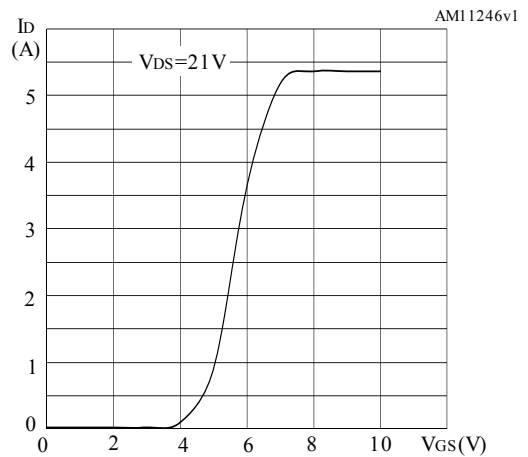
**Figure 2. Normalized transient thermal impedance**



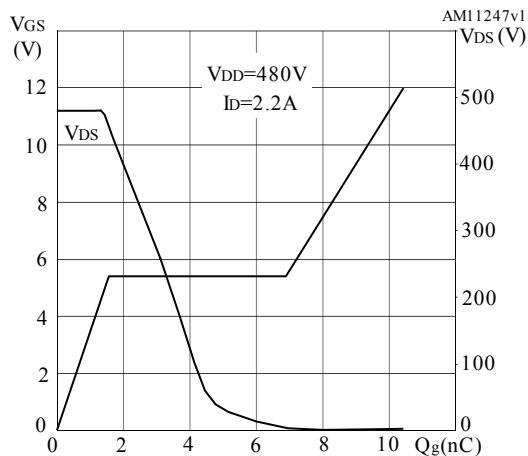
**Figure 3. Typical output characteristics**



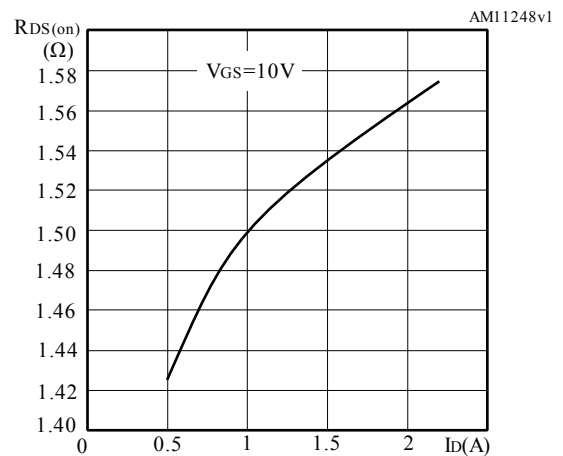
**Figure 4. Typical transfer characteristics**



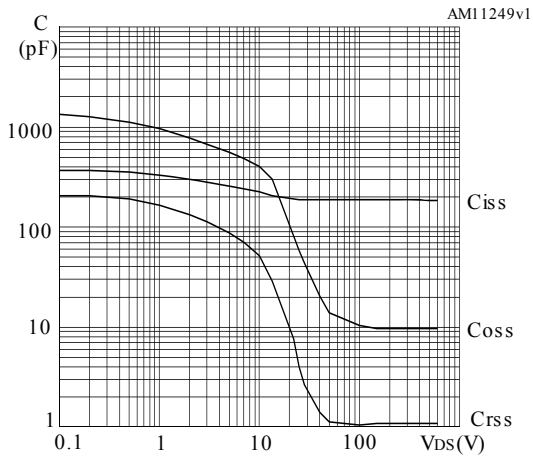
**Figure 5. Typical gate charge characteristics**



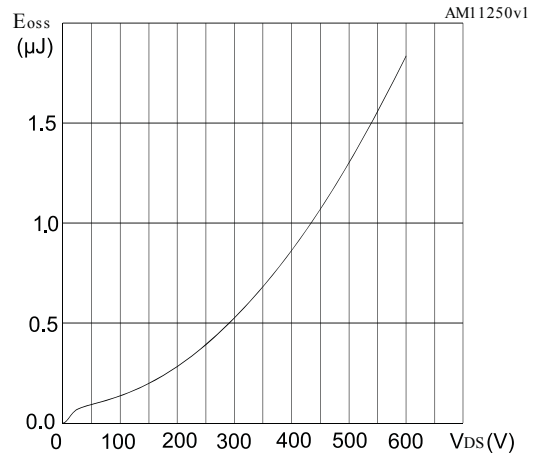
**Figure 6. Typical drain-source on-resistance**



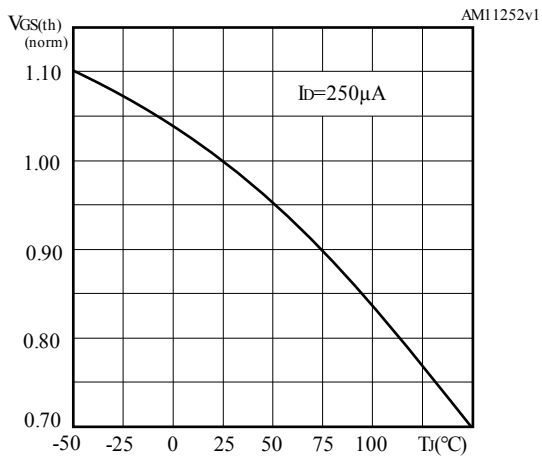
**Figure 7. Typical capacitance characteristics**



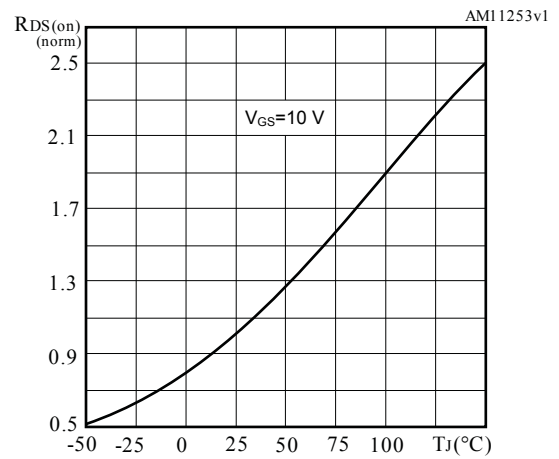
**Figure 8. Typical output capacitance stored energy**



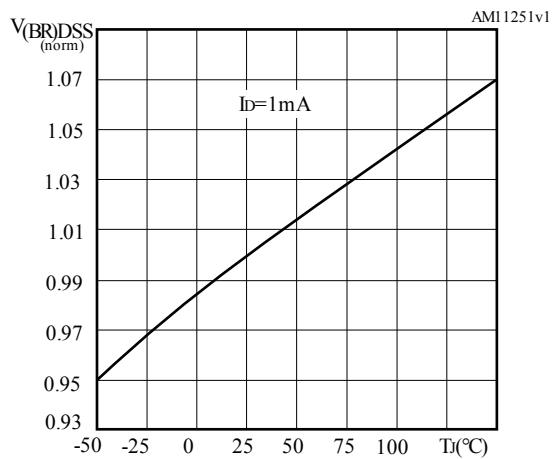
**Figure 9. Normalized gate threshold vs temperature**



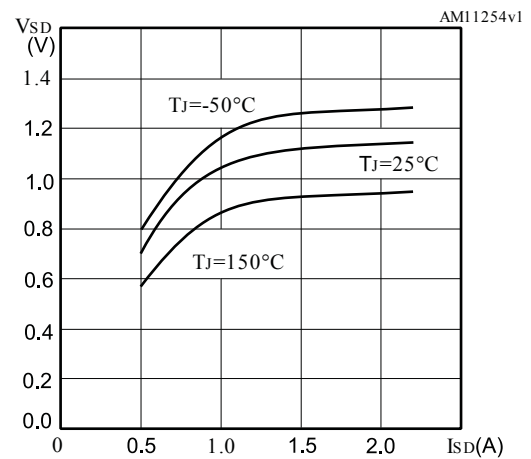
**Figure 10. Normalized on-resistance vs temperature**



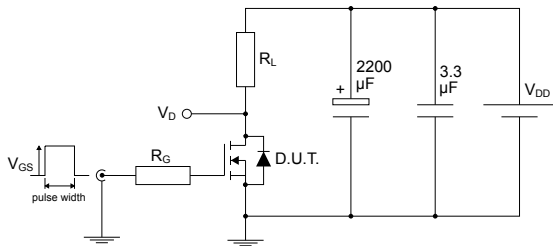
**Figure 11. Normalized breakdown voltage vs temperature**



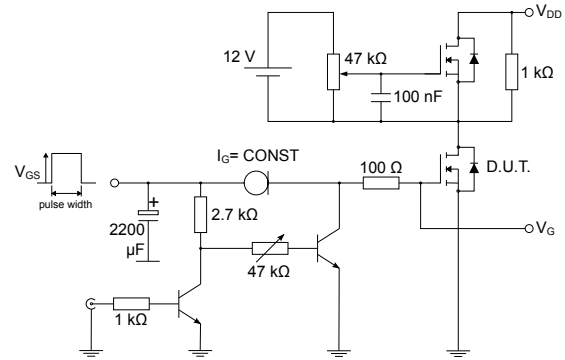
**Figure 12. Typical reverse diode forward characteristics**



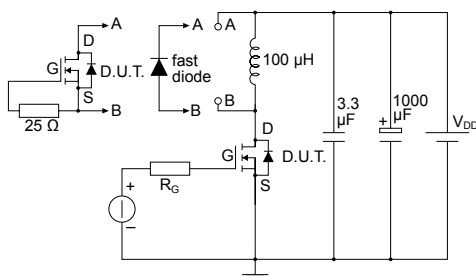
### 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**


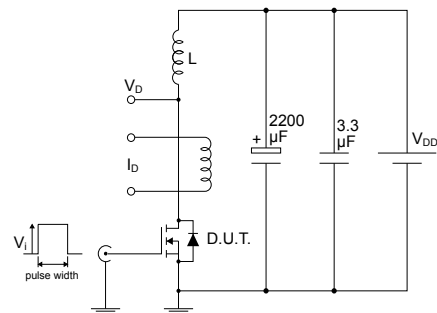
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**Figure 14. Test circuit for gate charge behavior**


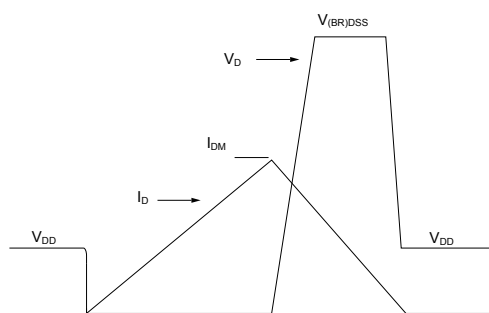
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**Figure 15. Test circuit for inductive load switching and diode recovery times**


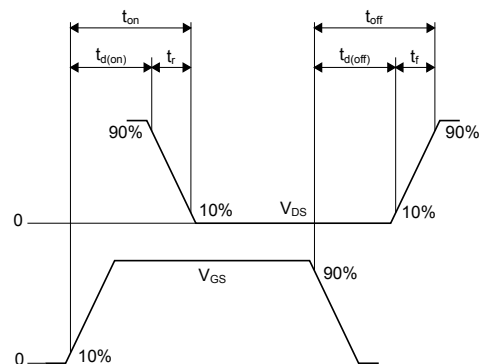
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**Figure 16. Unclamped inductive load test circuit**


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**Figure 17. Unclamped inductive waveform**


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**Figure 18. Switching time waveform**


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## 4 Package information

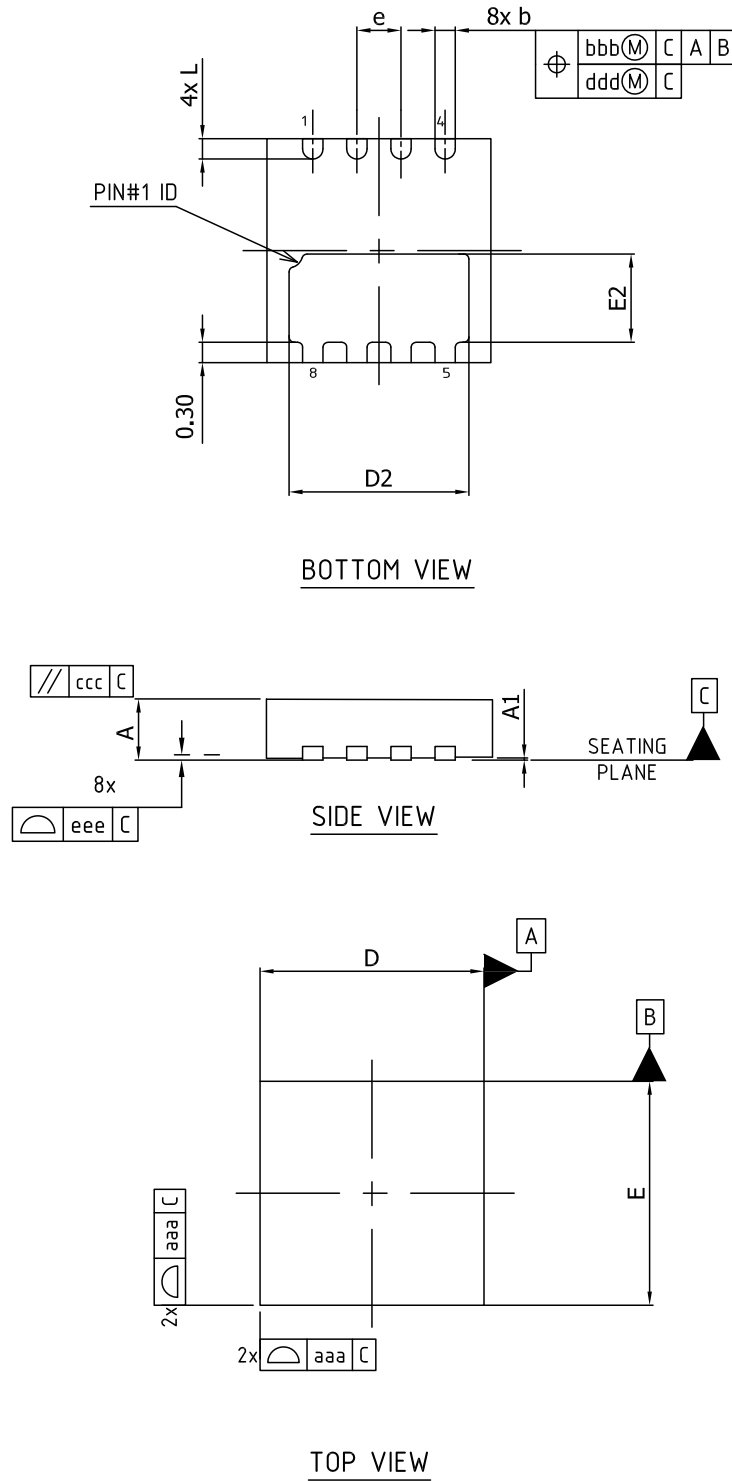
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In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.



### 4.1 PowerFLAT 3.3x3.3 HV package information

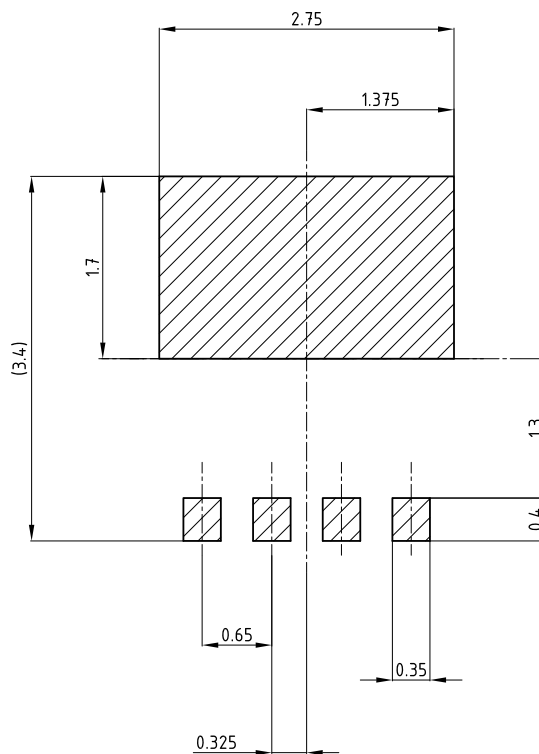
Figure 19. PowerFLAT 3.3x3.3 HV package outline



**Table 7. PowerFLAT 3.3x3.3 HV package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0	0.02	0.05
b	0.25	0.30	0.40
D		3.30	
D2	2.50	2.65	2.75
E		3.30	
E2	1.15	1.30	1.40
e		0.65	
L	0.20	0.30	0.40
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

**Figure 20. PowerFLAT 3.3x3.3 HV recommended footprint (dimensions are in mm)**



8374983\_footprint

## Revision history

**Table 8. Document revision history**

Date	Version	Changes
12-Mar-2012	1	First release.
19-Nov-2014	2	Document status changed from preliminary to production data. Updated <i>Figure 1.: Internal schematic diagram</i> , <i>Figure 2.: Safe operating area</i> , <i>Figure 3.: Thermal impedance</i> and <i>Figure 12.: Normalized <math>V_{(BR)DSS}</math> vs temperature.</i> Updated <i>Table 5.: Dynamic</i> and <i>Table 7.: Source drain diode.</i> Minor text changes.
26-May-2022	3	Modified marking on cover page Updated <i>Figure 1. Safe operating area</i> Modified $I_{SDM}$ value in <i>Table 6. Source-drain diode</i> Updated <i>Section 4.1 PowerFLAT 3.3x3.3 HV package information</i> Minor text changes.

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