34-Channel Symmetric Row Driver

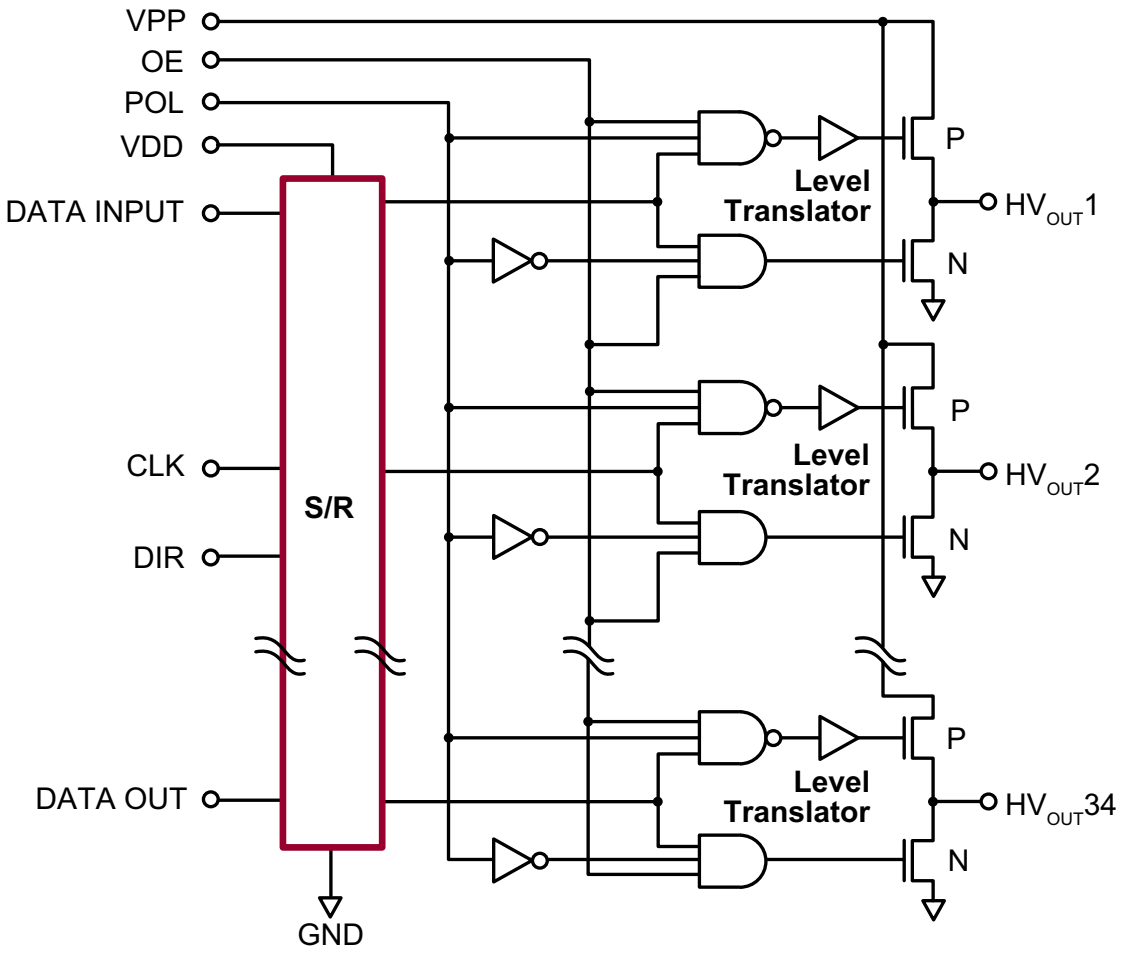
Features

- HVCMOS® technology
- Symmetric row drive (reduces latent imaging in ACTFEL displays)
- Output voltage up to +230V
- Low power level shifting
- Source/sink current minimum 70mA
- Shift register speed 4.0MHz
- Pin-programmable shift direction

General Description

The HV7022C is a low-voltage serial to high-voltage parallel converter with push-pull outputs. It is especially suited for use as a symmetric row driver in AC thin-film electroluminescent (ACTFEL) displays. The HV7022C offers 34 output lines, a direction (DIR) pin to give CW or CCW shift register loading, output enable (OE), and polarity (POL) control. After data is entered (on the falling edge of CLK), a logic high will cause the output to swing to VPP if POL is high, or to GND if POL is low.

Functional Block Diagram



Ordering Information

Device	Package Options	
	44-Lead Quad Cerpac Chip Carrier *.650x.650in body* *.190in height (max)* *.050in pitch*	44-Lead PLCC *.653x.653in body* *.180in height (max)* *.050in pitch*
HV7022-C	HV7022DJ-C*	HV7022PJ-C-G

-G indicates package is RoHS compliant ('Green')
** Hi-Rel process flow available.*

Absolute Maximum Ratings

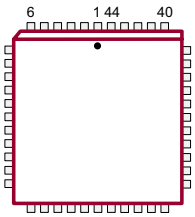
Parameter	Value
Supply voltage, V_{DD}	-0.3V to +15V
Supply voltage, V_{PP}	-0.3V to +250V
Logic input levels	-0.3V to V_{DD} +0.3V
Ground current[1]	1.5A
Continuous total power dissipation[2] Plastic Ceramic	 1200mW 1500mW
Operating temperature range Plastic Ceramic	 -40°C to +85°C -55°C to +125°C
Storage temperature range	-65°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

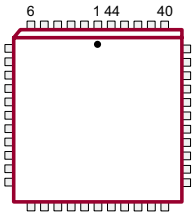
Notes:

1. *Duty cycle is limited by the total power dissipated in the package.*
2. *For operation above 25°C ambient derate linearly to maximum operating temperature at 25mW/°C for plastic and at 15mW/°C for ceramic.*

Pin Configuration



44-Lead Quad Cerpac Chip Carrier (DJ)
(top view)

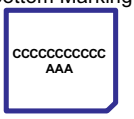


44-Lead PLCC (PJ)
(top view)

Product Marking

Top Marking

Bottom Marking



YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*

**May be part of top marking*

Package may or may not include the following marks: Si or

44-Lead Quad Cerpac Chip Carrier (DJ)

Top Marking

Bottom Marking

YY = Year Sealed
WW = Week Sealed
L = Lot Number
A = Assembler ID
C = Country of Origin*
_____ = "Green" Packaging

**May be part of top marking*

Package may or may not include the following marks: Si or

44-Lead PLCC (PJ)

Recommended Operating Conditions

Sym	Parameter		Min	Max	Units
V_{DD}	Logic supply voltage		10.8	13.2	V
V_{PP}	High voltage supply		-	230	V
V_{IH}	High-level input voltage	V_{DD} = 10.8	8.1	-	V
		V_{DD} = 13.2	9.9	-	
V_{IL}	Low-level input voltage	V_{DD} = 10.8	-	2.7	V
		V_{DD} = 13.2	-	3.3	
f_{CLK}	Clock frequency		-	4.0	MHz
T_A	Operating free-air temperature	Plastic	-40	+85	°C
		Ceramic	-55	+125	
I_{OD}	Allowable pulsed current through output diode		-	±300	mA

Power-up sequence should be the following:

1. *Connect ground.*
2. *Apply V_{DD}.*
3. *Set all inputs (Data, CLK, Enable, etc.) to a known state.*
4. *Apply V_{PP}.*

(The V_{PP} should not drop below V_{DD} or float during operation.)

Power-down sequence should be the reverse of the above.

DC Electrical Characteristics *(over recommended operating conditions of V_{DD} = 12V, V_{PP} = 230V, and T_A = 25°C unless noted)*

Sym	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current		-	10	mA	f_{CLK} = 4.0MHz, V_{DD} =13.2V
I_{PP}	V_{PP} supply current		-	4.0	mA	One output high[1]
			-	100	µA	All outputs low or High-Z
			-	750		All outputs low or High-Z (125°C)
I_{DDQ}	Quiescent V_{DD} supply current		-	100	µA	All V_{IN} = GND or V_{DD}
V_{OH}	High-level output	HV_{OUT}	195	-	V	I_O = -70mA
		DATA OUT	11	-	V	I_O = -500µA
V_{OL}	Low-level output	HV_{OUT}	-	30	V	I_O = +70mA
		DATA OUT	-	1.0	V	I_O = +500µA
I_{IH}	High-level logic input current		-	1.0	µA	V_{IH} = 12V
I_{IL}	Low-level logic input current		-	-1.0	µA	V_{IL} = 0V

Note:

1. *The total number of ON outputs times the duty cycle must not exceed the allowable package power dissipation.*

AC Electrical Characteristics (V_{DD} = 12V and T_A = 25°C)

Sym	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency	-	4.0	MHz	---
t_{WH}, t_{WL}	Pulse duration clock width high or low	125	-	ns	---
t_{SUD}	Data set-up time before falling clock	100	-	ns	---
t_{HD}	Data hold time after falling clock	100	-	ns	---
t_{SUC}	Setup time clock low before V_{PP}↑ or GND↓	300	-	ns	---
t_{SUE}	Setup time enable high before V_{PP}↑ or GND↓	300	-	ns	---
t_{SUP}	Setup time polarity high or low before V_{PP}↑ or GND↓	300	-	ns	---
t_{HC}	Hold time clock high after V_{PP}↑ or GND↓	500	-	ns	---
t_{HE}	Hold time enable high after V_{PP}↑ or GND↓	300	-	ns	---
t_{HP}	Hold time polarity high or low after V_{PP}↑ or GND↓	300	-	ns	---
t_{DHL}	Delay time high to low-level output from clock	-	150	ns	C_L = 10pF
t_{DLH}	Delay time low to high-level output from clock	-	200	ns	C_L = 10pF
t_{THL}	Transition time high to low-level serial output	-	200	ns	C_L = 15pF
t_{TLH}	Transition time low to high-level serial output	-	100	ns	C_L = 15pF
t_{ONH}	High-level turn-on time HV_{OUT} from enable	-	500	ns	V_{OH} = 195V, R_L = 2.0kΩ to 95V
t_{ONL}	Low-level turn-on time HV_{OUT} from enable	-	500	ns	V_{OH} = 130V, R_L = 2.0kΩ to 30V
t_{OFFH}	High-level turn-off time HV_{OUT} from enable	-	1000	ns	V_{OH} = 195V, R_L = 2.0kΩ to 95V
t_{OFFL}	Low-level turn-off time HV_{OUT} from enable	-	500	ns	V_{OH} = 130V, R_L = 2.0kΩ to 30V
SR	Slew rate, V_{PP} or GND	-	45	V/µs	One active output driving 4.7nF load to V_{PP} or GND

Function Table

I/O Relations	Inputs					Outputs		
	CLK	DIR	DATA	POL	OE	Shift Reg	HV_{OUT}	DATA OUT
O/P HIGH	X	X	H	H	H	*	H	*
O/P OFF	X	X	L	H	H	*	HIGH-Z	*
O/P LOW	X	X	H	L	H	*	L	*
O/P OFF	X	X	L	L	H	*	HIGH-Z	*
O/P OFF	X	X	X	X	L	*	All O/P HIGH-Z	*
Load S/R, set DIR	↓	L	X	X	X	$Q_n \rightarrow Q_{n+1}$	*	Q_{34}
	↓	H	X	X	X	$Q_n \rightarrow Q_{n-1}$	*	Q_1
	No ↓	X	X	X	X	*	No Change	No Change

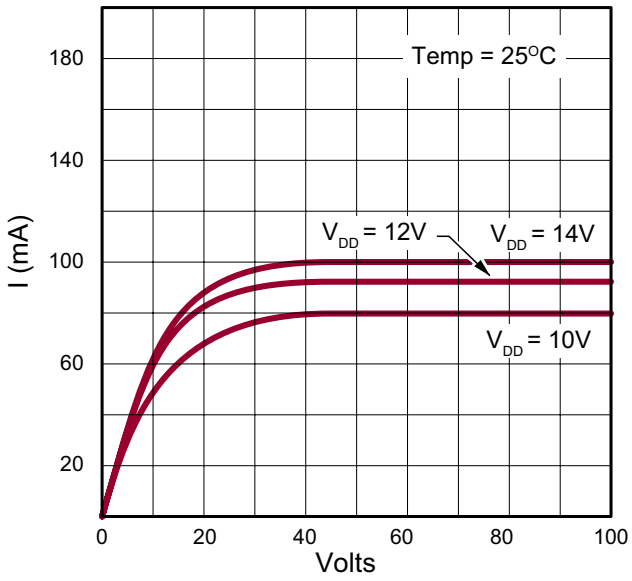
Notes:

H = logic high level, L = logic low level, X = irrelevant, ↓ = high-to-low transition

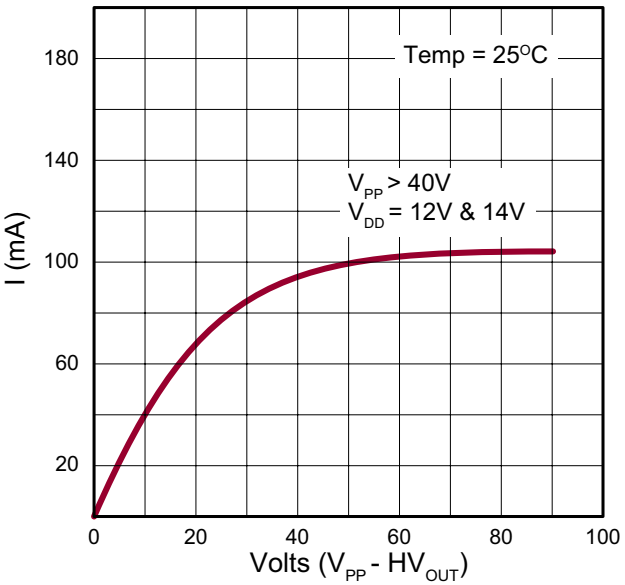
Q1 = $HV_{OUT}1$, Qn = $HV_{OUT}n$, etc.

** = dependent on previous state and whether an O/P or S/R command occurred.*

HV_{OUT} Characteristics

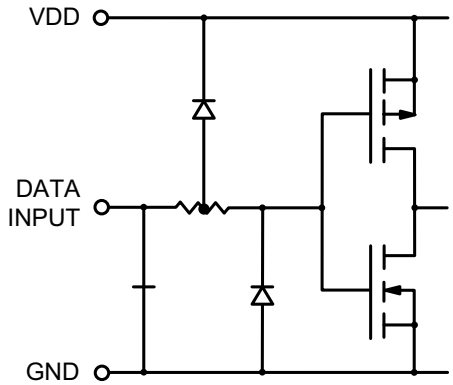


Output N-Channel Characteristics through FET

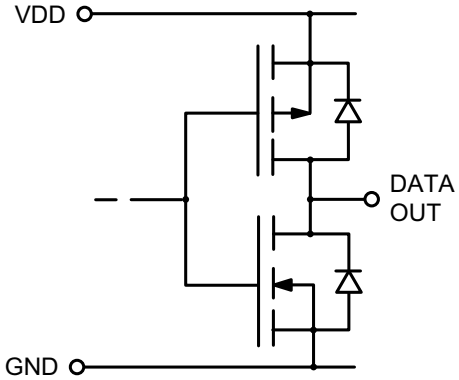


Output P-Channel Characteristics through FET

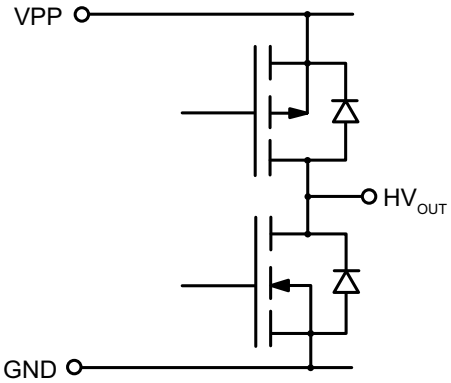
Input and Output Equivalent Circuits



Logic Inputs

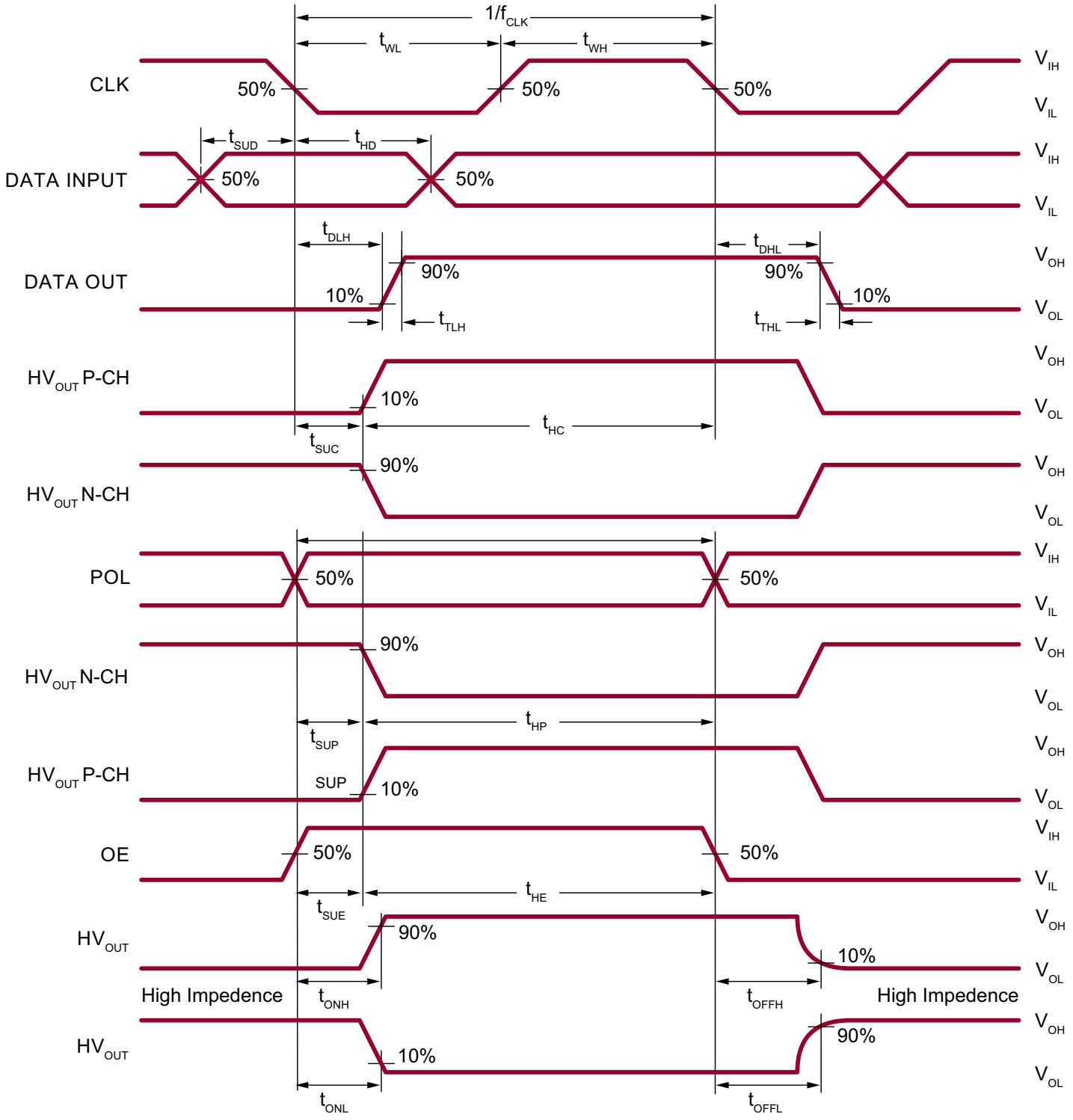


Logic Data Output



High Voltage Outputs

Switching Waveforms



Pin Descriptions

Pin #	Function
1	HV_{OUT}18/17
2	HV_{OUT}17/18
3	HV_{OUT}16/19
4	HV_{OUT}15/20
5	HV_{OUT}14/21
6	HV_{OUT}13/22
7	HV_{OUT}12/23
8	HV_{OUT}11/24
9	HV_{OUT}10/25
10	HV_{OUT}9/26
11	HV_{OUT}8/27
12	HV_{OUT}7/28
13	HV_{OUT}6/29
14	HV_{OUT}5/30
15	HV_{OUT}4/31
16	HV_{OUT}3/32
17	HV_{OUT}2/33
18	HV_{OUT}1/34
19	DATA OUT
20	OE
21	CLK
22	GND

Pin #	Function
23	DIR
24	VDD
25	POL
26	DATA INPUT
27	VPP
28	NC
29	HV_{OUT}34/1
30	HV_{OUT}33/2
31	HV_{OUT}32/3
32	HV_{OUT}31/4
33	HV_{OUT}30/5
34	HV_{OUT}29/6
35	HV_{OUT}28/7
36	HV_{OUT}27/8
37	HV_{OUT}26/9
38	HV_{OUT}25/10
39	HV_{OUT}24/11
40	HV_{OUT}23/12
41	HV_{OUT}22/13
42	HV_{OUT}21/14
43	HV_{OUT}20/15
44	HV_{OUT}19/16

Note:

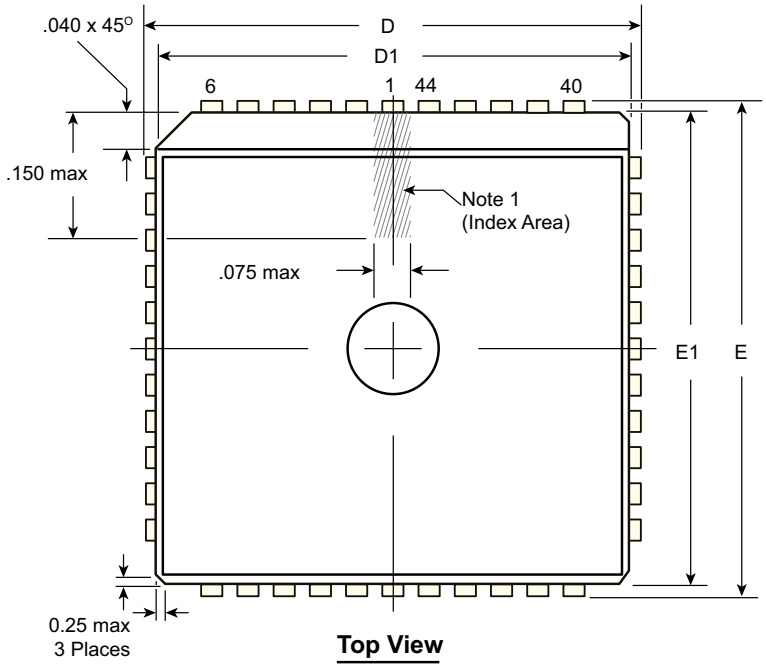
Pin designation for DIR H/L

Example: For DIR = H, pin 1 is HV_{OUT}18

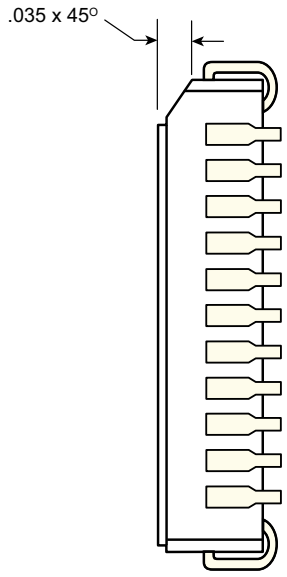
For DIR = L, pin 1 is HV_{OUT}17

44-Lead Quad Cerpac Package Outline (DJ)

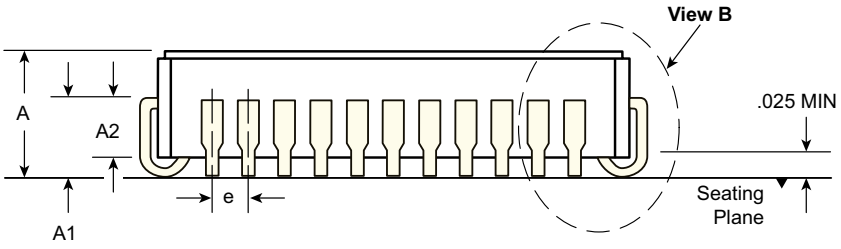
.650x.650in body, .190in height (max), .050in pitch



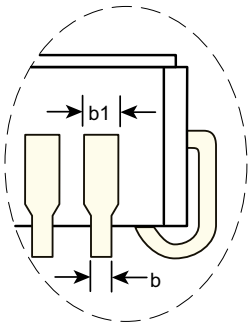
Top View



Vertical Side View



Horizontal Side View



View B

Note:

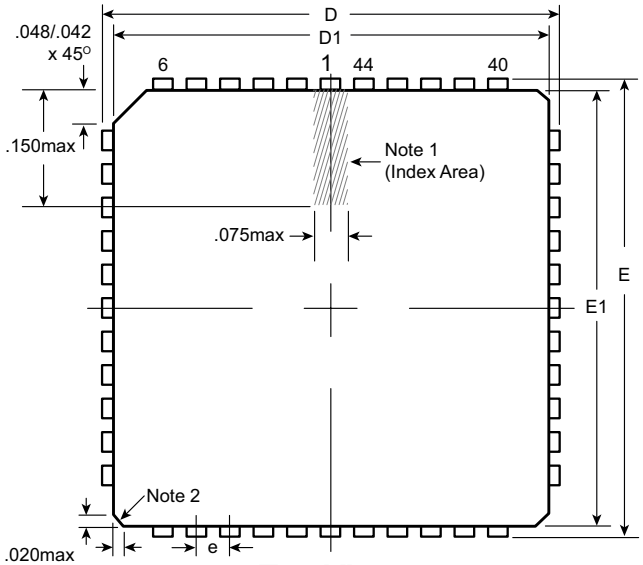
1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	b1	D	D1	E	E1	e
Dimension (inches)	MIN	.155	.090	.060 REF	.017	.026	.685	.630	.685	.630	.050 BSC
	NOM	.172	.100		.019	.029	.690	.650	.690	.650	
	MAX	.190	.120		.021	.032	.695	.665	.695	.665	

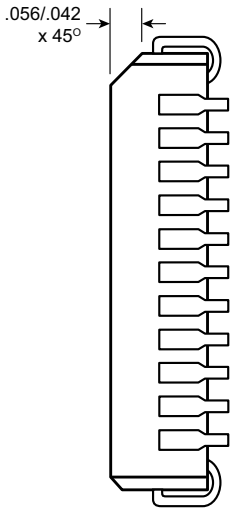
JEDEC Registration MO-087, Variation AB, Issue B, August, 1991.
Drawings not to scale.
Supertex Doc. #: *DSPD-44CERPACDJ, Version D090808.*

44-Lead PLCC Package Outline (PJ)

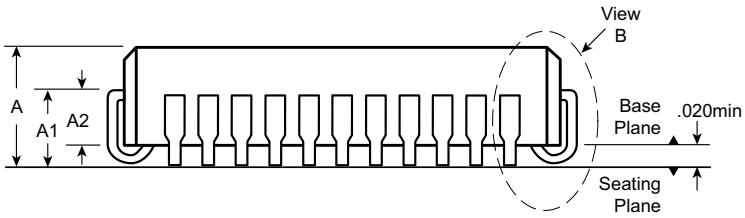
.653x.653in body, .180in height (max), .050in pitch



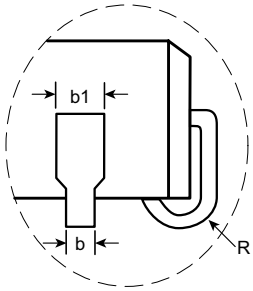
Top View



Vertical Side View



Horizontal Side View



View B

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Actual shape of this feature may vary.*

Symbol		A	A1	A2	b	b1	D	D1	E	E1	e	R
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.685	.650	.685	.650	.050 BSC	.025
	NOM	.172	.105	-	-	-	.690	.653	.690	.653		.035
	MAX	.180	.120	.083	.021	.036†	.695	.656	.695	.656		.045

JEDEC Registration MS-018, Variation AC, Issue A, June, 1993.
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
Supertex Doc. #: *DSPD-44PLCCPJ, Version F031111.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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