



# FAN302HL

## mWSaver™ PWM Controller for Low Standby Power Battery-Charger Applications

### Features

- mWSaver™ Technology Provides Industry's Best-in-Class Standby Power
  - Achieve Under 10mW; Far Below Energy Star's 5-Star Level (<30mW)
  - Proprietary 500V High-Voltage JFET Startup Reduces Startup Resistor Loss
  - Low Operation Current in Burst Mode: Maximum 350µA
- Constant-Current (CC) Control without Secondary-Feedback Circuitry
- Fixed PWM Frequency at 85kHz with Frequency Hopping to Solve EMI Problem
- Low Operating Current: 3.5mA
- Peak-Current-Mode Control in CV Regulation
- Cycle-by-Cycle Current Limiting
- V<sub>DD</sub> Over-Voltage Protection (Auto-Restart)
- V<sub>S</sub> Over-Voltage Protection (Latch Mode)
- V<sub>DD</sub> Under-Voltage Lockout (UVLO)
- Gate Output Maximum Voltage Clamped at 15V
- Fixed Over-Temperature Protection (Latch Mode)
- Available in an 8-Lead SOIC Package

### Applications

Battery chargers for cellular phones, cordless phones, PDA, digital cameras, and power tools. Replaces linear transformers and RCC SMPS.

### Description

This highly integrated PWM controller, FAN302HL, provides several features to enhance the performance of general flyback converters. The constant-current-control, proprietary topology enables simplified circuit designs without secondary feedback circuitry for battery-charger applications.

A proprietary Burst-Mode function with low operation current minimizes standby power consumption.

The FAN302HL controller also provides several protections. Cycle-by-cycle current limiting ensures the fixed peak current limit level, even if a short circuit occurs. The gate output is clamped at 15V to protect the power MOS from high gate-source voltage conditions. If either V<sub>S</sub> OVP or internal OTP is triggered, the circuit enters Latch Mode until AC power is removed.

Using FAN302HL, a charger can be implemented with few external components and minimized cost, compared to a conventional design or a linear transformer. A typical output CV/CC characteristic is shown in Figure 1.

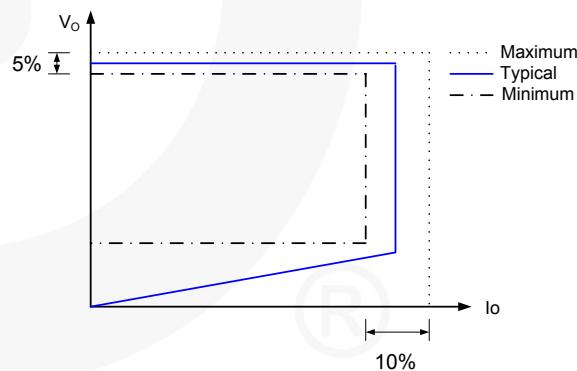


Figure 1. Typical Output V-I Characteristic

### Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN302HLMY	-40°C to +105°C	8-Lead, Small Outline Package (SOIC), JEDEC MS-012, .150-Inch Narrow Body	Tape & Reel

### Application Diagram

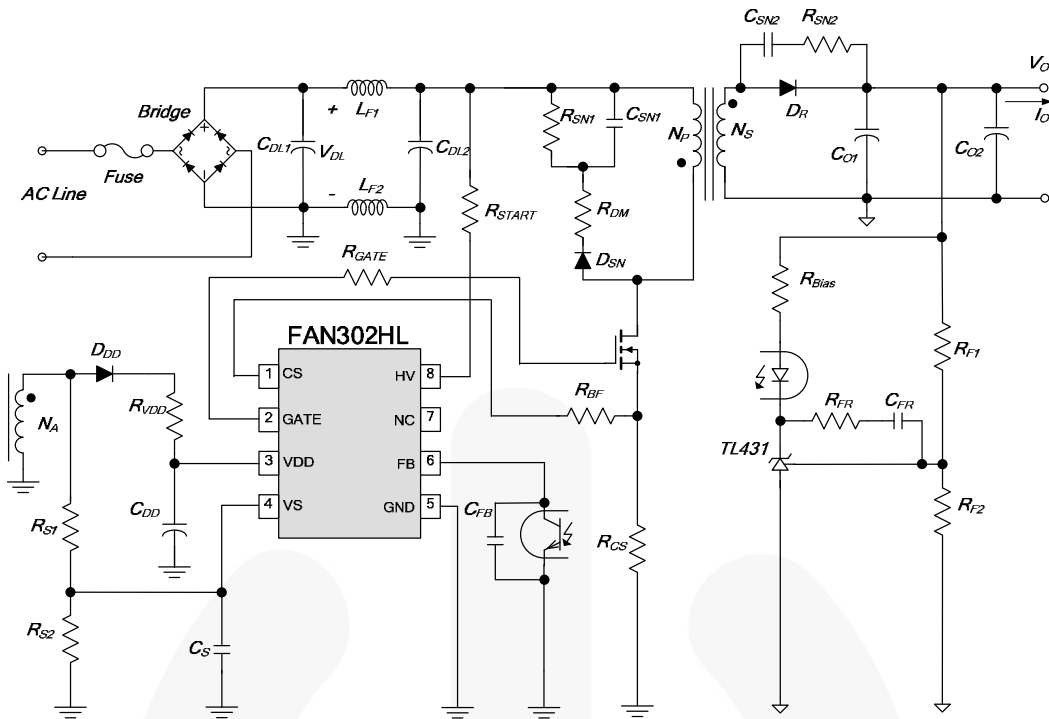


Figure 2. Typical Application

### Internal Block Diagram

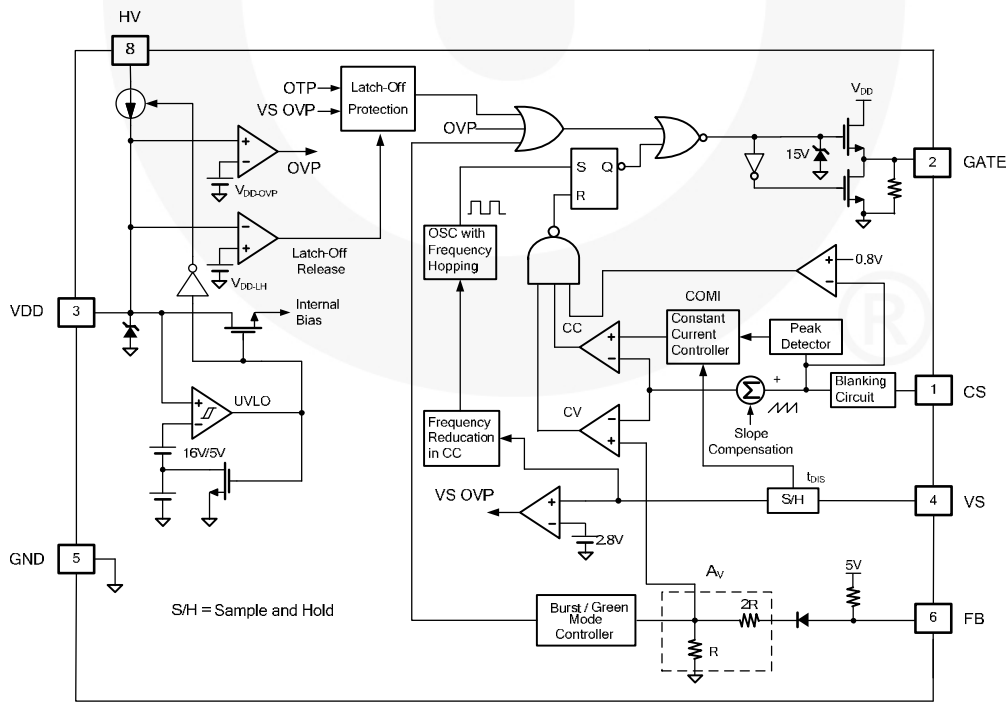
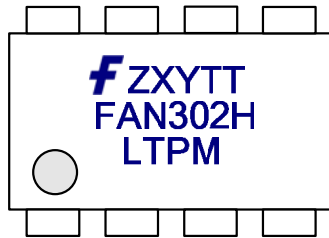


Figure 3. Functional Block Diagram

## Marking Information



F: Fairchild Logo  
 Z: Assembly Plant Code  
 X: Year Code  
 Y: Week Code  
 TT: Die Run Code  
 T: M=SOP  
 P: Y= Green Package  
 M: Manufacture Flow Code

Figure 4. Top Mark

## Pin Configuration

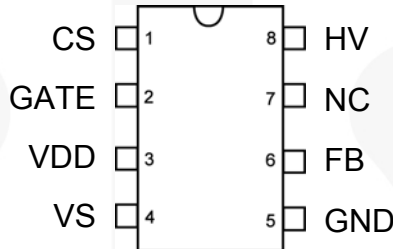


Figure 5. Pin Assignments

## Pin Definitions

Pin #	Name	Description
1	CS	<b>Current Sense.</b> This pin connects a current-sense resistor to detect the MOSFET current for Peak-Current-Mode control in CV regulation and provides the output-current regulation in CC regulation.
2	GATE	<b>PWM Signal Output.</b> This pin uses the internal totem-pole output driver to drive the power MOSFET. It is internally clamped below 15V.
3	VDD	<b>Power Supply.</b> IC operating current and MOSFET driving current are supplied using this pin. This pin is connected to an external $V_{DD}$ capacitor. The threshold voltages for startup and turn-off are 16V and 5V, respectively.
4	VS	<b>Voltage Sense.</b> This pin detects the output voltage information and discharge time based on voltage of auxiliary winding.
5	GND	<b>Ground</b>
6	FB	<b>Feedback.</b> The FB pin provides feedback information to the internal PWM comparator. This feedback is used to control the duty cycle in CV regulation.
7	NC	<b>No Connect</b>
8	HV	<b>High Voltage.</b> This pin connects to bulk capacitor for high-voltage startup.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V <sub>HV</sub>	HV Pin Input Voltage			500	V
V <sub>VDD</sub>	DC Supply Voltage <sup>(1,2)</sup>			30	V
V <sub>VS</sub>	VS Pin Input Voltage		-0.3	7.0	V
V <sub>CS</sub>	CS Pin Input Voltage		-0.3	7.0	V
V <sub>FB</sub>	FB Pin Input Voltage		-0.3	7.0	V
P <sub>D</sub>	Power Dissipation (T <sub>A</sub> =25°C)			660	mW
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Air)			150	°C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)			39	°C/W
T <sub>J</sub>	Operating Junction Temperature		-40	+150	°C
T <sub>STG</sub>	Storage Temperature Range		-55	+150	°C
T <sub>L</sub>	Lead Temperature, (Wave soldering or IR, 10 Seconds)			+260	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JEDEC:JESD22_A114 (Except HV Pin) <sup>(3)</sup>		5.0	kV
		Charged Device Model, JEDEC:JESD22_C101 (Except HV Pin) <sup>(3)</sup>		1.5	

### Notes:

- All voltage values, except differential voltages, are given with respect to GND pin.
- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
- ESD ratings including HV pin: HBM=400V, CDM=750V.

## Electrical Characteristics

$V_{DD}=15V$  and  $T_A=25^\circ C$  unless noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>HV Section</b>						
$V_{HV-MIN}$	Minimum Startup Voltage on HV Pin				50	V
$I_{HV}$	Supply Current Drawn from HV Pin	$V_{AC}=90V$ , $V_{DD}=0V$ , Controller Off	0.8	1.5	5.0	mA
$I_{HV-LC}$	Leakage Current Drawn from HV Pin	With Auxiliary Supply, $V_{HV}=500V$ , $V_{DD}=15V$ , Controller On		0.8	3.0	$\mu A$
<b>V<sub>DD</sub> Section</b>						
$V_{OP}$	Continuously Operation Voltage				25	V
$V_{DD-ON}$	Turn-On Threshold Voltage		15	16	17	V
$V_{DD-OFF}$	Turn-Off Threshold Voltage		4.7	5.0	5.3	V
$V_{DD-LH}$	Threshold Voltage for Latch-Off Release			2.50		V
$I_{DD-ST}$	Startup Current	$V_{DD}=V_{DD-ON} - 0.16V$		400	450	$\mu A$
$I_{DD-OP}$	Operating Supply Current	$V_{DD}=18V$ , $f=f_{OSC}$ , $C_L=1nF$		3.5	4.0	mA
$I_{DD-BURST}$	Burst-Mode Operating Supply Current	$V_{DD}=8V$ , $C_L=1nF$		200	350	$\mu A$
$V_{DD-OVP}$	$V_{DD}$ Over-Voltage Protection Level	Auto-Restart	25.5	26.5	27.5	V
$t_{D-VDDOVP}$	$V_{DD}$ Over-Voltage Protection Debounce Time	$f=85kHz$		100	180	$\mu s$
<b>Oscillator Section</b>						
$f_{OSC}$	Frequency	Center Frequency	$V_{CS}=5V$ , $V_S=2.5$ , $V_{FB}=5V$			kHz
		Hopping Range		$\pm 3$		
$t_{FHR}$	Frequency Hopping Period			2.84		ms
$f_{OSC-CM-MIN}$	Minimum Frequency if CCM (Continuous Current Mode)		13	18	23	kHz
$f_{OSC-CCM}$	Minimum Frequency in CC Regulation (Constant Current Regulation)	$V_{CS}=5V$ , $V_S=0V$	23	26	29	kHz
<b>Feedback Input Section</b>						
$A_V$	FB Input to Current Comparator Attenuation		1/3.5	1/3.0	1/2.5	V/V
$Z_{FB}$	Input Impedance		38	42	44	k $\Omega$
$V_{FB-OPEN}$	Output High Voltage	FB Pin Open		5.3		V
$V_{FB-G}$	Green Mode Ending Voltage		1.7	1.8	1.9	V
$V_{FB-L}$	Enter Zero Duty Cycle of FB Voltage	$V_{CS}=5V$ , $V_S=0V$	1.2	1.4	1.6	V
$V_{FB-H}$	Leave Zero Duty Cycle of FB Voltage	$V_{CS}=5V$ , $V_S=0V$	1.3	1.5	1.7	V
<b>Over-Temperature Protection Section</b>						
$T_{OTP}$	Threshold Temperature for Over-Temperature Protection		+130	+140	+150	$^\circ C$

Continued on the following page...

**Electrical Characteristics** (Continued)V<sub>DD</sub>=15V and T<sub>A</sub>=25°C unless noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>Voltage-Sense Section</b>						
I <sub>TC</sub>	Bias Current	V <sub>CS</sub> =5V	8.75	10.00	11.25	μA
V <sub>VS-CM-MIN</sub>	V <sub>S</sub> Threshold Voltage of ZCD Undetectable Protection			0.55		V
V <sub>VS-CM-MAX</sub>	V <sub>S</sub> Threshold Voltage of ZCD Undetectable Protection			0.75		V
V <sub>SN-CC</sub>	Starting Voltage of Frequency Decreasing of CC	V <sub>CS</sub> =5V, f <sub>S1</sub> =f <sub>OSC</sub> -2KHz		2.15		V
V <sub>SG-CC</sub>	Ending Voltage of Frequency Decreasing of CC	V <sub>CS</sub> =5V, f <sub>S2</sub> =f <sub>OSC</sub> +2KHz		0.70		V
S <sub>G-CC</sub>	Frequency Decreasing Slop of CC Regulation	$S_{G-CC} = \frac{(f_{S1}-f_{S2})}{(V_{SN-CC}-V_{SG-CC})}$	30	38	46	Hz/mV
V <sub>VS-OFFSET</sub>	ZCD Turn-Off Threshold			200		mV
V <sub>VS-OVP</sub>	Output Over-Voltage Protection		2.7	2.80	2.85	V
t <sub>VS-OVP</sub>	Output Over-Voltage Protection Debounce Time	f=85kHz		100	180	μs
<b>Current-Sense Section</b>						
V <sub>VR</sub>	Reference Voltage		2.475	2.500	2.525	V
V <sub>CCR</sub>	Variation Test Voltage on CS Pin for Constant Current Output	V <sub>CS</sub> =0.47V	2.405	2.430	2.455	V
V <sub>STH</sub>	Threshold Voltage for Current Limit			0.8		V
V <sub>STH-VA</sub>	Threshold Voltage for Current Limit at Power Mode (V <sub>VS-CM-MAX</sub> < 0.75V)	V <sub>VS</sub> =0.3V	0.25	0.30	0.35	V
t <sub>PD</sub>	Propagation Delay to GATE Output			100	200	ns
t <sub>MIN</sub>	Minimum On Time	V <sub>VS</sub> =0V, V <sub>CS</sub> =5V	430	530	630	ns
t <sub>LEB</sub>	Leading-Edge Blanking Time		300	400	500	ns
V <sub>SLOPE</sub>	Slope Compensation	Maximum Duty Cycle		0.3		V
<b>GATE Section</b>						
DCY <sub>MAX</sub>	Maximum Duty Cycle		64	67	70	%
V <sub>GATE-L</sub>	Output Voltage Low	V <sub>DD</sub> =25V, I <sub>O</sub> =10mA			1.5	V
V <sub>GATE-H</sub>	Output Voltage High	V <sub>DD</sub> =8V, I <sub>O</sub> =1mA	5		8	V
V <sub>GATE-H</sub>	Output Voltage High	V <sub>DD</sub> =5.5V, I <sub>O</sub> =1mA	4.0		5.5	V
t <sub>r</sub>	Rising Time	V <sub>DD</sub> =15V, C <sub>L</sub> =1nF	100	140	180	ns
t <sub>f</sub>	Falling Time	V <sub>DD</sub> =15V, C <sub>L</sub> =1nF	30	50	70	ns
V <sub>GATE-CLAMP</sub>	Output Clamp Voltage	V <sub>DD</sub> =25V	13	15	17	V

## Typical Performance Characteristics

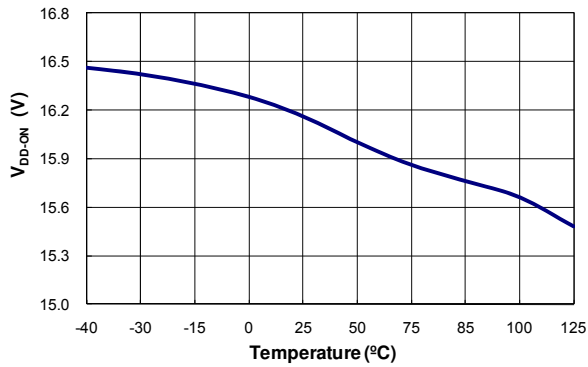


Figure 6. V<sub>DD</sub> Turn-On Threshold Voltage (V<sub>DD-ON</sub>) vs. Temperature

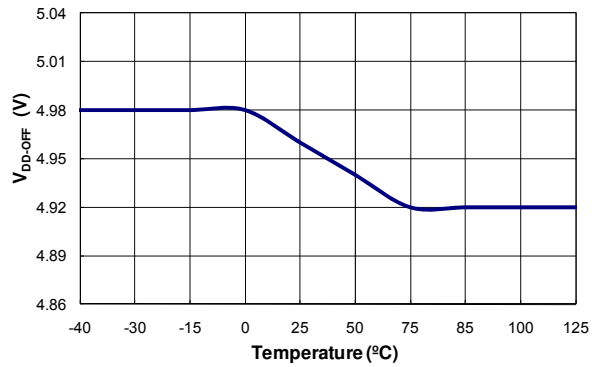


Figure 7. V<sub>DD</sub> Turn-Off Threshold Voltage (V<sub>DD-OFF</sub>) vs. Temperature

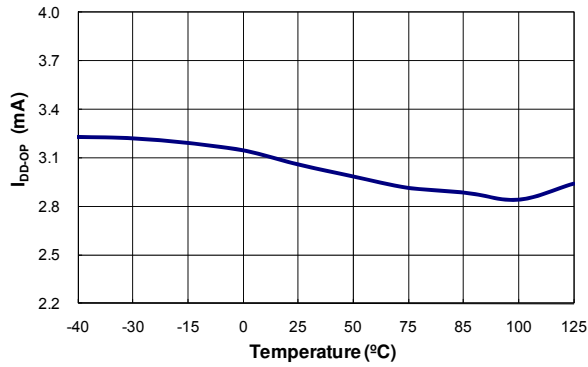


Figure 8. Operating Current (I<sub>DD-OP</sub>) vs. Temperature

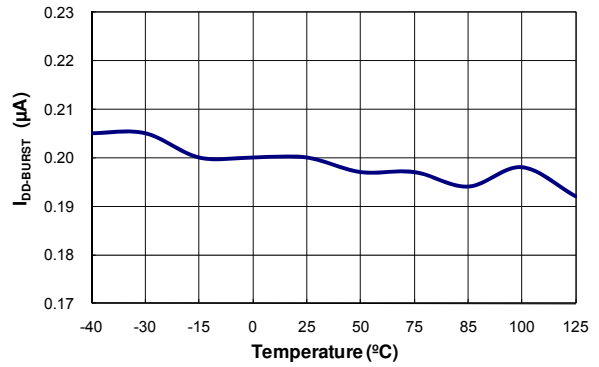


Figure 9. Burst Mode Operating Current (I<sub>DD-BURST</sub>) vs. Temperature

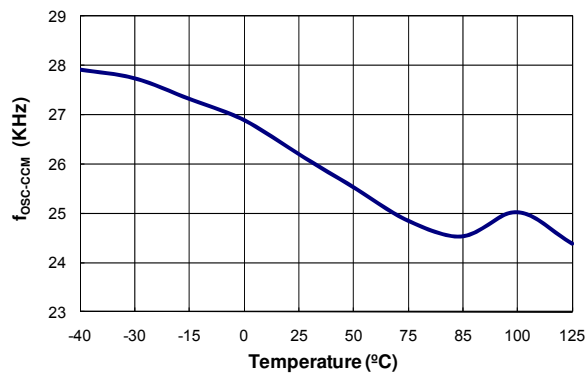


Figure 10. CC Regulation Minimum Frequency (f<sub>OSC-CCM</sub>) vs. Temperature

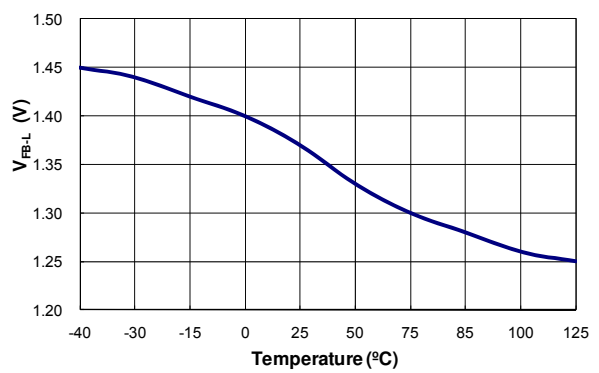
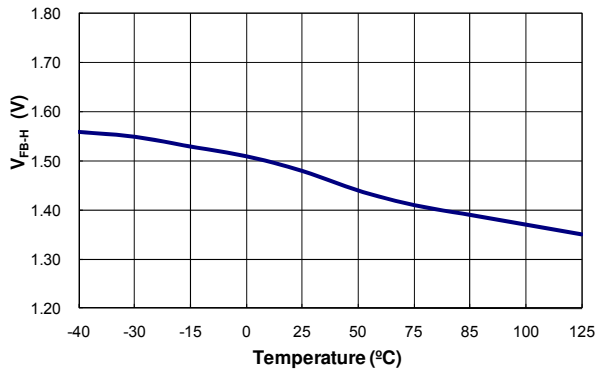
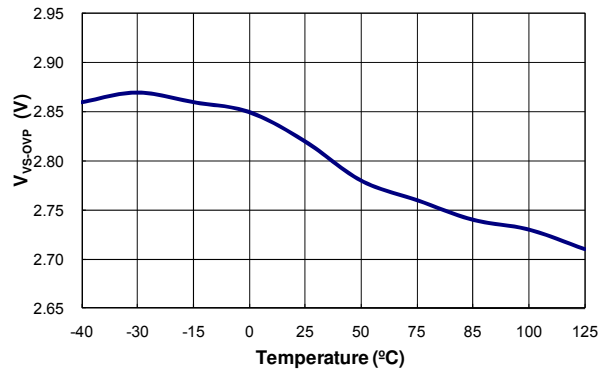


Figure 11. Enter Zero Duty Cycle of FB Voltage (V<sub>FB-L</sub>) vs. Temperature

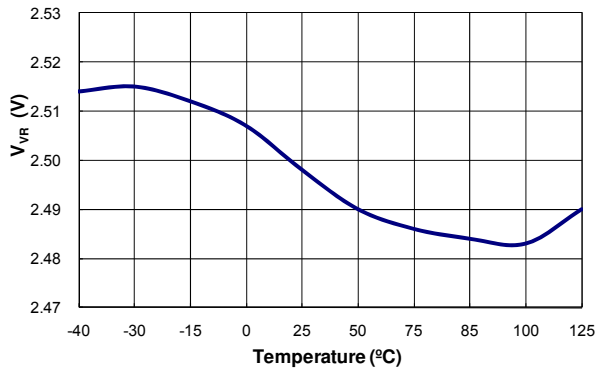
## Typical Performance Characteristics



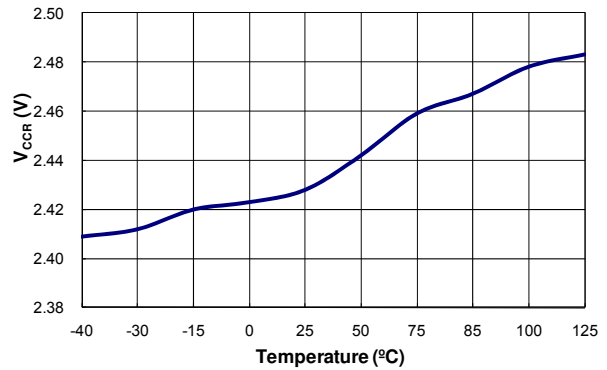
**Figure 12. Leave Zero Duty Cycle of FB Voltage (V<sub>FB-H</sub>) vs. Temperature**



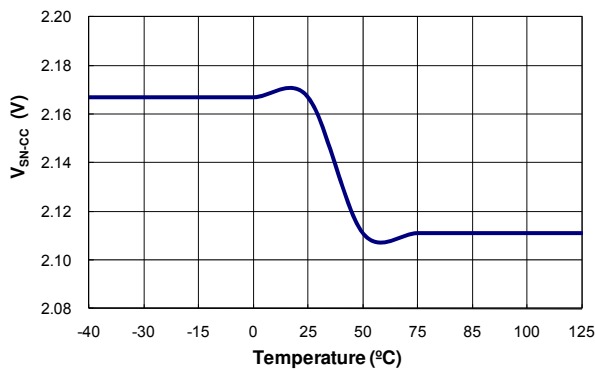
**Figure 13. V<sub>S</sub> Over-Voltage Protection (V<sub>VS-OVP</sub>) vs. Temperature**



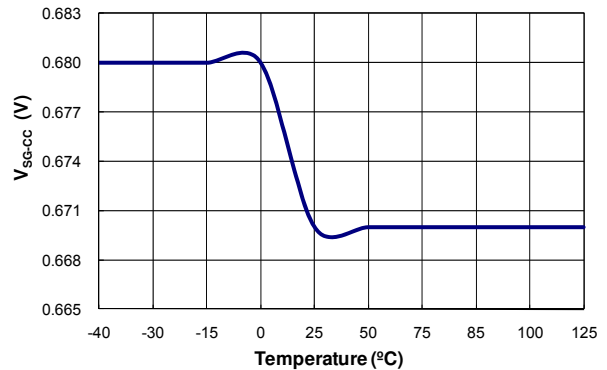
**Figure 14. Reference Voltage of CS (V<sub>VR</sub>) vs. Temperature**



**Figure 15. Variation Voltage on CS Pin for Constant-Current Regulation (V<sub>VCCR</sub>) vs. Temperature**



**Figure 16. Starting Voltage of Frequency Decreasing of CC Regulation (V<sub>VSN-CC</sub>) vs. Temperature**



**Figure 17. Ending Voltage of Frequency Decreasing of CC Regulation (V<sub>VSG-CC</sub>) vs. Temperature**



## Typical Performance Characteristics

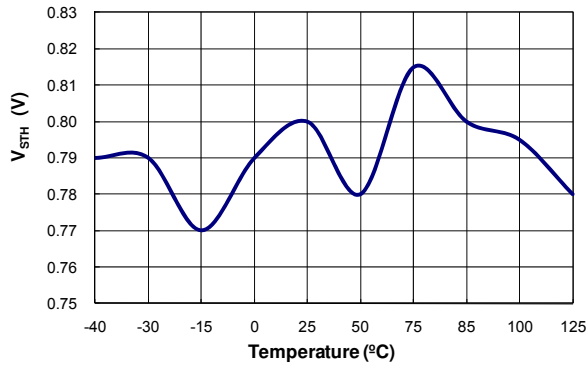


Figure 18. Threshold Voltage for Current Limit ( $V_{STH}$ ) vs. Temperature

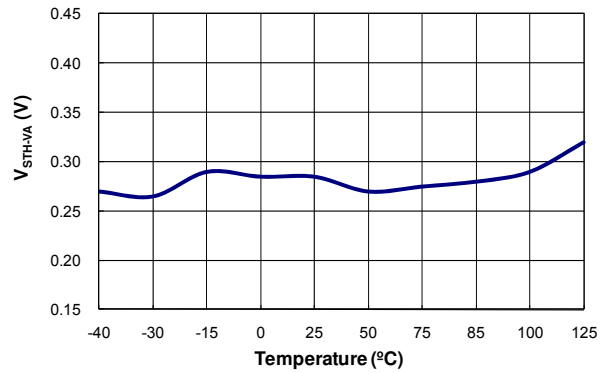


Figure 19. Threshold Voltage for Current Limit at Power Mode ( $V_{STH-VA}$ ) vs. Temperature

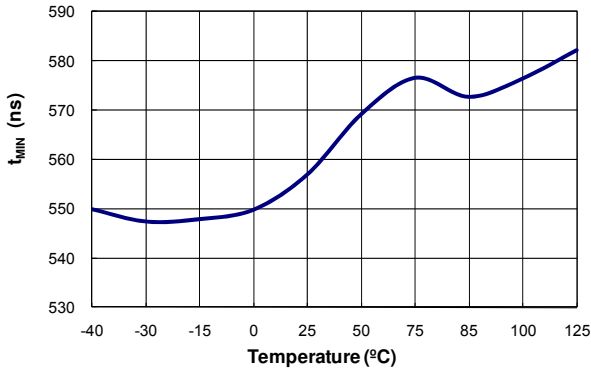


Figure 20. Minimum On Time ( $t_{MIN}$ ) vs. Temperature

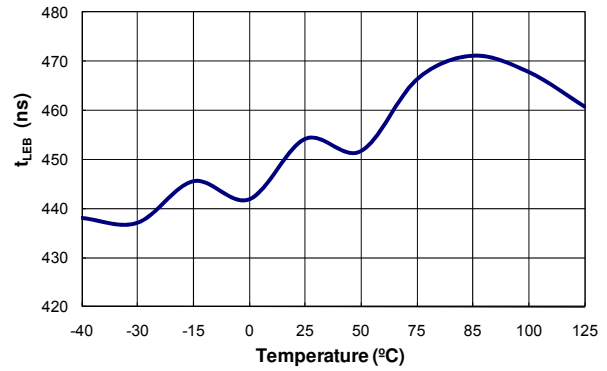


Figure 21. Leading-Edge Blanking Time ( $t_{LEB}$ ) vs. Temperature

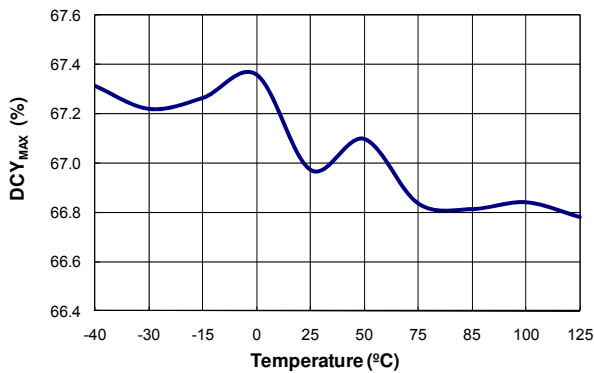


Figure 22. Maximum Duty Cycle ( $DCY_{MAX}$ ) vs. Temperature

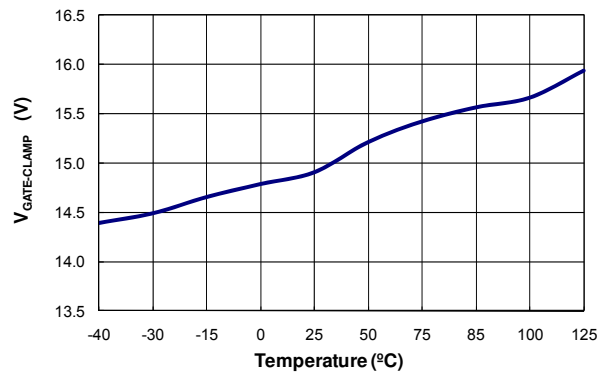


Figure 23. Gate Output Clamp Voltage ( $V_{GATE-CLAMP}$ ) vs. Temperature

## Operation Description

### Constant-Voltage Regulation Operation

FAN302HL is the high-frequency and ultra-low standby power IC with Constant Voltage (CV) / Constant Current (CC) regulation.

When FAN302HL operates in CV regulation, the feedback voltage ( $V_{FB}$ ) works as output load and modulates the PWM duty, as shown in Figure 24, causing fixed switching frequency (85kHz). Once the  $V_{FB}$  decreases below  $V_{FB-G}$ , frequency hopping is disabled and operation current decreases.

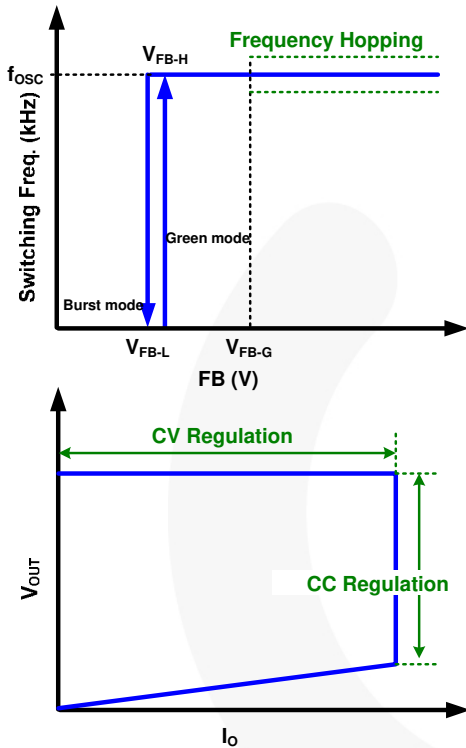


Figure 24.  $f_{OSC}$  vs.  $V_{FB}$  in CV Regulation

### Constant-Current Regulation Operation

During CC operation, the proprietary Primary-Side Regulation (PSR) topology simplifies circuit design without secondary feedback circuitry for battery-charger applications. The CC regulation achieved through PSR technique uses a mixed-signal algorithm to detect the primary-side current and to sample the voltage through primary-side auxiliary winding and calculate the average current on secondary side.

Figure 25 shows the basic circuit diagram of a flyback converter, with typical waveforms shown in Figure 26. Generally, Discontinuous Conduction Mode (DCM) operation is preferred for constant-current control since it allows better output regulation. The operation principles of DCM flyback converter are:

During the MOSFET on time ( $t_{ON}$ ), input voltage ( $V_{DL}$ ) is applied across the primary-side inductor ( $L_m$ ). Then, MOSFET current ( $I_{ds}$ ) increases linearly from zero to the

peak value ( $I_{pk}$ ). During this time, the energy is drawn from the input and stored in the inductor.

When the MOSFET is turned off, the energy stored in the inductor forces the rectifier diode (D) to be turned on. While the diode is conducting, the output voltage ( $V_O$ ), together with diode forward voltage drop ( $V_F$ ), are applied across the secondary-side inductor ( $L_m \times N_s^2 / N_p^2$ ) and the diode current ( $I_D$ ) decreases linearly from the peak value ( $I_{pk} \times N_p / N_s$ ) to zero. At the end of inductor current discharge time ( $t_{DIS}$ ), all the energy stored in the inductor has been delivered to the output.

When the diode current reaches zero,  $V_S$  voltage drops quickly: if it is greater than the  $V_{VS-OFFSET}$  drop voltage, the IC gets the  $t_{DIS}$  for CC regulation.

During the inductor current discharge time, the sum of output voltage and diode forward-voltage drop is reflected to the auxiliary winding side as  $(V_O + V_F) \times N_a / N_s$ . This voltage signal is proportional to the secondary winding. In constant-current output operation, this voltage signal is detected and examined by the precise constant-current regulation controller. The on time of the MOSFET is determined to control input power and provide constant-current output property. With feedback voltage  $V_{CS}$  across the current-sense resistor, the controller can obtain the input power of power supply. Therefore, the region of constant-current output operation can be adjusted by the current-sense resistor, as shown in Equation (1).

$$I_O = \frac{1}{2} \cdot I_{PK} \cdot \frac{N_P}{N_S} \cdot \frac{t_{DIS}}{t_s} = \frac{1}{2} \cdot \frac{N_P}{N_S} \cdot \frac{V_{CS}}{R_{CS}} \cdot \frac{t_{DIS}}{t_s} \quad (1)$$

During CC regulation, the  $V_S$  voltage decreases as output voltage decreases. The switching frequency reduces linearly from  $f_{OSC}$  to  $f_{OSC-CCM}$  as  $V_S$  voltage changes from  $V_{SN-CC}$  to  $V_{SG-CC}$ . Figure 27 shows the relationship between frequency and  $V_S$  voltage. Figure 28 shows the output V-I curve and  $V_S$  voltage.

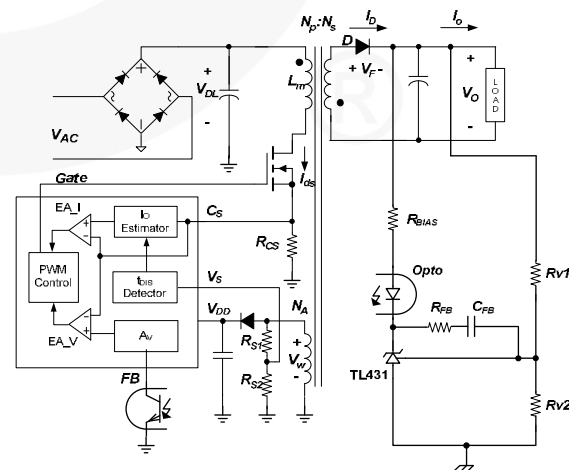


Figure 25. Simplified Flyback Converter Circuit

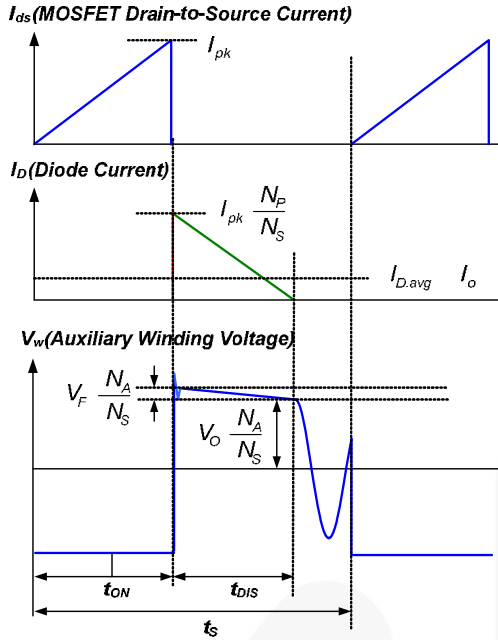


Figure 26. Waveforms of DCM Flyback Converter

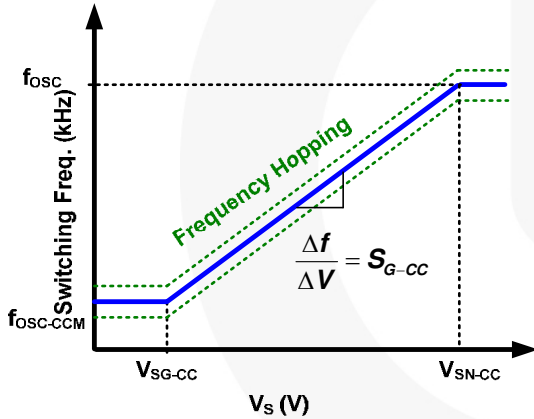


Figure 27. Frequency Reduction Curve in CC Regulation

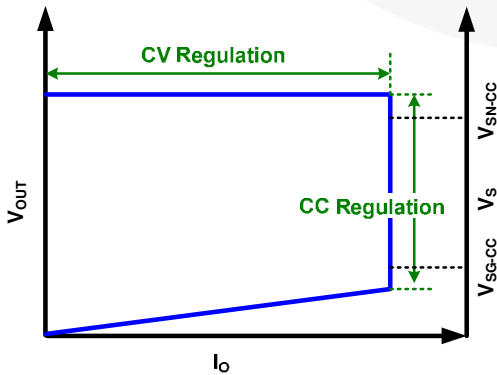


Figure 28. Output V-I Curve and  $V_s$  Voltage

### High-Voltage Startup

Figure 29 shows the high-voltage (HV) startup circuit for FAN302HL applications. The HV pin is connected to the line input or bulk capacitor through a resistor. During startup, the internal startup circuit is enabled and the line input supplies the current,  $I_{HV}$ , to charge the hold-up capacitor,  $C_{VDD}$ , through  $R_{START}$ . When the  $V_{DD}$  voltage reaches  $V_{DD-ON}$ , the internal HV startup circuit is disabled, blocking  $I_{HV}$  from flowing into the HV pin. Once the IC turns on,  $C_{VDD}$  is the only energy source to supply the IC consumption current before the PWM starts to switch. Therefore,  $C_{VDD}$  must be large enough to prevent  $V_{DD}$  from dropping to  $V_{DD-OFF}$  before the power can be delivered from the auxiliary winding.

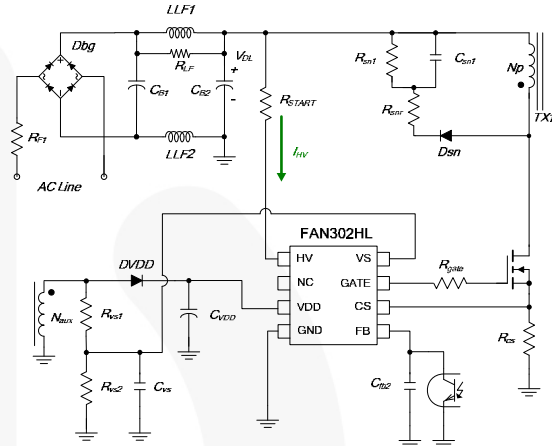


Figure 29. HV Startup Circuit

### Frequency Hopping

EMI reduction is accomplished by frequency hopping, which spreads the energy over a wider frequency range than the bandwidth measured by the EMI test equipment. The FAN302HL internal frequency-hopping circuit changes the switching frequency between 82kHz and 88kHz with a period, as shown in Figure 30.

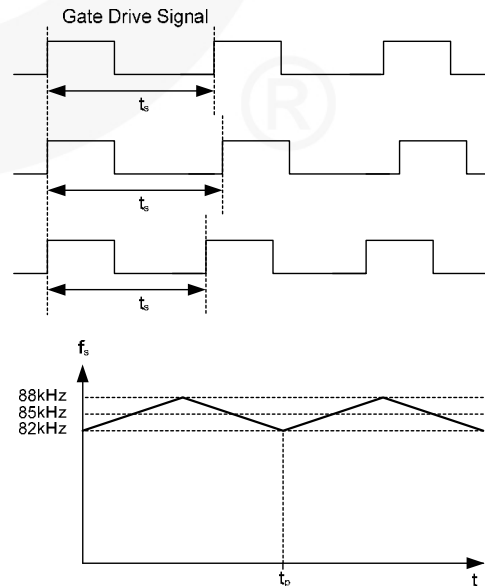


Figure 30. Frequency Hopping

## Burst-Mode Operation

The power supply enters “Burst-Mode” at no-load conditions. As shown in Figure 31, when  $V_{FB}$  drops below  $V_{FBL}$ , the PWM output shuts off and the output voltage drops at a rate dependent on load current. This causes the feedback voltage to rise. Once  $V_{FB}$  exceeds  $V_{FBH}$ , the internal circuit starts to provide switching pulse. The feedback voltage then falls and the process repeats. Burst Mode operation alternately enables and disables switching of the MOSFET, reducing the switching losses in Standby Mode.

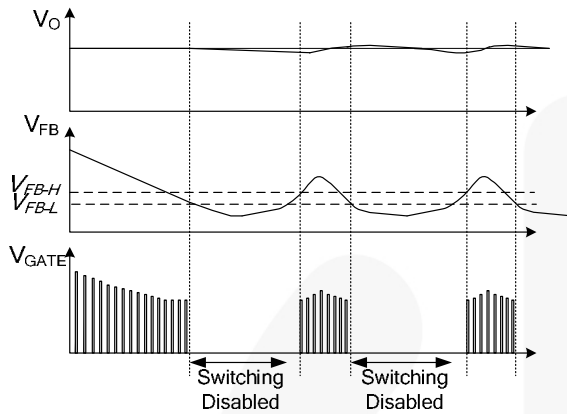


Figure 31. Burst-Mode Operation

## Operating Current

The typical operating current is 3.5mA. This low operating current results in higher efficiency and reduces the  $V_{DD}$  hold-up capacitance requirement. Once FAN302HL enters Burst Mode, the operating current is reduced to 200 $\mu$ A, allowing the power supply to meet power conservation requirements.

## Gate Output

The FAN302HL BiCMOS output stage is a fast totem-pole gate driver. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal Zener diode to protect the power MOSFET transistors against over-voltage gate signals.

## Slope Compensation

The sensed voltage across the current-sense resistor is used for Current-Mode control and pulse-by-pulse current limiting. Built-in slope compensation, a synchronized positively-sloped ramp built-in at each switching cycle, improves stability and prevents sub-harmonic oscillations due to Peak-Current Mode control.

## Constant Power Mode Control

When  $V_S$  is lower than  $V_{S-CM-MIN}$ , FAN302HL enters Constant-Power-Mode control, the primary-side current limit voltage ( $V_{CS}$ ) changes from  $V_{STH}$  to  $V_{STH-VA}$  to avoid mis-sampling  $V_S$  through the Zero Current Detection (ZCD). Once  $V_S$  is higher than  $V_{S-CM-MAX}$ , the  $V_{CS}$  returns to  $V_{STH}$ .

## Protections

The FAN302HL self-protection functions include  $V_{DD}$  Over-Voltage Protection ( $V_{DD}$  OVP), internal Over-Temperature Protection (OTP),  $V_S$  Over-Voltage Protection ( $V_S$  OVP), brownout protection, and pulse-by-pulse current limit.

The  $V_{DD}$  OVP protection is implemented as Auto-Restart Mode. Once an abnormal condition occurs, switching is terminated and the MOSFET remains off, causing  $V_{DD}$  to drop. When  $V_{DD}$  drops to the  $V_{DD}$  turn-off voltage of 5V, the internal startup circuit is enabled, and the supply current drawn from HV pin charges the hold-up capacitor. When  $V_{DD}$  reaches the turn-on voltage of 16V, FAN302HL resumes normal operation. In this manner, the auto-restart alternately enables and disables the switching of the MOSFET until the abnormal condition is eliminated (see Figure 32).

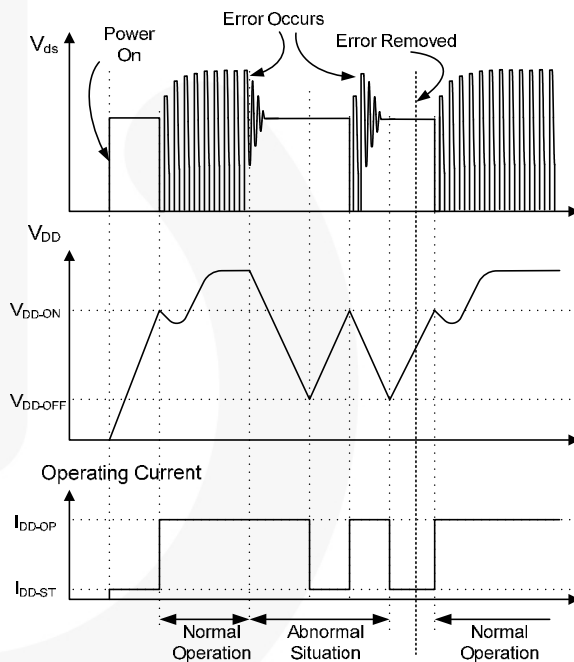
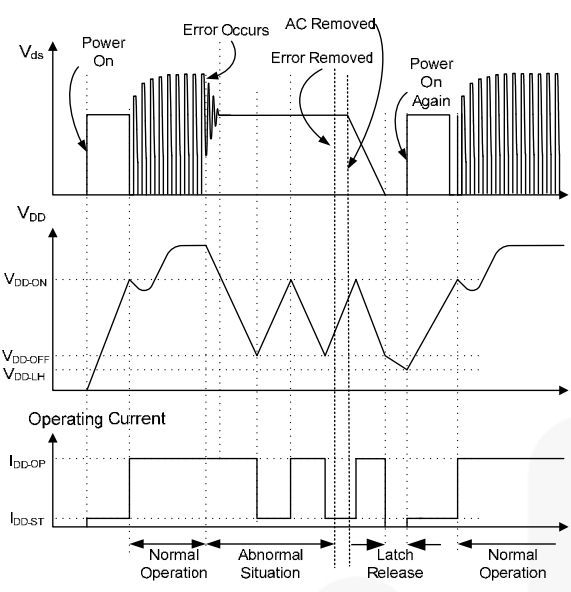


Figure 32. Auto-Restart Mode Operation

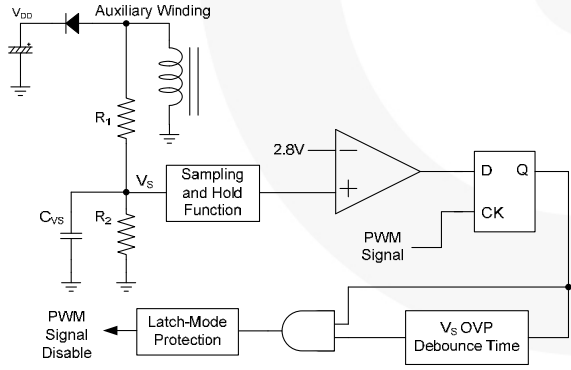
The  $V_S$  OVP and internal OTP protections are implemented as Latch Mode. If abnormal conditions occur, PWM switching is terminated and the MOSFET remains off. In this scenario,  $V_{DD}$  drops, but keeps working as auto-restart ( $V_{DD}$  auto-restart behavior doesn't trigger PWM pulses). FAN302HL enters Latch Mode, disables PWM switching of the MOSFET until  $V_{DD}$  is lower than  $V_{DD-LH}$  (AC power is removed), powers on again, then resumes normal operation (see Figure 33).



**Figure 33. Latch-Mode Operation**

**V<sub>S</sub> Over-Voltage Protection (OVP)**

V<sub>S</sub> over-voltage protection prevents damage due to output over-voltage conditions. Figure 34 shows the V<sub>S</sub> OVP protection method. When abnormal system conditions occur that cause V<sub>S</sub> to exceed 2.8V, after a period of debounce time; PWM pulses are disabled and FAN302HL enters Latch Mode until V<sub>DD</sub> drops to under V<sub>DD-LH</sub>. By that time, PWM pulses revive. V<sub>S</sub> over-voltage conditions are usually caused by open feedback loops or abnormal behavior by the VS pin divider resistor.



**Figure 34. V<sub>S</sub> OVP Protection**

**V<sub>DD</sub> Over-Voltage Clamping**

V<sub>DD</sub> over-voltage protection prevents damage due to over-voltage conditions. When the V<sub>DD</sub> voltage exceeds 26.5V due to abnormal conditions, PWM pulses are disabled until the V<sub>DD</sub> voltage drops below the UVLO, then starts again. Over-voltage conditions are usually caused by open feedback loops.

**Over-Temperature Protection (OTP)**

The FAN302HL temperature-sensing circuit shuts down PWM output if the junction temperature exceeds 140°C (T<sub>OTP</sub>). The PWM pulses are disabled until V<sub>DD</sub> voltage drops below the V<sub>DD-LH</sub>.

**Leading-Edge Blanking (LEB)**

Each time the power MOSFET is switched on, a turn-on spike occurs at the sense resistor. To avoid premature termination of the switching pulse, a 350ns leading-edge blanking time is built in. Conventional RC filtering can therefore be omitted. During this blanking period, the current-limit comparator is disabled and it cannot switch off the gate driver.

**Under Voltage Lockout (UVLO)**

The turn-on and turn-off thresholds are fixed internally at 16V and 5V, respectively. During startup, the hold-up capacitor must be charged to 16V through the startup resistor to enable the FAN302HL. The hold-up capacitor continues to supply V<sub>DD</sub> until power can be delivered from the auxiliary winding of the main transformer. V<sub>DD</sub> must not drop below 5V during this startup process. This UVLO hysteresis window ensures that the hold-up capacitor is adequate to supply V<sub>DD</sub> during startup.

**Noise Immunity**

Noise from the current sense or the control signal can cause significant pulse-width jitter, particularly in Continuous-Conduction Mode. While slope compensation helps alleviate these problems, further precautions should still be taken. Good placement and layout practices should be followed. Avoiding long PCB traces and component leads, locating compensation and filter components near the FAN302HL, and increasing the power MOS gate resistance are advised.

## Typical Application Circuit (Flyback Charger)

Application	Fairchild Devices	Input Voltage Range	Output
Cell Phone Charger	FAN302HL	90~265V <sub>AC</sub>	5V/1.2A (6W)

### Features

- High Efficiency (Avg. >71%), Meeting Energy Star V2.0 Standard (Avg. 68.17%)
- Ultra-Low Standby Power: Under 10mW at 230V<sub>AC</sub> (Pin=6.3mW for 115V<sub>AC</sub> and Pin=7.3mW for 230V<sub>AC</sub>)
- Output Regulation (CV: ±5%, CC: ±15%)

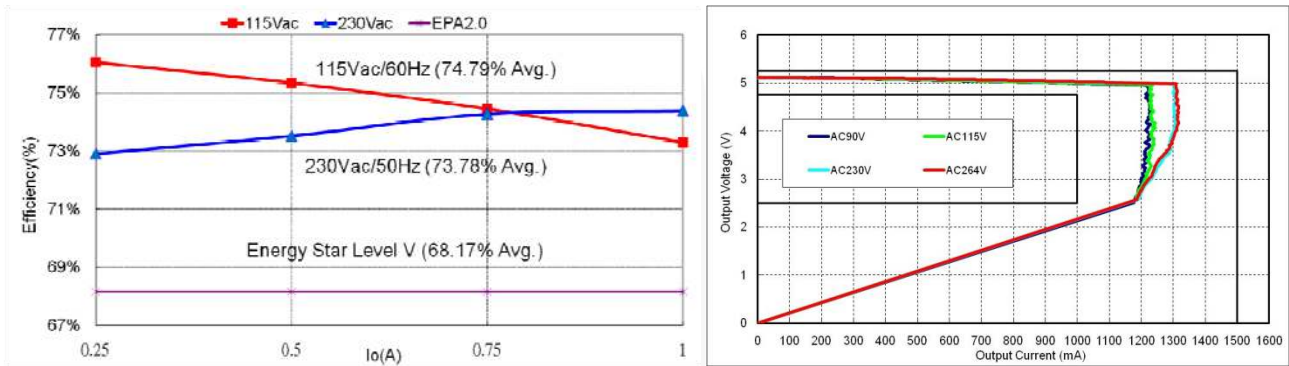


Figure 35. Measured Efficiency and Output Regulation

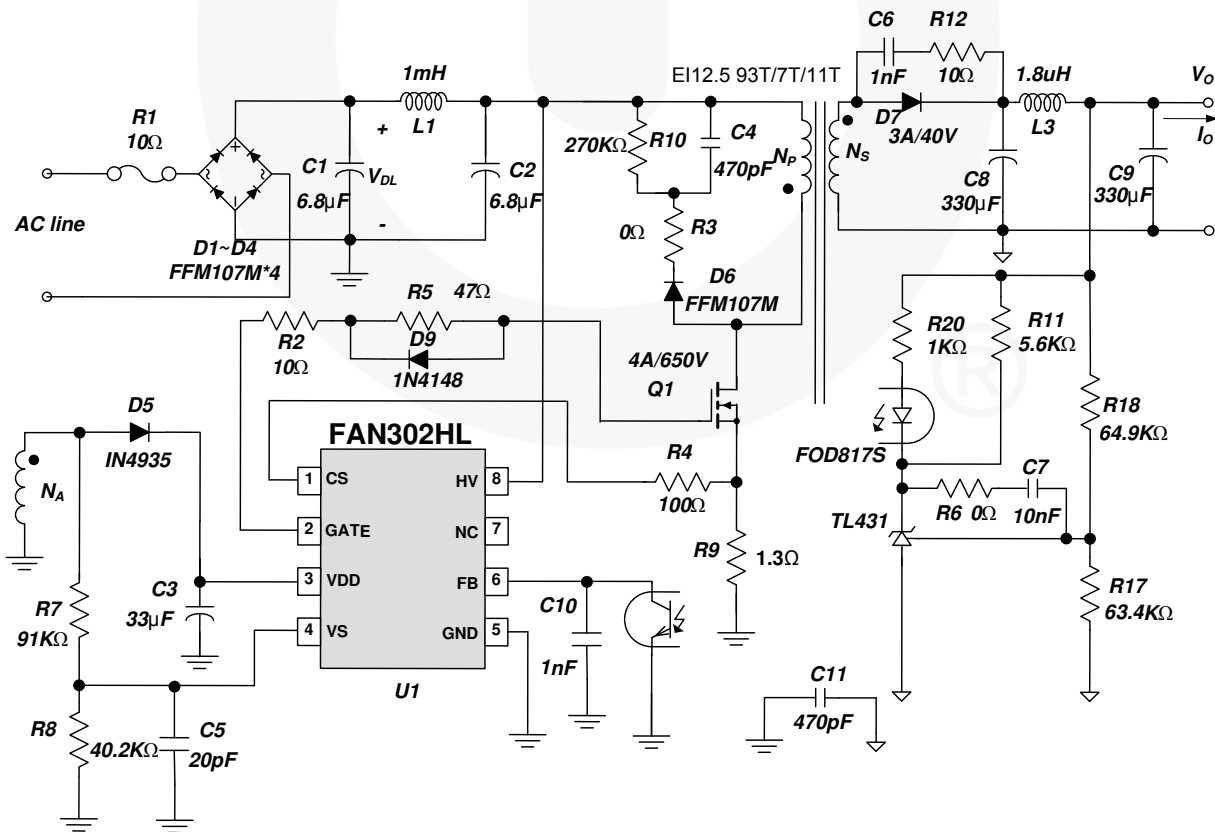


Figure 36. Schematic of Typical Application Circuit

## Typical Application Circuit (Continued)

### Transformer Specification

- Core: EI12.5
- Bobbin: EI12.5

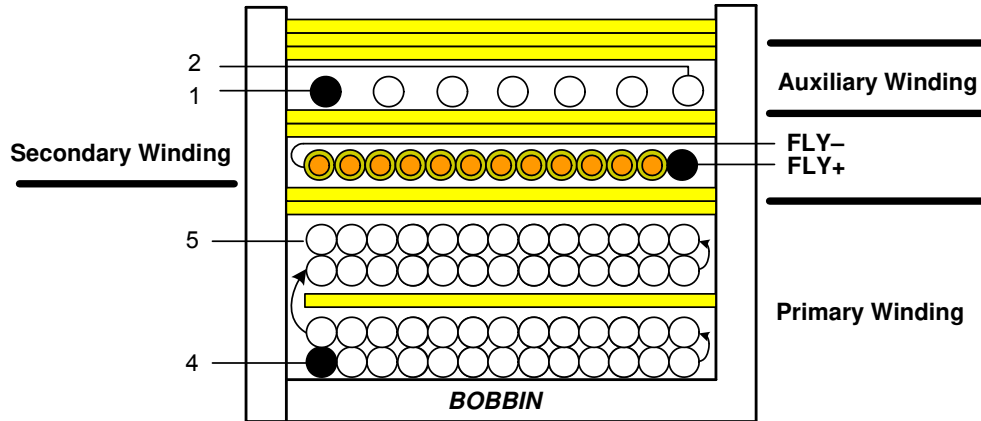


Figure 37. Transformer

- W1 is four winds; for each wind of turns, refer to Table 1. Add one insulating tape layer between the first and second layers.
- W2 is wound two layers and uses triple-insulated wire: end of positive fly line is 3.5cm, layer end of negative fly line is 2.5cm.
- W3 is spares winding in one layer.
- W4 is wound in the core of the outermost layer and sparse winding.

Table 1. Transformer Turns Specifications

NO	Terminal		Wire	Turns	Insulation
	Start Pin	End Pin			Turns
W1	4	5	2UEW 0.1*1	26	0
				25	1
				24	0
				18	2
W2	Fly+	Fly-	TEX-E 0.45*1	7	2
W3	1	2	2UEW 0.18*1	11	2
			CORE ROUNDING TAPE		3
			CORE		0
W4	2		2UEW 0.18*1	5	2

	Pin	Specifications	Remark
Primary-Side Inductance	4 – 5	700 $\mu$ H $\pm$ 7%	100kHz, 1V
Primary-Side Effective Leakage	4 – 5	200 $\mu$ H $\pm$ 5%	Short one of the secondary windings.

Physical Dimensions

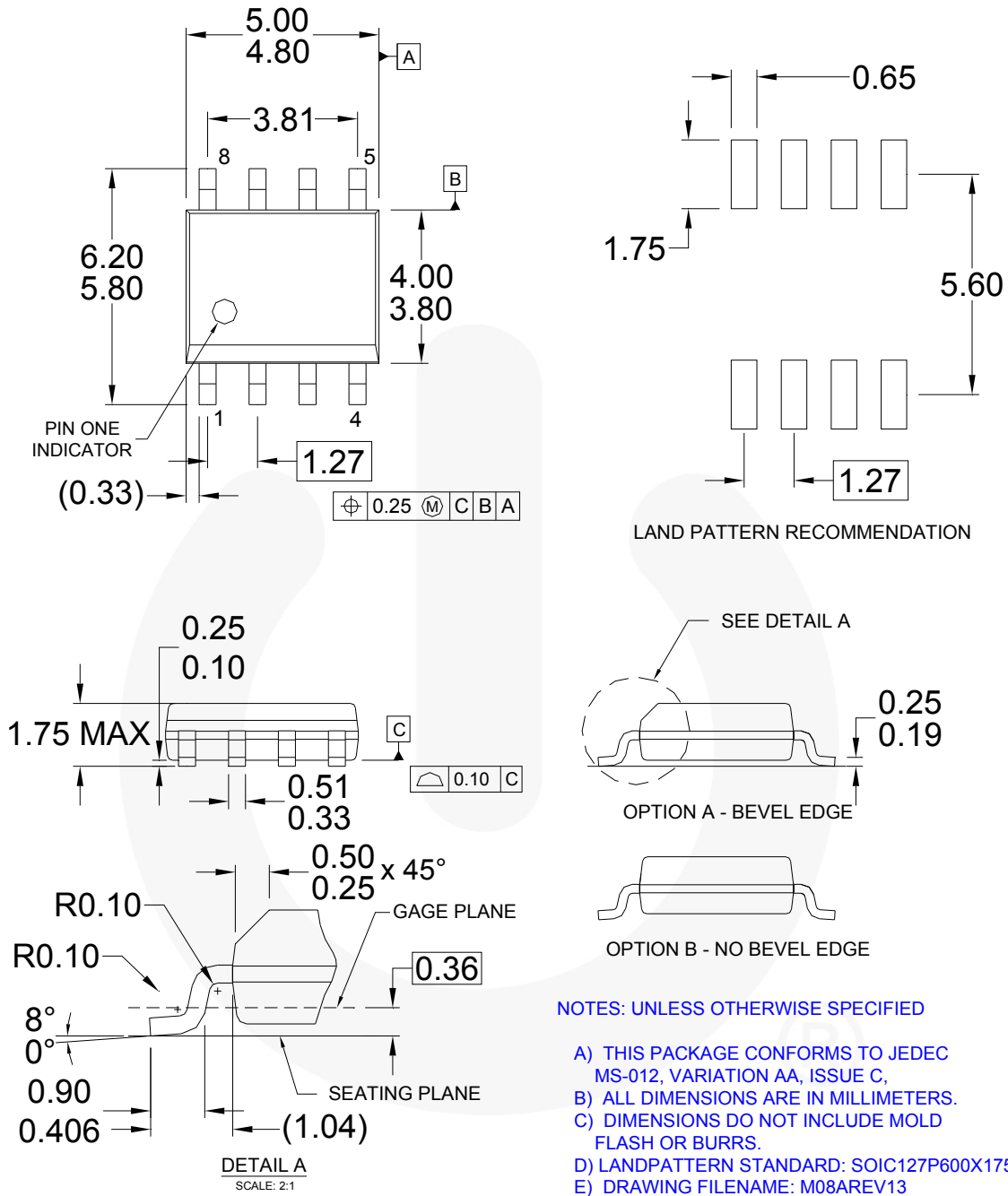


Figure 38. 8-Lead, Small Outline Package (SOIC), JEDEC MS-012, .150-Inch, Narrow Body

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.



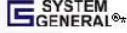
Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:  
<http://www.fairchildsemi.com/packaging/>.





**TRADEMARKS**

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

- |  |  |   |   |
|--|--|---|---|
| 2Cool™   | FPS™   | PDP-SPM™  | The Power Franchise®  |
| AccuPower™   | F-PFS™   | Power-SPM™  | <b>the power franchise</b>  |
| Auto-SPM™  | FRFET®   | PowerTrench®  | TinyBoost™  |
| AX-CAPT™   | Global Power Resource™                         | PowerXS™  | TinyBuck™   |
| BitSiC®  | Green FPS™                                     | Programmable Active Droop™  | TinyCalc™   |
| Build it Now™  | Green FPS™ e-Series™                           | QFET®   | TinyLogic®  |
| CorePLUS™  | Gmax™  | QST™  | TINYOPTO™   |
| CorePOWER™   | GTO™   | Quiet Series™   | TinyPower™  |
| CROSSVOLT™   | IntelliMAX™                                    | RapidConfigure™   | TinyPWM™  |
| CTL™   | ISOPLANAR™                                     |  Saving our world, 1mW/W/kW at a time™ | TinyWire™   |
| Current Transfer Logic™  | Making Small Speakers Sound Louder and Better™ | SignalWise™   | TranSiC®  |
| DEUXPEED®  | MegaBuck™                                      | SmartMax™   | TriFault Detect™  |
| Dual Cool™   | MICROCOUPLER™                                  | SMART START™  | TRUECURRENT®*   |
| EcoSPARK®  | MicroFET™                                      | SPM®  | µSerDes™  |
| EfficientMax™  | MicroPak™                                      | STEALTH™  |  SerDes® |
| ESBC™  | MicroPak2™                                     | SuperFET®   | UHC®  |
|  Fairchild® | MillerDrive™                                   | SuperSOT™-3   | Ultra FRFET™  |
| Fairchild Semiconductor®   | MotionMax™                                     | SuperSOT™-6   | UniFET™   |
| FACT Quiet Series™   | Motion-SPM™                                    | SuperSOT™-8   | VCC™  |
| FACT®  | mWSaver™                                       | SupreMOS®   | VisualMax™  |
| FAST®  | OptoHit™                                       | SyncFET™  | VoltagePlus™  |
| FastvCore™   | OPTOLOGIC®                                     | Sync-Lock™  | XST™  |
| FETBench™  | OPTOPLANAR®                                    |  SYSTEM GENERAL®*                      |   |
| FlashWriter®*  |  |   |   |

\* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

**DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
- A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**ANTI-COUNTERFEITING POLICY**

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, [www.fairchildsemi.com](http://www.fairchildsemi.com), under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I57