4731B/4731BX
QUAD 64-BIT STATIC SHIFT REGISTER

DESCRIPTION — The 4731B/4731BX is a Quad 64-Bit Shift Register each with separate Serial Data Inputs (D_A-D_D), Clock Inputs ($\overline{CP}_A$-$\overline{CP}_D$) and Data Outputs (Q_{63A}-Q_{63D}) from the 64th register position.

Information present on the Serial Data Inputs is shifted into the first register position and all the data in the register is shifted one position to the right on a HIGH-to-LOW transition of the Clock Inputs ($\overline{CP}_A$-$\overline{CP}_D$).

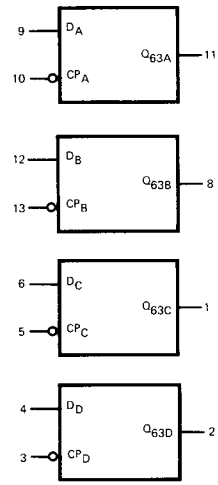
Low impedance outputs are provided for direct interface to TTL. The 4731B is specified to operate over a power supply voltage range of 4.5 V to 12.5 V, the 4731BX is specified to operate over a power supply voltage range of 3 V to 15 V.

- **FREQUENCIES UP TO 8 MHz AT V_{DD} = 10 V**
- **SERIAL-TO-SERIAL DATA TRANSFER**
- **SEPARATE CLOCK INPUTS, DATA INPUTS AND FULLY BUFFERED OUTPUTS FOR EACH REGISTER**
- **DIRECT INTERFACE TO TTL**
- **14-PIN PACKAGE**

PIN NAMES

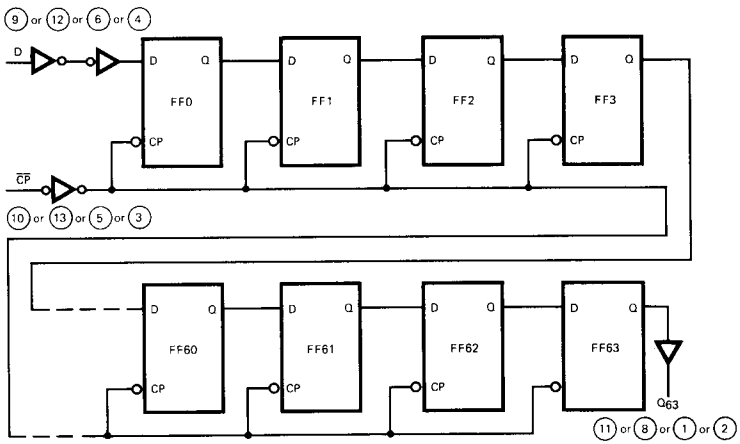
D_A-D_D	Serial Data Inputs
$\overline{CP}_A$-$\overline{CP}_D$	Clock Input (H→L Edge-Triggered)
Q_{63A}-Q_{63D}	Buffered Outputs from the 64th Register Position

LOGIC SYMBOL



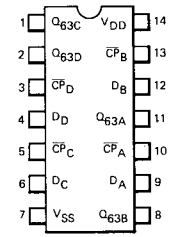
V_{DD} = Pin 14
V_{SS} = Pin 7

LOGIC DIAGRAM
1/4 OF A 4731B/4731BX

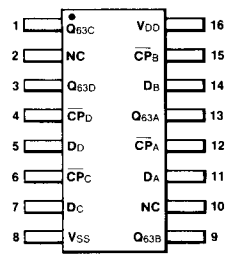


V_{DD}= Pin 14
V_{SS} = Pin 7
○ = Pin Number

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



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DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

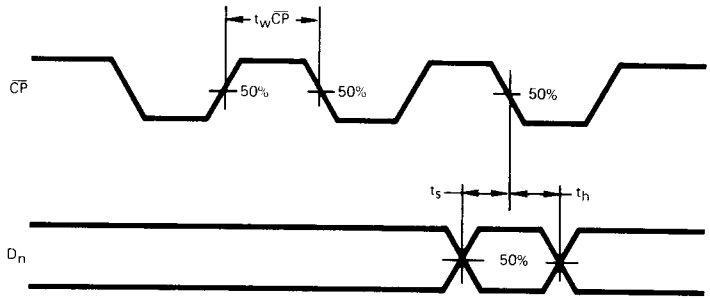
SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			100			200			400	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					750			1500			3000		MAX	
		XM			25			50			100	μA	MIN, 25°C	
					75			1500			3000		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, $\overline{CP}$ to Q_{63}		190	450		95	200		65	160	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ⩽ 20 ns
t_{PHL}			190	450		95	200		65	160		
t_{TLH}	Output Transition Time		45	135		30	70		20	45	ns	
t_{THL}			30	90		30	50		20	35		
$t_W\overline{CP}$	$\overline{CP}$ Minimum Pulse Width	300	100		150	50		120	40		ns	
t_s	Set-Up Time D to $\overline{CP}$	100	-20		40	-12		40	-7		ns	
t_h	Hold Time D to $\overline{CP}$	100	35		40	12		40	11			
f_{MAX}	Max. Input Clock Frequency (Note 3)	1.5	4		3	8		4	14		MHz	

NOTES:
1. Additional DC Characteristics are listed in this section unc0' 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs at V_{DD} = 5 V, 4 μs at V_{DD} = 10 V, and 3 μs at V_{DD} = 15 V.

SWITCHING WAVEFORMS



MINIMUM CLOCK PULSE WIDTH AND SET-UP AND HOLD TIMES, D TO $\overline{CP}$

NOTE:
1. Set-up and Hold Times are shown as positive values but may be specified as negative values.