19-3505; Rev 1; 6/05

EVALUATION KIT AVAILABLE

Low-Dropout, Wide-Input-Voltage, Step-Down Controllers

General Description

The MAX8597/MAX8598/MAX8599 voltage-mode PWM step-down controllers are designed to operate from a 4.5V to 28V input supply and generate output voltages down to 0.6V. A proprietary switching algorithm stretches the duty cycle to >99.5% for low-dropout design. Unlike conventional step-down regulators using a p-channel high-side MOSFET to achieve high duty cycle, the MAX8597/MAX8598/MAX8599 drive n-channel MOSFETs resulting in high efficiency and high-current-capability designs.

The MAX8597 is available in a 20-pin thin QFN package and is designed for applications that use an analog signal to control the output voltage with an adjustable offset, such as DC fan-speed control. This is achieved with an internal uncommitted operational amplifier. The MAX8597 is also targeted for tracking output-voltage applications for chipsets, ASIC and DSP cores, and I/O supplies. The MAX8598/MAX8599 are available in a 16-pin thin QFN package and do not have the uncommitted operational amplifier, reference input, and reference output, but offer an open-drain, power-OK output.

The MAX8597/MAX8598/MAX8599 allow startup with prebias voltage on the output for applications where a backup supply or a tracking device may charge the output capacitor before the MAX8597/MAX8598/MAX8599 are enabled. In addition, the MAX8599 features output overvoltage protection.

These controllers also feature lossless high-side peak inductor current sensing, adjustable current limit, and hiccup-mode short-circuit protection. Switching frequency is set with an external resistor from 200kHz to 1.4MHz. This wide frequency range combined with a wide-bandwidth error amplifier enables the loop compensation scheme to give the user ample flexibility to optimize for cost, size, and efficiency.

Applications

Nonisolated Power Modules

Variable-Speed DC Fan Power Supplies (MAX8597)

Tracking Power Supplies (MAX8597)

Chipset Power Supplies

Features

- **Low Dropout with >99.5% Duty Cycle**
- **Lossless High-Side Current Limit**
- **Wide 4.5V to 28V Input Range**
- **Dynamic Output Voltage Adjustment with Adjustable Offset (MAX8597)**
- **Remote Voltage Sensing for Both Positive and Negative Rails (MAX8597)**
- **Tracking Output Through REFIN (MAX8597)**
- **Adjustable Switching Frequency from 200kHz to 1.4MHz**
- **Adjustable Soft-Start**
- **Prebias Startup**
- **Enable and Power-OK (MAX8598/MAX8599) for Flexible Sequencing**
- **25MHz Error Amplifier**
- **Adjustable Hiccup Current Limit for Output Short-Circuit Protection**
- **Output Overvoltage Protection (MAX8599)**
- **Small, Low-Profile Thin QFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8597ETP	-40°C to +85°C	20 Thin QFN 4mm x 4mm (T2044-3)
MAX8597ETP+	-40°C to +85°C	20 Thin QFN 4mm x 4mm (T2044-3)
MAX8598ETE	-40°C to +85°C	16 Thin QFN 4mm x 4mm (T1644-4)
MAX8598ETE+	-40°C to +85°C	16 Thin QFN 4mm x 4mm (T1644-4)
MAX8599ETE	-40°C to +85°C	16 Thin QFN 4mm x 4mm (T1644-4)
MAX8599ETE+	-40°C to +85°C	16 Thin QFN 4mm x 4mm (T1644-4)

+Denotes lead-free package.

Pin Configurations appear at end of data sheet.

Low-Dropout, Wide-Input-Voltage, Step-Down Controllers

ABSOLUTE MAXIMUM RATINGS

V+, ILIM to GND .....-0.3V to +30V
AVL, VL to GND .....-0.3V to +6V
PGND to GND .....-0.3V to +0.3V
FB, EN, POK, AIN-, AIN+, REFIN to GND .....-0.3V to +6V
AOUT, REFOUT, FREQ, SS, COMP to GND .....-0.3V to (V_{AVL} + 0.3V)
BST to GND .....-0.3V to +36V
DH to LX .....-0.3V to (V_{BST} + 0.3V)
LX to GND .....-2V (-2.5V for less than 50ns) to +30V
LX to BST .....-6V to +0.3V
DL to PGND .....-0.3V to (V_{VL} + 0.3V)
Continuous Power Dissipation
16- or 20-Pin Thin QFN
Up to +70°C (derate 16.9mW/°C above +70°C) 1349mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{V+} = V_{VL} = V_{AVL} = V_{EN} = V_{REFIN} = 5V, V_{BST} = 6V, V_{LX} = 1V, C_{VL} = 4.7µF, C_{REFOUT} = 1µF, V_{AIN-} = V_{AOUT}, V_{AIN+} = 2.5V, V_{ILIM} = V_{LX} - 0.2V, V_{FB} = 0.65V, GND = PGND = 0V, C_{SS} = 0.01µF, R_{FREQ} = 20kΩ, **T_A = 0°C to +85°C**, typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL					
V+ Operating Range		5.5		28.0	V
V+/VL Operating Range	V+ = VL	4.5		5.5	V
V+ Operating Supply Current	V_{V+} = 12V, VL unloaded, no MOSFETs connected, V_{FB} = 0V		3.4	5.0	mA
V+ Standby Supply Current	V_{V+} = 12V, VL unloaded, V_{FB} = 0V		2.0		mA
VL REGULATOR					
Output Voltage	5.5V < V_{V+} < 28V, 1mA < I_{LOAD} < 35mA	4.7	5.0	5.3	V
VL Undervoltage-Lockout Trip Level	Rising edge, typical hysteresis = 460mV	4.05	4.2	4.35	V
Thermal Shutdown	Rising temperature, typical hysteresis = 10°C		+160		°C
REFERENCE (MAX8597 only)					
REFOUT Output Voltage	I_{REFOUT} = 150µA, V_{V+} = V_{VL} = 4.5V or 5.5V	2.49	2.50	2.51	V
REFOUT Load Regulation	I_{REFOUT} = 10µA to 1mA			10	mV
REFOUT Internal Discharge Switch On-Resistance	During VL UVLO		15		Ω
CURRENT-LIMIT COMPARATOR (all current limits are tested at V_{V+} = V_{VL} = 4.5V and 5.5V)					
ILIM Sink Current	1.8V < V_{LX} < 28V, V_{BST} = V_{LX} + 5V	180	200	220	µA
Comparator Input Offset Voltage Error	V_{LX} = 28V, V_{BST} = V_{LX} + 5V	-10		+10	mV
SOFT-START					
Soft-Start Source Current	V_{SS} = 100mV	3	5	7	µA
Soft-Start Sink Current	V_{SS} = (0.6V or V_{REFIN})	3	5	7	µA
FREQUENCY					
Frequency	R_{FREQ} = 100kΩ	150	200	240	kHz
	R_{FREQ} = 20.0kΩ	800	1000	1200	
	R_{FREQ} = 14.3kΩ	1100	1400	1700	

ELECTRICAL CHARACTERISTICS (continued)

(V_{V+} = V_{VL} = V_{AVL} = V_{EN} = V_{REFIN} = 5V, V_{BST} = 6V, V_{LX} = 1V, C_{VL} = 4.7µF, C_{REFOUT} = 1µF, V_{AIN-} = V_{AOUT}, V_{AIN+} = 2.5V, V_{ILIM} = V_{LX} - 0.2V, V_{FB} = 0.65V, GND = PGND = 0V, C_{SS} = 0.01µF, R_{FREQ} = 20kΩ, **T_A = 0°C to +85°C**, typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DH Minimum Off-Time		180	200	220	ns
DH Minimum On-Time			115	140	ns
FB ERROR AMPLIFIER					
FB Input Bias Current				100	nA
FB Input Voltage Set Point	Over load and line	0.594	0.600	0.606	V
FB Offset Error	V_{REFIN} = 1.25V and 2.5V, measured with respect to REFIN	+10		-10	mV
Error-Amp Open-Loop Voltage Gain	V_{COMP} = 1.2V to 2.4V	72	90		dB
Slew Rate	C_{LOAD} = 80pF		18		V/µs
UNCOMMITTED OPERATIONAL AMPLIFIER (MAX8597 only)					
Open-Loop Voltage Gain (A_{VOL})	R_{LOAD} = 100kΩ		90		dB
	R_{LOAD} = 10kΩ		70		
Output-Voltage Swing High	V_{AIN+} = 2.5V, V_{AIN-} = (V_{AIN+} - 100mV), I_{SOURCE} = 100µA	V_{AVL} - 20mV			V
Output-Voltage Swing Low	V_{AIN+} = 2.5V, V_{AIN-} = (V_{AIN+} + 100mV), I_{SINK} = 100µA			20	mV
Unity-Gain BW			1.5		MHz
Phase Margin	C_{LOAD} = 10pF, R_{LOAD} = 10kΩ to 100kΩ		+80		Degrees
	C_{LOAD} = 100pF, R_{LOAD} = 10kΩ to 100kΩ		+40		
Slew Rate	C_{LOAD} = 100pF		3.5		V/µs
Input Offset Voltage	V_{CM} = 1.25V and 2.5V	-3		+3	mV
Input Leakage Current		-10		+10	nA
Input Common-Mode Range (CMVR)		+0.50		V_{AVL} - 2.0	V
Common-Mode Rejection Ratio (CMRR)			75		dB
DRIVERS					
DH, DL Break-Before-Make Time	C_{LOAD} = 2000pF		20		ns
DH On-Resistance in Low State	V_{BST} - V_{LX} = 5V		1.0	2.5	Ω
DH On-Resistance in High State	V_{BST} - V_{LX} = 5V		1.5	3.3	Ω
DL On-Resistance in Low State	V_{VL} = V_{V+} = 5V		0.45	1.0	Ω
DL On-Resistance in High State	V_{VL} = V_{V+} = 5V		1.3	2.5	Ω
BST Bias Current	V_{BST} = 33V, V_{LX} = 28V, V_{EN} = 0V		230	520	µA
LX Bias Current	V_{BST} = 33V, V_{LX} = 28V, V_{EN} = 0V		-230	-520	µA
BST/LX Leakage Current	V_{BST} = V_{LX} = 28V, V_{EN} = 0V			50	µA
LOGIC INPUTS (EN)					
Input Low Level	4.5V < V_{VL} = V_{V+} = V_{AVL} < 5.5V		1.14	0.80	V
Input High Level	4.5V < V_{VL} = V_{V+} = V_{AVL} < 5.5V	2.40	1.73		V
Input Bias Current	V_{VL} = V_{V+} = V_{AVL} = 5.5V, V_{EN} = 0 to 5.5V	-1		+1	µA

Low-Dropout, Wide-Input-Voltage, Step-Down Controllers

ELECTRICAL CHARACTERISTICS (continued)

(V_{V+} = V_{VL} = V_{AVL} = V_{EN} = V_{REFIN} = 5V, V_{BST} = 6V, V_{LX} = 1V, C_{VL} = 4.7µF, C_{REFOUT} = 1µF, V_{AIN-} = V_{AOUT}, V_{AIN+} = 2.5V, V_{ILIM} = V_{LX} - 0.2V, V_{FB} = 0.65V, GND = PGND = 0V, C_{SS} = 0.01µF, R_{FREQ} = 20kΩ, **T_A = 0°C to +85°C**, typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
REFIN INPUT (MAX8597 only)					
REFIN Input Voltage Range		0		2.75	V
REFIN Dual Mode™ Threshold		V_{AVL} - 1.0		V_{AVL} - 0.5	V
REFIN Input Bias Current	V_{REFIN} = 1.25V or 2.5V	-250		+250	nA
OV AND UV FAULT COMPARATORS					
Upper FB Fault Threshold (OV)	Rising edge, hysteresis = 15mV (MAX8599 only)	115	117	120	%
Lower FB Fault Threshold (UV)	Falling edge, hysteresis = 15mV	67	70	73	%
POWER-OK OUTPUT (POK) (MAX8598/MAX8599 only)					
POK Delay	For both FB rising and falling edges		8		Clock cycles
Lower FB POK Threshold	FB falling, hysteresis = 20mV	85	88	90	%
POK Output Low Level	I_{SINK} = 2mA			0.4	V
POK Output High Leakage	V_{POK} = 5.5V			5	µA

ELECTRICAL CHARACTERISTICS

(V_{V+} = V_{VL} = V_{AVL} = V_{EN} = V_{REFIN} = 5V, V_{BST} = 6V, V_{LX} = 1V, C_{VL} = 4.7µF, C_{REFOUT} = 1µF, V_{AIN-} = V_{AOUT}, V_{AIN+} = 2.5V, V_{ILIM} = V_{LX} - 0.2V, V_{FB} = 0.65V, GND = PGND = 0V, C_{SS} = 0.01µF, R_{FREQ} = 20kΩ, **T_A = -40°C to +85°C**, typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL					
V+ Operating Range		5.5		28.0	V
V+/VL Operating Range	V+ = VL	4.5		5.5	V
V+ Operating Supply Current	V_{V+} = 12V, VL unloaded, no MOSFETs connected, V_{FB} = 0V			5.0	mA
VL REGULATOR					
Output Voltage	5.5V < V_{V+} < 28V, 1mA < I_{LOAD} < 35mA	4.7		5.3	V
VL Undervoltage-Lockout Trip Level	Rising edge, typical hysteresis = 460mV	4.05		4.35	V
REFERENCE (MAX8597 only)					
REFOUT Output Voltage	I_{REFOUT} = 150µA, V_{V+} = V_{VL} = 4.5V or 5.5V	2.47		2.51	V
REFOUT Load Regulation	I_{REFOUT} = 10µA to 1mA			10	mV
CURRENT-LIMIT COMPARATOR (all current limits are tested at V_{V+} = V_{VL} = 4.5V and 5.5V)					
ILIM Sink Current	V_{ILIM} = V_{LX} - 0.2V, 1.8V < V_{LX} < 28V, V_{BST} = V_{LX} + 5V	180		220	µA
Comparator Input Offset Voltage Error		-10		+10	mV
SOFT-START					
Soft-Start Source Current	V_{SS} = 100mV	3		7	µA
Soft-Start Sink Current	V_{SS} = (0.6V or V_{REFIN})	3		7	µA

Dual Mode is a trademark of Maxim Integrated Products, Inc.

ELECTRICAL CHARACTERISTICS (continued)

(V_{V+} = V_{VL} = V_{AVL} = V_{EN} = V_{REFIN} = 5V, V_{BST} = 6V, V_{LX} = 1V, C_{VL} = 4.7µF, C_{REFOUT} = 1µF, V_{AIN-} = V_{AOUT}, V_{AIN+} = 2.5V, V_{ILIM} = V_{LX} - 0.2V, V_{FB} = 0.65V, GND = PGND = 0V, C_{SS} = 0.01µF, R_{FREQ} = 20kΩ, **T_A = -40°C to +85°C**, typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
FREQUENCY					
Frequency	R_{FREQ} = 100kΩ	140		240	kHz
	R_{FREQ} = 20.0kΩ	800		1200	
	R_{FREQ} = 14.3kΩ	1100		1700	
DH Minimum Off-Time		180		230	ns
DH Minimum On-Time				140	ns
FB ERROR AMPLIFIER					
FB Input Bias Current				150	nA
FB Input Voltage Set Point	Over load and line	0.591		0.606	V
FB Offset Error	V_{REFIN} = 1.25V and 2.5V, measured with respect to REFIN	+20		-20	mV
Error-Amp Open-Loop Voltage Gain	V_{COMP} = 1.2V to 2.4V	72			dB
UNCOMMITTED OPERATIONAL AMPLIFIER (MAX8597 only)					
Output Voltage Swing High	V_{AIN+} = 2.5V, V_{AIN-} = (V_{AIN+} - 100mV), I_{SOURCE} = 100µA	V_{AVL} - 20mV			V
Output Voltage Swing Low	V_{AIN+} = 2.5V, V_{AIN-} = (V_{AIN+} + 100mV), I_{SINK} = 100µA			20	mV
Input Offset Voltage	V_{CM} = 1.25V and 2.5V	-3		+3	mV
Input Common-Mode Range (CMVR)		+0.50		V_{AVL} - 2.0	V
DRIVERS					
DH On-Resistance in Low State	V_{BST} - V_{LX} = 5V			2.5	Ω
DH On-Resistance in High State	V_{BST} - V_{LX} = 5V			3.3	Ω
DL On-Resistance in Low State	V_{VL} = V_{V+} = 5V			1.0	Ω
DL On-Resistance in High State	V_{VL} = V_{V+} = 5V			3.5	Ω
BST Bias Current	V_{BST} = 33V, V_{LX} = 28V, V_{EN} = 0V			520	µA
LX Bias Current	V_{BST} = 33V, V_{LX} = 28V, V_{EN} = 0V			-520	µA
BST/LX Leakage Current	V_{BST} = V_{LX} = 28V, V_{EN} = 0V			50	µA
LOGIC INPUTS (EN)					
Input Low Level	4.5V < V_{VL} = V_{V+} = V_{AVL} < 5.5V			0.8	V
Input High Level	4.5V < V_{VL} = V_{V+} = V_{AVL} < 5.5V	2.4			V
Input Bias Current	V_{VL} = V_{V+} = V_{AVL} = 5.5V, V_{EN} = 0 to 5.5V	-1		+1	µA
REFIN INPUT (MAX8597 only)					
REFIN Input Voltage Range		0		2.75	V
REFIN Dual-Mode Threshold		V_{AVL} - 1.0		V_{AVL} - 0.5	V
REFIN Input Bias Current	V_{REFIN} = 1.25V or 2.5V	-250		+250	nA

Low-Dropout, Wide-Input-Voltage, Step-Down Controllers

ELECTRICAL CHARACTERISTICS (continued)

(V_{V+} = V_{VL} = V_{AVL} = V_{EN} = V_{REFIN} = 5V, V_{BST} = 6V, V_{LX} = 1V, C_{VL} = 4.7µF, C_{REFOUT} = 1µF, V_{AIN-} = V_{AOUT}, V_{AIN+} = 2.5V, V_{ILIM} = V_{LX} - 0.2V, V_{FB} = 0.65V, GND = PGND = 0V, C_{SS} = 0.01µF, R_{FREQ} = 20kΩ, **T_A = -40°C to +85°C**, typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

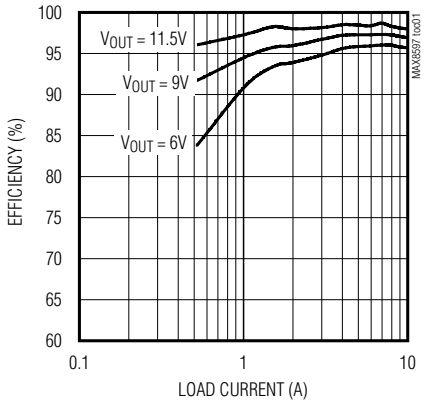
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OV AND UV FAULT COMPARATORS					
Upper FB Fault Threshold (OV)	Rising edge, hysteresis = 15mV (MAX8599 only)	115		120	%
Lower FB Fault Threshold (UV)	Falling edge, hysteresis = 15mV	67		73	%
POWER-OK OUTPUT (POK) (MAX8598/MAX8599 only)					
Lower FB POK Threshold	FB falling, hysteresis = 20mV	85		90	%
POK Output Low Level	I_{SINK} = 2mA			0.4	V
POK Output High Leakage	V_{POK} = 5.5V			5	µA

Note 1: Limits to -40°C are guaranteed by design and characterization.

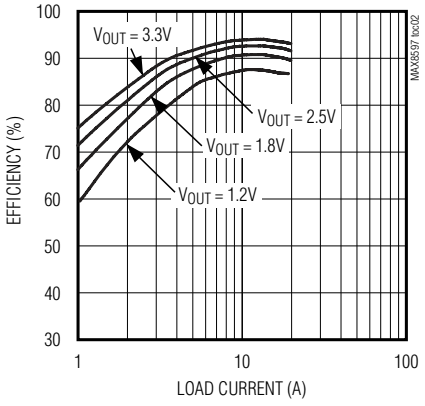
Typical Operating Characteristics

(Circuit of Figure 4, T_A = +25°C, 500kHz switching frequency, V_{IN} = 12V, unless otherwise noted.)

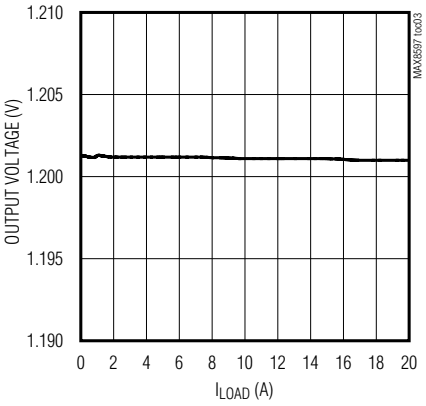
EFFICIENCY vs. LOAD CURRENT CIRCUIT OF FIGURE 1



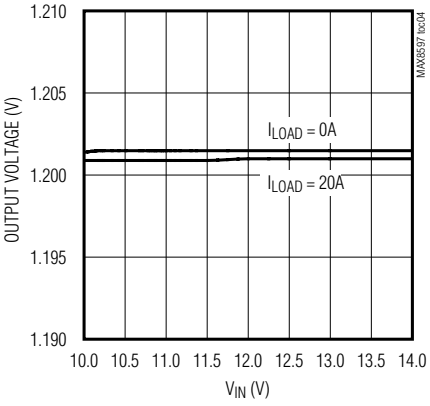
EFFICIENCY vs. LOAD CURRENT CIRCUIT OF FIGURE 2



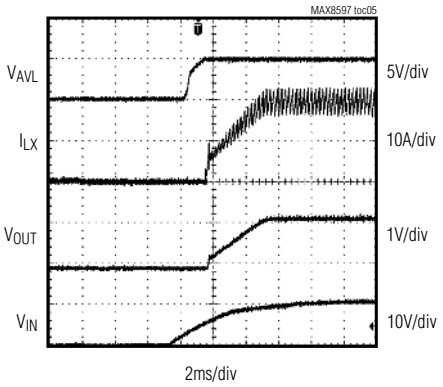
OUTPUT VOLTAGE vs. LOAD CURRENT



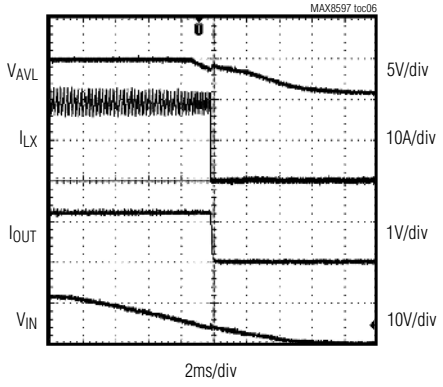
OUTPUT VOLTAGE vs. INPUT VOLTAGE



POWER-UP WAVEFORMS



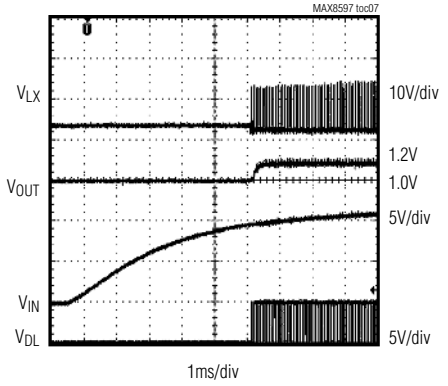
POWER-DOWN WAVEFORMS



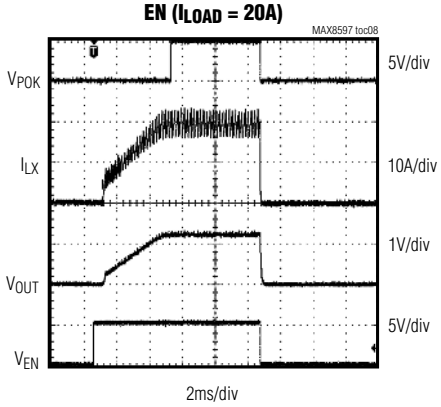
Typical Operating Characteristics (continued)

(Circuit of Figure 4, T_A = +25°C, 500kHz switching frequency, V_{IN} = 12V, unless otherwise noted.)

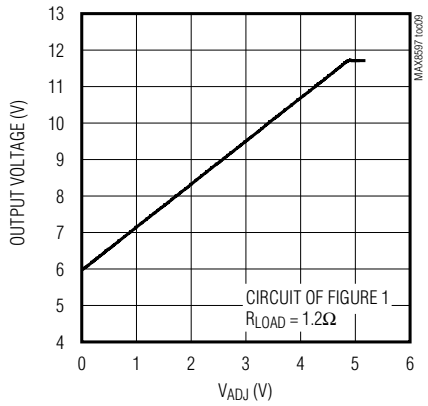
OUTPUT PREBIASED STARTUP



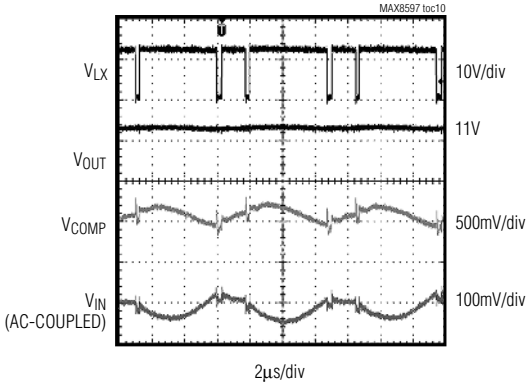
STARTUP/SHUTDOWN WITH EN (I_{LOAD} = 20A)



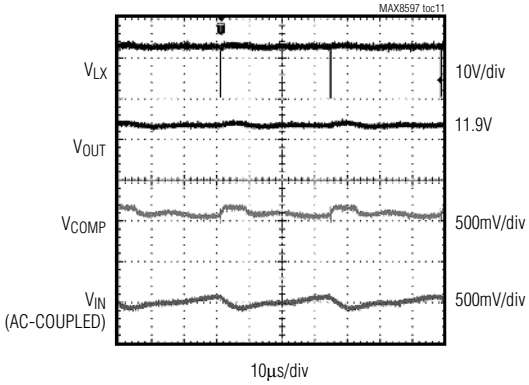
OUTPUT VOLTAGE vs. V_{ADJ} (V_{IN} = 12V)



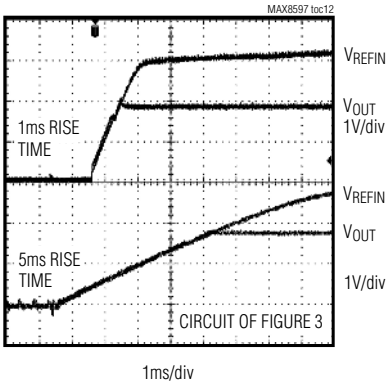
ENTERING DROPOUT WAVEFORMS CIRCUIT OF FIGURE 1



HEAVY-DROPOUT WAVEFORMS CIRCUIT OF FIGURE 1



OUTPUT TRACKING REFIN

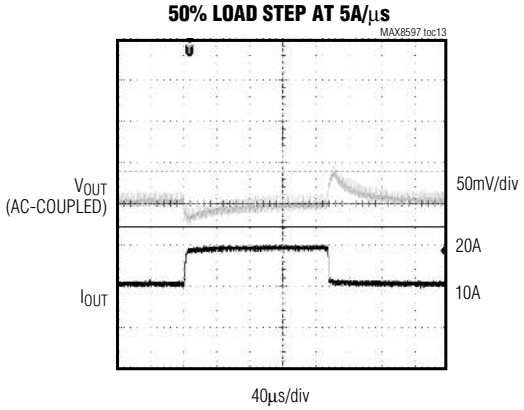


Low-Dropout, Wide-Input-Voltage, Step-Down Controllers

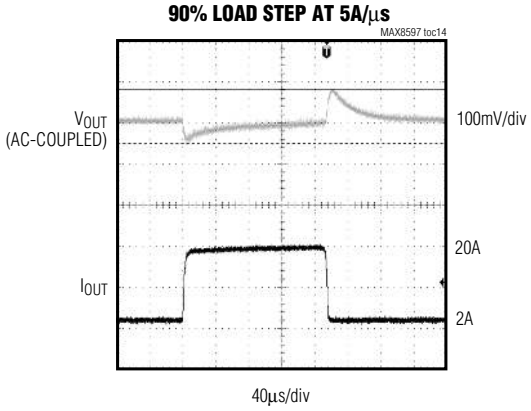
Typical Operating Characteristics (continued)

(Circuit of Figure 4, T_A = +25°C, 500kHz switching frequency, V_{IN} = 12V, unless otherwise noted.)

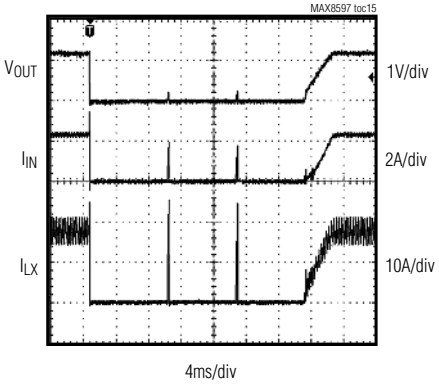
50% LOAD STEP AT 5A/µs



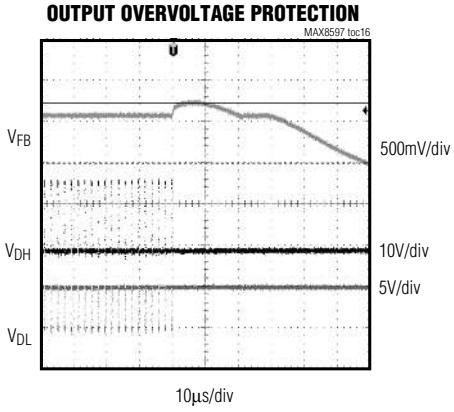
90% LOAD STEP AT 5A/µs



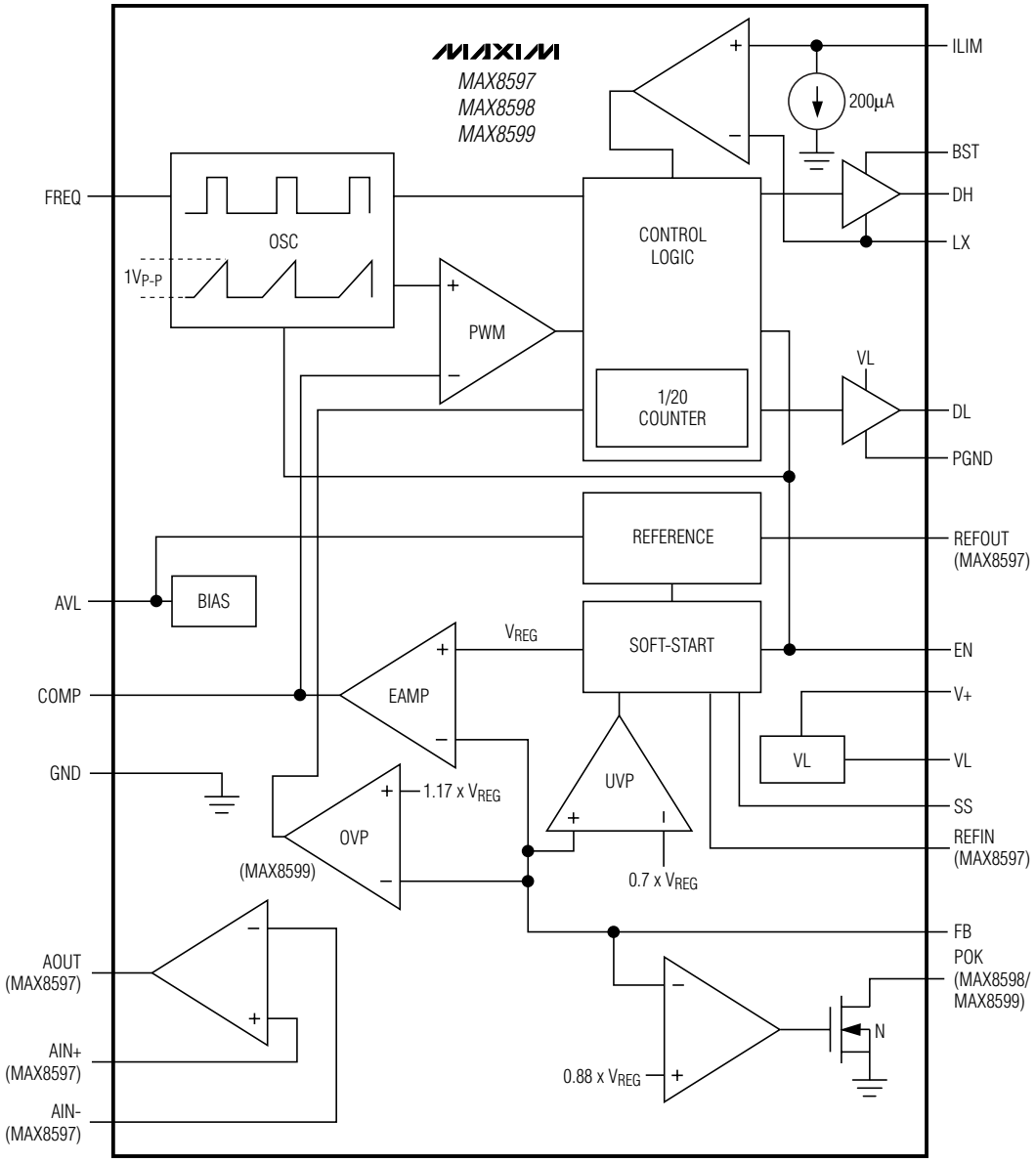
SHORT-CIRCUIT RESPONSE



OUTPUT OVERVOLTAGE PROTECTION



Block Diagram



Pin Description

PIN		NAME	FUNCTION
MAX8597	MAX8598/ MAX8599		
1	1	AVL	Filtered VL Input. Connect to VL through a 10Ω resistor. Bypass to GND with a 0.22µF or larger ceramic capacitor.
2	—	REFIN	External Reference Input. FB tracks the voltage input to REFIN. Connect REFIN to AVL to use the internal 0.6V reference.
3	2	GND	Analog Ground. Connect to the exposed paddle and analog ground plane and then connect to PGND at the output ground.
4	3	SS	Soft-Start Programming Input. Connect a capacitor from SS to GND to set the soft-start time. See the *Selecting the Soft-Start Capacitor* section for details.
5	4	FB	Feedback Input. Connect to the center tap of an external resistor-divider to set the output voltage. Regulates to 0.6V for the MAX8598/MAX8599 and MAX8597 when REFIN is connected to AVL. Regulates to V_{REFIN} (MAX8597) when using an external reference.
6	5	COMP	Compensation Input. Connect to the required compensation network. See the *Compensation Design* section for details.
7	6	EN	Enable Input. Drive EN high to enable the IC. Drive low to shut down the IC.
8	—	REFOUT	Internal Reference Output. REFOUT regulates to 2.5V and can source up to 1mA. REFOUT discharges to GND during UVLO.
9	7	V+	Input Supply Voltage for Internal VL Regulator. Connect to an input supply in the 4.5V to 28V range. Bypass to GND with a 1µF or larger ceramic capacitor through a 3Ω resistor.
10	8	VL	Internal 5V Linear-Regulator Output. VL provides power for the internal MOSFET gate drivers. Bypass to PGND with a 1µF or larger ceramic capacitor. VL is always enabled except in thermal shutdown. See the *Internal 5V Linear Regulator* section for details.
11	9	DL	Low-Side Gate-Driver Output. Connect to the gate of the synchronous rectifier. DL swings from PGND to VL. DL is held low during shutdown.
12	10	PGND	Power Ground. Connect to the synchronous rectifier's source and PGND plane.
13	11	BST	Bootstrap Input Supply for the High-Side MOSFET Driver. Connect to the cathode of an external diode from VL and connect a 0.1µF or larger capacitor from BST to LX.
14	12	DH	High-Side Gate-Driver Output. Connect to the gate of the high-side MOSFET. DH swings from LX to BST. DH is low (connected to LX) during shutdown.
15	13	LX	External Inductor Connection. LX is the low supply for the DH gate driver as well as the sense connection for the current-limit circuitry. Connect LX to the switched side of the inductor as well as the source of the high-side MOSFET and the drain of the synchronous rectifier.
16	14	ILIM	Current-Limit Sense Input. Connect a resistor from ILIM to the current-sense point to set the output current limit. See the *Setting the Current Limit* section for details.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX8597	MAX8598/ MAX8599		
17	15	FREQ	Frequency Adjust Input. Connect a resistor from FREQ to GND to set the switching frequency. The range of the FREQ resistor is 14.3kΩ to 100kΩ (corresponding to 1400kHz to 200kHz).
18	—	AOUT	Output of the Uncommitted Operational Amplifier. AOUT is high impedance during undervoltage lockout.
19	—	AIN-	Inverting Input of the Uncommitted Operational Amplifier
20	—	AIN+	Noninverting Input of the Uncommitted Operational Amplifier
—	16	POK	Power-OK Output. POK is an open-drain output that goes high impedance when the regulator output is greater than 88% of the regulation threshold. POK is low during shutdown.
—	—	EP	Exposed Paddle. Connect to analog ground plane for improved thermal performance.

Detailed Description

The MAX8597/MAX8598/MAX8599 voltage-mode PWM step-down controllers are designed to operate from 4.5V to 28V input and generate output voltages down to 0.6V. A proprietary switching algorithm stretches the duty cycle to >99.5% for low-dropout design. Unlike conventional step-down regulators using a p-channel high-side MOSFET to achieve high duty cycle, the MAX8597/MAX8598/MAX8599 drive n-channel MOSFETs permitting high efficiency and high-current designs.

The MAX8597 is available in a 20-pin thin QFN package and is designed for applications that use an analog signal to control the output voltage with adjustable offset, such as DC fan speed control. For example, a 12VDC fan can be driven from 6V to 12V with 12V input power source depending on the system's cooling requirement to minimize fan noise and power consumption. This is achieved with an internal uncommitted operational amplifier. With the addition of an external RC filter, a PWM input can also be used to control the output voltage. The MAX8597 also generates a tracking output for chipsets, ASICs, and DSP where core and I/O supplies are split and require tracking. In applications where tighter output tolerance is required, the MAX8597 output can be set by an external precision reference source feeding to REFIN. The MAX8598/MAX8599 are available in a 16-pin thin QFN package and do not have the uncommitted operational amplifier, reference input, and reference output, but offer a power-OK output (POK). With the enable input and POK output, the MAX8598/MAX8599 can easily be configured to have power sequencing of multiple supply rails.

The MAX8597/MAX8598/MAX8599 allow startup with prebias voltage on the output for applications where a backup supply or a tracking device may charge the output capacitor before the MAX8597/MAX8598/MAX8599 are enabled. The MAX8599 has output overvoltage protection.

These controllers feature lossless high-side peak inductor current sensing, adjustable current limit, and hiccup-mode short-circuit protection. Switching frequency is set with an external resistor from 200kHz to 1.4MHz. This wide frequency range combined with a wide-bandwidth error amplifier enable the loop-compensation scheme to give the user ample flexibility to optimize for cost, size, and efficiency.

DC-DC Controller

The MAX8597/MAX8598/MAX8599 step-down DC-DC controllers use a PWM voltage-mode control scheme. An internal high-bandwidth (25MHz) operational amplifier is used as an error amplifier to regulate the output voltage. The output voltage is sensed and compared with an internal 0.6V reference or REFIN (MAX8597) to generate an error signal. The error signal is then compared with a fixed-frequency ramp by a PWM comparator to give the appropriate duty cycle to maintain output voltage regulation. The high-side MOSFET turns on at the rising edge of the internal clock 20ns after DL (the low-side MOSFET gate drive) goes low. The high-side MOSFET turns off once the internal ramp voltage reaches the error-amplifier output voltage. The process repeats for every clock cycle. During the high-side MOSFET on-time, current flows from the input through the inductor to the output capacitor and load. At the moment the high-side MOSFET turns off, the energy stored in the inductor during the on-time is released to support the load as the inductor

current ramps down through the low-side MOSFET body diode; 20ns after DH goes low, the low-side MOSFET turns on, resulting in a lower voltage drop to increase efficiency. The low-side MOSFET turns off at the rising edge of the next clock pulse, and when its gate voltage discharges to zero, the high-side MOSFET turns on and another cycle starts.

These controllers also sense peak inductor current and provide hiccup-overload and short-circuit protection (see the *Current Limit* section). The MAX8597/MAX8598/MAX8599 operate in forced-PWM mode where the inductor current is always continuous. The controller maintains constant switching frequency under all loads, except under dropout conditions where it skips DL pulses.

Current Limit

The MAX8597/MAX8598/MAX8599 DC-DC step-down controllers sense the peak inductor current either with the on-resistance of the high-side MOSFET for lossless sensing, or a series resistor for more accurate sensing. When the voltage across the sensing element exceeds the current-limit threshold set with ILIM, the controller immediately turns off the high-side MOSFET. The low-side MOSFET is then turned on to let the inductor current ramp down. As the output load current increases above the ILIM threshold, the output voltage sags because the truncated duty cycle is insufficient to support the load current. When FB falls 30% below its nominal threshold, the output undervoltage protection is triggered and the controller enters hiccup mode to limit power dissipation. This current-limit method allows the circuit to withstand a continuous output short circuit.

The MAX8597/MAX8598/MAX8599 current-limit threshold is set by an external resistor that works in conjunction with an internal 200µA current sink (see the *Setting the Current Limit* section for more details).

Synchronous-Rectifier Driver (DL)

Synchronous rectification reduces the conduction loss in the rectifier by replacing the normal Schottky catch diode with a low-resistance MOSFET switch. The MAX8597/MAX8598/MAX8599 also use the synchronous rectifier to ensure proper startup of the boost gate-drive circuit.

High-Side Gate-Drive Supply (BST)

Gate-drive voltage for the high-side n-channel MOSFET is generated by an external flying capacitor and diode boost circuit (D1 and C5 in Figure 1). When the synchronous rectifier is on, C5 is charged from the VL supply through the Schottky diode. When the synchronous rectifier is turned off, the Schottky is reverse biased and the voltage on C5 is stacked above LX to provide the necessary turn-on voltage for the high-side MOSFET. A low-current Schottky diode, such as Central Semiconductor's CMDSH-3, works well for most applications. The capacitor should be large enough to prevent it from charging to excessive voltage, but small enough to adequately charge during the minimum low-side MOSFET on-time, which occurs at minimum input voltage. A capacitor in the 0.1µF to 0.47µF range works well for most applications.

Internal 5V Linear Regulator

The MAX8597/MAX8598/MAX8599 contain a low-dropout 5V regulator that provides up to 35mA to supply gate drive for the external MOSFETs, and supplies AVL, which powers the IC's internal circuitry. Bypass the regulator's output (VL) with 1µF per 10mA of VL load, or greater ceramic capacitor. The current required to drive the external MOSFET can be estimated by multiplying the total gate charge (at V_{GS} = 5V) of the MOSFETs by the switching frequency.

Undervoltage Lockout (UVLO)

When V_{VL} drops below 3.75V (typ), the MAX8597/MAX8598/MAX8599s' undervoltage-lockout (UVLO) circuitry inhibits switching, forces POK (MAX8598/MAX8599) low, and forces DH and DL low. Once V_{VL} rises above 4.2V (typ), the controller powers up the output in startup mode (see the *Startup* section).

Startup

The MAX8597/MAX8598/MAX8599 start switching once all the following conditions are met:

1) EN is high.
2) V_{VL} > 4.2V (typ).
3) Soft-start voltage V_{SS} exceeds V_{FB}.
4) Thermal limit is not exceeded.

The third condition ensures that the MAX8597/MAX8598/MAX8599 do not discharge a prebiased output. Once all of these conditions are met, the IC begins switching and the soft-start cycle is initiated.

Power-OK Signal (POK, MAX8598/MAX8599 Only)

The power-OK signal (POK) is an open-drain output that goes high impedance when FB is above 91% of its nominal threshold. There is an eight clock-cycle delay before POK goes high impedance. For 500kHz switching frequency, this delay is typically 16µs. To obtain a logic voltage output, connect a pullup resistor from POK to AVL. A 100kΩ resistor works well for most applications. If unused, connect POK to GND or leave it unconnected.

Enable and Soft-Start

The MAX8597/MAX8598/MAX8599 are enabled using the EN input. A logic high on EN enables the output of the IC. Conversely, a logic low on EN disables the output. On the rising edge of EN, the controllers enter soft-start. Soft-start gradually ramps up the reference voltage seen at the error amplifier to control the output rate of rise and reduce the inrush current during start-up. The soft-start period is determined by a capacitor connected from SS to GND (C6 in Figure 1). A 5µA current source charges the external capacitor to the reference voltage (0.6V or V_{REFIN}). The capacitor value is determined as follows:

$$C6 = \frac{5\mu A \times t_{SS}}{V_{FB}}$$

where t_{SS} is the soft-start time in seconds and V_{FB} is 0.6V or V_{REFIN}. The output reaches regulation when soft-start is completed.

Output Undervoltage Protection (UVP)

Output UVP begins when the controller is at its current limit and V_{FB} is 30% below its nominal threshold. This condition causes the controller to drive DH and DL low and discharges the soft-start capacitor with a 5µA pull-down current until V_{SS} reaches 50mV. Then the controller begins in soft-start mode. If the overload condition still exists, the UVP process begins again. The result is "hiccup" mode, where the controller attempts to restart periodically as long as the overload condition exists. In hiccup mode, the soft-start capacitor voltage ramps up to 112% of the nominal V_{FB} threshold and then ramps down to 50mV. For the MAX8597, V_{REFIN} must be greater than 450mV to trigger UVP. The soft-start capacitor voltage then ramps up to 112% of V_{REFIN} and then down to 50mV.

Output Overvoltage Protection (OVP, MAX8599)

The output voltage is continuously monitored for overvoltage (MAX8599 only). If the output voltage is more than 117% of its nominal set value, OVP is triggered after a 12µs (typ) delay. The MAX8599 latches DH low to turn off the high-side MOSFET, and DL high to turn on the low-side MOSFET to clamp the output to PGND. The latch is reset either by toggling EN or by cycling V+ below the UVLO threshold. Note that DL latching high causes a negative spike at the output due to the energy stored in the output LC at the instant of OVP trip. If the load cannot tolerate this negative spike, add a power Schottky diode across the output to act as a reverse polarity clamp.

Thermal-Overload Protection

Thermal-overload protection limits the total power dissipation in the MAX8597/MAX8598/MAX8599. When the junction temperature exceeds +160°C, a thermal sensor shuts down the device, forcing DH and DL low, allowing the IC to cool. The thermal sensor turns the part on after the junction temperature cools by 10°C, resulting in a pulsed output during continuous thermal-overload conditions. During a thermal event, the switching converter is turned off, the reference is turned off, the VL regulator is turned off, POK is high impedance, and the soft-start capacitor is discharged.

Low-Dropout, Wide-Input-Voltage, Step-Down Controllers

Design Procedure

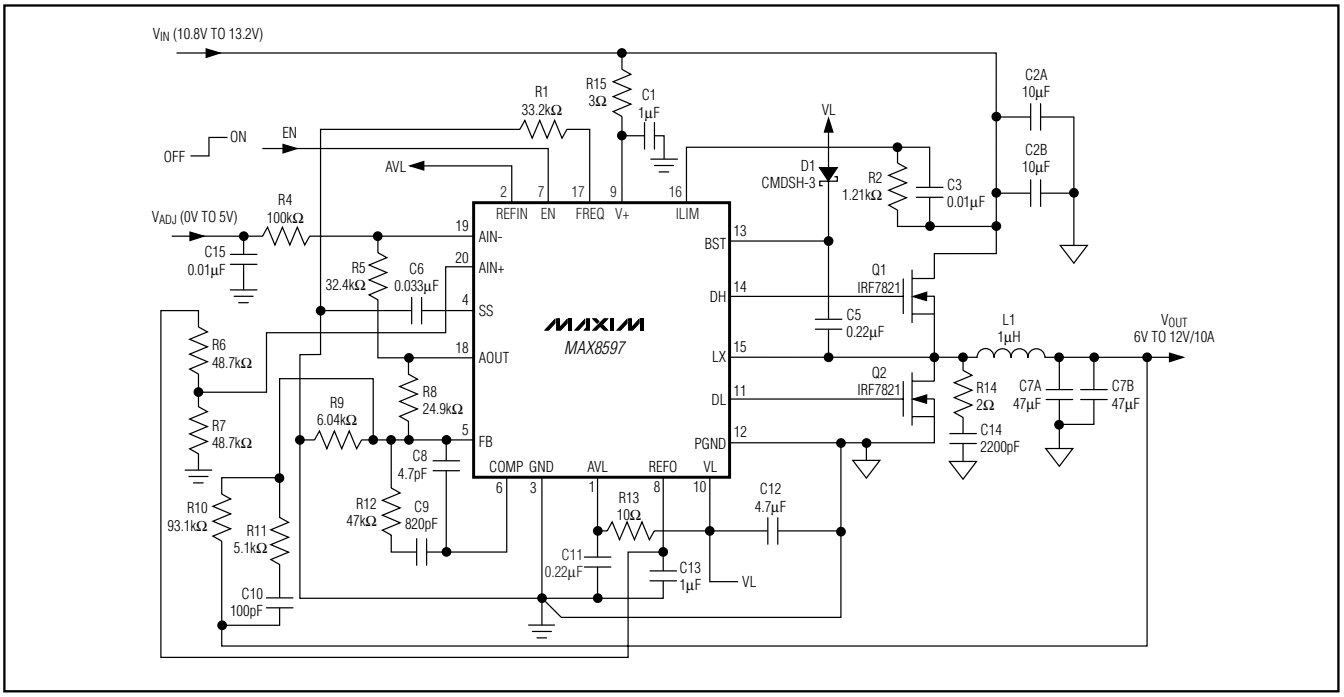


Figure 1. MAX8597 (600kHz): Live Adjustable Output Voltage from 6V to 12V at 10A

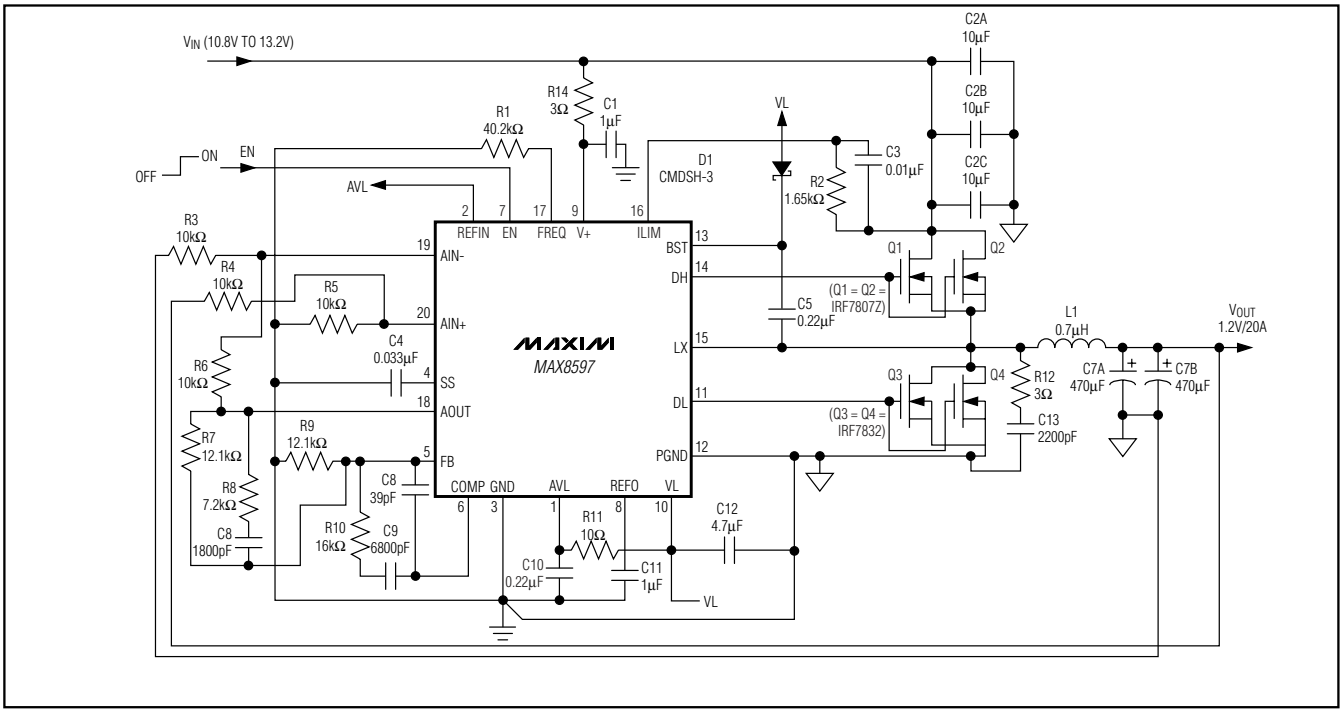


Figure 2. 1.2V at 20A Output with Remote Sensing

Design Procedure (continued)

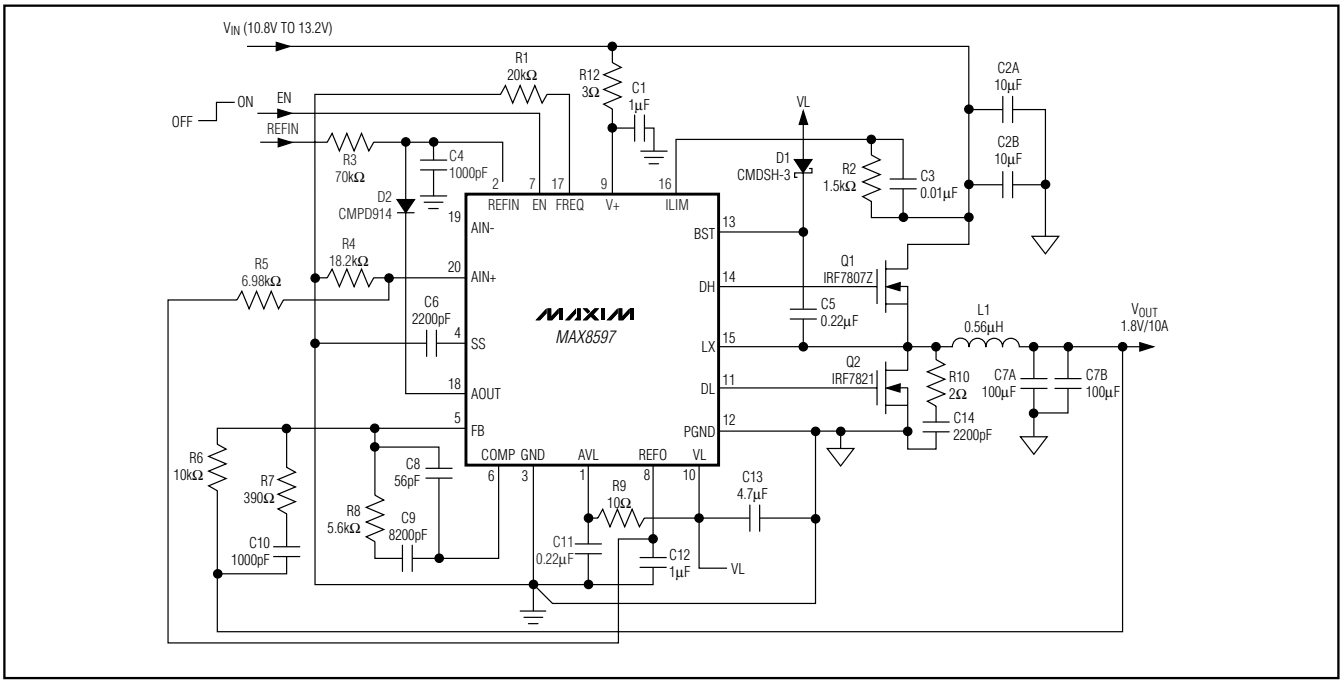


Figure 3. MAX8597 1MHz Tracking Supply with Clamp (Output voltage tracks V_{REFIN} from 0V up to the nominal output regulation voltage.)

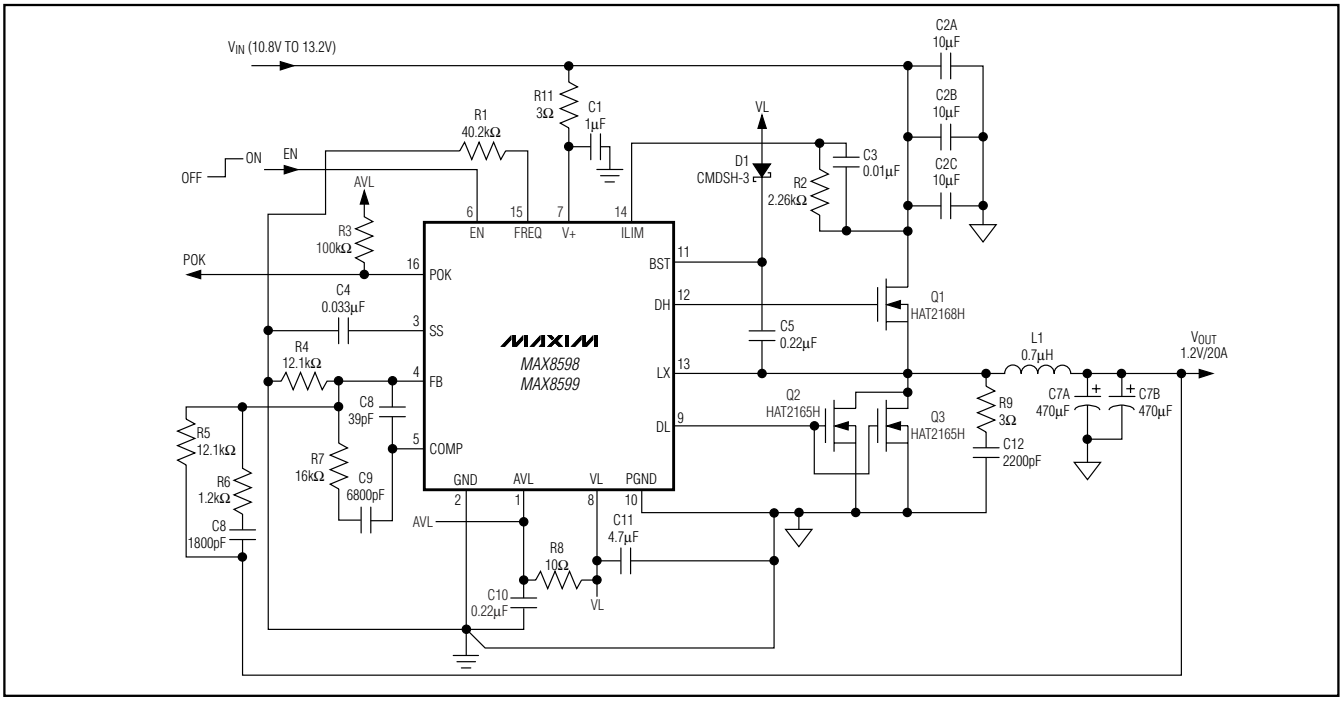


Figure 4. MAX8598/MAX8599 500kHz, 1.2V, 20A Output Power Supply

Low-Dropout, Wide-Input-Voltage, Step-Down Controllers

Setting the Output Voltage

Fixed Output Voltage

The output voltage is set by a resistor-divider network from the output to GND with FB at the center tap (R4 and R5 in Figure 4). Select R4 between 5kΩ and 15kΩ and calculate R5 by:

$$R5 = R4 \times [(V_{OUT} / V_{FB}) - 1]$$

Live Adjustable Output Voltage (see Figure 1)

Using the uncommitted operational amplifier, the MAX8597 can be configured such that the output voltage is adjustable using a voltage source (V_{ADJ}). The following parameters must be defined before starting the design:

- The minimum desired output voltage, V_{OUT_MIN}
- The maximum desired output voltage, V_{OUT_MAX}
- The desired input that corresponds to the minimum output voltage, V_{ADJ_MIN}
- The desired input that corresponds to the maximum output voltage, V_{ADJ_MAX}

Select V_{AOUT} (uncommitted operational-amplifier output) between 0.05V and 3V and V_{AOUT_MAX} higher than V_{AOUT_MIN}. Calculate the required AIN+ reference (V_{AIN+}) as:

$$V_{AIN+} = \frac{V_{AOUT\_MAX} \times V_{ADJ\_MAX} - V_{AOUT\_MIN} \times V_{ADJ\_MIN}}{(V_{ADJ\_MAX} - V_{ADJ\_MIN}) + (V_{AOUT\_MAX} - V_{AOUT\_MIN})}$$

V_{AIN+} is set using a resistor-divider from REFOUT to GND (R6 and R7). Select R7 to be approximately 50kΩ as a starting point and then calculate R6 as:

$$R6 = R7 \times [(2.5V / V_{AIN+}) - 1]$$

Select R4 to be 100kΩ and calculate R5 as:

$$R5 = \frac{(V_{AIN+} - V_{AOUT\_MIN}) \times R4}{(V_{ADJ\_MAX} - V_{AIN+})}$$

Select R9 between 5kΩ and 15kΩ, then calculate R8 and R10 as follows:

$$R8 = \frac{\left[(V_{OUT\_MIN} - V_{FB}) \times (V_{FB} - V_{AOUT\_MIN}) + (V_{OUT\_MAX} - V_{FB}) \times (V_{AOUT\_MAX} - V_{FB})\right]}{\left((V_{OUT\_MAX} - V_{FB}) - (V_{OUT\_MIN} - V_{FB})\right) \times V_{FB}} \times R9$$

$$R10 = \frac{R8 \times R9 \times (V_{OUT\_MAX} - V_{FB})}{(V_{FB} \times R8) + \left[(V_{FB} - V_{AOUT\_MIN}) \times R9\right]}$$

where V_{FB} is the feedback regulation voltage (0.6V with REFIN connected to AVL).

Additionally, to minimize error, R6 and R7 should be chosen such that:

$$\frac{R6 \times R7}{R6 + R7} = \frac{R4 \times R5}{R4 + R5}$$

Inductor Selection

There are several parameters that must be examined when determining which inductor is to be used: input voltage, output voltage, load current, switching frequency, and LIR. LIR is the ratio of inductor current ripple to DC load current. A higher LIR value allows for a smaller inductor but results in higher losses and higher output ripple. A good compromise between size and efficiency is a 30% LIR. Once all the parameters are chosen, the inductor value is determined as follows:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_S \times I_{LOAD(MAX)} \times LIR}$$

where f_S is the switching frequency. Choose a standard value close to the calculated value. The exact inductor value is not critical and can be adjusted in order to make trade-offs among size, cost, and efficiency. Lower inductor values minimize size and cost, but also increase the output ripple and reduce the efficiency due to higher peak currents. On the other hand, higher inductor values increase efficiency, but eventually resistive losses due to extra turns of wire exceed the benefit gained from lower AC current levels. Find a low-loss inductor having the lowest possible DC resistance that fits the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well up to 300kHz. The chosen inductor's saturation current rating must exceed the peak inductor current determined as:

$$I_{PEAK} = I_{LOAD(MAX)} + \left(\frac{LIR}{2}\right) \times I_{LOAD(MAX)}$$

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents defined by the following equation:

$$I_{RMS} = \frac{I_{LOAD} \times \sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage (V_{IN} = 2 x V_{OUT}), so $I_{RMS(MAX)}$ = I_{LOAD} / 2. Ceramic capacitors are recommended due to their low ESR and ESL at high frequency, with relatively lower cost. Choose a capacitor that exhibits less than 10°C temperature rise at the maximum operating RMS current for optimum long-term reliability.

Output Capacitor

The key selection parameters for the output capacitor are the actual capacitance value, the equivalent series resistance (ESR), the equivalent series inductance (ESL), and the voltage-rating requirements, which affect the overall stability, output ripple voltage, and transient response. The output ripple has three components: variations in the charge stored in the output capacitor, voltage drop across the capacitor's ESR, and voltage drop across the capacitor's ESL, caused by the current into and out of the capacitor. The following equations estimate the worst-case ripple:

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} = I_{P-P} \times ESR$$

$$V_{RIPPLE(ESL)} = \frac{V_{IN} \times ESL}{L + ESL}$$

$$V_{RIPPLE(C)} = \frac{I_{P-P}}{8 \times C_{OUT} \times f_S}$$

$$I_{P-P} = \left(\frac{V_{IN} - V_{OUT}}{f_S \times L}\right) \times \left(\frac{V_{OUT}}{V_{IN}}\right)$$

where I_{P-P} is the peak-to-peak inductor current.

The response to a load transient depends on the selected output capacitor. After a load transient, the output instantly changes by (ESR x ΔI_{LOAD}) + (ESL x di/dt). Before the controller can respond, the output deviates further depending on the inductor and output capacitor values. After a short period of time (see the *Typical Operating Characteristics*), the controller responds by regulating the output voltage back to its nominal state. The controller response time depends on the closed-loop bandwidth. With higher bandwidth, the response time is faster, preventing the output capacitor voltage from further deviation from its regulation value. Do not exceed the capacitor's voltage or ripple current ratings.

MOSFET Selection

The MAX8597/MAX8598/MAX8599 controllers drive external, logic-level, n-channel MOSFETs as the circuit-switch elements. The key selection parameters are:

- On-resistance ($R_{DS(ON)}$): the lower, the better.
- Maximum drain-to-source voltage (V_{DSS}): should be at least 20% higher than the input supply rail at the high-side MOSFET's drain.
- Gate charges (Q_g, Q_{gd}, Q_{gs}): the lower, the better.

Choose MOSFETs with $R_{DS(ON)}$ rated at V_{GS} = 4.5V. For a good compromise between efficiency and cost, choose the high-side MOSFET that has conduction loss equal to the switching loss at the nominal input voltage and maximum output current. For the low-side MOSFET, make sure it does not spuriously turn on due to dv/dt caused by the high-side MOSFET turning on, resulting in efficiency degrading shoot-through current. MOSFETs with a lower Q_{gd}/Q_{gs} ratio have higher immunity to dv/dt.

For proper thermal-management design, the power dissipation must be calculated at the desired maximum operating junction temperature, maximum output current, and worst-case input voltage (for low-side MOSFET, worst case is at $V_{IN(MAX)}$; for high-side MOSFET, it could be either at $V_{IN(MIN)}$ or $V_{IN(MAX)}$).

High-side and low-side MOSFETs have different loss components due to the circuit operation. The low-side MOSFET operates as a zero-voltage switch; therefore, the major losses are the channel-conduction loss (P_{LSCC}) and the body-diode conduction loss (P_{LSDC}):

$$P_{LSCC} = [1 - (V_{OUT} / V_{IN})] \times (I_{LOAD})^2 \times R_{DS(ON)}$$

$$P_{LSDC} = 2 \times I_{LOAD} \times V_F \times t_{dt} \times f_S$$

where V_F is the body-diode forward-voltage drop, t_{dt} is the dead-time between the high-side MOSFET and the low-side MOSFET switching transitions, and f_S is the switching frequency. The high-side MOSFET operates as a duty-cycle control switch and has the following major losses: the channel-conduction loss (P_{HSCC}), the V-I overlapping switching loss (P_{HSSW}), and the drive loss (P_{HSDR}). The high-side MOSFET does not have body-diode conduction loss because the diode never conducts current:

$$P_{HSCC} = (V_{OUT} / V_{IN}) \times I_{LOAD}^2 \times R_{DS(ON)}$$

Use $R_{DS(ON)}$ at $T_{J(MAX)}$:

$$P_{HSSW} = V_{IN} \times I_{LOAD} \times f_S \times [(Q_{gs} + Q_{gd}) / I_{GATE}]$$

where I_{GATE} is the average DH-high driver output-current capability determined by:

$$I_{GATE} = 2.5 / (R_{DH} + R_{GATE})$$

Low-Dropout, Wide-Input-Voltage, Step-Down Controllers

where R_{DH} is the high-side MOSFET driver's average on-resistance (1.25Ω typ) and R_{GATE} is the internal gate resistance of the MOSFET (typically 0.5Ω to 2Ω):

$$P_{HSDR} = Q_{gs} \times V_{GS} \times f_S \times R_{GATE} / (R_{GATE} + R_{DH})$$

where $V_{GS} \sim V_{VL} = 5V$.

In addition to the losses above, add approximately 20% more for additional losses due to MOSFET output capacitances and low-side MOSFET body-diode reverse-recovery charge dissipated in the high-side MOSFET that exists, but is not well defined in the MOSFET data sheet. Refer to the MOSFET data sheet for thermal-resistance specification to calculate the PC board area needed to maintain the desired maximum operating junction temperature with the above-calculated power dissipation. To reduce EMI caused by switching noise, add a 0.1µF or larger ceramic capacitor from the high-side switch drain to the low-side switch source or add resistors in series with DH and DL to slow down the switching transitions. However, adding a series resistor increases the power dissipation of the MOSFETs, so be sure this does not overheat the MOSFETs. The minimum load current must exceed the high-side MOSFET's maximum leakage plus the maximum LX bias current over temperature.

Setting the Current-Limit

The MAX8597/MAX8598/MAX8599 controllers sense the peak inductor current to provide constant-current and hiccup current limit. The peak current-limit threshold is set by an external resistor (R2 in Figure 1) together with the internal current sink of 200µA. The voltage drop across the resistor R2 due to the 200µA current sets the maximum peak inductor current that can flow through the high-side MOSFET or the optional current-sense resistor (between the high-side MOSFET source and LX) by the equations below:

$$I_{PEAK(MAX)} = 200\mu A \times R2 / R_{DSON(HSFET)}$$

$$I_{PEAK(MAX)} = 200\mu A \times R2 / R_{SENSE}$$

The actual corresponding maximum load current is lower than the $I_{PEAK(MAX)}$ by half of the inductor ripple current. If the $R_{DS(ON)}$ of the high-side MOSFET is used for current sensing, use the maximum $R_{DS(ON)}$ at the highest operating junction temperature to avoid false tripping of the current limit at elevated temperature. Consideration should also be given to the tolerance of the 200µA current sink. When the $R_{DS(ON)}$ of the high-side MOSFET is used for current sensing, ringing on the LX voltage waveform can interfere with the current limit. Below is the procedure for selecting the value of the series RC snubber circuit (R14 and C14 in Figure 1):

1) Connect a scope probe to measure V_{LX} to GND, and observe the ringing frequency, f_R.
2) Find the capacitor value (connected from LX to GND) that reduces the ringing frequency by half. The circuit parasitic capacitance (C_{PAR}) at LX is then equal to 1/3 the value of the added capacitance above. The circuit parasitic inductance (L_{PAR}) is calculated by:

$$L_{PAR} = \frac{1}{(2\pi \times f_R)^2 \times C_{PAR}}$$

The resistor for critical dampening (R14) is equal to $2\pi \times f_R \times L_{PAR}$. Adjust the resistor value up or down to tailor the desired damping and the peak voltage excursion.

The capacitor (C14) should be at least 2 to 4 times the value of the C_{PAR} in order to be effective. The power loss of the snubber circuit is dissipated in the resistor (R14) and is calculated as:

$$P_{R14} = C14 \times (V_{IN})^2 \times f_S$$

where V_{IN} is the input voltage and f_S is the switching frequency. Choose an R14 power rating that meets the specific application's derating rule for the power dissipation calculated.

Additionally, there is parasitic inductance of the current-sensing element, whether the high-side MOSFET (L_{SENSE_FET}) or the optional current-sense resistor (L_{RSENSE}) are used, which is in series with the output filter inductor. This parasitic inductance, together with the output inductor, forms an inductive divider and causes error in the current-sensing voltage. To compensate for this error, a series RC circuit can be added in parallel with the sensing element (see Figure 5). The RC time constant should equal L_{RSENSE} / R_{SENSE}, or $L_{SENSE\_FET} / R_{DS(ON)}$. First, set the value of R equal to or less than R2 / 100. Then, the value of C is calculated as:

$$C = L_{RSENSE} / (R_{SENSE} \times R) \text{ or}$$
$$C = L_{SENSE\_FET} / (R_{DS(ON)} \times R)$$

Any PC board trace inductance in series with the sensing element and output inductor should be added to the specified FET or resistor inductance per the respective manufacturer's data sheet. For the case of

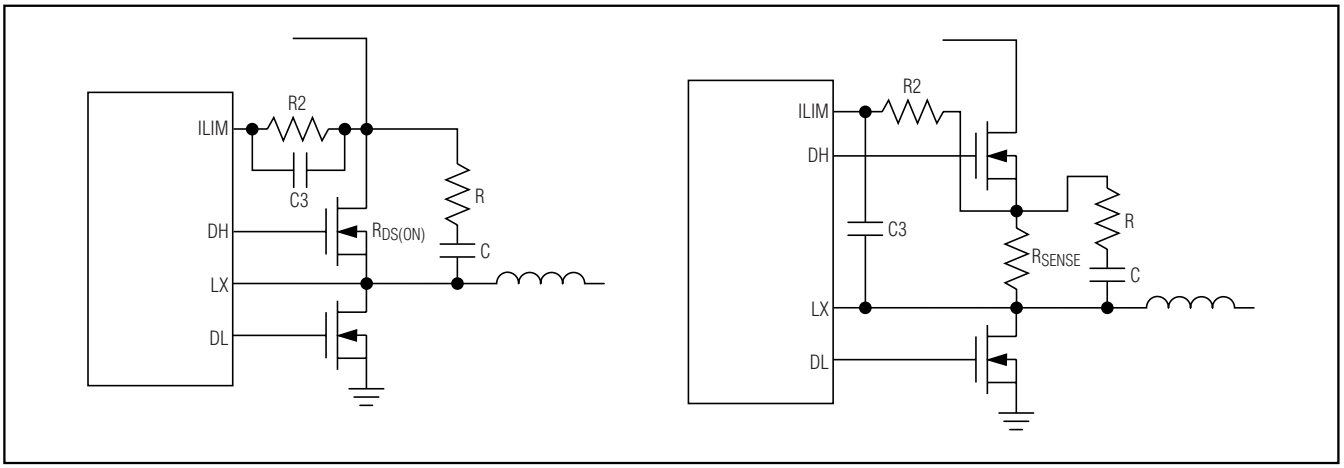


Figure 5. Adding RC for More Accurate Sensing

the MOSFET, it is the inductance from the drain to the source lead.

Alternately, to save board space and cost, the RC networks above can be omitted; however, the value of R_{ILIM} should be raised to account for the voltage step caused by the inductive divider.

An additional switching noise filter may be needed at ILIM by connecting a capacitor in parallel with R2 (in the case of $R_{DS(ON)}$ sensing) or from ILIM to LX (in the case of resistor sensing). For the case of $R_{DS(ON)}$ sensing, the value of the capacitor should be:

$$C3 > 15 / (\pi \times f_S \times R2)$$

For the case of resistor sensing:

$$C3 < 25 \times 10^{-9} / R2$$

Selecting the Soft-Start Capacitor

An external capacitor from SS to GND is charged by an internal 5µA current source, to the corresponding feedback threshold. Therefore, the soft-start time is calculated as:

$$t_{SS} = C_{SS} \times V_{FB} / 5\mu A$$

For example, 0.033µF from SS to GND yields approximately a 3.96ms soft-start period.

In the tracking application (see Figure 3), the output voltage is required to track REFIN during REFIN rise and fall time. C_{SS} must be chosen so that t_{ss} is less than REFIN rise and fall time.

Compensation Design

The MAX8597/MAX8598/MAX8599 use a voltage-mode control scheme that regulates the output voltage by comparing the error-amplifier output (COMP) with a fixed internal ramp to produce the required duty cycle. The error amplifier is an operational amplifier with 25MHz bandwidth to provide fast response. The output lowpass LC filter creates a double pole at the resonant frequency that introduces a gain drop of 40dB per decade and a phase shift of 180 degrees per decade. The error amplifier must compensate for this gain drop and phase shift to achieve a stable high-bandwidth closed-loop system. The Type III compensation scheme (Figure 6) is used to achieve this stability.

The basic regulator loop can be thought of as consisting of a power modulator and an error amplifier. The power modulator has a DC gain set by V_{IN} / V_{RAMP}, with a double pole, f_{P_LC}, and a single zero, f_{Z_ESR}, set by the output inductor (L), the output capacitor (C_O), and its equivalent series resistance (R_{ESR}). Below are the equations that define the power modulator:

$$G_{MOD(DC)} = \frac{V_{IN}}{V_{RAMP}}, \text{ where } V_{RAMP} = 1V \text{ (typ)}$$

$$f_{P\_LC} = \frac{1}{2\pi\sqrt{L \times C_O}}$$

$$f_{Z\_ESR} = \frac{1}{2\pi \times R_{ESR} \times C_O}$$

where C_O is the total output capacitance and R_{ESR} is the total ESR of the output capacitors.

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When the output capacitor is comprised of paralleling n number of the same capacitors, then:

$$C_O = n \times C_{EACH}$$

and

$$R_{ESR} = R_{ESR\_EACH} / n$$

Thus, the resulting f_{Z_ESR} is the same as that of a single capacitor.

The total closed-loop gain must be equal to unity at the crossover frequency, where the crossover frequency is less than or equal to 1/5 the switching frequency (f_S):

$$f_C \le f_S / 5$$

So the loop-gain equation at the crossover frequency is:

$$G_{EA(FC)} \times G_{MOD(FC)} = 1$$

where $G_{EA(FC)}$ is the error-amplifier gain at f_C, and $G_{MOD(FC)}$ is the power-modulator gain at f_C.

The loop compensation is affected by the choice of output filter capacitor due to the position of its ESR-zero frequency with respect to the desired closed-loop crossover frequency. Ceramic capacitors are used for higher switching frequencies and have low capacitance and low ESR; therefore, the ESR-zero frequency is higher than the closed-loop crossover frequency. Electrolytic capacitors (e.g., tantalum, solid polymer, and OS-CON) are needed for lower switching frequencies and have high capacitance (and some have higher ESR); therefore, the ESR-zero frequency can be lower than the closed-loop crossover frequency. Thus, the compensation design procedures are separated into two cases:

Case 1: Crossover frequency is less than the output-capacitor ESR-zero ($f_C < f_{Z\_ESR}$).

The modulator gain at f_C is:

$$G_{MOD(FC)} = G_{MOD(DC)} \times (f_{P\_LC} / f_C)^2$$

Since the crossover frequency is lower than the output capacitor ESR-zero frequency and higher than the LC double-pole frequency, the error-amplifier gain must have a +1 slope at f_C so that, together with the -2 slope of the LC double pole, the loop crosses over at the desired -1 slope.

The error amplifier has a dominant pole at a very low frequency (~0Hz), and two additional zeros and two additional poles as indicated by the equations below and illustrated in Figure 7:

$$f_{Z1\_EA} = 1 / (2 \pi \times R4 \times C2)$$

$$f_{Z2\_EA} = 1 / (2 \pi \times (R1 + R3) \times C1)$$

$$f_{P2\_EA} = 1 / (2 \pi \times R3 \times C1)$$

$$f_{P3\_EA} = 1 / (2 \pi \times R4 \times (C2 \times C3 / (C2 + C3)))$$

Note that f_{Z2_EA} and f_{P2_EA} are chosen to have the converter closed-loop crossover frequency, f_C, occur when the error-amplifier gain has +1 slope, between f_{Z2_EA} and f_{P2_EA}. The error-amplifier gain at f_C must meet the requirement below:

$$G_{EA(FC)} = 1 / G_{MOD(FC)}$$

The gain of the error amplifier between f_{Z1_EA} and f_{Z2_EA} is:

$$G_{EA(fZ1\_EA - fZ2\_EA)} = G_{EA(FC)} \times f_{Z2\_EA} / f_C = f_{Z2\_EA} / (f_C \times G_{MOD(FC)})$$

This gain is set by the ratio of R4/R1 (Figure 6), where R1 is calculated as illustrated in the *Setting the Output Voltage* section. Thus:

$$R4 = R1 \times f_{Z2\_EA} / (f_C \times G_{MOD(FC)})$$

where $f_{Z2\_EA} = f_{P\_LC}$.

Due to the underdamped (Q > 1) nature of the output LC double pole, the first error-amplifier zero frequency must be set less than the LC double-pole frequency in order to provide adequate phase boost. Set the error-amplifier first zero, f_{Z1_EA}, at 1/4 of the LC double-pole frequency. Hence:

$$C2 = 2 / (\pi \times R4 \times f_{P\_LC})$$

Set the error amplifier f_{P2_EA} at f_{Z_ESR} and

$$f_{p3\_EA} \text{ at } \frac{f_S}{2} \text{ if } f_{Z\_ESR} \text{ is less than } \frac{f_S}{2}.$$

$$\text{If } f_{Z\_ESR} \text{ is greater than } \frac{f_S}{2}, \text{ then set}$$

$$f_{p2\_EA} \text{ at } \frac{f_S}{2} \text{ and } f_{p3\_EA} \text{ at } f_{Z\_ESR}.$$

The error-amplifier gain between f_{P2_EA} and f_{P3_EA} is set by the ratio of R4/RM and is equal to:

$$G_{EA(fZ1\_EA - fZ2\_EA)} \times (f_{P2\_EA} / f_{P\_LC})$$

where RM = R1 x R3 / (R1 + R3). Then:

$$RM = R4 \times f_{P\_LC} / (G_{EA(fZ1\_EA - fZ2\_EA)} \times f_{P2\_EA}) = R4 \times f_C \times G_{MOD(FC)} / f_{P2\_EA}$$

The value of R3 can then be calculated as:

$$R3 = R1 \times RM / (R1 - RM)$$

Now we can calculate the value of C1 as:

$$C1 = 1 / (2 \pi \times R3 \times f_{p2\_EA})$$

and C3 as:

$$C3 = C2 / ((2 \pi \times C2 \times R4 \times f_{P3\_EA}) - 1)$$

Case 2: Crossover frequency is greater than the output-capacitor ESR zero ($f_C > f_{Z\_ESR}$).

The modulator gain at f_C is:

$$G_{MOD(FC)} = G_{MOD(DC)} \times (f_{P\_LC})^2 / (f_{Z\_ESR} \times f_C)$$

Since the output-capacitor ESR-zero frequency is higher than the LC double-pole frequency but lower than the closed-loop crossover frequency, where the modulator already has -1 slope, the error-amplifier gain must have zero slope at f_C so the loop crosses over at the desired -1 slope.

The error-amplifier circuit configuration is the same as case 1 above; however, the closed-loop crossover frequency is now between f_{P2} and f_{P3} as illustrated in Figure 8.

The equations that define the error amplifier's zeros (f_{Z1_EA}, f_{Z2_EA}) and poles (f_{P2_EA}, f_{P3_EA}) are the same as case 1; however, f_{P2_EA} is now lower than the closed-loop crossover frequency. Therefore, the error-amplifier gain between f_{Z1_EA} and f_{Z2_EA} is now calculated as:

$$G_{EA(f_{Z1\_EA} - f_{Z2\_EA})} = G_{EA(FC)} \times f_{Z2\_EA} / f_{P2\_EA} = f_{Z2\_EA} / (f_{P2\_EA} \times G_{MOD(FC)})$$

This gain is set by the ratio of R4/R1, where R1 is calculated as illustrated in the *Setting the Output Voltage* section. Thus:

$$R4 = R1 \times f_{Z2\_EA} / (f_{P2\_EA} \times G_{MOD(FC)})$$

where $f_{Z2\_EA} = f_{P\_LC}$ and $f_{P2\_EA} = f_{Z\_ESR}$.

Similar to case 1, C2 is calculated as:

$$C2 = 2 / (\pi \times R4 \times f_{P\_LC})$$

Set the error-amplifier third pole, f_{P3_EA}, at half the switching frequency, and let RM = (R1 x R3) / (R1 + R3). The gain of the error amplifier between f_{P2_EA} and f_{P3_EA} is set by the ratio of R4/RM and is equal to $G_{EA(FC)} = 1 / G_{MOD(FC)}$. Then:

$$RM = R4 \times G_{MOD(FC)}$$

Similar to case 1, R3, C1, and C3 are calculated as:

$$R3 = R1 \times RM / (R1 - RM)$$

$$C1 = 1 / (2\pi \times R3 \times f_{Z\_ESR})$$

$$C3 = C2 / ((2\pi \times C2 \times R4 \times f_{P3\_EA}) - 1)$$

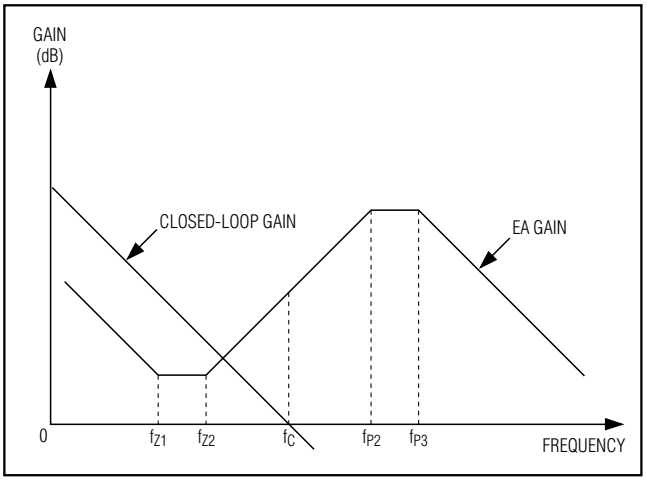


Figure 7. Closed-Loop and Error-Amplifier Gain Plot for Case 1

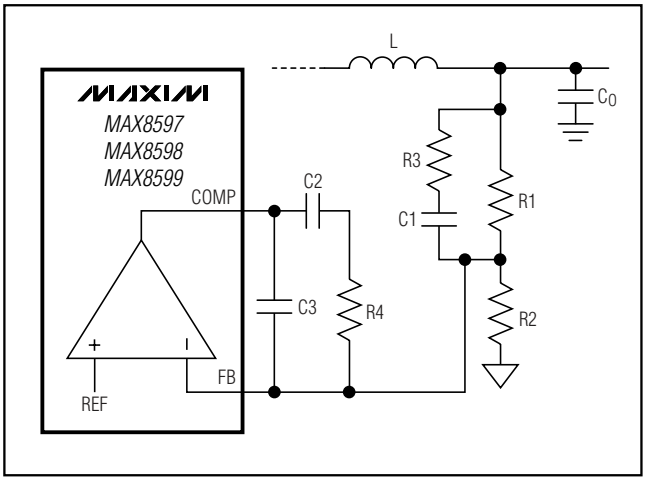


Figure 6. Type III Compensation Network

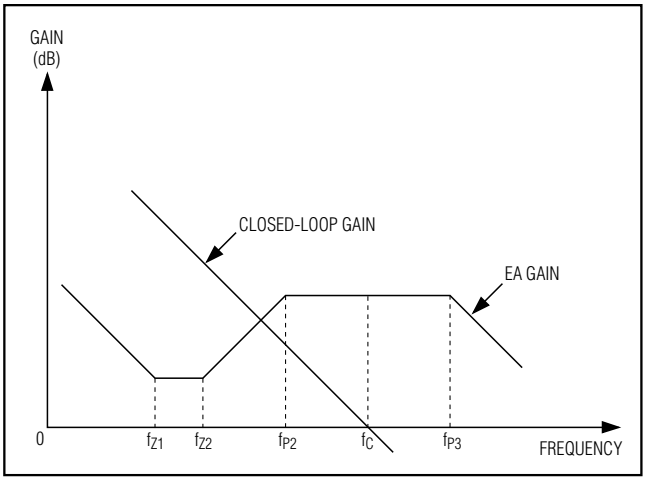


Figure 8. Closed-Loop and Error-Amplifier Gain Plot for Case 2

Low-Dropout, Wide-Input-Voltage, Step-Down Controllers

Applications Information

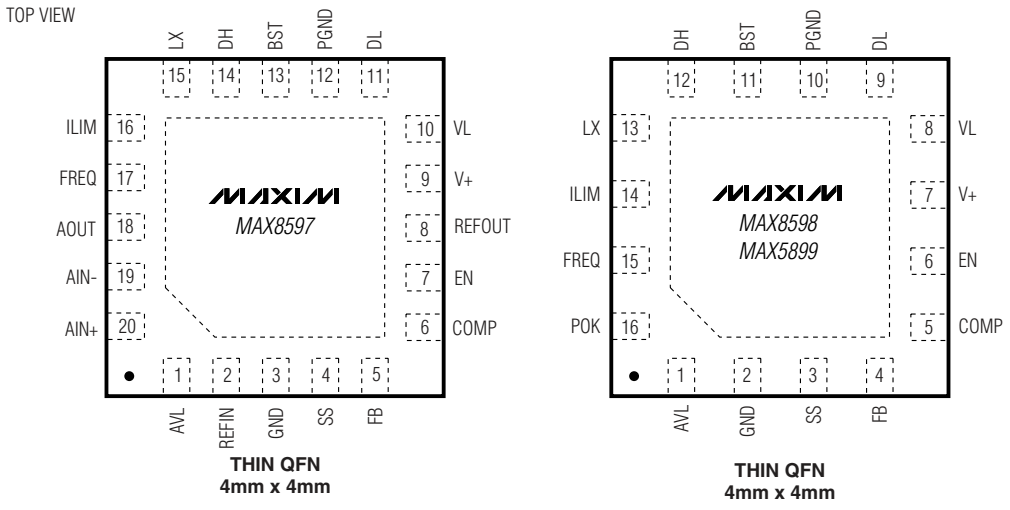
PC Board Layout Guide

Careful PC board layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention. Follow these guidelines for good PC board layout:

1) Place the high-side MOSFET close to the low-side MOSFET and arrange them in such a way that the drain of the high-side MOSFET and the source of the low-side MOSFET can be tightly decoupled with a 10µF or larger ceramic capacitor. The MOSFETs should also be placed close to the controller IC, preferably not more than 1.5in away from the IC.
2) Place the IC's pin decoupling capacitors as close to pins as possible.
3) A current-limit setting resistor must be connected from ILIM directly to the drain of the high-side MOSFET.
4) Try to keep the LX node connection to the IC pin separate from the connection to the flying boost capacitor.
5) Keep the power ground plane (connected to the source of the low-side MOSFET, PGND pin, input and output capacitors' ground, VL decoupling ground) and the signal ground plane (connected to GND pin and the rest of the circuit ground returns) separate. Connect the two ground planes together at the ground of the output capacitor(s).
6) Place the RC snubber circuit as close to the low-side MOSFET as possible.
7) Keep the high-current paths as short as possible.
8) Connect the drains of the MOSFETs to a large copper area to help cool the devices and further improve efficiency and long-term reliability.
9) Ensure the feedback connection is short and direct. Place the feedback resistors as close to the IC as possible.
10) Route high-speed switching nodes, such as LX, DH, and DL away from sensitive analog areas (FB, COMP, ILIM, AIN+, AIN-).

    Refer to the MAX8597/MAX8598/MAX8599 evaluation kit for a sample board layout.

Pin Configurations



Chip Information

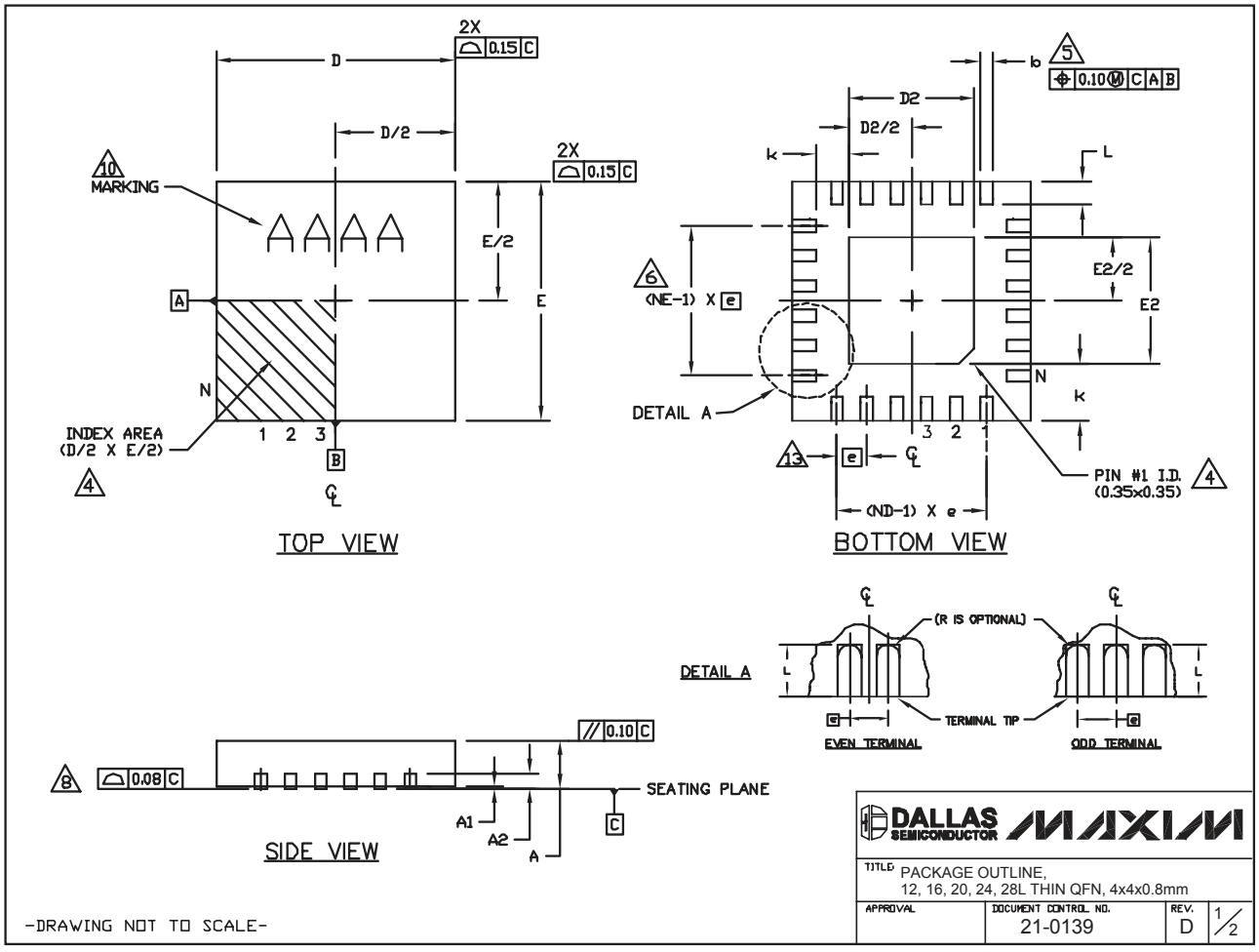
TRANSISTOR COUNT: 4493

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

24L QFN THIN.EPS



Low-Dropout, Wide-Input-Voltage, Step-Down Controllers

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS															
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE		

EXPOSED PAD VARIATIONS							
PKG. CODES	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T1244-2	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-2	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-1	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2444-1	2.45	2.60	2.63	2.45	2.60	2.63	NO
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	YES
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	NO
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-1, T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm
12. WARPAGE SHALL NOT EXCEEND 0.10mm
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 12, 16, 20, 24, 28L THIN QFN, 4x4x0.8mm			
APPROVAL	DOCUMENT CONTROL NO. 21-0139	REV. D	2/2

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