# Low Voltage, 1:10 Differential HSTL Clock Fanout Buffer

# MC100ES8111

**DATASHEET**

The MC100ES8111 is a bipolar monolithic differential clock fanout buffer. Designed for most demanding clock distribution systems, the MC100ES8111 supports various applications that require the distribution of precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver are high performance clock distribution in computing, networking and telecommunication systems.

**LOW-VOLTAGE 1:10 DIFFERENTIAL HSTL CLOCK FANOUT BUFFER**

**FA SUFFIX**
**32-LEAD LQFP PACKAGE**
**CASE 873A-04**

**AC SUFFIX**
**32-LEAD LQFP PACKAGE**
**Pb-FREE PACKAGE**
**CASE 873A-04**

### Features

- 1:10 differential clock fanout buffer
- 80 ps maximum device skew
- SiGe technology
- Supports DC to 625 MHz operation of clock or data signals
- HSTL compatible differential clock outputs
- PECL and HSTL compatible differential clock inputs
- 3.3 V power supply for device core, 1.5 V or 1.8 V HSTL output supply
- Supports industrial temperature range
- Standard 32 lead LQFP package
- 32-lead Pb-free package available

### Functional Description

The MC100ES8111 is designed for low skew clock distribution systems and supports clock frequencies up to 625 MHz. The device accepts two clock sources. The CLK0 input accepts HSTL compatible signals and CLK1 accepts PECL compatible signals. The selected input signal is distributed to 10 identical, differential HSTL compatible outputs.

In order to meet the tight skew specification of the device, both outputs of a differential output pair should be terminated, even if only one output is used. In the case where not all 10 outputs are used, the output pairs on the same package side as the parts being used on that side should be terminated.

The HSTL compatible output levels are generated with an open emitter architecture. This minimizes part-to-part and output-to-output skew. The open-emitter outputs require a 50 Ω DC termination to GND (0 V). The output supply voltage can be either 1.5 V or 1.8 V, the core voltage supply is 3.3 V. The output enable control is synchronized internally preventing output runt pulse generation. Outputs are only disabled or enabled when the outputs are already in logic low state (true outputs logic low, inverted outputs logic high). The internal synchronizer eliminates the setup and hold time requirements for the external clock enable signal. The device is packaged in a 7x7 $mm^2$ 32-lead LQFP package.

**ORDERING INFORMATION**

| Device | Package |
|---|---|
| MC100ES8111FA | LQFP-32 |
| MC100ES8111FAR2 | LQFP-32 |
| MC100ES8111AC | LQFP-32 (Pb-Free) |
| MC100ES8111ACR2 | LQFP-32 (Pb-Free) |

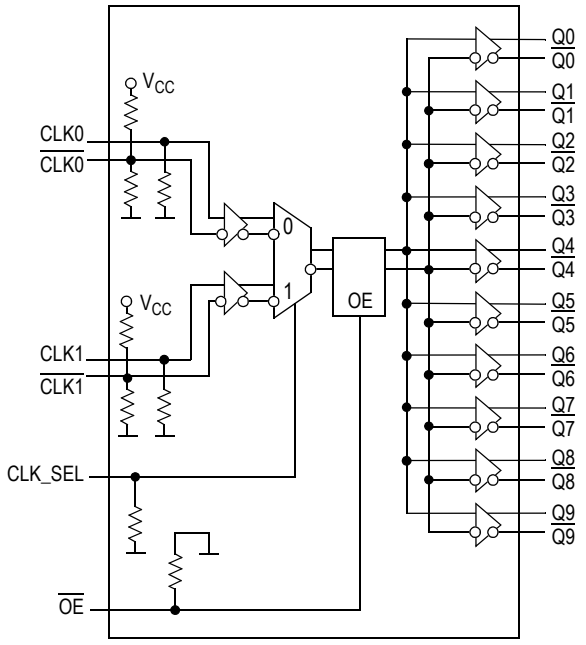



**Figure 1. MC100ES8111 Logic Diagram**

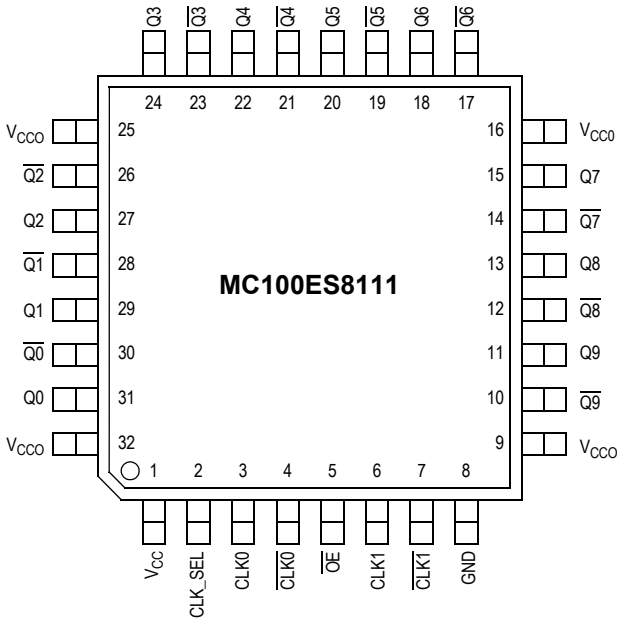



**Figure 2. 23-Lead Package Pinout** (Top View)

**Table 1. Pin Configuration(1)**

| Pin | I/O | Type | Function |
|---|---|---|---|
| CLK0, $\overline{\text{CLK0}}$ | Input | HSTL | Differential HSTL reference clock signal input |
| CLK1, $\overline{\text{CLK1}}$ | Input | PECL | Differential PECL reference clock signal input |
| CLK_SEL | Input | LVCMOS | Reference clock input select |
| OE | Input | LVCMOS | Output enable/disable. OE is synchronous to tlhe input reference clock which eliminates possible output runt pulses when the OE state is changed. |
| Q[0-9], $\overline{\text{Q[0-9]}}$ | Output | HSTL | Differential clock outputs |
| GND | Supply | | Negative power supply |
| $V_{CC}$ | Supply | | Positive power supply of the device core (3.3 V) |
| $V_{CCO}$ | Supply | | Positive power supply of the HSTL outputs. All $V_{CCO}$ pins must be connected to the positive power supply (1.5 V or 1.8 V) for correct DC and AC operation. |

1. Input pull-up/pull-down resistors have a value of 75 kΩ.

**Table 2. Function Table**

| Control | Default | 0 | 1 |
|---|---|---|---|
| CLK_SEL | 0 | CLK0, $\overline{\text{CLK0}}$ (HSTL) is the active differential clock input | CLK1, $\overline{\text{CLK1}}$ (PECL) is the active differential clock input |
| $\overline{\text{OE}}$ | 0 | Q[0-9], $\overline{\text{Q[0-9]}}$ are active. Deassertion of $\overline{\text{OE}}$ can be asynchronous to the reference clock without generation of output runt pulses. | Q[0-9] = L, $\overline{\text{Q[0-9]}}$ =H (outputs disabled). Assertion of $\overline{\text{OE}}$ can be asynchronous to the reference clock without generation of output runt pulses. |

**Table 3. Absolute Maximum Ratings[1]**

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.3 | 3.6 | V | |
| $V_{CCO}$ | Supply Voltage | –0.3 | 3.1 | V | |
| $V_{IN}$ | DC Input Voltage | –0.3 | $V_{CC}$ + 0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | –0.3 | $V_{CC}$ + 0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage Temperature | –65 | 125 | °C | |
| $T_{Func}$ | Functional Temperature Range | $T_A$ = –40 | $T_J$ = +110 | °C | |

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 4. General Specifications**

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output termination voltage | | 0 | | V | |
| MM | ESD Protection (Machine model) | 200 | | | V | |
| HBM | ESD Protection (Human body model) | 2000 | | | V | |
| CDM | ESD Protection (Charged device model) | 2000 | | | V | |
| LU | Latch-up Immunity | 200 | | | mA | |
| $C_{IN}$ | Input Capacitance | | 4.0 | | pF | Inputs |
| $\theta_{JA}$ | Thermal resistance junction to ambient | | | | | |
| | JESD 51-3, single layer test board | | 83.1 | 86.0 | °C/W | Natural convection |
| | | | 73.3 | 75.4 | °C/W | 100 ft/min |
| | | | 68.9 | 70.9 | °C/W | 200 ft/min |
| | | | 63.8 | 65.3 | °C/W | 400 ft/min |
| | | | 57.4 | 59.6 | °C/W | 800 ft/min |
| | JESD 51-6, 2S2P multilayer test board | | 59.0 | 60.6 | °C/W | Natural convection |
| | | | 54.4 | 55.7 | °C/W | 100 ft/min |
| | | | 52.5 | 53.8 | °C/W | 200 ft/min |
| | | | 50.4 | 51.5 | °C/W | 400 ft/min |
| | | | 47.8 | 48.8 | °C/W | 800 ft/min |
| $\theta_{JC}$ | Thermal Resistance Junction to Case | | 23.0 | 26.3 | °C/W | MIL-SPEC 883E Method 1012.1 |
| $T_J$ | Operating Junction Temperature[1] (continuous operation) MTBF = 9.1 years | | | 110 | °C | |

1. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 and the application section in this datasheet for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES8111 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES8111 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

**Table 5. DC Characteristics** ($V_{CC}$ = 3.3 V ± 5%, $V_{CCO}$ = 1.5 V ± 0.1 V or $V_{CCO}$ = 1.8 V ± 0.1 V), $T_J$ = 0°C to +110°C

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Clock Input Pair CLK0, $\overline{CLK0}$ (HSTL differential signals) | | | | | | |
| $V_{DIF}$ | Differential Input Voltage(1) | 0.2 | | | V | |
| $V_{X, IN}$ | Differential Cross Point Voltage(2) | 0.25 | 0.68 - 0.9 | $V_{CC}$-1.3 | V | |
| $V_{IH}$ | Input High Voltage | $V_X$+0.1 | | | V | |
| $V_{IL}$ | Input Low Voltage | | | $V_X$-0.1 | V | |
| $I_{IN}$ | Input Current | | | ±150 | µA | $V_{IN} = V_X \pm 0.1$ V |
| Clock Input Pair CLK1, $\overline{CLK1}$ (PECL differential signals) | | | | | | |
| $V_{PP}$ | Differential Input Voltage(3) | 0.15 | | 1.0 | V | Differential operation |
| $V_{CMR}$ | Differential Cross Point Voltage(4) | 1.0 | | $V_{CC}$-0.6 | V | Differential operation |
| $V_{IH}$ | Input Voltage High | $V_{CC}$-1.165 | | $V_{CC}$-0.880 | V | |
| $V_{IL}$ | Input Voltage Low | $V_{CC}$-1.810 | | $V_{CC}$-1.475 | V | |
| $I_{IN}$ | Input Current | | | ±150 | µA | $V_{IN} = V_{IH}$ or $V_{IN}$ |
| LVCMOS Control Inputs $\overline{OE}$, CLK_SEL | | | | | | |
| $V_{IL}$ | Input Voltage Low | | | 0.8 | V | |
| $V_{IH}$ | Input Voltage High | 2.0 | | | V | |
| $I_{IN}$ | Input Current | | | ±150 | µA | $V_{IN} = V_{IH}$ or $V_{IN}$ |
| HSTL Clock Outputs (Q[0-9], $\overline{Q[0-9]}$) | | | | | | |
| $V_{X, OUT}$ | Output Differential Crosspoint | 0.68 | 0.75 | 0.9 | V | |
| $V_{OH}$ | Output High Voltage | 1.0 | | | V | |
| $V_{OL}$ | Output Low Voltage | | | 0.4 | V | |
| Supply Current | | | | | | |
| $I_{CC}$ | Maximum Supply Current without output termination current | | 80 | 105 | mA | $V_{CC}$ pin (core) |
| $I_{CCO}$(5) | Maximum Supply Current, outputs terminated 50 Ω to $V_{TT}$ | | 350 | 410 | mA | $V_{CCO}$ pins (outputs) |

1. $V_{DIF}$ (DC) is the minimum differential HSTL input voltage swing required for device functionality.
2. $V_X$ (DC) is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the $V_X$ (DC) range and the input swing lies within the $V_{PP}$ (DC) specification.
3. $V_{PP}$ (DC) is the minimum differential input voltage swing required to maintain device functionality.
4. $V_{CMR}$ (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the $V_{CMR}$ (DC) range and the input swing lies within the $V_{PP}$ (DC) specification.
5. $I_{CC}$ includes current through the output resistors (all outputs terminated to $V_{TT}$). See also “Power Consumption and Junction Temperature” on page 6.

**Table 6. AC Characteristics** ($V_{CC}$ = 3.3 V ± 5%, $V_{CCO}$ = 1.5 V ± 0.1 V or $V_{CCO}$ = 1.8 V ± 0.1 V), $T_J$ = 0°C to +110°C[1]

| Symbol | Characteristics | | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| REF_SEL= 0, Active Clock Input Pair CLK0, $\overline{CLK0}$ (HSTL differential signals) | | | | | | | |
| $V_{DIF}$ | Differential Input Voltage[2] (Peak-to-Peak) | | 0.4 | | | V | |
| $V_{X, IN}$ | Differential Cross Point Voltage[3] | | 0.68 | | 0.9 | V | |
| $f_{CLK}$ | Input Frequency | | 0 | | 625 | MHz | |
| $t_{PD}$ | Propagation Delay CLK0 to Qn | $V_{CCO}$ = 1.8 V<br>$V_{CCO}$ = 1.5 V | 700<br>700 | 990<br>1030 | 1270<br>1420 | ps<br>ps | Differential |
| $t_{SK(PP)}$ | Output-to-Output Skew (Part-to-Part) | $V_{CCO}$ = 1.8 V<br>$V_{CCO}$ = 1.5 V | | | 570<br>720 | ps<br>ps | Differential |
| $t_{SK(P)}$ | Output Pulse Skew[4] | $V_{CCO}$ = 1.8 V<br>$V_{CCO}$ = 1.5 V | | | 100<br>150 | ps<br>ps | |
| REF_SEL = 1, Active Clock Input Pair CLK1, $\overline{CLK1}$ (PECL differential signals) | | | | | | | |
| $V_{PP}$ | Differential Input Voltage[5] (Peak-to-Peak) | | 0.2 | | 1.0 | V | |
| $V_{CMR}$ | Differential Input Crosspoint Voltage[6] | | 1.0 | | $V_{CC}$-0.6 | V | |
| $f_{CLK}$ | Input Frequency | | 0 | | 625 | MHz | Differential |
| $t_{PD}$ | Propagation Delay CLK1 to Qn | $V_{CCO}$ = 1.8 V<br>$V_{CCO}$ = 1.5 V | 590<br>590 | 860<br>910 | 1220<br>1360 | ps<br>ps | Differential |
| $t_{SK(PP)}$ | Output-to-Output Skew (Part-to-Part) | $V_{CCO}$ = 1.8 V<br>$V_{CCO}$ = 1.5 V | | | 630<br>770 | ps<br>ps | Differential |
| $t_{SK(P)}$ | Output Pulse Skew[7] | $V_{CCO}$ = 1.8 V<br>$V_{CCO}$ = 1.5 V | | | 150<br>200 | ps<br>ps | |
| HSTL Clock Outputs (Qn, $\overline{Qn}$) | | | | | | | |
| $V_{X, OUT}$ | Output Differential Crosspoint | | 0.68 | 0.91 | 1.1 | V | |
| $V_{OH}$ | Output High Voltage | $V_{CCO}$ = 1.8 V<br>$V_{CCO}$ = 1.5 V | $V_{CCO}$-0.8 V<br>$V_{CCO}$-0.5 V | | 1.5<br>1.5 | V<br>V | |
| $V_{OL}$ | Output Low Voltage | | 0.2 | | 0.8 | V | |
| $V_{O(P-P)}$ | Differential Output Voltage (Peak-to-Peak) | $V_{CCO}$ = 1.8 V<br>$V_{CCO}$ = 1.5 V | 0.45<br>0.40 | | 1.0<br>1.0 | V<br>V | |
| $t_{SK(O)}$ | Output-to-Output Skew | $V_{CCO}$ = 1.8 V<br>$V_{CCO}$ = 1.5 V | | 37<br>60 | 80<br>105 | ps<br>ps | Differential |
| $t_{JIT(CC)}$ | Output Cycle-to-Cycle Jitter RMS (1 σ) | | | | 1.0 | ps | |
| $t_r$, $t_f$ | Output Rise/Fall Time | | 150 | | 800 | ps | 20% to 80% |
| $t_{PDL}$[8] | Output Disable Time | | 2.5·T + $t_{PD}$ | | 3.5·T + $t_{PD}$ | ns | T=CLKn period |
| $t_{PLE}$[9] | Output Enable Time | | 3.0·T + $t_{PD}$ | | 4.0·T + $t_{PD}$ | ns | T=CLKn period |

1. AC characteristics apply for parallel output termination of 50 Ω to $V_{TT}$ (GND).
2. $V_{DIF}$ (DC) is the minimum differential HSTL input voltage swing required for device functionality.
3. $V_X$ (DC) is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the $V_X$ (DC) range and the input swing lies within the $V_{DIF}$ (DC) specification.
4. Output duty cycle is DC = (0.5 ± 150 ps · $f_{OUT}$) · 100%. E.g. the DC range at $f_{OUT}$ = 100 MHz is 48.5% < DC < 51.5%.
5. $V_{PP}$ (AC) is the minimum differential PECL input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
6. $V_{CMR}$ (AC) is the crosspoint of the differential HSTL input signal. Normal AC operation is obtained when the crosspoint is within the $V_{CMR}$ (AC) range and the input swing lies within the $V_{PP}$ (AC) specification. Violation of $V_{CMR}$ (AC) or $V_{PP}$ (AC) impacts the device propagation delay, device and part-to-part skew.
7. Output pulse skew is the absolute difference of the propagation delay times: | $t_{PLH}$ - $t_{PHL}$ |. The output duty cycle is DC = (0.5 ± 200 ps · $f_{OUT}$) · 100%. E.g. the DC range at $f_{OUT}$ = 100 MHz and $V_{CCO}$ = 1.5 V is 48.0% < DC < 52.0%.
8. Propagation delay $\overline{OE}$ deassertion to differential output disabled (differential low: true output low, complementary output high).
9. Propagation delay $\overline{OE}$ assertion to output enabled (active).

## APPLICATIONS INFORMATION

### Test Reference and Output Termination

The MC100ES8111 is designed for high-frequency and low-skew clock distribution. The high-speed differential outputs are capable of driving 50 Ω transmission lines and always require a DC termination to $V_{TT}$ (GND). In order to maintain the tight skew and timing specifications, it is recommend to terminate the differential outputs by 50 Ω to GND, with the termination resistor located as close as possible to the end of the clock transmission line. All DC and AC specifications apply to this termination method (see the reference circuit shown in Figure 3 “MC100ES8111 AC Test Reference”). The MC100ES8111 does not support an output termination to $V_{TT} = V_X$ = 0.75 V (center voltage termination).

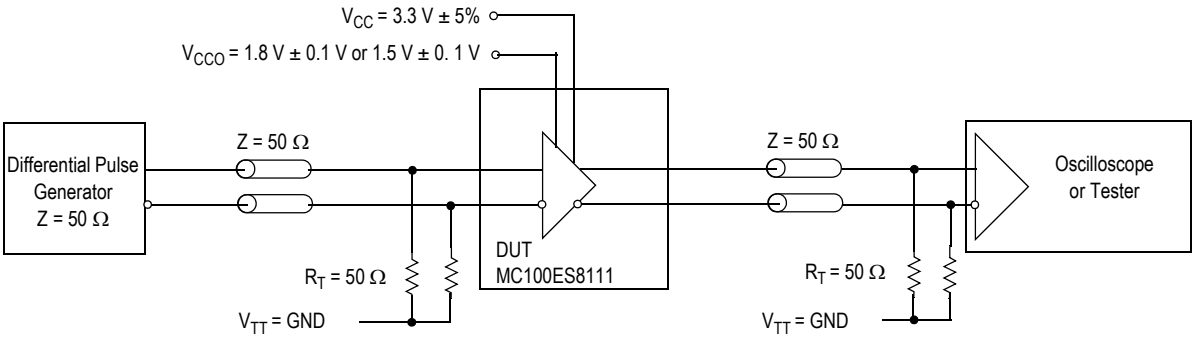



**Figure 3. MC100ES8111 AC Test Reference**

### Power Consumption and the Junction Temperature

The power consumption $P_{TOT}$ of the MC100ES8111 depends on the supply voltages and the DC output termination. The clock frequency has a negligible effect on $P_{TOT}$. If all outputs are terminated by 50 Ω to GND, the device power consumption is calculated by:

$$P_{TOT} = V_{CC} \cdot I_{CC} + I_{CCO} \cdot (V_{CCO} - V_X)$$

For instance, at a supply voltage of $V_{CC}$ = 3.3 V and a termination of 50 Ω to GND, the typical device power consumption is 579 mW at $V_{CCO}$ = 1.8 V and 474 mW at $V_{CCO}$ = 1.5 V.

**Table 7. Power Consumption**

| MC100ES8111 | $P_{TOT, TYP}$(1) | $P_{TOT, MAX}$(2) |
|---|---|---|
| $V_{CCO}$ = 1.5 V | 470 mW | 647 mW |
| $V_{CCO}$ = 1.8 V | 575 mW | 769 mW |

1. Typical case: $V_{CC}$, $V_{CCO}$ at nominal values and using typical $I_{CC}$, $I_{CCO}$ data.
2. Worst case: $V_{CC}$, $V_{CC}$ at max. values and using max. $I_{CC}$, $I_{CCO}$ limits.

To make the optimum use of high clock frequency and low skew capabilities of the MC100ES8111, the device is specified, characterized and tested for the junction temperature range of $T_J$ = 0°C to +110°C. Because the exact thermal performance depends on the PCB type, design, thermal management and natural or forced air convection, the junction temperature provides an exact way to correlate the application specific conditions to the published performance data of this datasheet. The correlation of the junction temperature range to the application ambient temperature range and vice versa can be done by calculation:

$$T_J = T_A + R_{thja} \cdot P_{tot}$$

Assuming a thermal resistance (junction to ambient) of 54.4°C/W (2s2p board, 100 ft/min airflow, see Table 8) and a typical power consumption of 575 mW (all outputs terminated 50 ohms to GND, $V_{CCO}$ = 1.8 V), the junction temperature of the MC100ES8111 is approximately $T_A$ + 31°C, and the minimum ambient temperature in this example case calculates to -31°C (the maximum ambient temperature is 79°C. See Table 8). Exceeding the minimum junction temperature specification of the MC100ES8111 does not have a significant impact on the device functionality. However, the continuous use the MC100ES8111 at high ambient temperatures requires thermal management to not exceed the specified maximum junction temperature.

**Table 8. Ambient Temperature Ranges** ($P_{tot}$ = 575 mW)

| $R_{thja}$ (2s2p board) | | $T_{A, min}$(1) | $T_{A, max}$ |
|---|---|---|---|
| Natural convection | 59.0°C/W | -34°C | 76°C |
| 100 ft/min | 54.4°C/W | -31°C | 79°C |
| 200 ft/min | 52.5°C/W | -30°C | 80°C |
| 400 ft/min | 50.4°C/W | -29°C | 81°C |
| 800 ft/min | 47.8°C/W | -27.5°C | 82.5°C |

1. The MC100ES8111 device function is guaranteed from $T_A$ = -40°C to $T_J$ = 110°C.

### Maintaining Lowest Device Skew

The MC100ES8111 guarantees low output-to-output skew of max. 80 ps and a part-to-part skew of max. 630 ps ($V_{CCO}$ = 1.8 V). To ensure low skew clock signals in the application, both outputs of any differential output pair need to be terminated identically, even if only one output is used. When fewer than all ten output pairs are used, identical termination of all output pairs within the output bank (same package side) is recommended. If an entire output bank is not used, it is recommended to leave all of these outputs open and unterminated. This will reduce the device power consumption while maintaining minimum output skew.

### Power Supply Bypassing

The MC100ES8111 is a mixed analog/digital product. The differential architecture of the MC100ES8111 supports low noise signal operation at high frequencies. In order to maintain its superior signal quality, all $V_{CC}$ pins should be bypassed by high-frequency ceramic capacitors connected to GND. If the spectral frequencies of the internally generated switching noise on the supply pins cross the

series resonant point of an individual bypass capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the noise bandwidth.

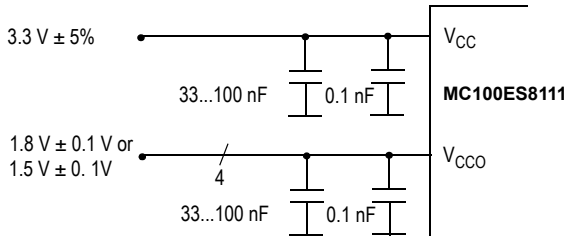



**Figure 4. $V_{CC}$, $V_{CCO}$ Power Supply Bypass**

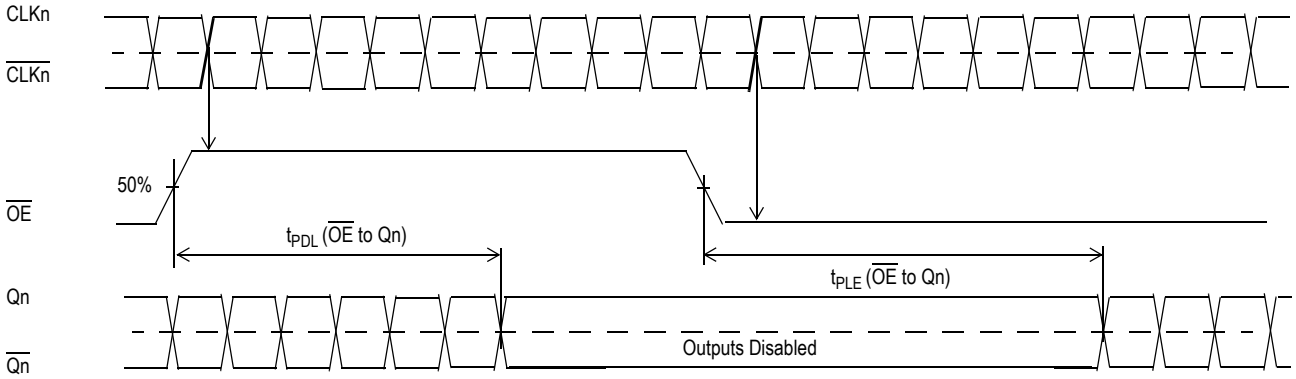



**Figure 5. MC100ES8111 Output Disable/Enable Timing**

**Output Enable/Disable Control**

The MC100ES8111 enables and disables outputs synchronously to the input clock signal. The user may enable and disable the outputs by using the $\overline{OE}$ control regardless of any hold and setup time constraints. Output runt pulses are prevented in any case. Outputs are disabled in logic low state (Qn=Low, $\overline{Qn}$=High) without a change of the output impedance.

## AC MEASUREMENT REFERENCES

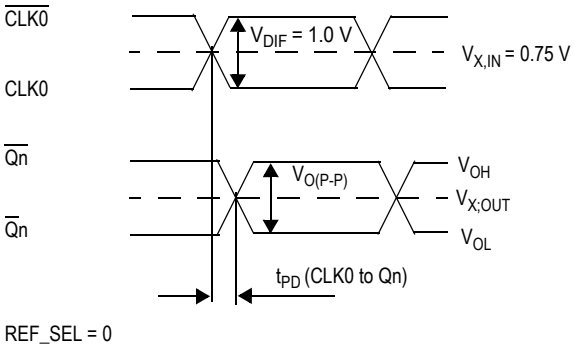



**Figure 6. MC100ES8111 AC Reference Measurement Waveform (HSTL Input)**

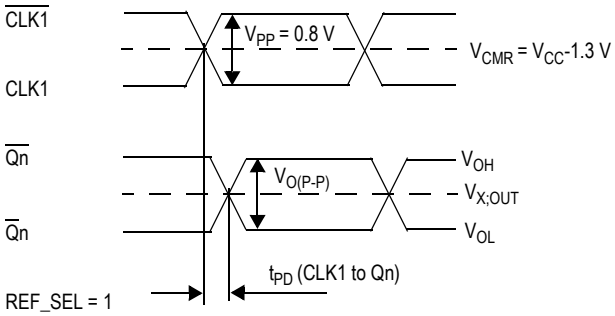



**Figure 7. MC100ES8111 AC Reference Measurement Waveform (PECL Input)**

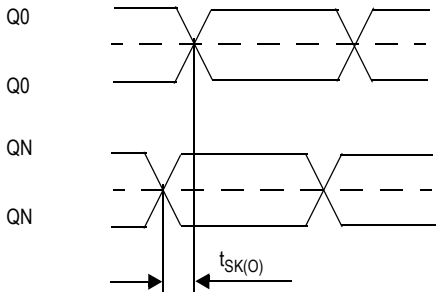



**Figure 8. Output-to-Output Skew**

The output-to-output skew is defined as the worst case difference in propagation delay between any two similar delay paths within a single device.

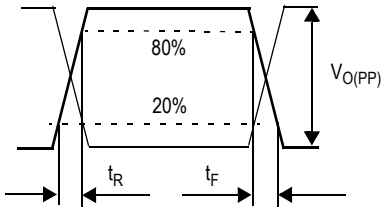
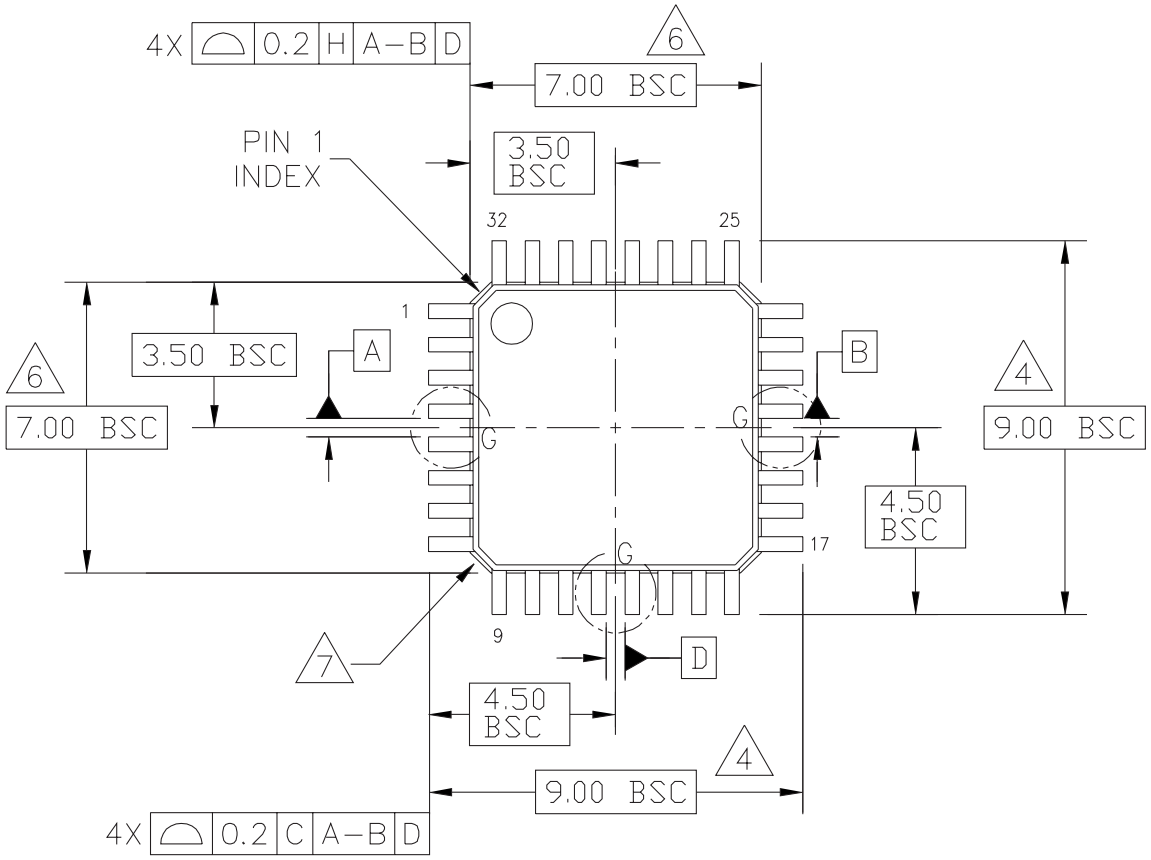
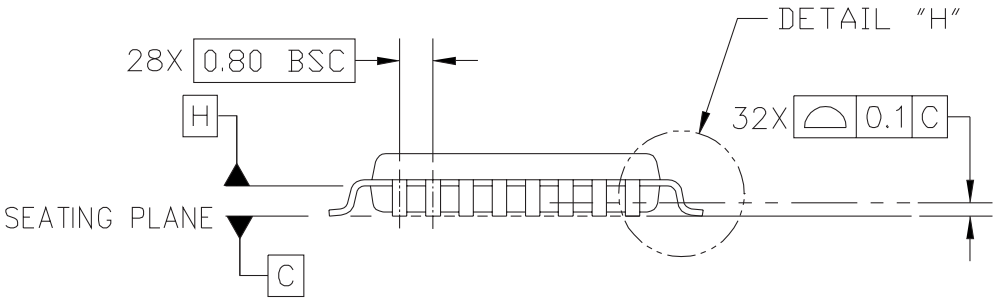



**Figure 9. HSTL Output Rise/Fall Time**

## PACKAGE DIMENSIONS

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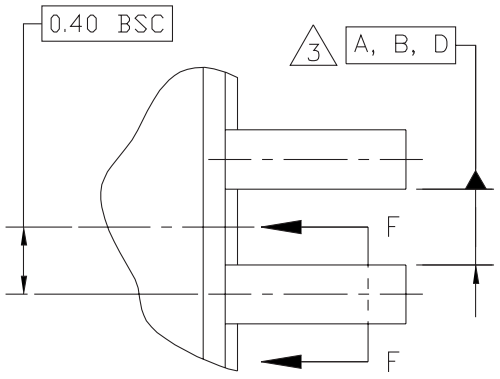
|---|---|---|
| TITLE: LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4) | DOCUMENT NO: 98ASH70029A | REV: C |
| | CASE NUMBER: 873A-04 | 01 APR 2005 |
| | STANDARD: JEDEC MS-026 BBA | |

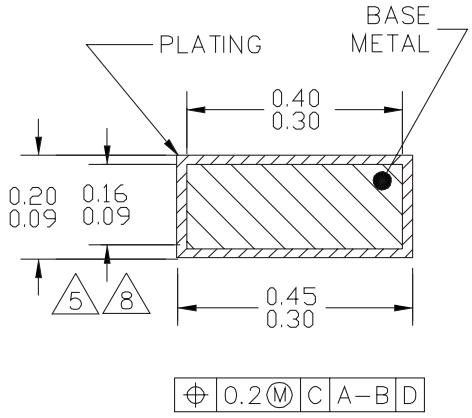


**CASE 873A-04**
**ISSUE C**
**32-LEAD LQFP PACKAGE**

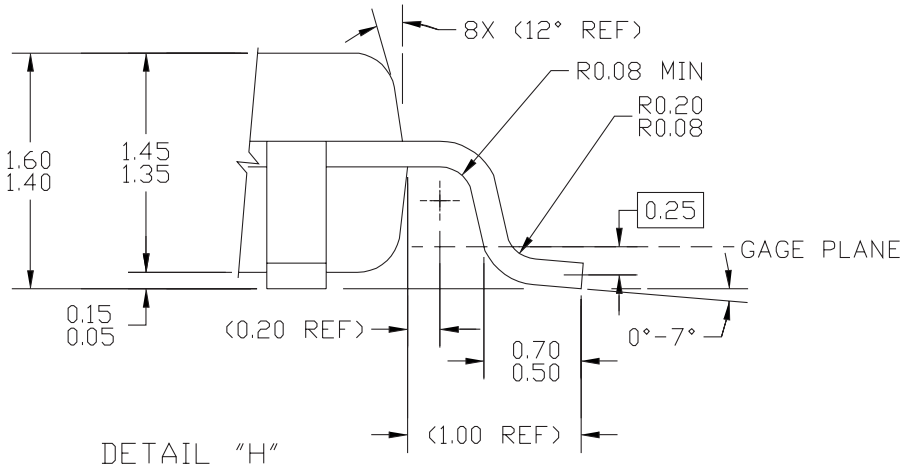
## PACKAGE DIMENSIONS




DETAIL G




SECTION F–F
ROTATED 90°CW
32 PLACES




DETAIL "H"

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|---|---|---|
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## PACKAGE DIMENSIONS

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5–1994.

3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.

4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE DATUM C.

5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07 MM.

6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.

| | | |
|---|---|---|
|  | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE |
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