DRV8701 Brushed DC Motor Full-Bridge Gate Driver

1 Features

- Single H-Bridge Gate Driver
  - Drives Four External N-Channel MOSFETs
  - Supports 100% PWM Duty Cycle
- 5.9-V to 45-V Operating Supply Voltage Range
- Two Control Interface Options
  - PH/**EN** (DRV8701**E**)
  - **PWM** (DRV8701**P**)
- Adjustable Gate Drive (5 Levels)
  - 6-mA to 150-mA Source Current
  - 12.5-mA to 300-mA Sink Current
- Supports 1.8-V, 3.3-V, and 5-V Logic Inputs
- Current Shunt Amplifier (20 V/V)
- Integrated PWM Current Regulation
  - Limits Motor Inrush Current
- Low-Power Sleep Mode (9 µA)
- Two LDO Voltage Regulators to Power External Components
  - AVDD: 4.8 V, up to 30-mA Output Load
  - DVDD: 3.3 V, up to 30-mA Output Load
- Small Package and Footprint
  - 24-Pin VQFN (PowerPAD™)
  - 4.0 × 4.0 × 0.9 mm
- Protection Features:
  - VM Undervoltage Lockout (UVLO)
  - Charge Pump Undervoltage (CPUV)
  - Overcurrent Protection (OCP)
  - Pre-Driver Fault (PDF)
  - Thermal Shutdown (TSD)
  - Fault Condition Output (nFAULT)

2 Applications

- Industrial Brushed-DC Motors
- Robotics
- Home Automation
- Industrial Pumps and Valves
- Power Tools
- Handheld Vacuum Cleaners

3 Description

The DRV8701 is a single H-bridge gate driver that uses four external N-channel MOSFETs targeted to drive a 12-V to 24-V bidirectional brushed DC motor.

A PH/EN (DRV8701E) or PWM (DRV8701P) interface allows simple interfacing to controller circuits. An internal sense amplifier allows for adjustable current control. The gate driver includes circuitry to regulate the winding current using fixed off-time PWM current chopping.

DRV8701 drives both high- and low-side FETs with 9.5-V V_{GS} gate drive. The gate drive current for all external FETs is configurable with a single external resistor on the IDRIVE pin.

A low-power sleep mode is provided which shuts down internal circuitry to achieve very-low quiescent current draw. This sleep mode can be set by taking the nSLEEP pin low.

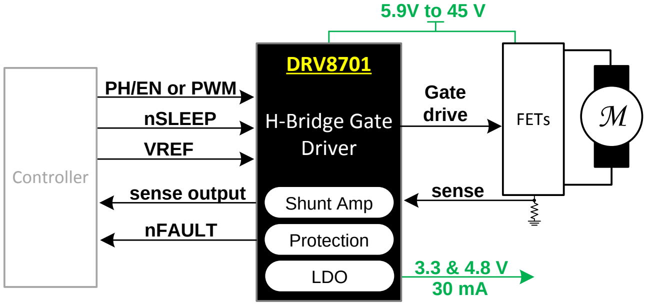
Internal protection functions are provided: undervoltage lockout, charge pump faults, overcurrent shutdown, short-circuit protection, predriver faults, and overtemperature. Fault conditions are indicated on the nFAULT pin.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8701	VQFN (24)	4.00 × 4.00 x 0.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified System Block Diagram



Gate-Drive Current

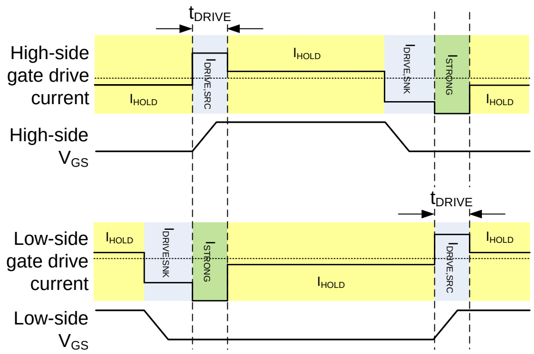


Table of Contents

---

4 Revision History

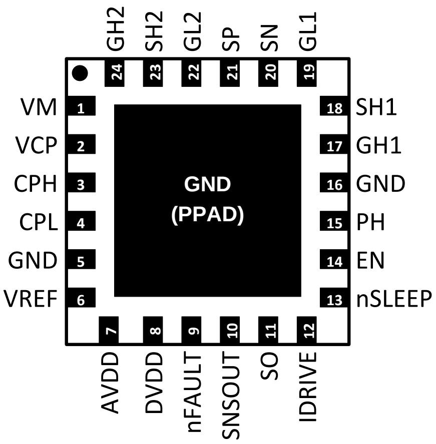
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2015) to Revision B	Page
• Updated test conditions for $I_{DRIVE,SNK}$ and corrected TYP values	8

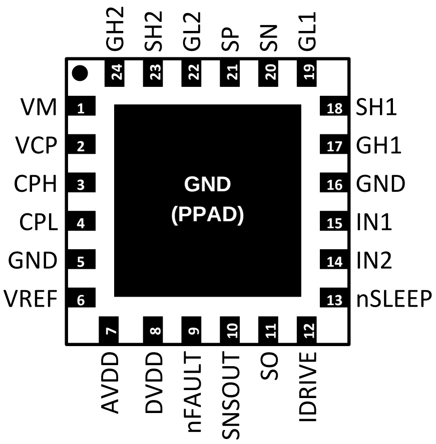
Changes from Original (March 2015) to Revision A	Page
• Updated device status to production data	1

5 Pin Configuration and Functions

RGE Package
24-Pin VQFN
DRV8701E Top View



RGE Package
24-Pin VQFN
DRV8701P Top View



DRV8701E (PH/EN)

PIN		TYPE	DESCRIPTION	
NAME	NO.			
EN	14	Input	Bridge enable input	Logic low places the bridge in brake mode; see Table 1
PH	15	Input	Bridge phase input	Controls the direction of the H-bridge; see Table 1

DRV8701P (PWM)

PIN		TYPE	DESCRIPTION	
NAME	NO.			
IN1	15	Input	Bridge PWM input	Logic controls the state of H-bridge; see Table 2
IN2	14	Input		

Common Pins

PIN		TYPE	DESCRIPTION	
NAME	NO.			
VM	1	Power	Power supply	Connect to motor supply voltage; bypass to GND with a 0.1-µF ceramic plus a 10-µF minimum capacitor rated for VM; additional capacitance may be required based on drive current
GND	5	Power	Device ground	Must be connected to ground
	16			
	PPAD			
VCP	2	Power	Charge pump output	Connect a 16-V, 1-µF ceramic capacitor to VM
CPH	3	Power	Charge pump switching nodes	Connect a 0.1-µF X7R capacitor rated for VM between CPH and CPL
CPL	4			
DVDD	8	Power	Logic regulator	3.3-V logic supply regulator; bypass to GND with a 6.3-V, 1-µF ceramic capacitor
AVDD	7	Power	Analog regulator	4.8-V analog supply regulator; bypass to GND with a 6.3-V, 1-µF ceramic capacitor
nSLEEP	13	Input	Device sleep mode	Pull logic low to put device into a low-power sleep mode with FETs High-Z; internal pulldown
IDRIVE	12	Input	Gate drive current setting pin	Resistor value or voltage forced on this pin sets the gate drive current; see applications section for more details

Common Pins (continued)

PIN		TYPE	DESCRIPTION	
NAME	NO.			
VREF	6	Input	Analog reference input	Controls the current regulation; apply a voltage between 0.3 V and AVDD
nFAULT	9	Open Drain	Fault indication pin	Pulled logic low with fault condition; open-drain output requires an external pullup
SNSOUT	10	Open Drain	Sense comparator output	Pulled logic low when the drive current hits the current chopping threshold; open-drain output requires an external pullup
SO	11	Output	Shunt amplifier output	Voltage on this pin is equal to the SP voltage times A_V plus an offset; place no more than 1 nF of capacitance on this pin
SN	20	Input	Shunt amplifier negative input	Connect to SP through current sense resistor and to GND
SP	21	Input	Shunt amplifier positive input	Connect to low-side FET source and to SN through current sense resistor
GH1	17	Output	High-side gate	Connect to high-side FET gate
GH2	24			
GL1	19	Output	Low-side gate	Connect to low-side FET gate
GL2	22			
SH1	18	Input	Phase node	Connect to high-side FET source and low-side FET drain
SH2	23			

External Passive Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	GND	0.1-µF ceramic capacitor rated for VM
C_{VM2}	VM	GND	≥10-µF capacitor rated for VM
C_{VCP}	VCP	VM	16-V, 1-µF ceramic capacitor
C_{SW}	CPH	CPL	0.1-µF X7R capacitor rated for VM
C_{DVDD}	DVDD	GND	6.3-V, 1-µF ceramic capacitor
C_{AVDD}	AVDD	GND	6.3-V, 1-µF ceramic capacitor
R_{IDRIVE}	IDRIVE	GND	See *Typical Applications* for resistor sizing
R_{nFAULT}	VCC (1)	nFAULT	≥10-kΩ pullup
R_{SNSOUT}	VCC (1)	SNSOUT	≥10-kΩ pullup
R_{SENSE}	SP	SN/GND	Optional low-side sense resistor

(1) VCC is not a pin on the DRV8701, but a VCC supply voltage pullup is required for open-drain outputs nFAULT and SNSOUT. The system controller supply can be used for this pullup voltage, or these pins can be pulled up to either AVDD or DVDD.

External FETs

Component	Gate	Drain	Source	Recommended
Q_{HS1}	GH1	VM	SH1	Supports up to 200-nC FETs at 40-kHz PWM; see *Detailed Design Procedure* for more details
Q_{LS1}	GL1	SH1	SP or GND	
Q_{HS2}	GH2	VM	SH2	
Q_{LS2}	GL2	SH2	SP or GND	

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range referenced with respect to GND (unless otherwise noted) (1)

	MIN	MAX	UNIT
Power supply voltage (VM)	–0.3	47	V
Power supply voltage ramp rate (VM)	0	2	V/µs
Charge pump voltage (VCP, CPH)	–0.3	VM + 12	V
Charge pump negative switching pin (CPL)	–0.3	VM	V
Internal logic regulator voltage (DVDD)	–0.3	3.8	V
Internal analog regulator voltage (AVDD)	–0.3	5.75	V
Control pin voltage (PH, EN, IN1, IN2, nSLEEP, nFAULT, VREF, IDRIVE, SNSOUT)	–0.3	5.75	V
High-side gate pin voltage (GH1, GH2)	–0.3	VM + 12	V
Continuous phase node pin voltage (SH1, SH2)	–1.2	VM + 1.2	V
Pulsed 10 µs phase node pin voltage (SH1, SH2)	–2.0	VM + 2	V
Low-side gate pin voltage (GL1, GL2)	–0.3	12	V
Continuous shunt amplifier input pin voltage (SP, SN)	–0.5	1	V
Pulsed 10-µs shunt amplifier input pin voltage (SP, SN)	–1	1	V
Shunt amplifier output pin voltage (SO)	–0.3	5.75	V
Open-drain output current (nFAULT, SNSOUT)	0	10	mA
Gate pin source current (GH1, GL1, GH2, GL2)	0	250	mA
Gate pin sink current (GH1, GL1, GH2, GL2)	0	500	mA
Shunt amplifier output pin current (SO)	0	5	mA
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM) ESD stress voltage (1)	±2000	V
		Charged device model (CDM) ESD stress voltage (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VM	Power supply voltage range	5.9	45	V
VCC	Logic level input voltage	0	5.5	V
VREF	Reference RMS voltage range (VREF)	0.3 (1)	AVDD	V
f_{PWM}	Applied PWM signal (PH/EN or IN1/IN2)		100	kHz
I_{AVDD}	AVDD external load current		30 (2)	mA
I_{DVDD}	DVDD external load current		30 (2)	mA
I_{SO}	Shunt amplifier output current loading (SO)		5	mA
T_A	Operating ambient temperature	–40	125	°C

(1) Operational at VREF = 0 to 0.3 V, but accuracy is degraded
(2) Power dissipation and thermal limits must be observed

6.4 Thermal Information

THERMAL METRIC[1]		**DRV8701** **RGE (VQFN)** **24 PINS**	**UNIT**
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	12.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, AVDD, DVDD)							
VM	VM operating voltage			5.9		45	V
I_{VM}	VM operating supply current	VM = 24 V; nSLEEP high			6	9.5	mA
I_{VMQ}	VM sleep mode supply current	nSLEEP = 0 VM = 24 V	T_A = 25°C		9	15	µA
			T_A = 125°C (1)		14	25	
t_{SLEEP}	Sleep time	nSLEEP low to sleep mode				100	µs
t_{WAKE}	Wake-up time	nSLEEP high to output change				1	ms
t_{ON}	Turn-on time	VM > UVLO to output transition				1	ms
DVDD	Internal logic regulator voltage	External load 0 to 30 mA		3.0	3.3	3.5	V
AVDD	Internal logic regulator voltage	External load 0 to 30 mA		4.4	4.8	5.2	V
CHARGE PUMP (VCP, CPH, CPL)							
VCP	VCP operating voltage	VM = 12 V; I_{VCP} = 0 to 12 mA		20.5	21.5	22.5	V
		VM = 8 V; I_{VCP} = 0 to 10 mA		13.5	14.4	15	
		VM = 5.9 V; I_{VCP} = 0 to 8 mA		9.4	9.9	10.4	
I_{VCP}	Charge pump current capacity	VM > 12 V		12			mA
		8 V < VM < 12 V		10			
		5.9 V < VM < 8 V		8			
f_{VCP} (1)	Charge pump switching frequency	VM > UVLO		200	400	700	kHz
CONTROL INPUTS (PH, EN, IN1, IN2, nSLEEP)							
V_{IL}	Input logic low voltage					0.8	V
V_{IH}	Input logic high voltage			1.5			V
V_{HYS}	Input logic hysteresis			100			mV
I_{IL}	Input logic low current	V_{IN} = 0 V		–5		5	µA
I_{IH}	Input logic high current	V_{IN} = 5 V				78	µA
R_{PD}	Pulldown resistance			64	115	173	kΩ
t_{PD}	Propagation delay	PH/EN, IN1/IN2 to GHx/GLx			500		ns
CONTROL OUTPUTS (nFAULT, SNSOUT)							
V_{OL}	Output logic low voltage	I_O = 2 mA				0.1	V
I_{OZ}	Output high impedance leakage	V_{IN} = 5 V		–2		2	µA
FET GATE DRIVERS (GH1, GH2, SH1, SH2, GL1, GL2)							
V_{GHS}	High-side VGS gate drive (gate-to-source)	VM > 12 V; V_{GHS} with respect to SHx		8.5	9.5	10.5	V
		VM = 8 V; V_{GHS} with respect to SHx		5.5	6.4	7	
		VM = 5.9 V; V_{GHS} with respect to SHx		3.5	4.0	4.5	
V_{GLS}	Low-side VGS gate drive (gate-to-source)	VM > 12 V		8.5	9.3	10.5	V
		VM = 5.9 V		3.9	4.3	4.9	
t_{DEAD}	Output dead time	Observed t_{DEAD} depends on IDRIVE setting			380		ns
t_{DRIVE}	Gate drive time				2.5		µs
$I_{DRIVE,SRC}$	Peak source current	R_{IDRIVE} < 1 kΩ to GND			6		mA
		R_{IDRIVE} = 33 kΩ ±5% to GND			12.5		
		R_{IDRIVE} = 200 kΩ ±5% to GND, **or** R_{IDRIVE} < 1 kΩ to AVDD			25		
		R_{IDRIVE} > 500 kΩ ±5% to GND			100		
		R_{IDRIVE} = 68 kΩ ±5% to AVDD			150		

(1) Specified by design and characterization data

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{DRIVE,SNK}$	Peak sink current	$R_{IDRIVE} < 1$ kΩ to GND		12.5		mA
		$R_{IDRIVE} = 33$ kΩ ±5% to GND		25		
		$R_{IDRIVE} = 200$ kΩ ±5% to GND, or $R_{IDRIVE} < 1$ kΩ to AVDD		50		
		$R_{IDRIVE} > 500$ ±5% kΩ to GND		200		
		$R_{IDRIVE} = 68$ kΩ ±5% to AVDD		300		
I_{HOLD}	FET holding current	Source current after t_{DRIVE}		6		mA
		Sink current after t_{DRIVE}		25		
I_{STRONG}	FET hold-off strong pulldown	GHx		490		mA
		GLx		690		
R_{OFF}	FET gate hold-off resistor	Pulldown GHx to SHx		200		kΩ
		Pulldown GLx to GND		150		
CURRENT SHUNT AMPLIFIER AND PWM CURRENT CONTROL (SP, SN, SO, VREF)						
V_{VREF}	VREF input voltage	For current internal chopping	0.3[2]		AVDD	V
A_V	Amplifier gain	$50 < V_{SP} < 200$ mV; V_{SN} = GND	18	20	22	V/V
		$10 < V_{SP} < 50$ mV; V_{SN} = GND	16	20	24	
V_{OFF}	SO offset	$V_{SP} = V_{SN}$ = GND		50	250	mV
I_{SP}	SP input current	$V_{SP} = 100$ mV; V_{SN} = GND		-40		µA
t_{SET} [3]	Settling time to ±1%	$V_{SP} = V_{SN}$ = GND to $V_{SP} = 100$ mV, V_{SN} = GND			1.5	µs
C_{SO} [3]	Allowable SO pin capacitance				1	nF
t_{OFF}	PWM current regulation off-time			25		µs
t_{BLANK}	PWM blanking time			2		µs
PROTECTION CIRCUITS						
V_{UVLO}	VM undervoltage lockout	VM falling; UVLO report		5.4	5.8	V
		VM rising; UVLO recovery		5.6	5.9	
$V_{UVLO,HYS}$	VM undervoltage hysteresis	Rising to falling threshold	100			mV
t_{UVLO}	VM UVLO falling deglitch time	VM falling; UVLO report		10		µs
V_{CPUV}	Charge pump undervoltage	CPUV report		VM + 2.8		V
$V_{DS\ OCP}$	Overcurrent protection trip level, VDS of each external FET	High-side FETs: VM – SHx Low-side FETs: SHx – SP	0.8	1		V
$V_{SP\ OCP}$	Overcurrent protection trip level, measured by sense amplifier	V_{SP} voltage with respect to GND	0.8	1		V
t_{OCP}	Overcurrent deglitch time			4.5		µs
t_{RETRY}	Overcurrent retry time			3		ms
T_{TSD} [3]	Thermal shutdown temperature	Die temperature, T_J	150			°C
T_{HYS} [3]	Thermal shutdown hysteresis	Die temperature, T_J		20		°C
$V_{GS\ CLAMP}$	Gate drive clamping voltage	Positive clamping voltage	10.5		13	V
		Negative clamping voltage	–1	–0.7	–0.5	

[2] Operational at VREF = 0 to 0.3 V, but accuracy is degraded
[3] Specified by design and characterization data

6.6 Typical Characteristics

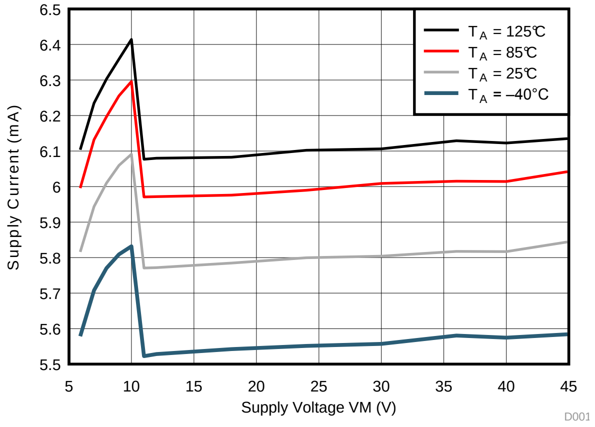


Figure 1. Supply Current over VM

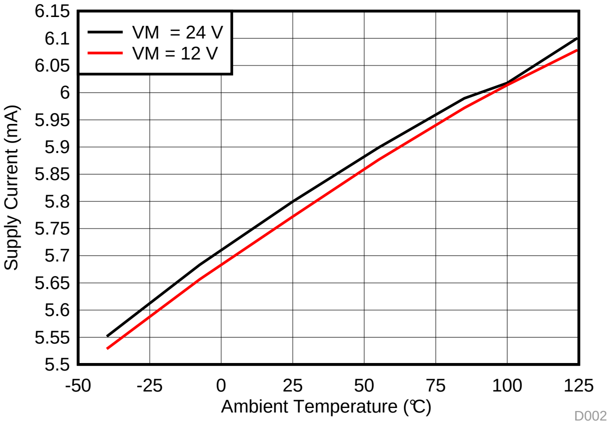


Figure 2. Supply Current over Temperature

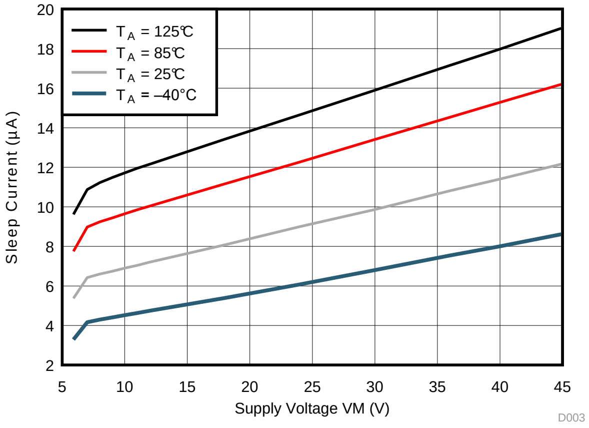


Figure 3. Sleep Current over VM

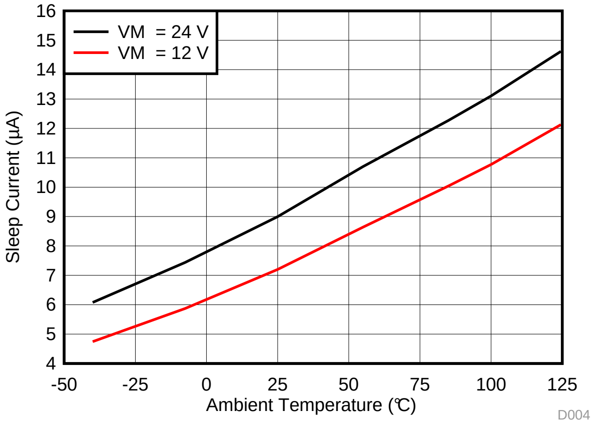


Figure 4. Sleep Current over Temperature

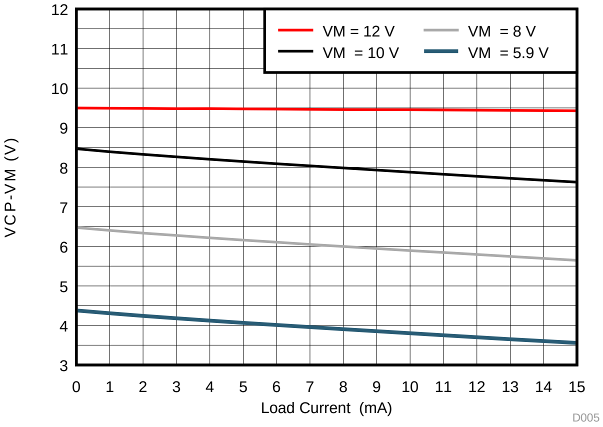


Figure 5. VCP over Load (T_A = 25°C)

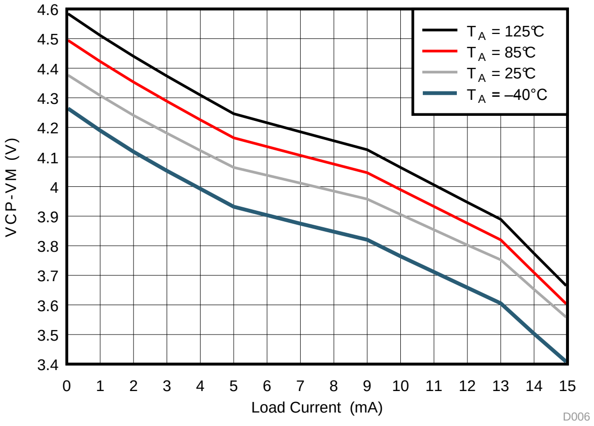


Figure 6. VCP over Load (VM = 5.9 V)

Typical Characteristics (continued)

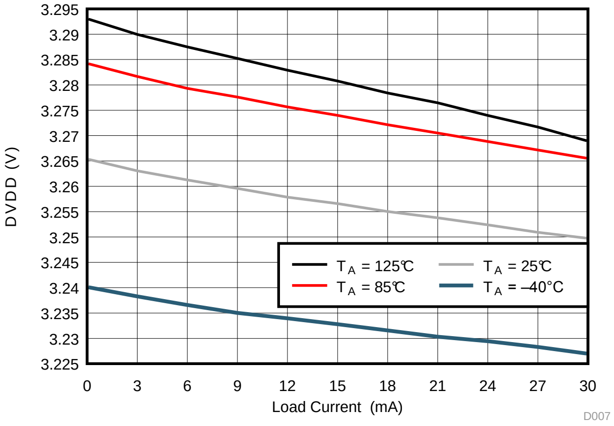


Figure 7. DVDD Regulator over Load (VM = 12 V)

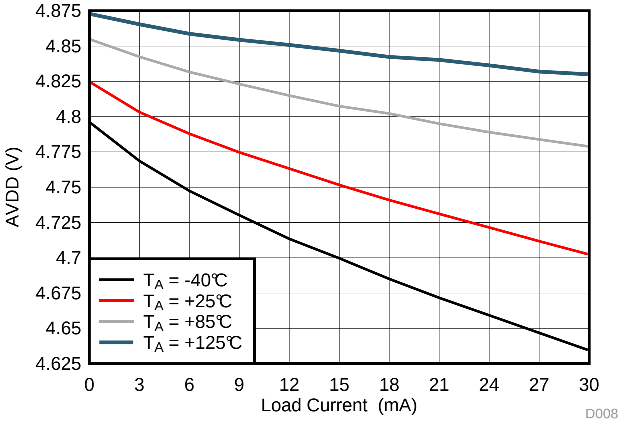


Figure 8. AVDD Regulator over Load (VM = 12 V)

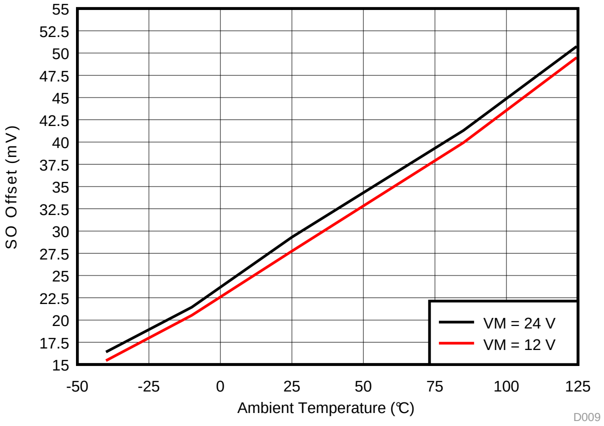


Figure 9. SO Offset over Temperature

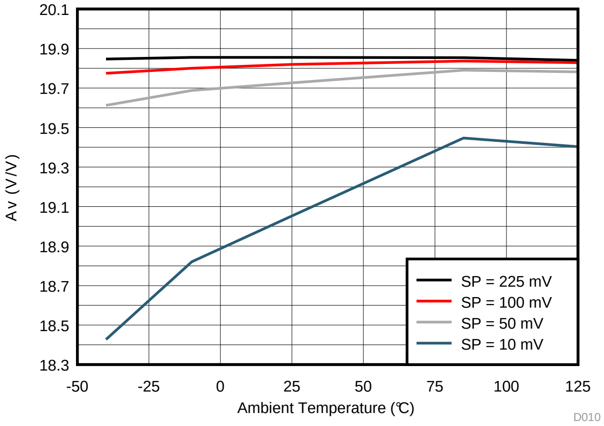


Figure 10. Amplifier Gain over Temperature

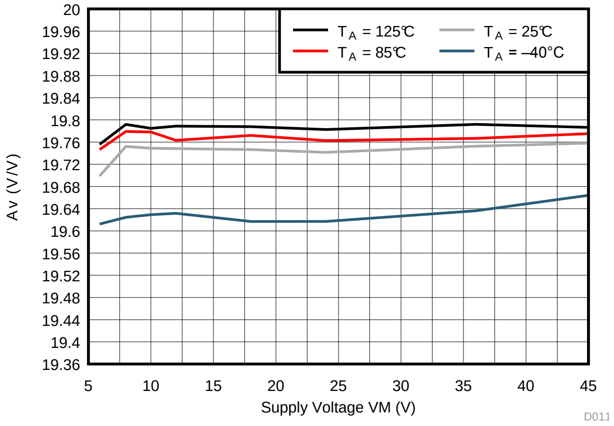


Figure 11. Amplifier Gain over VM (SP = 50 mV)

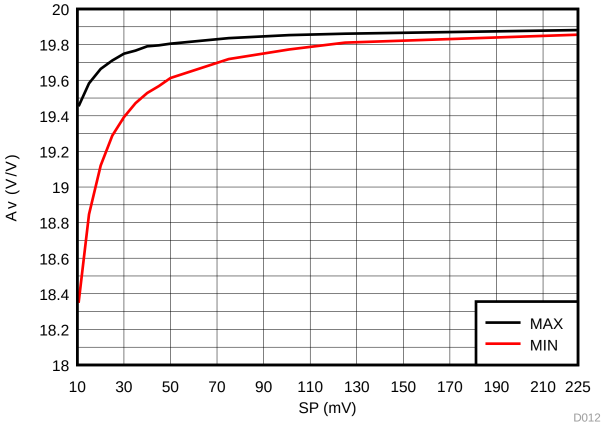


Figure 12. Amplifier Gain over VM and Temperature Range

Typical Characteristics (continued)

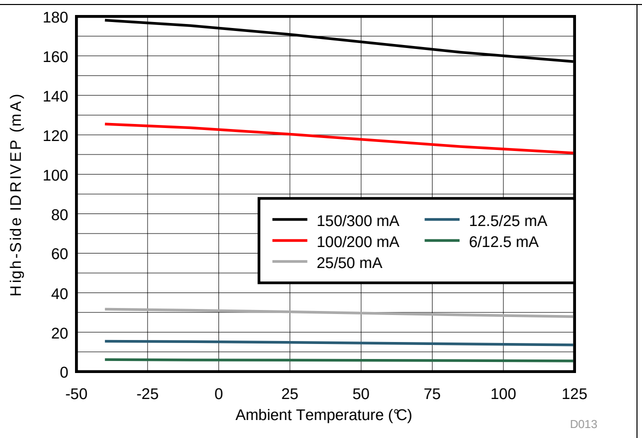


Figure 13. High-Side IDRIVEP over Temperature (VM = 12 V)

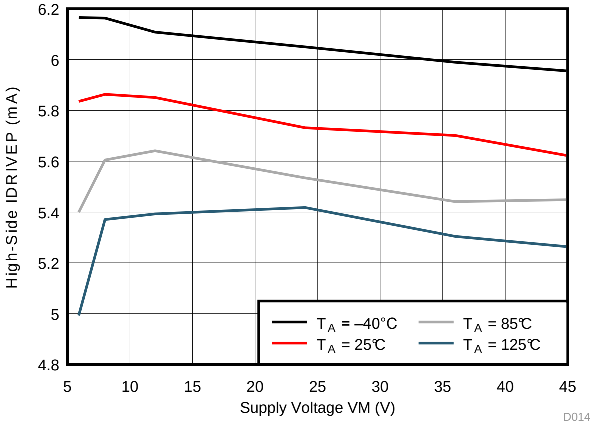


Figure 14. 6-/12.5-mA High-Side IDRIVEP over VM

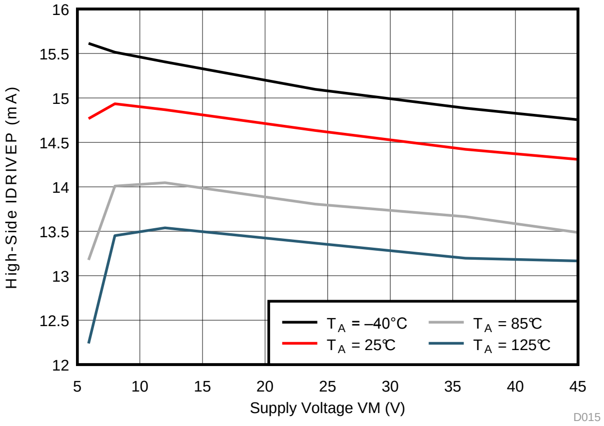


Figure 15. 12.5-/25-mA High-Side IDRIVEP over VM

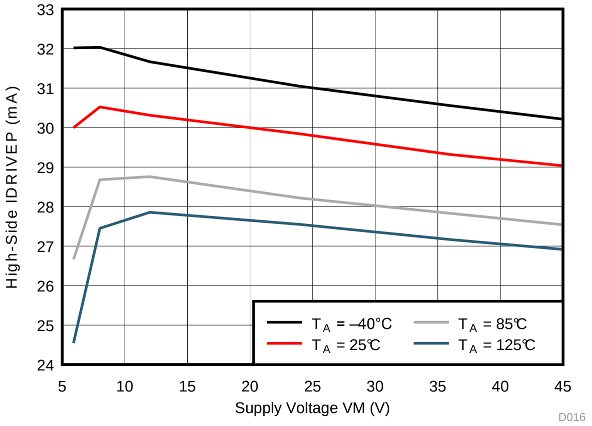


Figure 16. 25-/50-mA High-Side IDRIVEP over VM

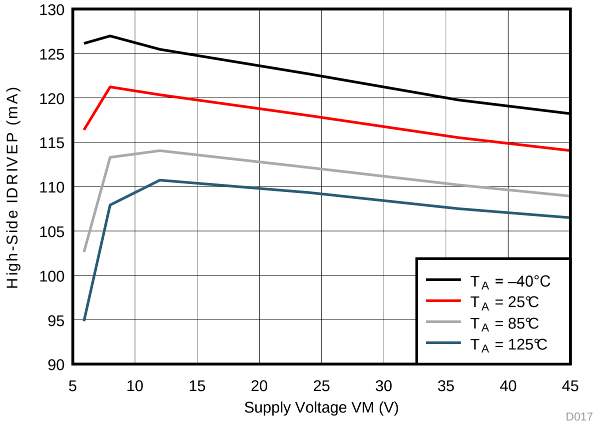


Figure 17. 100-/200-mA High-Side IDRIVEP over VM

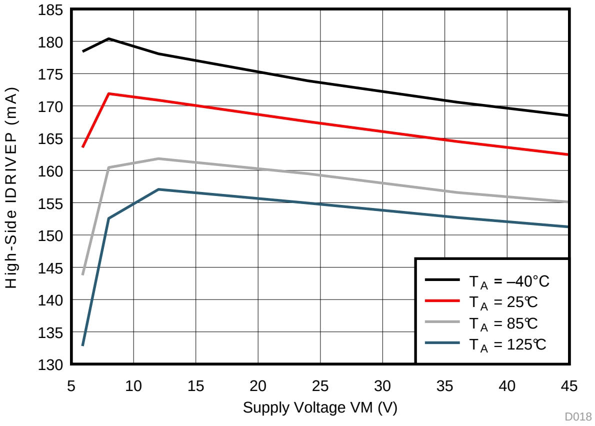


Figure 18. 150-/300-mA High-Side IDRIVEP over VM

7 Detailed Description

7.1 Overview

The DRV8701 is an H-bridge gate driver (also called a pre-driver or controller). The device integrates FET gate drivers in order to control four external NMOS FETs. The device can be powered with a supply voltage between 5.9 and 45 V.

A simple PH/EN (DRV8701E) or PWM (DRV8701P) interface allows interfacing to the controller circuit.

A low-power sleep mode is included, which can be enabled using the nSLEEP pin.

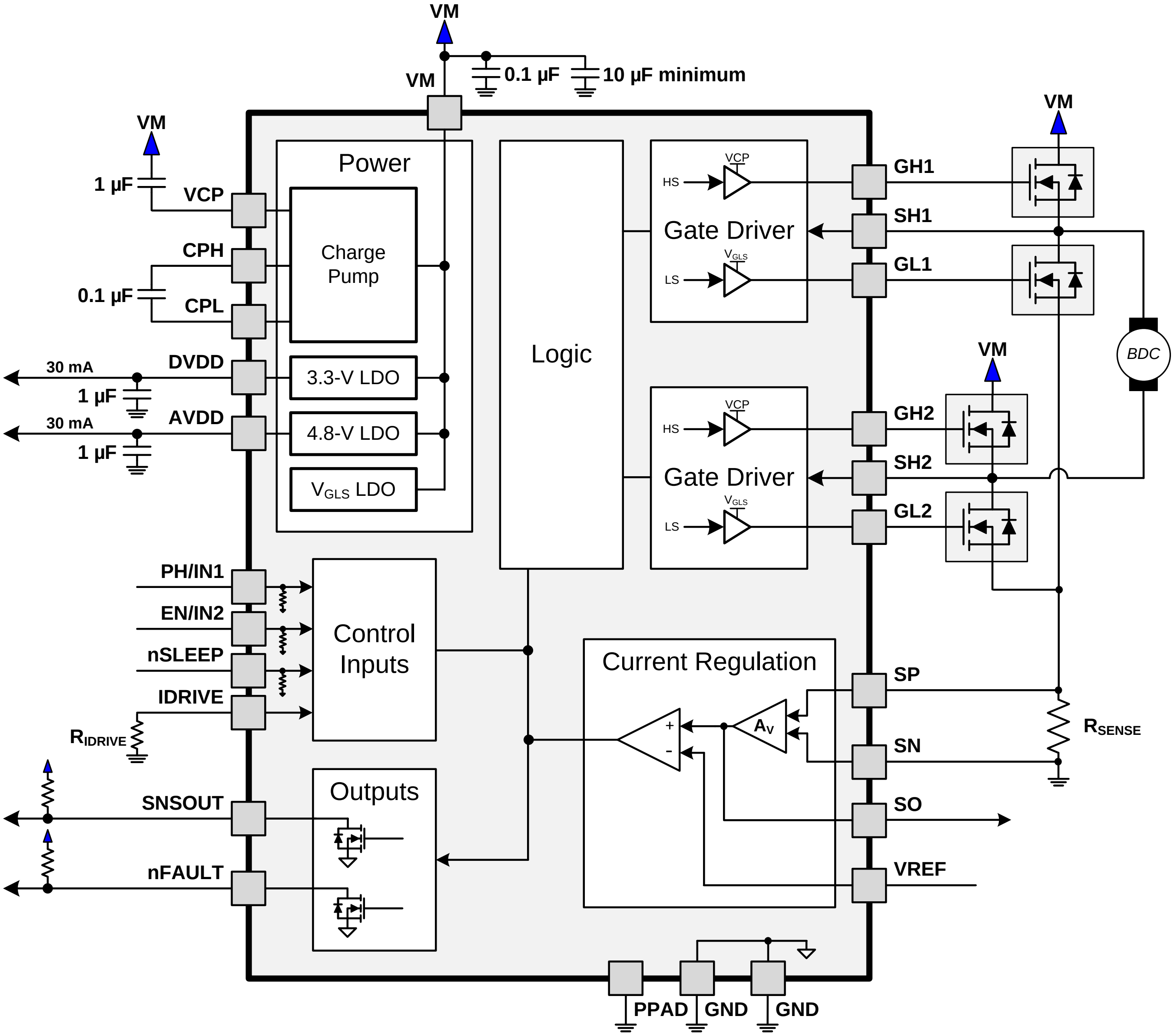
The gate drive strength can be adjusted to optimize a system for a given FET without adding external resistors in series with the FET gates. The IDRIVE pin allows for selection of the peak current driven into the external FET gate. Both the high-side and low-side FETs are driven with a V_{GS} of 9.5 V nominally when VM > 12 V. At lower VM voltages, the V_{GS} is reduced. The high-side gate drive voltage is generated using a doubler-architecture charge pump that regulates to VM + 9.5 V.

This device greatly reduces the component count of discrete motor driver systems by integrating the necessary FET drive circuitry into a single device. In addition, the DRV8701 adds protection features above traditional discrete implementations: UVLO, OCP, pre-driver faults, and thermal shutdown.

A start-up (inrush) or running current limitation is built in using a fixed time-off current chopping scheme. The chopping current level is set by choosing the sense resistor value and by setting a voltage on the VREF pin.

A shunt amplifier output is provided for accurate current measurements by the system controller. The SO pin outputs a voltage that is 20 times the voltage seen across the sense resistor.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Bridge Control

The DRV8701E is controlled using a PH/EN interface. The following logic table (Table 1) gives the full H-bridge state when driving a single brushed DC motor. Note that Table 1 does not take into account the current control built into the DRV8701E. Positive current is defined in the direction of xOUT1 → xOUT2.

Table 1. DRV8701E (PH/EN) Control Interface

nSLEEP	EN	PH	SH1	SH2	AVDD/DVDD	Description
0	X	X	High-Z	High-Z	Disabled	Sleep mode; H-bridge disabled High-Z
1	0	X	L	L	Enabled	Brake, low-side slow decay
1	1	0	L	H	Enabled	Reverse drive (current SH2 → SH1)
1	1	1	H	L	Enabled	Forward drive (current SH1 → SH2)

The DRV8701P is controlled using a PWM interface (IN1/IN2). The following logic table (Table 2) gives the full H-bridge state when driving a single brushed DC motor. Note that Table 2 does not take into account the current control built into the DRV8701P. Positive current is defined in the direction of xOUT1 → xOUT2.

Table 2. DRV8701P (PWM) Control Interface

nSLEEP	IN1	IN2	SH1	SH2	AVDD/DVDD	Description
0	X	X	High-Z	High-Z	Disabled	Sleep mode; H-bridge disabled High-Z
1	0	0	High-Z	High-Z	Enabled	Coast; H-bridge disabled High-Z
1	0	1	L	H	Enabled	Reverse (current SH2 → SH1)
1	1	0	H	L	Enabled	Forward (current SH1 → SH2)
1	1	1	L	L	Enabled	Brake; low-side slow decay

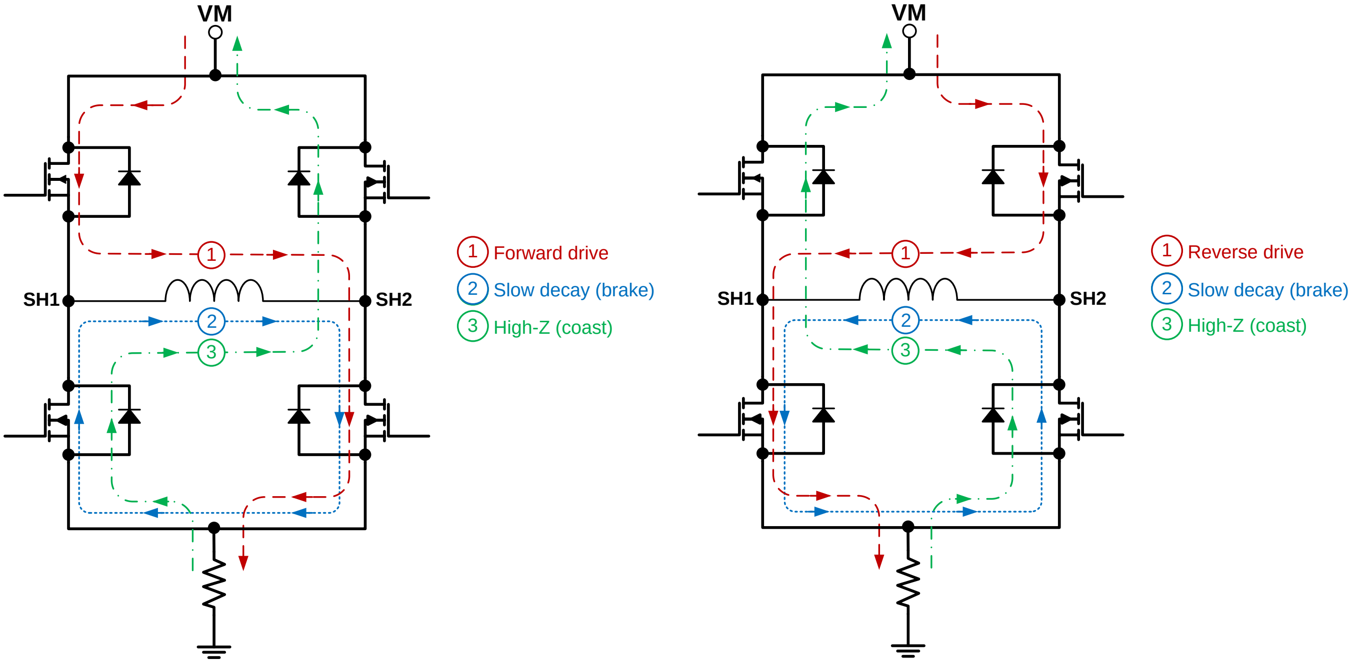


Figure 19. H-Bridge Operational States

7.3.2 Half-Bridge Operation

The DRV8701 can be used to drive only a single half-bridge instead of a full H-bridge. To operate in this mode, leave GH1 and GL1 disconnected. Also, connect a 1/10 W, 330-Ω 5% resistor from SH1 to GND.

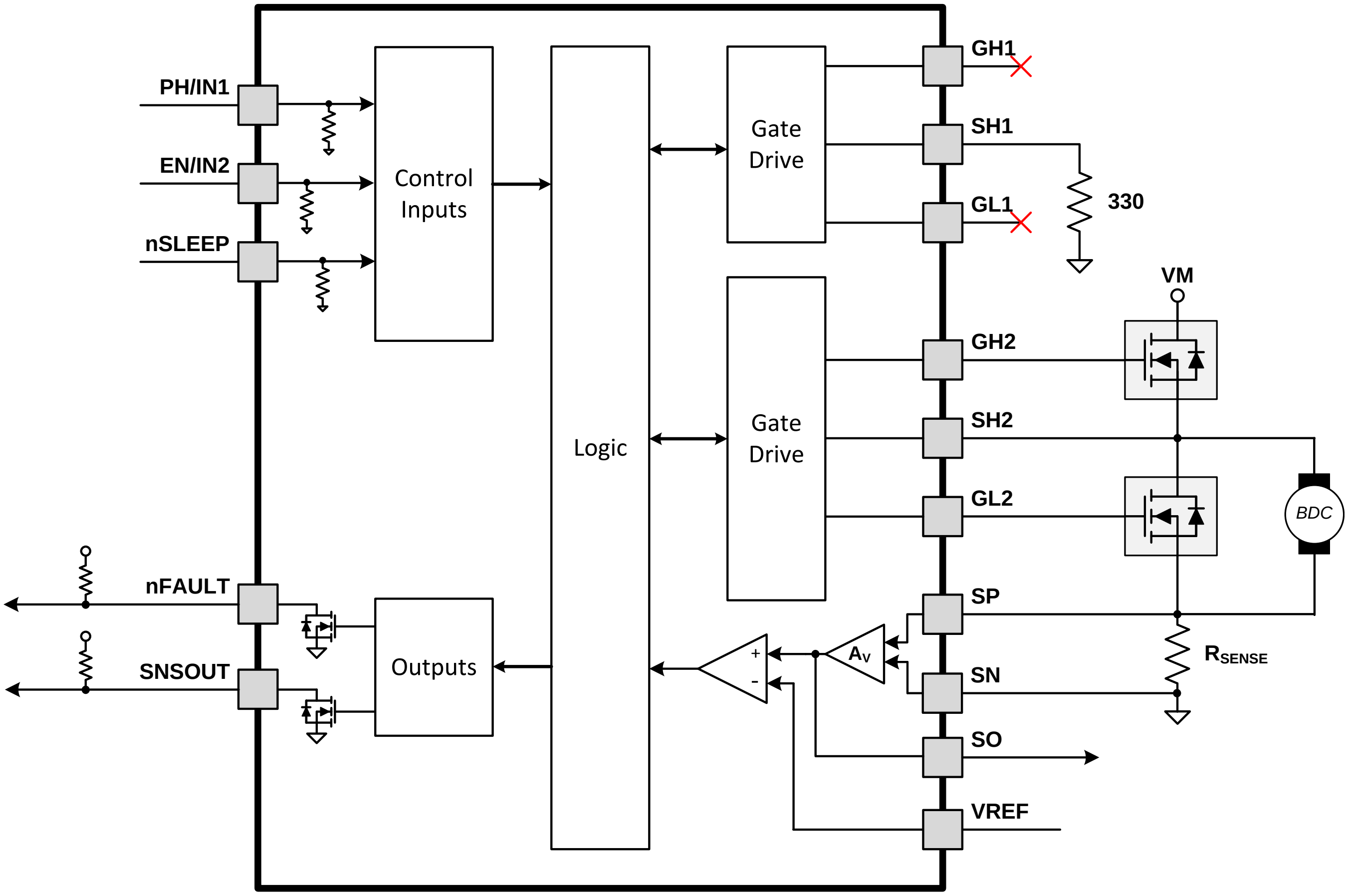


Figure 20. Half-H Bridge Operation Mode

For the DRV8701E, this mode is controlled by tying the PH pin low. Table 3 gives the control scheme. EN = 1 enables the high-side FET, and EN = 0 enables the low-side FET. EN = 1 and PH = 1 is an invalid state.

Table 3. DRV8701E (PH/EN) Control Interface for Half-H Bridge Mode

nSLEEP	EN	PH	SH2	AVDD/DVDD	Description
0	X	X	High-Z	Disabled	Sleep mode; disabled High-Z
1	0	X	L	Enabled	Brake, low-side slow decay
1	1	0	H	Enabled	Drive (Current SH2 → GND)
1	1	1	Invalid state		

For the DRV8701P, Table 4 gives the control scheme. IN1 = 1 and IN2 = 0 is an invalid state.

Table 4. DRV8701P (PWM) Control Interface for Half-H Bridge Mode

nSLEEP	IN1	IN2	SH2	AVDD/DVDD	Description
0	X	X	High-Z	Disabled	Sleep mode; disabled High-Z
1	0	0	High-Z	Enabled	Coast; disabled High-Z
1	0	1	H	Enabled	Drive (current SH2 → GND)
1	1	0	Invalid state		
1	1	1	L	Enabled	Brake; low-side slow decay

7.3.3 Current Regulation

The maximum current through the motor winding is regulated by a fixed off-time PWM current regulation, or current chopping. When an H-bridge is enabled in forward or reverse drive, current rises through the winding at a rate dependent on the DC voltage and inductance of the winding. After the current hits the current chopping threshold, the bridge enters a brake (low-side slow decay) mode until t_{OFF} has expired.

Note that immediately after the current is enabled, the voltage on the SP pin is ignored for a period of time (t_{BLANK}) before enabling the current sense circuitry.

The PWM chopping current is set by a comparator which compares the voltage across a current sense resistor connected to the SP pin, multiplied by a factor of A_V, with a reference voltage from the VREF pin. The factor A_V is the shunt amplifier gain, which is 20 V/V in the DRV8701.

The chopping current is calculated as follows:

$$I_{CHOP} = \frac{V_{REF} - V_{OFF}}{A_V \times R_{SENSE}} \tag{1}$$

Example: If a 50 mΩ sense resistor is used and VREF = 3.3 V, the full-scale chopping current will be 3.25 A. A_V is 20 V/V and V_{OFF} is assumed to be 50 mV in this example.

For DC motors, current regulation is generally used to limit the start-up and stall current of the motor. If the current regulation feature is not needed, it can be disabled by tying VREF directly to AVDD and tying SP and SN to GND.

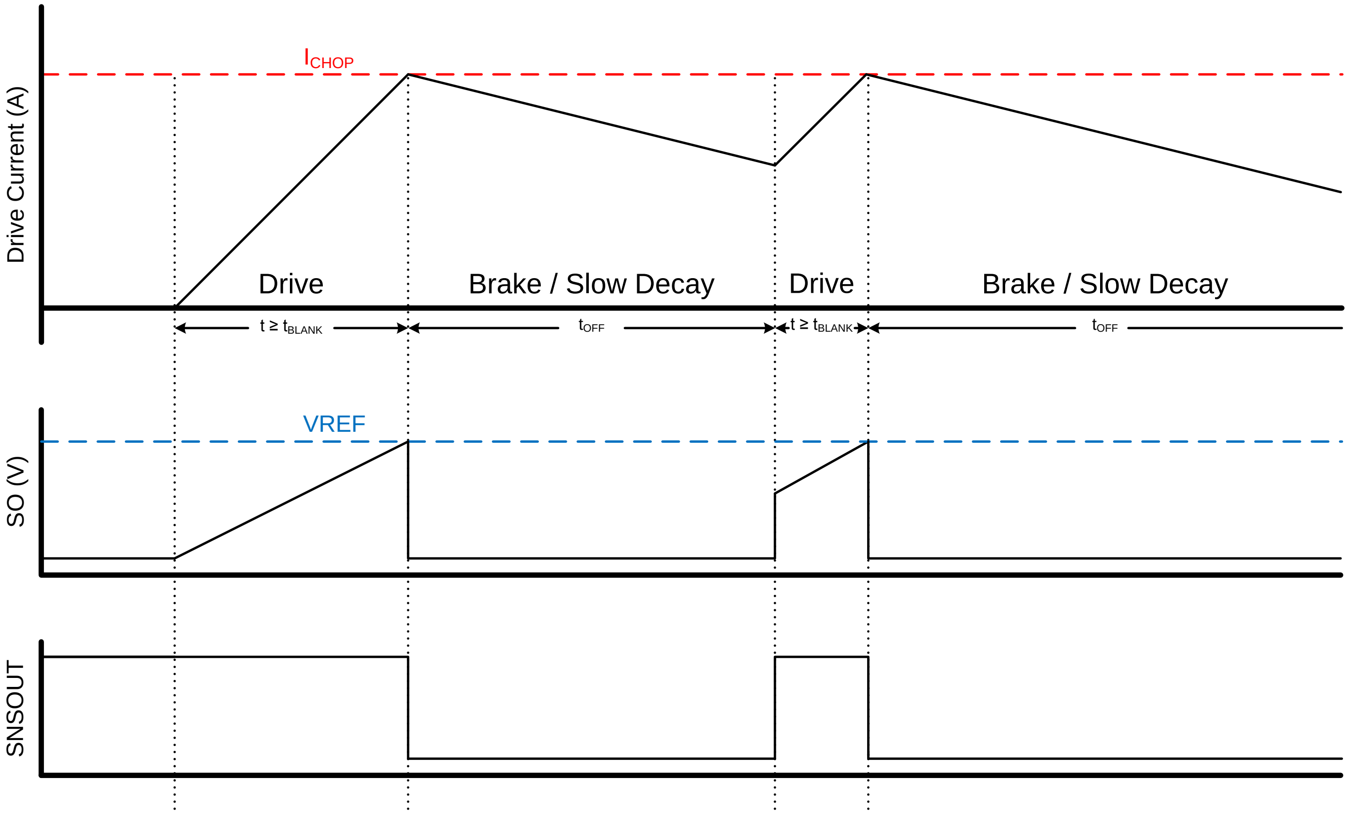


Figure 21. Sense Amplifier and Current Chopping Operation

During brake mode (slow decay), current is recirculated through the low-side FETs. Because current is not flowing through the sense resistor, SO does not represent the motor current.

7.3.4 Amplifier Output SO

The SO pin on the DRV8701 outputs an analog voltage equal to the voltage seen across the SP and SN pins multiplied by A_V. The factor A_V is the shunt amplifier gain, which is 20 V/V in the DRV8701. SO is only valid during forward or reverse drive. The H-bridge current is approximately equal to:

$$I = \frac{SO - V_{OFF}}{A_V \times R_{SENSE}} \tag{2}$$

When SP and SN are 0 V, SO outputs the amplifier offset voltage V_{OFF}. No capacitor is required on the SO pin.

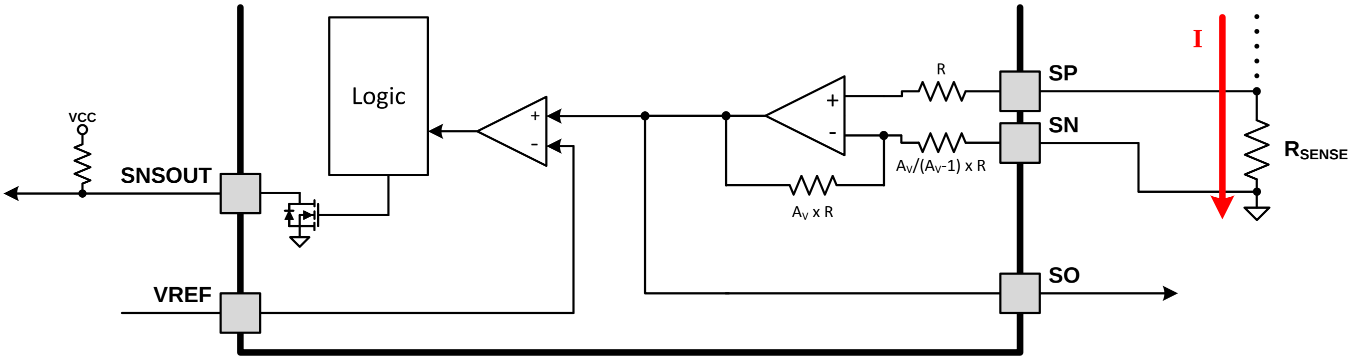


Figure 22. Sense Amplifier Diagram

If the voltage across SP and SN exceeds 1 V, then the DRV8701 flags an overcurrent condition.

The SO pin can source up to 5 mA of current. If the pin is shorted to GND, or if a higher-current load is driven by this pin, the output acts as a constant-current source. The output voltage is not representative of the H-bridge current in this state.

This shunt amplifier feature can be disabled by tying the SP and SN pins to GND. When the amplifier is disabled, current regulation is also disabled.

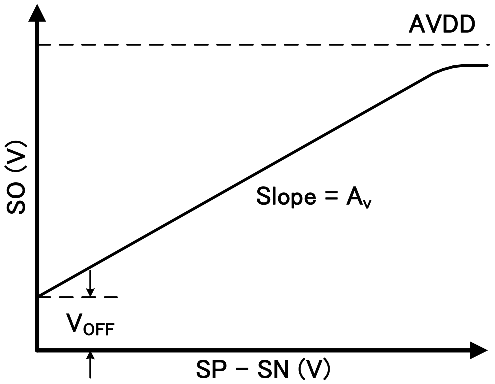


Figure 23. Sense Amplifier Output

7.3.4.1 SNSOUT

The SNSOUT pin of the DRV8701 indicates when the device is in current chopping mode. When the driver is in a slow decay mode caused by internal PWM current chopping (I_{CHOP} threshold hit), the open-drain SNSOUT output is pulled low. If the current regulation is disabled, then the SNSOUT pin will be high-Z.

Note that if the H-bridge is put into a slow decay mode using the inputs (PH/EN or IN1/IN2), then SNSOUT is not pulled low.

During forward or reverse drive mode, SNSOUT is high until the DRV8701 is internally forced into current chopping. If the drive current rises above I_{CHOP}, the driver enters a brake mode (low-side slow decay). The SNSOUT pin will be pulled low during this current chopping brake mode. After the driver is re-enabled, the SNSOUT pin is released high-Z and the drive mode is restarted.

7.3.5 PWM Motor Gate Drivers

The DRV8701 contains gate drivers for a single H-bridge with external NMOS FETs. Figure 24 shows a block diagram of the gate driver circuitry.

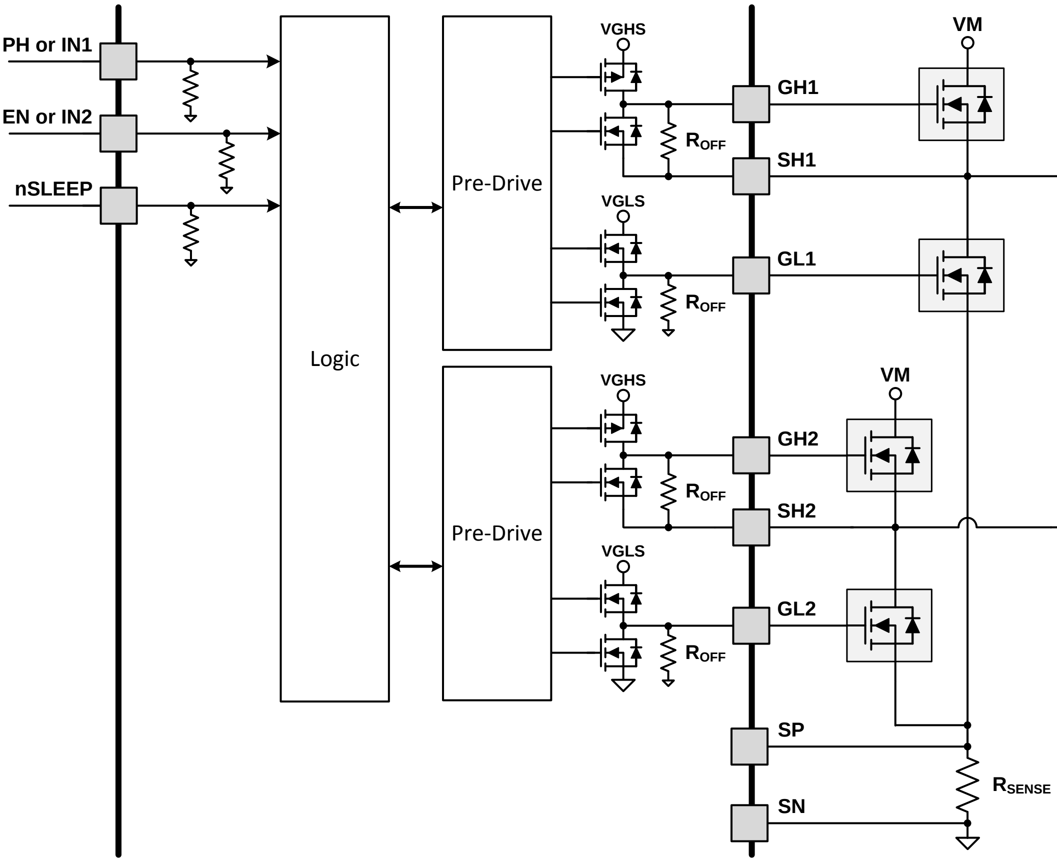


Figure 24. PWM Motor Gate Drivers

Gate drivers inside the DRV8701 directly drive N-channel MOSFETs, which drive the motor current. The high-side gate drive is supplied by the charge pump, while the low-side gate drive voltage is generated by an internal regulator.

The peak drive current of the gate drivers is adjustable through the IDRIVE pin. Peak source currents may be set to 6, 12.5, 25, 100, or 150 mA. The peak sink current is approximately 2× the peak source current. Adjusting the peak current changes the output slew rate, which also depends on the FET input capacitance and gate charge.

The peak drive current is selected by setting the value of the R_{IDRIVE} resistor on the IDRIVE pin or by forcing a voltage onto the IDRIVE pin (see Table 6 for details).

Fast switching times can cause extra voltage noise on VM and GND. This can be especially due to a relatively slow reverse-recovery time of the low-side body diode, where it conducts reverse-bias momentarily, being similar to shoot-through. Slow switching times can cause excessive power dissipation since the external FETs take a longer time to turn on and turn off.

When changing the state of the output, the peak current (I_{DRIVE}) is applied for a short drive period (t_{DRIVE}) to charge the gate capacitance. After this time, a weaker current source (I_{HOLD}) is used to keep the gate at the desired state. When selecting the gate drive strength for a given external FET, the selected current must be high enough to fully charge and discharge the gate during t_{DRIVE}, or excessive power will be dissipated in the FET.

During high-side turn-on, the low-side gate is pulled low with a strong pull-down (I_{STRONG}). This prevents the low-side FET Q_{GS} from charging and keeps the FET off, even when there is fast switching at the outputs.

The pre-driver circuits include enforcement of a dead time in analog circuitry, which prevents the high-side and low-side FETs from conducting at the same time. When switching FETs on, this handshaking prevents the high- or low-side FET from turning on until the opposite FET has been turned off.

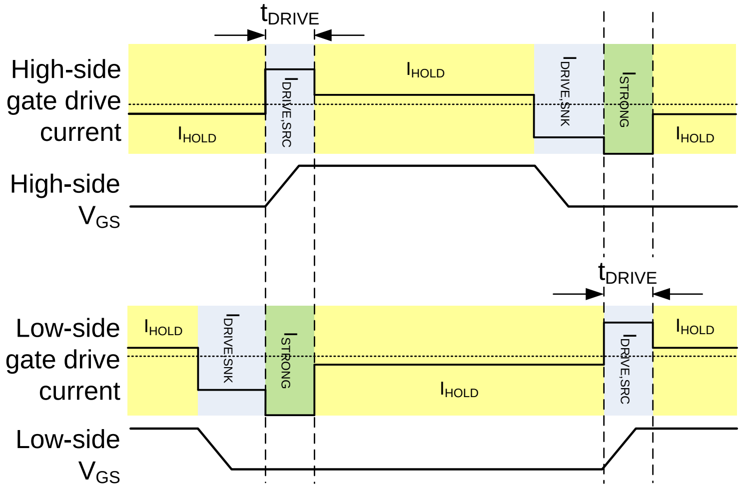


Figure 25. Gate Driver Output to Control External FETs

Q_{GD} Miller charge

When a FET gate is turned on, three different capacitances must be charged.

- Q_{GS} – Gate-to-source charge
- Q_{GD} – Gate-to-drain charge (miller charge)
- Remaining Q_G

The FET output is slewing primarily during the Q_{GD} charge.

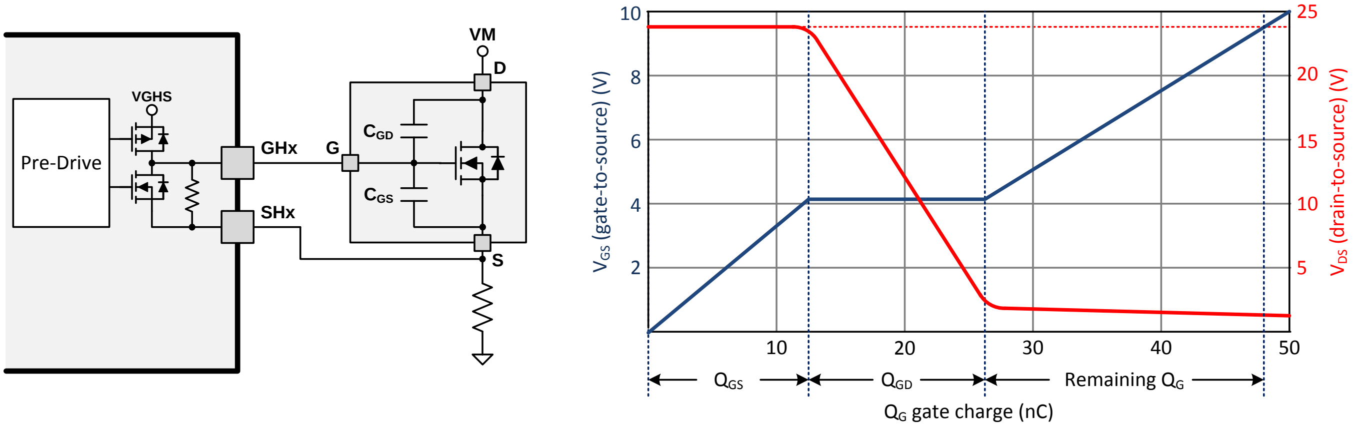


Figure 26. Example FET Gate Charging Profile

7.3.6 IDRIVE Pin

The rise and fall times of the H-bridge output (SHx pins) can be adjusted by setting the IDRIVE resistor value or forcing a voltage onto the IDRIVE pin. The FET gate voltage ramps faster if a higher IDRIVE setting is chosen. The FET gate ramp directly affects the H-bridge output rise and fall time.

Tying IDRIVE to GND selects the lowest drive setting of 6-mA source and 12.5-mA sink. If this pin is left unconnected, then the 100-mA source and 200-mA sink setting are selected.

If IDRIVE is shorted to AVDD, then the VDS OCP monitor on the high-side FETs is disabled. In this setting, the gate driver is configured as 25-mA source and 50-mA sink.

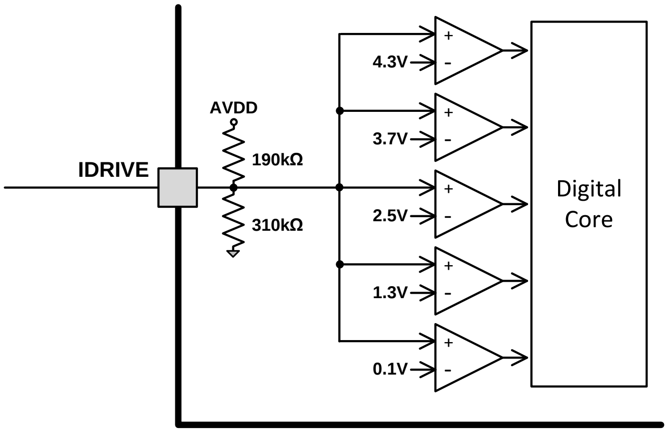
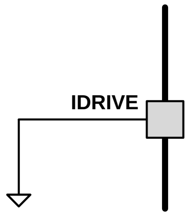
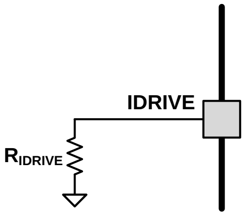
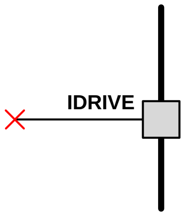
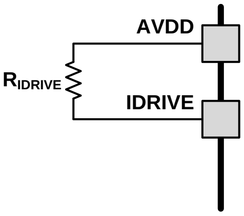
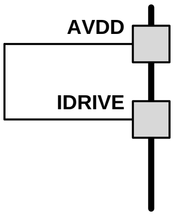


Figure 27. IDRIVE Pin Internal Circuitry

Table 5. IDRIVE Pin Configuration Settings

IDRIVE Resistance	IDRIVE Voltage	Source Current ($I_{DRIVE,SRC}$)	Sink Current ($I_{DRIVE,SNK}$)	HS OCP Monitor
<1 kΩ to GND	GND	6 mA	12.5 mA	ON
33 kΩ ±5% to GND	0.7 V ±5%	12.5 mA	25 mA	ON
200 kΩ ±5% to GND	2 V ±5%	25 mA	50 mA	ON
>500 kΩ to GND, High-Z	3 V ±5%	100 mA	200 mA	ON
68 kΩ ±5% to AVDD	4 V ±5%	150 mA	300 mA	ON
<1 kΩ to AVDD	AVDD	25 mA	50 mA	OFF

Table 6. IDRIVE Pin Resistor Settings

<1 kΩ to GND	33 kΩ ±5% to GND 200 kΩ ±5% to GND	>500 kΩ to GND, High-Z	68 kΩ ±5% to AVDD	<1 kΩ to AVDD
				
IDRIVE	IDRIVE	IDRIVE	IDRIVE	IDRIVE
6 / 12.5 mA	12.5 / 25 mA (33 kΩ) 25 / 50 mA (200 kΩ)	100 / 200 mA	150 / 300 mA	25 / 50 mA HS OCP monitor off

7.3.7 Dead Time

Dead time (t_{DEAD}) is measured as the time when SHx is High-Z between turning off one of the H-bridge FETs and turning on the other. For example, the output is High-Z between turning off the high-side FET and turning on the low-side FET.

The DRV8701 inserts a digital dead time of approximately 150 ns. The total dead time also includes the FET gate turn-on time.

The total dead time is dependent on the IDRIVE resistor setting because a portion of the FET gate ramp (GHx and GLx pins) includes the observable dead time.

7.3.8 Propagation Delay

The propagation delay time (t_{DELAY}) is measured as the time between an input edge to an output change. This time is composed of two parts: an input deglitch time and output slewing delay. The input deglitcher prevents noise on the input pins from affecting the output state.

The gate drive slew rate also contributes to the delay time. For the output to change state during normal operation, first, one FET must be turned off. The FET gate is ramped down according to the IDRIVE setting, and the observed propagation delay ends when the FET gate has fallen below the threshold voltage.

7.3.9 Overcurrent V_{DS} Monitor

The gate driver circuit monitors the V_{DS} voltage of each external FET when it is driving current. When the voltage monitored is greater than the OCP threshold voltage ($V_{DS\ OCP}$), after the OCP deglitch time (t_{OCP}) has expired, an OCP condition will be detected.

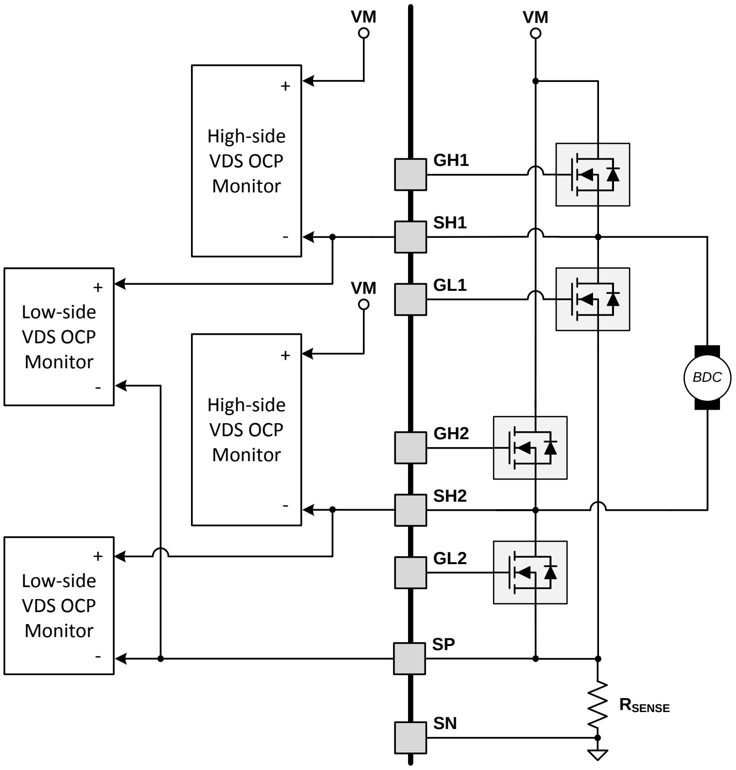


Figure 28. Overcurrent VDS Monitors

When IDRIVE is shorted to AVDD, the V_{DS} OCP monitor on the high-side FETs is disabled. In cases where the VM supplied to the DRV8701 can be different from the external H-bridge supply, this setting must be used in order to prevent false overcurrent detection. In this mode, the IDRIVE current is set to 25-mA source and 50-mA sink.

7.3.10 Charge Pump

A charge pump is integrated to supply a high-side NMOS gate drive voltage of V_{HGS}. The charge pump requires a capacitor between the VM and VCP pins. Additionally a low-ESR ceramic capacitor is required between pins CPH and CPL. When VM is below 12 V, this charge pump behaves as a doubler and generates VCP = 2 × VM – 1.5 V if unloaded. Above VM = 12 V, the charge pump regulates VCP such that VCP = VM + 9.5 V.

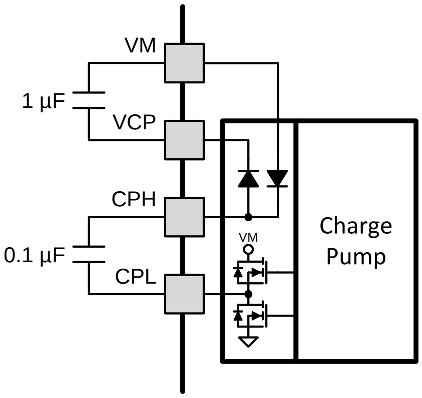


Figure 29. Charge Pump Diagram

7.3.11 LDO Voltage Regulators

Two LDO regulators are integrated into the DRV8701. They can be used to provide the supply voltage for a low-power microcontroller or other low-current devices. For proper operation, bypass the AVDD and DVDD pins to GND using ceramic capacitors.

The AVDD output voltage is nominally 4.8 V, and the DVDD output is nominally 3.3 V. When the AVDD or DVDD current load exceeds 30 mA, the LDO behaves like a constant current source. The output voltage drops significantly with currents greater than this limit.

Note that AVDD and DVDD are disabled when the device is in sleep mode (nSLEEP = 0). In addition, when an overtemperature (TSD) or undervoltage (UVLO) fault is encountered, the AVDD regulator is shut off.

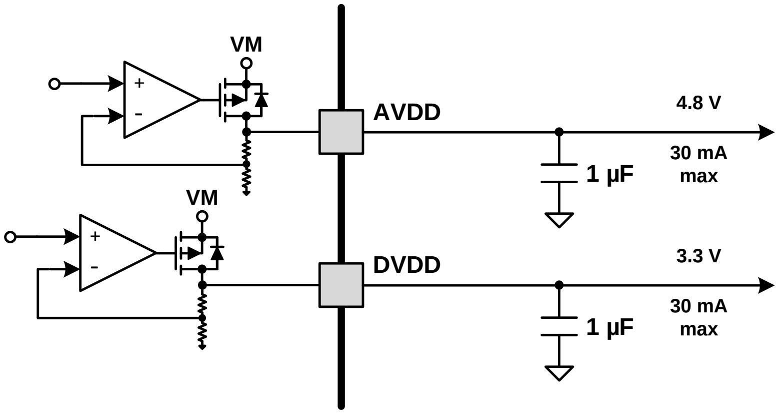


Figure 30. AVDD and DVDD LDOs

The power dissipated in the DRV8701 due to these LDOs may be approximated by:

$$\text{Power} = (\text{VM} - \text{AVDD}) \times I_{AVDD} + (\text{VM} - \text{DVDD}) \times I_{DVDD} \quad (3)$$

For example at VM = 24 V, drawing 10 mA out of both AVDD and DVDD results in a power dissipation of:

$$\text{Power} = (24\text{ V} - 4.8\text{ V}) \times 10\text{ mA} + (24\text{ V} - 3.3\text{ V}) \times 10\text{ mA} = 192\text{ mW} + 207\text{ mW} = 399\text{ mW} \quad (4)$$

7.3.12 Gate Drive Clamp

A clamping structure limits the gate drive output voltage to $V_{GS\ CLAMP}$ to protect the power FETs from damage. The positive voltage clamp is realized using a series of diodes. The negative voltage clamp uses the body diodes of the internal gate driver FET.

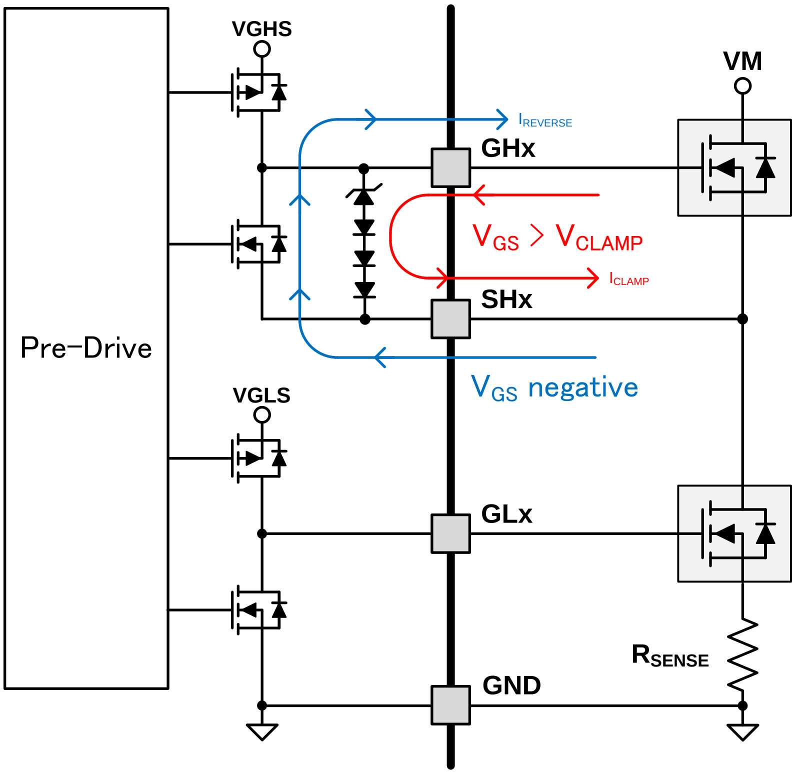


Figure 31. Gate Drive Clamp Diagram

7.3.13 Protection Circuits

The DRV8701 is fully protected against VM undervoltage, charge pump undervoltage, overcurrent, gate driver shorts, and overtemperature events.

7.3.13.1 VM Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the UVLO threshold voltage, all FETs in the H-bridge are disabled, the charge pump is disabled, AVDD is disabled, and the nFAULT pin is driven low. Operation resumes when VM rises above the UVLO threshold. The nFAULT pin is released after operation has resumed.

7.3.13.2 VCP Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin falls below the charge pump undervoltage threshold voltage (V_{CPUV}), all FETs in the H-bridge are disabled and the nFAULT pin is driven low. Operation resumes when VCP rises above the CPUV threshold. The nFAULT pin is released after operation has resumed.

7.3.13.3 Overcurrent Protection (OCP)

Overcurrent is sensed by monitoring the V_{DS} voltage drop across the external FETs (see Figure 28). If the voltage across a driven FET exceeds the overcurrent trip threshold ($V_{DS\ OCP}$) for longer than the OCP deglitch time (t_{OCP}), an OCP event is recognized. As a result, all FETs in the H-bridge are disabled and the nFAULT pin is driven low; the driver is re-enabled after the OCP retry period (t_{RETRY}) has passed. nFAULT releases high-Z again at after the retry time. If the fault condition is still present, the cycle repeats. If the fault is no longer present, normal operation resumes and nFAULT remains released high-Z.

This V_{DS} overcurrent monitor on the high-side FETs can be disabled by using a specific IDRIVE setting. This allows the system to have a higher DRV8701 VM supply than the H-bridge supply.

In addition to this FET V_{DS} monitor, an overcurrent condition is also detected if the voltage at SP exceeds $V_{SP\ OCP}$.

7.3.13.4 Pre-Driver Fault (PDF)

The GHx and GLx pins are monitored such that if the voltage on the external FET gate does not increase above 1 V (when sourcing current) or decrease below 1 V (when sinking current) after t_{DRIVE}, a pre-driver fault is detected. The device encounters this fault if GHx or GLx are shorted to GND, SHx, or VM. Additionally, the device encounters the pre-driver fault if the IDRIVE setting selected is not sufficient to turn on the external FET. As a result, all FETs in the H-bridge are disabled and the nFAULT pin is driven low. The driver is re-enabled after the retry period (t_{RETRY}) has passed. The nFAULT pin is released after operation has resumed.

7.3.13.5 Thermal Shutdown (TSD)

If the die temperature exceeds T_{TSD}, all FETs in the H-bridge are disabled, the charge pump is shut down, AVDD is disabled, and the nFAULT pin is driven low. After the die temperature has fallen below $T_{TSD} – T_{HYS}$, operation automatically resumes. The nFAULT pin is released after operation has resumed.

Table 7. Fault Response

Fault	Condition	H-Bridge	Charge Pump	AVDD	DVDD	Recovery
VM undervoltage (UVLO)	$VM \le V_{UVLO}$	Disabled	Disabled	Disabled	Operating	$VM \ge V_{UVLO}$
VCP undervoltage (CPUV)	$VCP < V_{CPUV}$	Disabled	Operating	Operating	Operating	$VCP > V_{CPUV}$
External FET overload (OCP)	$V_{DS} \ge 1.0$ V or $V_{SP} – V_{SN} > 1.0$ V	Disabled	Operating	Operating	Operating	t_{RETRY}
Pre-driver fault (PDF)	Gate voltage unchanged after t_{DRIVE}	Disabled	Operating	Operating	Operating	t_{RETRY}
Thermal shutdown (TSD)	$T_J \ge 150°C$	Disabled	Disabled	Disabled	Operating	$T_J \le 130°C$

7.3.14 Reverse Supply Protection

The following circuit may be implemented to protect the system from reverse supply conditions. This circuit requires the following additional components:

- NMOS FET
- npn BJT
- Diode
- 10-kΩ resistor
- 43-kΩ resistor

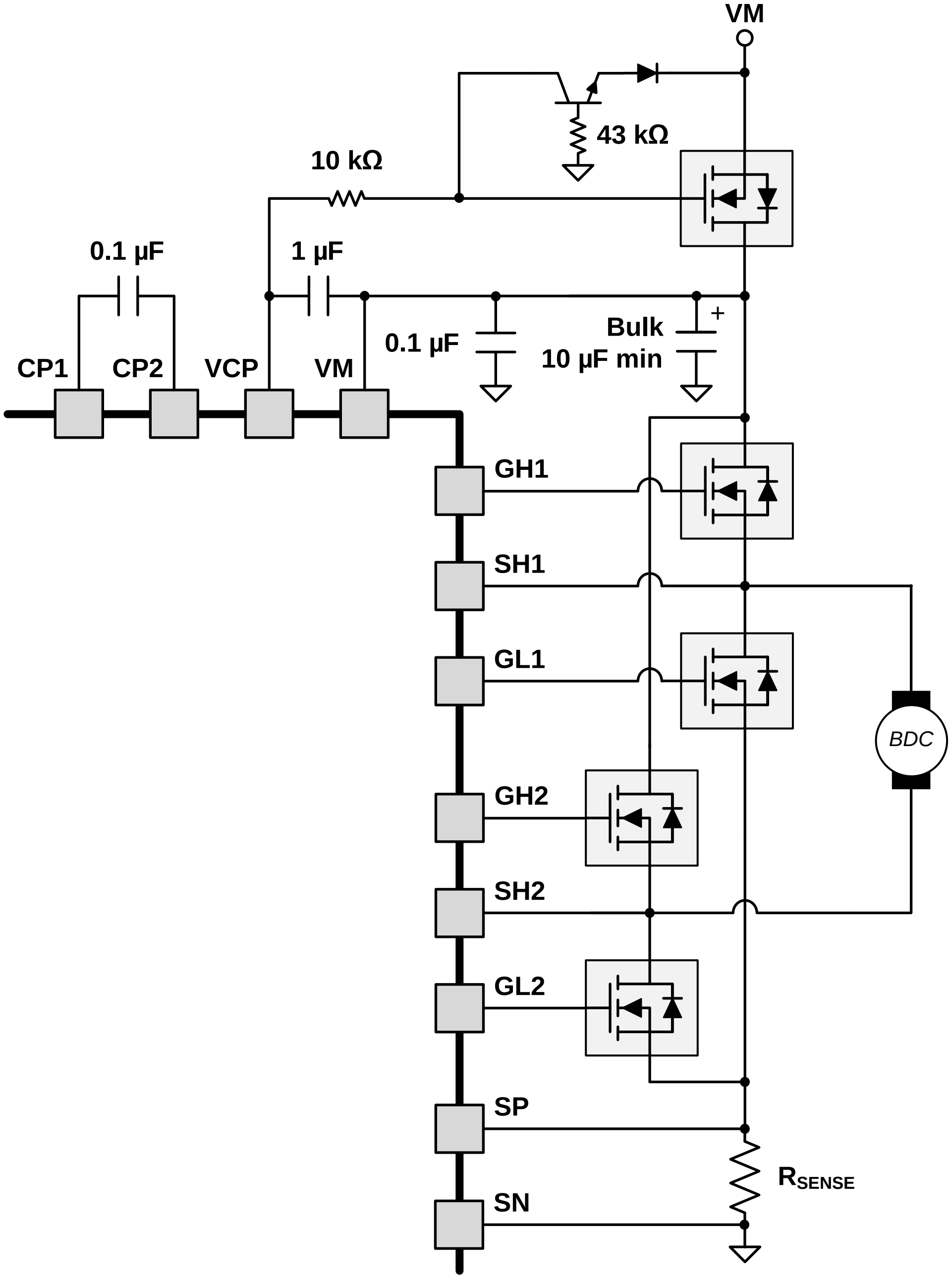


Figure 32. Reverse Supply Protection External Circuitry

7.4 Device Functional Modes

The DRV8701 is active unless the nSLEEP pin is brought low. In sleep mode, the charge pump is disabled, the H-bridge FETs are High-Z, and the AVDD and DVDD regulators are disabled. Note that t_{SLEEP} must elapse after a falling edge on the nSLEEP pin before the device is in sleep mode. The DRV8701 is brought out of sleep mode if nSLEEP is brought high. Note that t_{WAKE} must elapse before the outputs change state after wake-up.

While nSLEEP is brought low, all external H-bridge FETs are disabled. The high-side gate pins GHx are pulled to the output node SHx by an internal resistor, and the low-side gate pins GLx are pulled to GND.

When VM is not applied, and during the power-on time (t_{ON}), the outputs are disabled using weak pulldown resistors between the GHx and SHx pins and between GLx and GND.

Table 8. Functional Modes

Condition		Charge Pump	GHx	GLx	AVDD and DVDD
Unpowered	$VM < V_{UVLO}$	Disabled	Weak pulldown to SHx	Weak pulldown to GND	Disabled
Sleep mode	$V_{UVLO} < VM$ nSLEEP low	Disabled	Strong pulldown to GND	Strong pulldown to GND	Disabled
Operating	$V_{UVLO} < VM$ nSLEEP high	Enabled	Depends on inputs	Depends on inputs	Operating

7.4.1 Operating DRV8701 and H-Bridge on Separate Supplies

The DRV8701 can operate with a different supply voltage (VM) than the system H-bridge supply (VBAT). Case 1 describes normal operation when VM and VBAT are roughly the same. Special considerations must be taken into account for Cases 2, 3, and 4.

- **Case 1**: VM ≈ VBAT. Recommended operation
- **Case 2**: VM > VBAT. IDRIVE must be shorted to AVDD to disable the high-side OCP. The IDRIVE current is fixed at 25-mA source and 50-mA sink. This case can allow the driver to better enhance the external FETs for VBAT < 11.5 V, or operate down to a lower supply voltage below 5.9 V.
- **Case 3**: VM > VBAT (higher than Case 2). IDRIVE must be shorted to AVDD to disable the high-side OCP. This case can also allow the driver to better enhance the external FETs, or operate down to a lower supply voltage below 5.9 V. The IDRIVE current is fixed at 25-mA source and 50-mA sink. Excess gate drive current may be driven through the DRV8701 gate clamps causing additional power dissipation in the DRV8701.
- **Case 4**: VM < VBAT. The high-side FETs may not be in saturation. There may be a significant voltage drop across the high-side FET when driving current. This causes high power dissipation in the external FET. When operating in Case 4, the external FET threshold voltage must be greater than 2 V. Otherwise the DRV8701 will report a pre-driver fault whenever the FET is out of saturation.

Table 9. VM Operational Range based on VBAT

VBAT Range	Case 3	Case 2	Case 1	Case 4
1 V ≤ VBAT < 5.9 V	VM ≥ 0.5 × VBAT + 5.75 V VM ≤ 45 V	VM ≥ 5.9 V VM < 0.5 × VBAT + 5.75 V	N/A	N/A
5.9 V ≤ VBAT < 6.4 V		VM > VBAT VM < 0.5 × VBAT + 5.75 V	VM = VBAT	VM ≥ 5.9 V VM < VBAT
6.4 V ≤ VBAT < 11.5 V			VM > 0.6 × VBAT + 2.5 V VM ≤ VBAT	VM ≥ 5.9 V VM ≤ 0.6 × VBAT + 2.5 V
11.5 V ≤ VBAT < 14 V	VM > VBAT VM ≤ 45 V	N/A		
14 V ≤ VBAT ≤ 45 V			VM > VBAT – 4 V VM ≤ VBAT	VM ≥ 5.9 V VM ≤ VBAT – 4 V

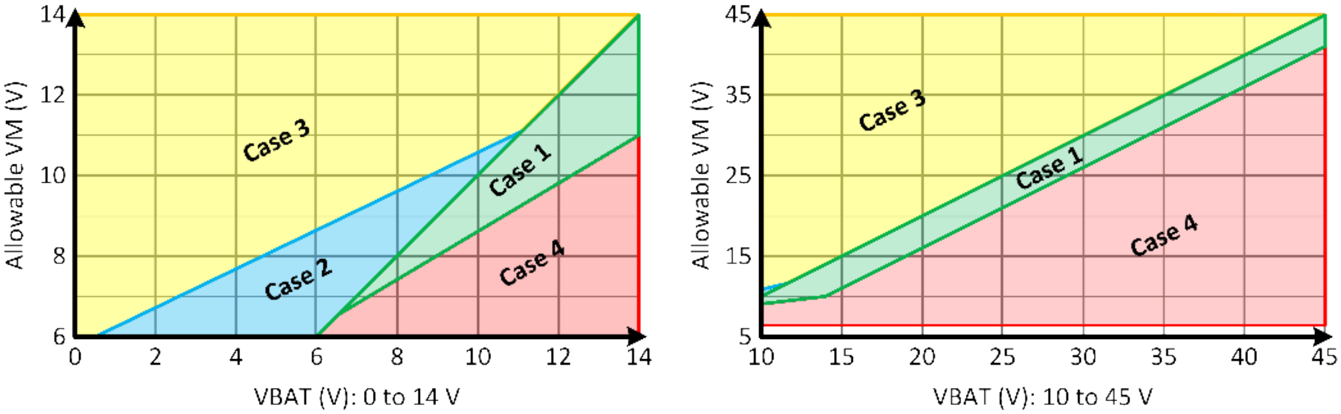


Figure 33. VM Operating Range Based on Motor Supply Voltage

When nSLEEP is low, VM may be reduced down to 0 V with up to 45 V present at VBAT. However, nSLEEP should not be brought high until VM is supplied with a voltage aligning with one of the cases outlined above.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8701 is used in brushed-DC, solenoid, or relay control.

8.2 Typical Applications

8.2.1 Brushed-DC Motor Control

The following design procedure can be used to configure the DRV8701.

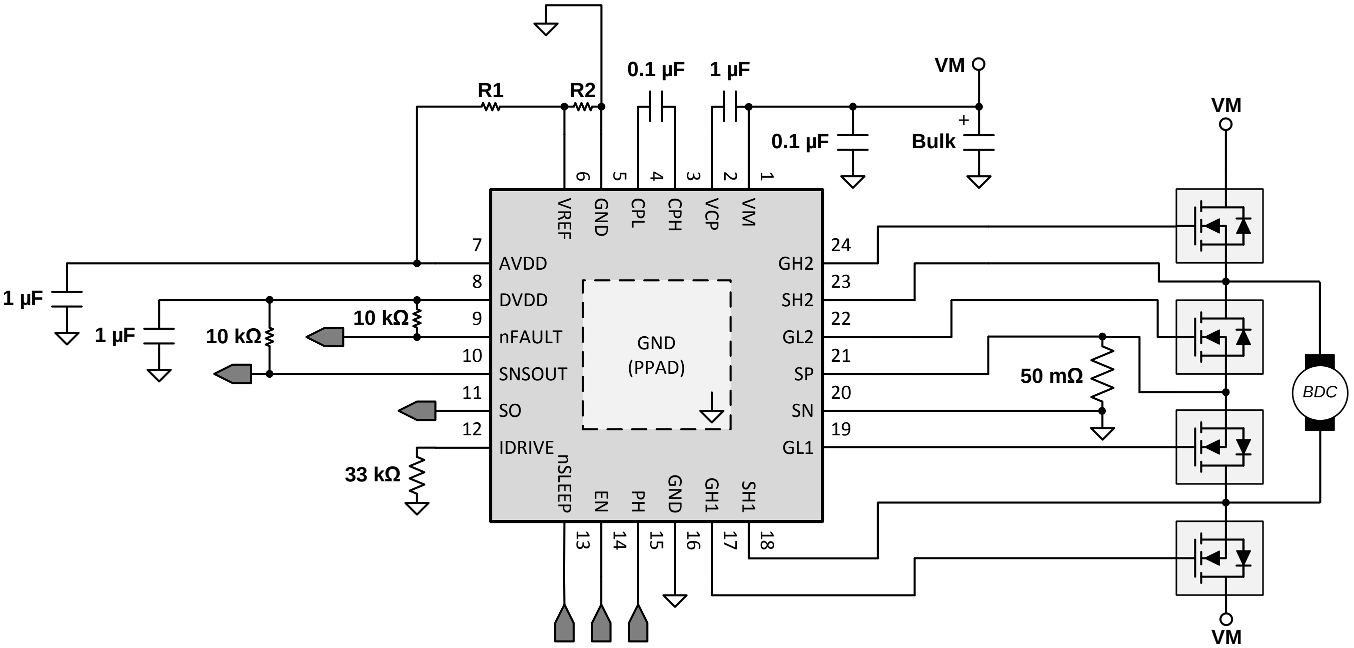


Figure 34. Typical Application Schematic

8.2.1.1 Design Requirements

Table 10 gives design input parameters for system design.

Table 10. Design Parameters

Design Parameter	Reference	Example Value
Nominal supply voltage	VM	18 V
Supply voltage range	VM_{MIN}, VM_{MAX}	12 to 24 V
FET total gate charge (1)	Q_G	14 nC (typically)
FET gate-to-drain charge (1)	Q_{GD}	2.3 nC (typically)
Target FET gate rise time	RT	100 to 300 ns
Motor current chopping level	I_{CHOP}	3 A

(1) FET part number is CSD88537ND.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 External FET Selection

The DRV8701 FET support is based on the charge pump capacity and output PWM frequency. For a quick calculation of FET driving capacity, use the following equations when drive and brake (slow decay) are the primary modes of operation:

$$Q_G < \frac{I_{VCP}}{f_{PWM}}$$

where

- f_{PWM} is the maximum desired PWM frequency to be applied to the DRV8701 inputs or the current chopping frequency, whichever is larger.
- I_{VCP} is the charge pump capacity, which depends on VM. (5)

The internal current chopping frequency is at most:

$$f_{PWM} < \frac{1}{t_{OFF} + t_{BLANK}} \approx 38\text{ kHz} \quad (6)$$

Example: If a system at VM = 7 V (I_{VCP} = 8 mA) uses a maximum PWM frequency of 40 kHz, then the DRV8701 will support Q_G < 200 nC FETs.

If the application will require a forced fast decay (or alternating between drive and reverse drive), the maximum FET driving capacity is given by:

$$Q_G < \frac{I_{VCP}}{2 \times f_{PWM}} \quad (7)$$

8.2.1.2.2 IDRIVE Configuration

Select IDRIVE based on the gate charge of the FETs. Configure this pin so that the FET gates are charged completely during t_{DRIVE}. If the designer chooses an IDRIVE that is too low for a given FET, then the FET may not turn on completely. TI suggests to adjust these values in-system with the required external FETs and motor to determine the best possible setting for any application.

For FETs with a known gate-to-drain charge (Q_{GD}) and desired rise time (RT), select IDRIVE based on:

$$\text{IDRIVE} > \frac{Q_{GD}}{RT} \quad (8)$$

Example: If the gate-to-drain charge is 2.3 nC, and the desired rise time is around 100 to 300 ns,

IDRIVE1 = 2.3 nC / 100 ns = 23 mA

IDRIVE2 = 2.3 nC / 300 ns = 7.7 mA

Select IDRIVE between 7.7 and 23 mA

Select IDRIVE as 12.5-mA source (25-mA sink)

Requires a 33-kΩ resistor from the IDRIVE pin to GND

8.2.1.2.3 Current Chopping Configuration

The chopping current is set based on the sense resistor value and the analog voltage at VREF. Calculate the current using Equation 9. The amplifier gain A_V is 20 V/V and V_{OFF} is typically 50 mV.

Example: If the desired chopping current is 3 A,

Set R_{SENSE} = 50 mΩ

$$I_{CHOP} = \frac{VREF - V_{OFF}}{A_V \times R_{SENSE}} \quad (9)$$

VREF would have to be 3.05 V.

Create a resistor divider from AVDD (4.8 V) to set VREF ≈ 3 V

Set R2 = 3.3 kΩ; set R1 = 2 kΩ.

8.2.1.3 Application Curves

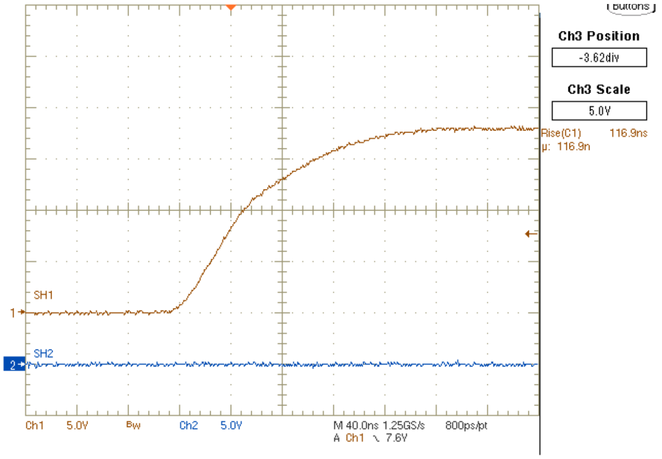


Figure 35. SH1 Rise Time (12.5-mA Source, 25-mA Sink)

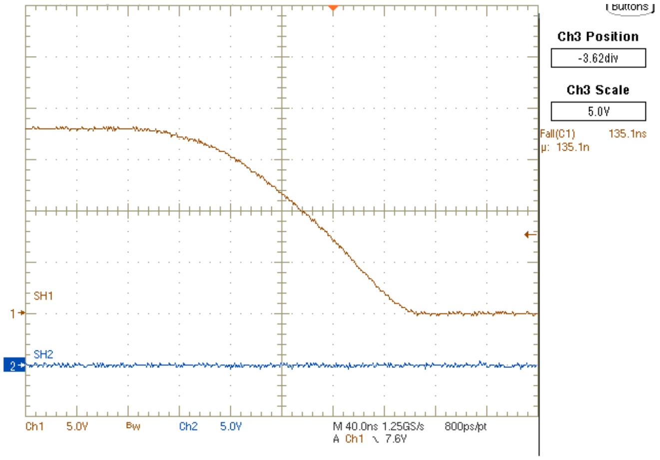


Figure 36. SH1 Fall Time (12.5-mA Source, 25-mA Sink)

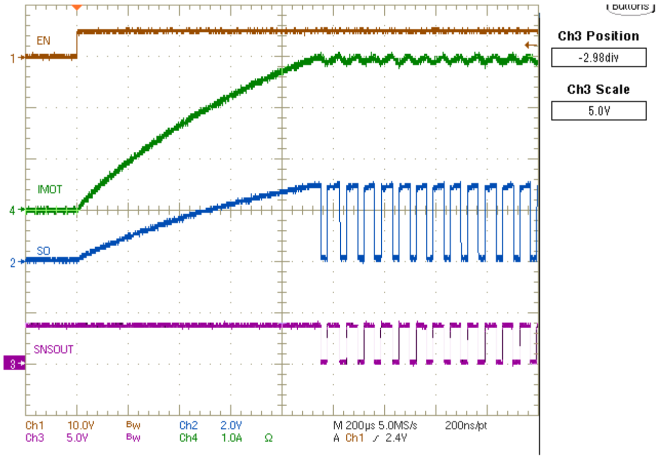


Figure 37. Current Regulating at 3 A on Motor Startup

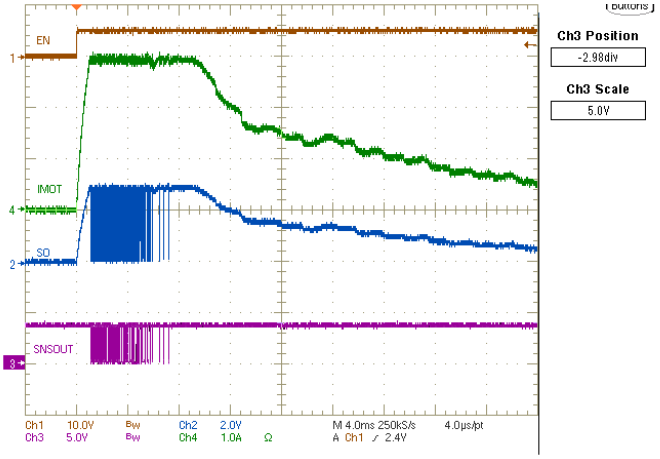


Figure 38. Current Profile on Motor Startup With Regulation

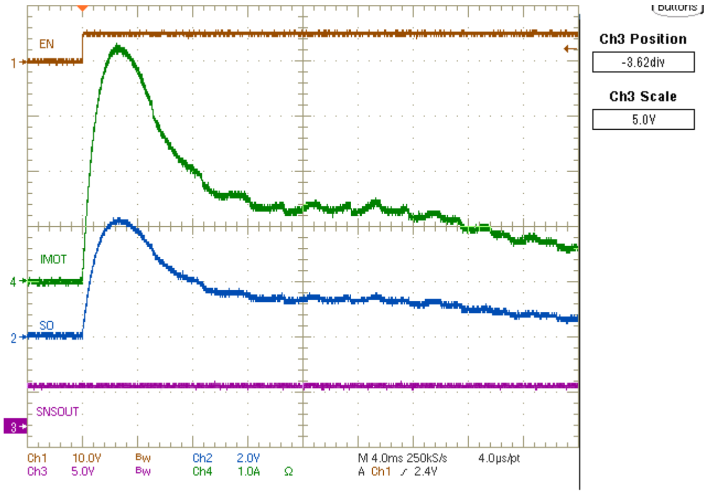


Figure 39. Current Profile on Motor Startup Without Regulation

8.2.2 Alternate Application

In this example, the DRV8701 is powered from a supply that is boosted above VBAT. This allows the system to work at lower VBAT voltages, but requires the user to disable OCP monitoring.

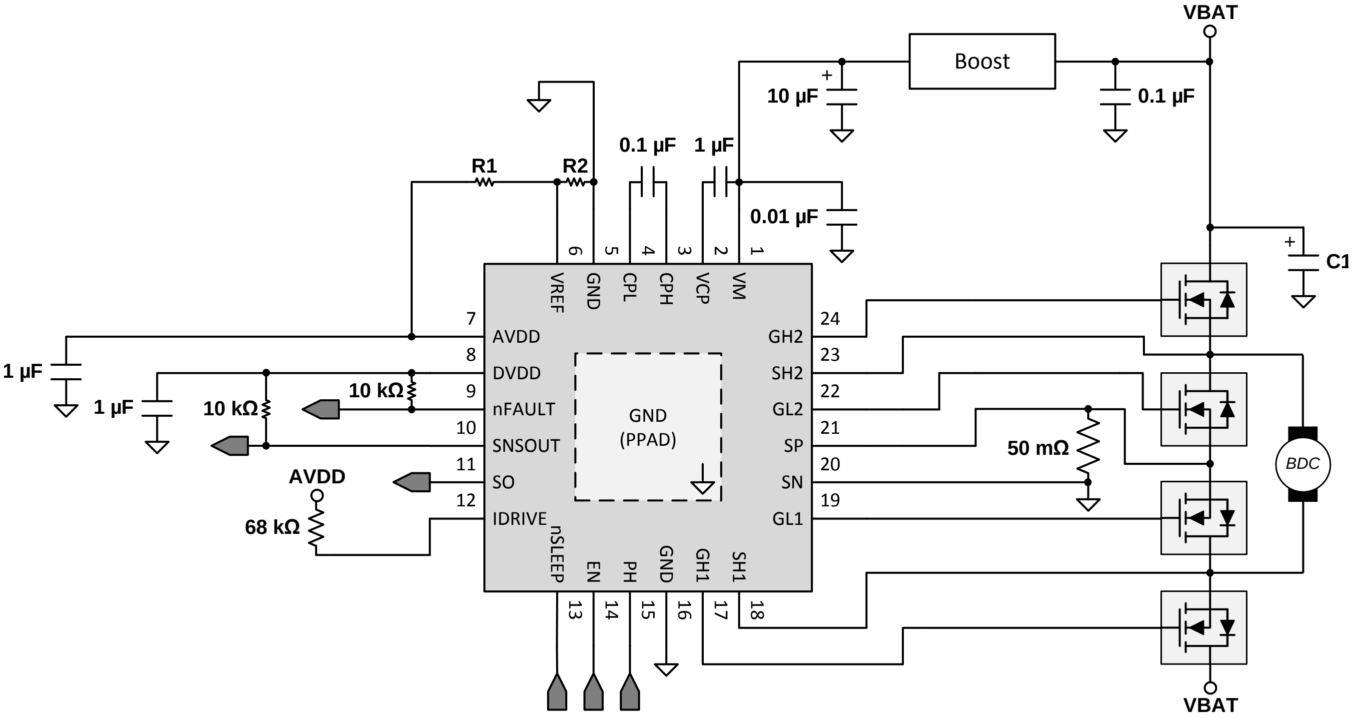


Figure 40. DRV8701 on Boosted Supply

8.2.2.1 Design Requirements

Table 11 gives design input parameters for system design.

Table 11. Design Parameters

Design Parameter	Reference	Example Value
Battery voltage	VBAT	12 V nominal Minimum operation: 4.0 V
DRV8701 supply voltage	VM	VM = 7 V when VBAT < 7 V VM = VBAT when VBAT ≥ 7 V
FET total gate charge	Q_G	42 nC
FET gate-to-drain charge	Q_{GD}	11 nC
Motor current chopping level	I_{CHOP}	3 A

8.2.3 Detailed Design Procedure

8.2.3.1 IDRIVE Configuration

Because the VM supply to the DRV8701 is different from the external H-bridge supply VBAT, the designer must disable the overcurrent monitor to prevent false overcurrent detection. The designer must place a 68-kΩ resistor between the IDRIVE pin and AVDD.

IDRIVE is fixed at 25-mA source and 50-mA sink in this mode.

So, the rise time is 11 nC / 25 mA = 440 ns.

8.2.3.2 VM Boost Voltage

To determine an effective voltage to boost VM, first determine the minimum VBAT at which the system must operate. Select VM such that the gate driver clamps do not turn on during normal operation.

$$VM < \frac{VBAT + 11.5\ V}{2} \tag{10}$$

Example: If VBAT minimum is 4.0 V,

VM < 7.75 V

So VM = 7 V is selected to allow for adequate margin.

9 Power Supply Recommendations

The DRV8701 is designed to operate from an input voltage supply (VM) range between 5.9 and 45 V. A 0.1-µF ceramic capacitor rated for VM must be placed as close to the DRV8701 as possible. In addition, the designer must include a bulk capacitor with a valued of at least 10 µF on VM.

Bypassing the external H-bridge FETs requires additional bulk capacitance.

9.1 Bulk Capacitance Sizing

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The datasheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

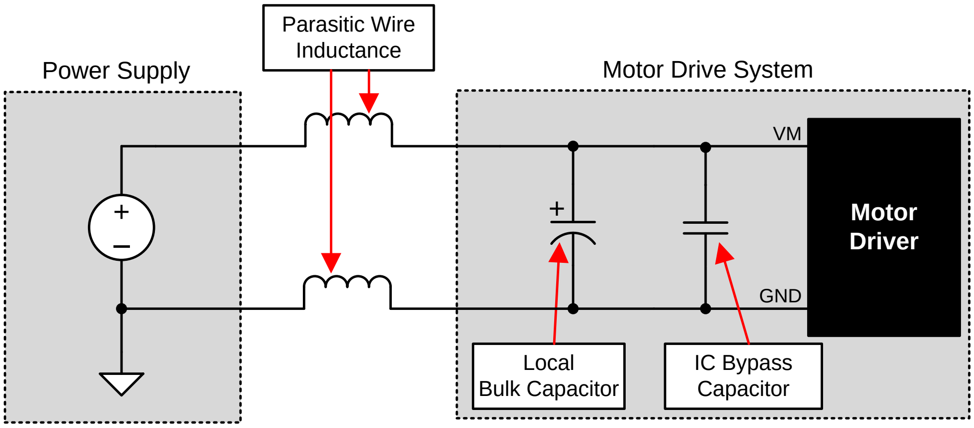


Figure 41. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

10 Layout

10.1 Layout Guidelines

Bypass the VM pin to GND using a low-ESR ceramic bypass capacitor with a recommended value of 0.1 µF rated for VM. Place this capacitor as close to the VM pin as possible with a thick trace or ground plane connection to the device GND pin.

Bypass the VM pin to ground using a bulk capacitor rated for VM. This component may be an electrolytic. This capacitance must be at least 10 µF. The bulk capacitor should be placed to minimize the distance of the high-current path through the external FETs. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Place a low-ESR ceramic capacitor in between the CPL and CPH pins. The value for this component is 0.1 µF rated for VM. Place this component as close to the pins as possible.

Place a low-ESR ceramic capacitor in between the VM and VCP pins. The value for this component is 1 µF rated for 16 V. Place this component as close to the pins as possible.

Bypass AVDD and DVDD to ground with ceramic capacitors rated at 6.3 V. Place these bypassing capacitors as close to the pins as possible.

If desired, align the external NMOS FETs as shown in Figure 42 to facilitate layout. Route the SH2 and SH1 nets to the motor.

Use separate traces to connect the SP and SN pins to the R_{SENSE} terminals.

10.2 Layout Example

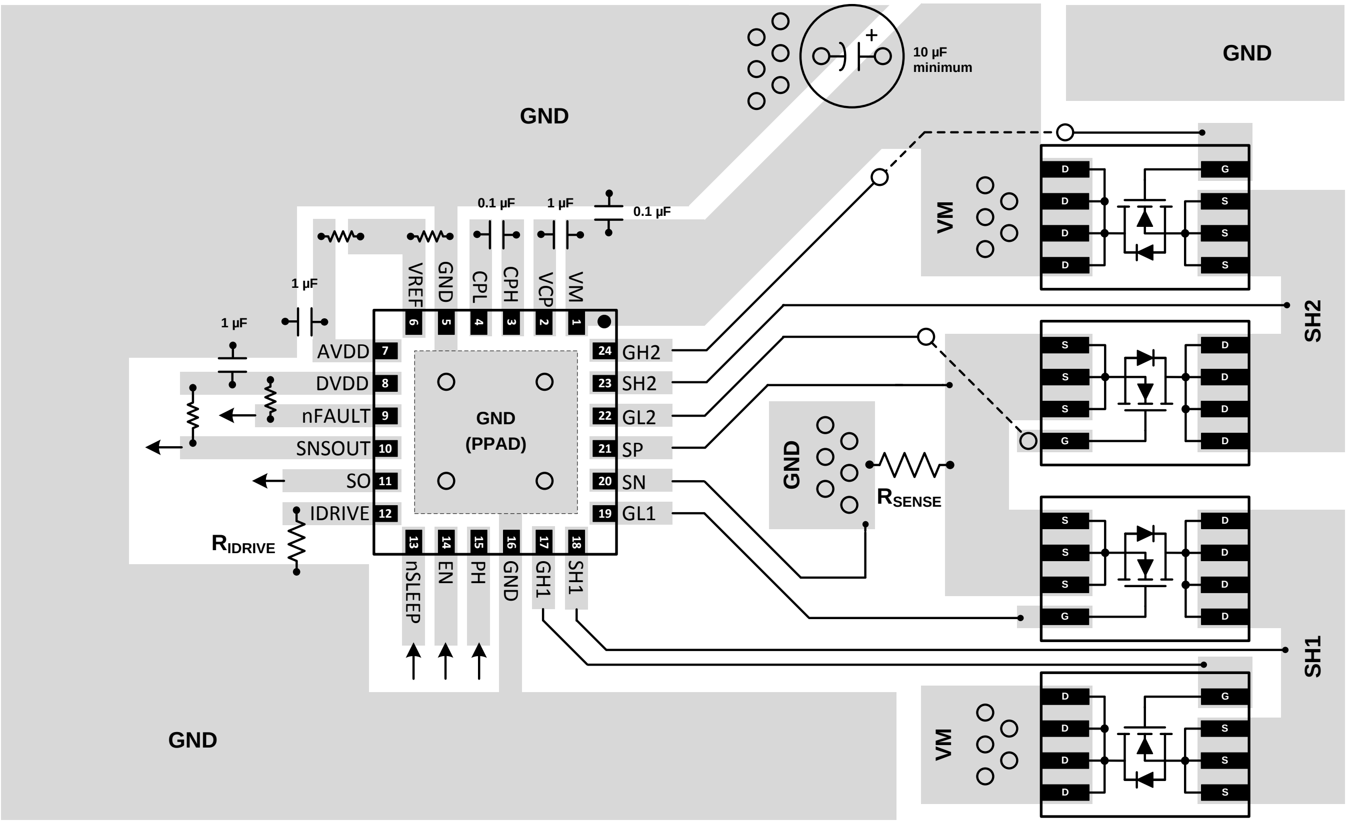


Figure 42. Layout Recommendation

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

- *PowerPAD™ Thermally Enhanced Package*, SLMA002
- *PowerPAD™ Made Easy*, SLMA004
- *Current Recirculation and Decay Modes*, SLVA321

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8701ERGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8701E	Samples
DRV8701ERGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8701E	Samples
DRV8701PRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8701P	Samples
DRV8701PRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8701P	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

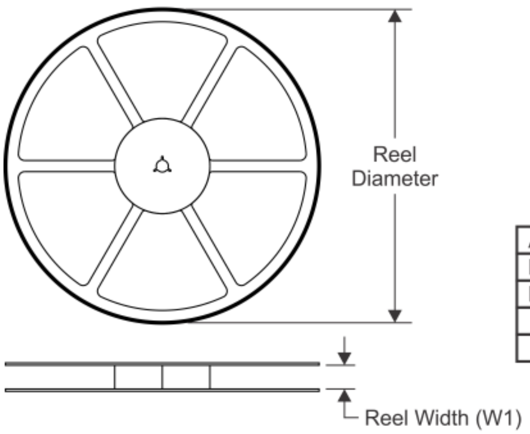
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

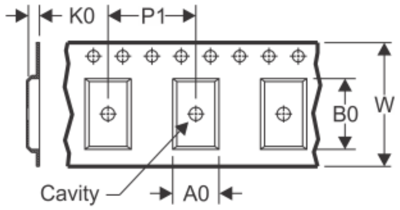
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

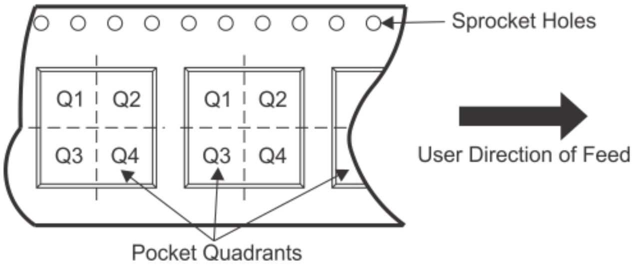


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

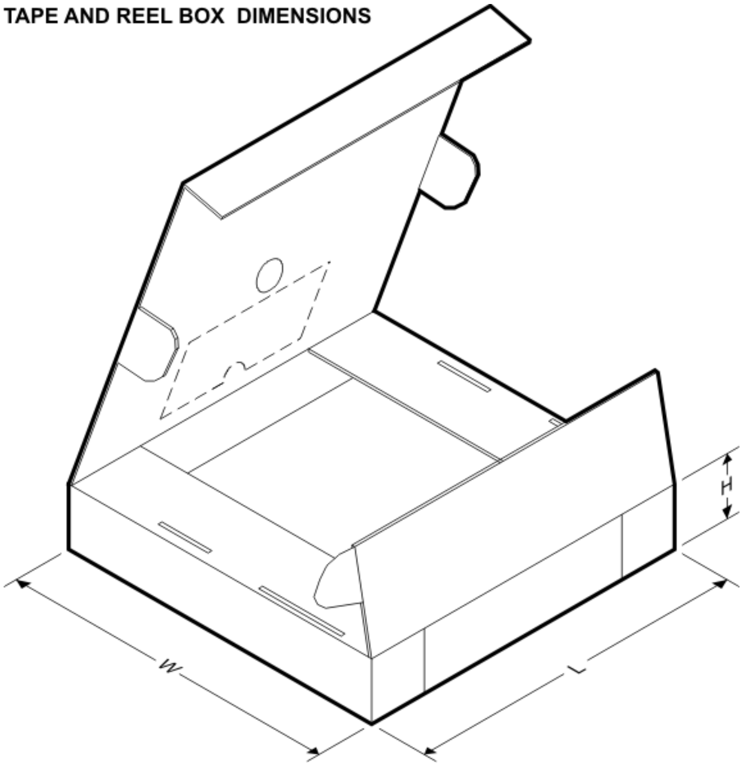
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8701ERGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
DRV8701ERGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
DRV8701PRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
DRV8701PRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

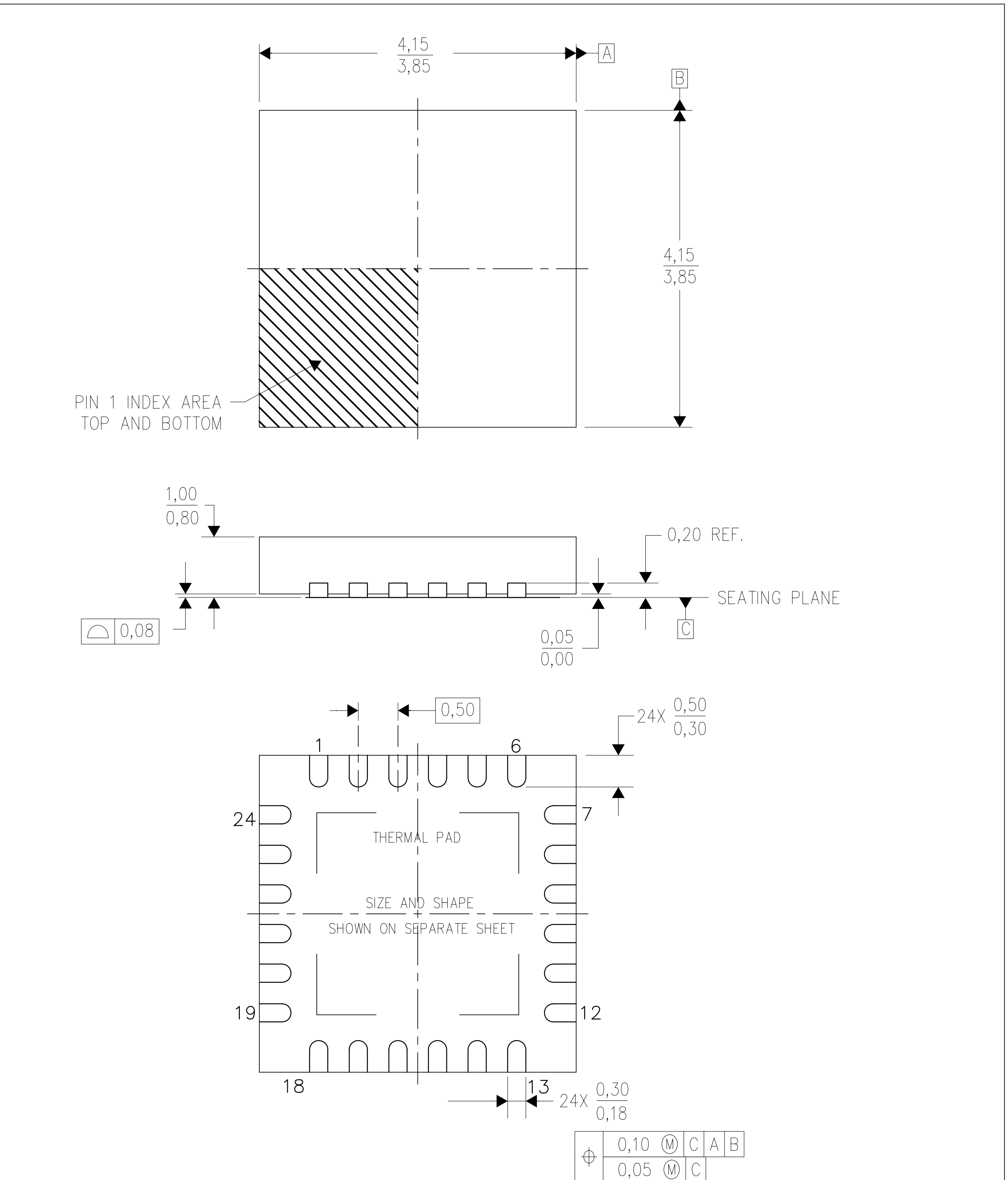
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8701ERGER	VQFN	RGE	24	3000	367.0	367.0	35.0
DRV8701ERGET	VQFN	RGE	24	250	210.0	185.0	35.0
DRV8701PRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
DRV8701PRGET	VQFN	RGE	24	250	210.0	185.0	35.0

RGE (S-PVQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD



4204104/G 07/11

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No—Leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO—220.

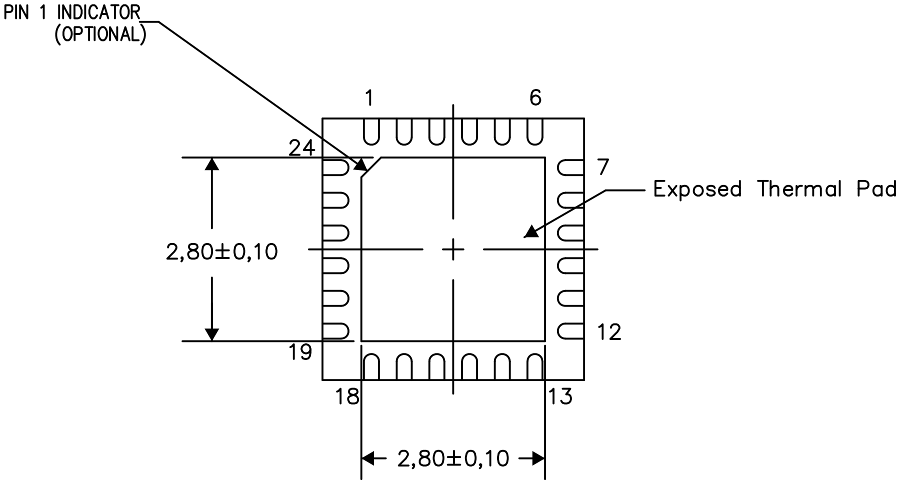
RGE (S-PVQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



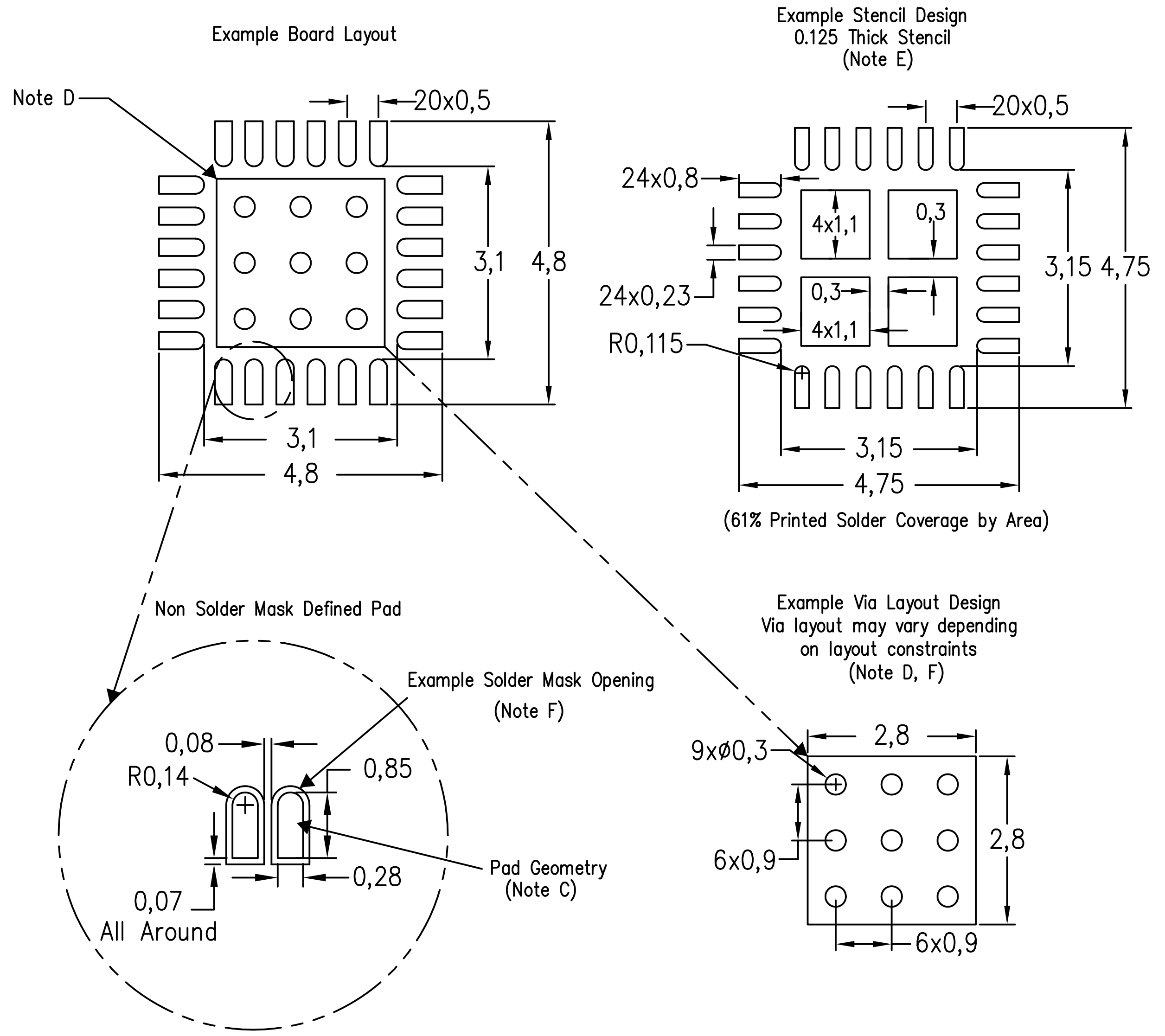
Bottom View

Exposed Thermal Pad Dimensions

4206344-6/AK 08/15

NOTES: A. All linear dimensions are in millimeters

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



4207991–4/U 05/15

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265