National Semiconductor

January 18, 2007
Rev – 1.1/CS
RoHS Compliant

Evaluation Board User's Guide

ADC121S705 12-Bit, 500 kSPS to 1 MSPS, Differential Input, Micro-Power Sampling A/D Converter

Table of Contents

1.0 Introduction

The ADC121S705EB/RoHS Design Kit (consisting of the ADC121S705 Evaluation Board and this User's Guide) is designed to ease evaluation and design-in of the National Semiconductor ADC121S705 12-bit Analog-to-Digital Converter, which can operate at speeds up to 1 MSPS.

The evaluation board can be used in either of two modes. In the Stand-Alone or Manual mode, suitable test equipment, such as a logic analyzer, can be used with the board to evaluate the ADC121S705's performance.

In the Computer or Automatic mode, data capture and evaluation is simplified by connecting this board to National Semiconductor's Data Capture Board (order number WAVEVSN BRD 4.1) which is connected to a personal computer through a USB port and is running WaveVision4 software. The WaveVision4 program can be downloaded from the web at http://www.national.com/adc.

The WaveVision4 software operates under Microsoft Windows. The signal at the Analog Input is digitized, captured, and displayed on a PC monitor in the time and frequency domain.

The software will perform an FFT on the captured data upon command. This FFT plot shows dynamic performance in the form of SNR, SINAD, THD, SFDR and ENOB. A histogram of the captured data is also available.

The differential signal at analog inputs J2 (ac-coupled) or J3 (dc-coupled) is digitized by U1, the ADC121S705.

The ADC121S705 uses an oscillator that is provided on this board by Y2 or is supplied at J6.

2.0 Board Assembly

The ADC121S705 evaluation board comes fully assembled and ready for use. Refer to the Bill of Materials for a description of components, to *Figure 1* for major component placement and to *Figure 2* for the Evaluation Board schematic.

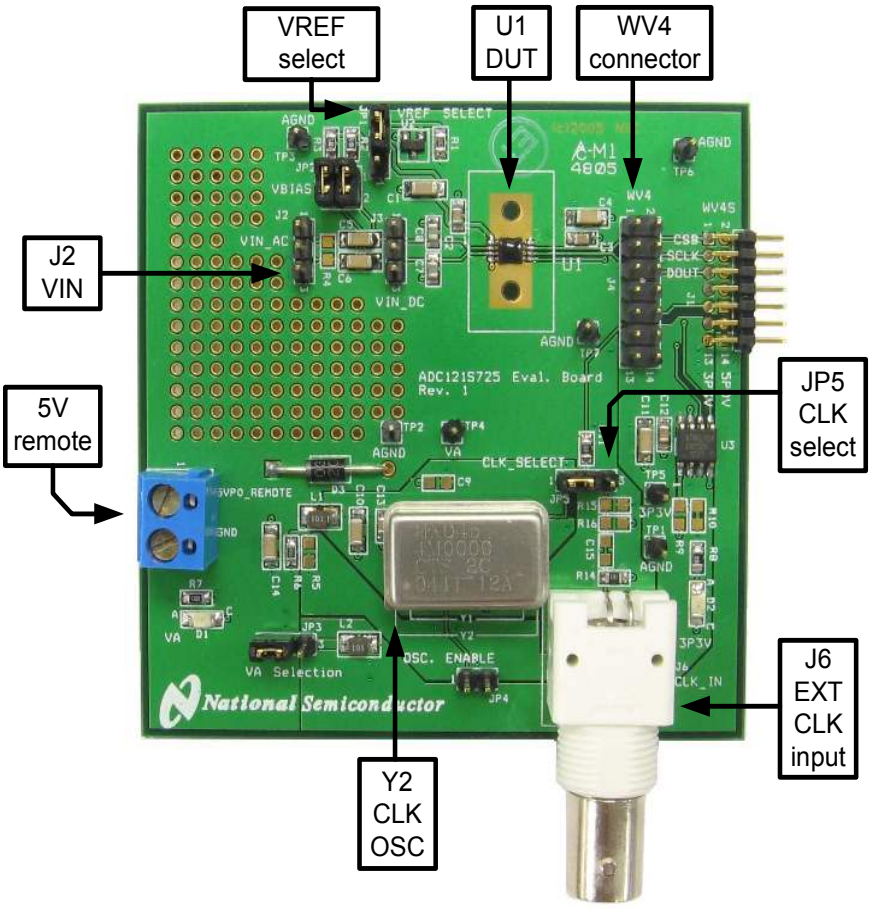


Figure 1 Component and Test Point Locations

3.0 Quick Start

The ADC121S705 evaluation board may be used in the Stand-Alone mode to capture data with a logic analyzer or third party equipment, or it may be used in the Computer Mode with a WaveVision4.1 Data Capture (WV) Board. In both cases, the data may be analyzed with the WaveVision4 software.

3.1 Stand Alone Mode

Refer to *Figure 1* for locations of test points and major components.

1. Remove the jumper from JP5 and the oscillator Y2 from its socket. The SPI interface signals (CSB and SCLK) will be driven directly at J4 (step 10). DOUT will also be monitored at J4. Frequently a Logic Analyzer with a built in pattern generator is used to drive CSB and SCLK while monitoring DOUT. It is necessary to remove Y2 because the presence of a second clock source could add noise to the conversion process.
2. Connect a clean analog (non-switching) +5V power source to Power Connector J5.
3. Short pins 1 & 2 of JP3 and turn on the power supply.
4. Dynamic differential signal sources centered around ground (ac-coupled) should be connected across pins 1 & 3 of J2. Pin 2 of J2 is ground. If the source has a 50 ohm output impedance, install a 51 ohm resistor at R4. Otherwise, the signal level will be twice as large as expected. To accurately evaluate the performance of the ADC121S705, the source must be better than 90dB THD.
5. Short pins 1 & 2 and pins 3 & 4 of JP2 to bias the input of the ADC121S705 at VREF. It is necessary to bias the inputs when driving the ADC from J2.
6. Differential DC sources or dynamic differential signal sources centered at a DC bias point should be connected across pins 1 & 3 of J3. Pin 2 of J3 is ground. Refer to the datasheet for acceptable common mode input voltages.
7. Remove the shorts across pins 1 & 2 and pins 3 & 4 of JP2 when driving the ADC input from J3. An external bias voltage for the ADC121S705 is not required under this circumstance.
8. Select the 2.5V shunt voltage reference as VREF by shorting pins 2 & 3 of JP1. This accomplishes two things at the same time. It provides a reference voltage of 2.5V for the ADC121S705 and it biases the input stage at 2.5V (sets the input's common mode voltage).
9. If it is desirable to provide an external reference voltage, the jumper must be removed from JP1 and pin 2 may be driven directly. Refer to the datasheet for acceptable common mode voltages ranges for specific reference voltages. Ideally the ADC121S705 is biased at half of the supply voltage, V_A.
10. Apply the signals to control the SPI interface at J4.

3.2 Computer Mode

Refer to *Figure 1* for locations of test points and major components.

1. Run the WaveVision4 program. Version 4.3 or higher is required to interface the WaveVision4.1 Data Capture (WV) board with the ADC121S705 evaluation board. While the program is loading, continue below.
2. Connect an analog +5V power source to power connector J1 on the WV board and turn on the power.
3. Connect a USB cable between the WV Board and the PC running the WaveVision4 program.
4. Connect J1 of the ADC121S705 board to J7 of the WV board.
5. Connect a separate, clean analog (non-switching) +5V power source to Power Connector J5 of the .
6. Short pins 1 & 2 of JP3 and turn on the power supply. *See Section 4.5 for detailed Power Supply Information.*
7. Install an appropriate crystal oscillator into socket Y2 and short pins 1 & 2 of JP5 (See *Table 1*). Alternatively, connect a signal generator with CMOS logic levels to BNC connector J6 and short pins 2 & 3 of JP5.
8. Perform steps 4 & 5 or 6 & 7 of section 3.1 to drive the analog inputs.
9. Perform step 8 or 9 of section 3.1 to select the reference voltage.
10. Refer to section 5.0 on Software Operation and Settings.

4.0 Functional Description

Table 1 describes the function of the various jumpers on the ADC121S705 evaluation board. The Evaluation Board schematic is shown in *Figure 2*.

Jumper	Pins 1 & 2	Pins 2 & 3
JP1	Select VA as VREF	Select 2.5V reg. as VREF
JP2	Short pins 1 & 2 and pins 3 & 4 to bias input pins at VREF	
JP3	Select 5P0V_REMOTE from J5	Select 5P0V from J1 (WV)
JP4	Enable OSC (not required)	
JP5	Select on-board clock OSC Y2	Select clock OSC at BNC J6

Table 1 Jumper Functions

4.1 Analog Input Signal

The input signal to be digitized should be applied across pins 1 & 3 of J2 or J3.

For input signals centered around ground, J2 should be utilized. Pin 2 of J2 is ground. Resistor R4 is a terminating resistor for the input source. Since all sources do not have the same output impedance, R4 is not stuffed. However, it is recommended that it is stuffed by the end user with the appropriate value that matches the source.

The DC biasing for inputs applied to J2 is supplied through JP2. Short pins 1 & 2 and 3 & 4 of JP2 to properly bias the input to VREF.

If it is desired to digitize a differential DC voltage or a dynamic signal that is already properly biased for the ADC121S705, apply the signal to be digitized across pins 1 & 3 of J3. Pin 2 of J3 is ground. When applying the input at J3, all shorts on JP2 need to be removed.

If V_A is selected as the reference voltage, the input signal must be applied at J3 and thus requires proper dc-biasing. Under this circumstance, JP2 is no longer capable of providing a proper dc-bias voltage for the input to the ADC121S705 since it is directly connected to V_A through R2 and R3. If the input signal is not properly biased, the side of R2 and R3 that connects to VREF would need to be lifted and driven with a voltage of V_A / 2. This allows the maximum voltage swing at +IN and –IN.

Dynamic input signals should be applied through a bandpass filter to eliminate the noise and harmonics commonly associated with signal sources. To accurately evaluate the performance of the ADC121S705, the source must be better than -90dBc THD

4.2 ADC Reference Circuitry

This evaluation board includes the option of selecting a fixed 2.5V shunt voltage reference or V_A as the reference voltage. Select the 2.5V reference as VREF by shorting pins 2 & 3 of JP1 or select V_A as VREF by shorting pins 1 & 2 of JP1. If it is desirable to provide an external reference voltage, the jumper must be removed from JP1 and pin 2 may be driven directly.

If it is desirable to change the LM4040DIM3-2.5 to an LM4040 with a different voltage, carefully change it and adjust the value of R1 to limit the current through the LM4040.

4.3 SPI Interface

4.3.1 ADC Clock (SCLK)

The crystal-based oscillator provided on the evaluation board is selected by shorting pins 1 & 2 of JP5. It is best to remove any external signal generator from J6 when using this oscillator to reduce any unnecessary noise.

This board will also accept a clock signal from an external source by connecting that source to BNC J6 and shorting pins 2 & 3 of JP5. The input applied at J6 is 51 ohm terminated by R14. The external clock signal must meet CMOS input requirements. If the external source is an ac-source that is centered around ground, the short across C15 can be cut and C15 should be populated with a 0.1uF capacitor. It is also necessary to populate R15 and R16 with 5.1k ohm resistors. To reduce any unnecessary noise, it is best to remove the oscillator at Y2 when using an external clock source.

Regardless of the clock source selected by JP5, the clock signal is designed to be routed off the ADC121S705 evaluation board to the WV board. This assumes a “computer mode” operation of the evaluation board. For applications utilizing the evaluation board in manual mode, the clock is applied directly at J4.

4.3.2 Digital Data Output (DOUT)

The DOUT pin from this board may be monitored at J1 or J4. In “computer mode” DOUT is monitored by the WV board. In “manual mode” DOUT should be monitored directly at J4. The

signal level for DOUT is CMOS compatible. See the ADC121S705 datasheet for logic output levels.

4.3.3 Chip Select Bar (CSB)

The CSB pin may be monitored at J1 or J4. In "computer mode" CSB is provided by the WV board. In "manual mode" CSB should be driven directly at J4. The signal level for CSB needs to be CMOS compatible. See the ADC121S705 datasheet for logic threshold limits.

4.4 Power Supply Connections

In "computer and manual mode", the remote 5P0V voltage needs to be set between +4.5V and +5.5V.

When operating in "computer mode", the supply voltage for VA can be applied remotely at J5 or is supplied directly by the WV board through J1. The remote 5P0V voltage is selected by shorting pins 1 & 2 on JP3. While the 5P0V from the WV board is selected by shorting pins 2 & 3 on JP3. For best performance from the ADC121S705, a remote supply voltage should be applied to J5. The 3P3V voltage is always obtained through J1 from the WV board/

When operating in "manual mode", only voltage 5P0V needs to be applied to J5 and pins 1 & 2 on JP3 need to be shorted.

5.0 Software Operation and Settings

The WaveVision4 software is included with the WV board and the latest version can be downloaded for free from National's web site at http://www.national.com/adc. To install this software, follow the procedure in the WaveVision4.1 Board User's Guide. Once the software is installed, run it and set it up as follows:

1. Connect the WV board to the host computer with a USB cable.
2. From the WaveVision main menu, go to Settings, then Board Settings and do the following:

   Select the following from the WaveVision4 main menu:
   - WaveVision 4.0 (USB)
   - # of Samples: 2K to 32K, as desired
3. Apply power as specified in Section 4.5, click on the **"Test"** button and await the firmware to download.
4. Click on the **"Accept"** button.
5. After the steps outlined in Section 3.2 are completed, click on 'Acquire' then 'Samples' from the Main Menu (you can also press the *F1* shortcut key). If a dialog box opens, select 'Discard' or press the *Escape* key to start collecting new, updated samples.

A plot of the selected number of samples will be displayed. Make sure there is no clipping of data samples. The samples may be further analyzed by clicking on the magnifying glass icon, then clicking and dragging across a specific area of the plot for better data inspection. See the WaveVision4 Board User's Guide for details.

To view an FFT of the data captured, click on the 'FFT' tab. This plot may be zoomed in on like the data plot. A display of dynamic performance parameters in the form of SINAD, SNR, THD, SFDR and ENOB will be displayed at the top right hand corner of the FFT plot.

Acquired data may be saved to a file. Plots may also be exported as graphics. See the Data Capture Board User's Guide for details.

6.0 Evaluation Board Specifications

Board Size:	3.0" x 3.0" (7.6 cm x 7.6 cm)	
Power Requirements	Min: +4.5V, 100mA	Max: +5.5V, 100 mA
Clock Frequency Range:	800 kHz to 4.0 MHz	
Analog Input	0V to 2VREF	

7.0 Test Points, Connectors, and Jumpers

Test Points on the ADC121S705 Evaluation Board

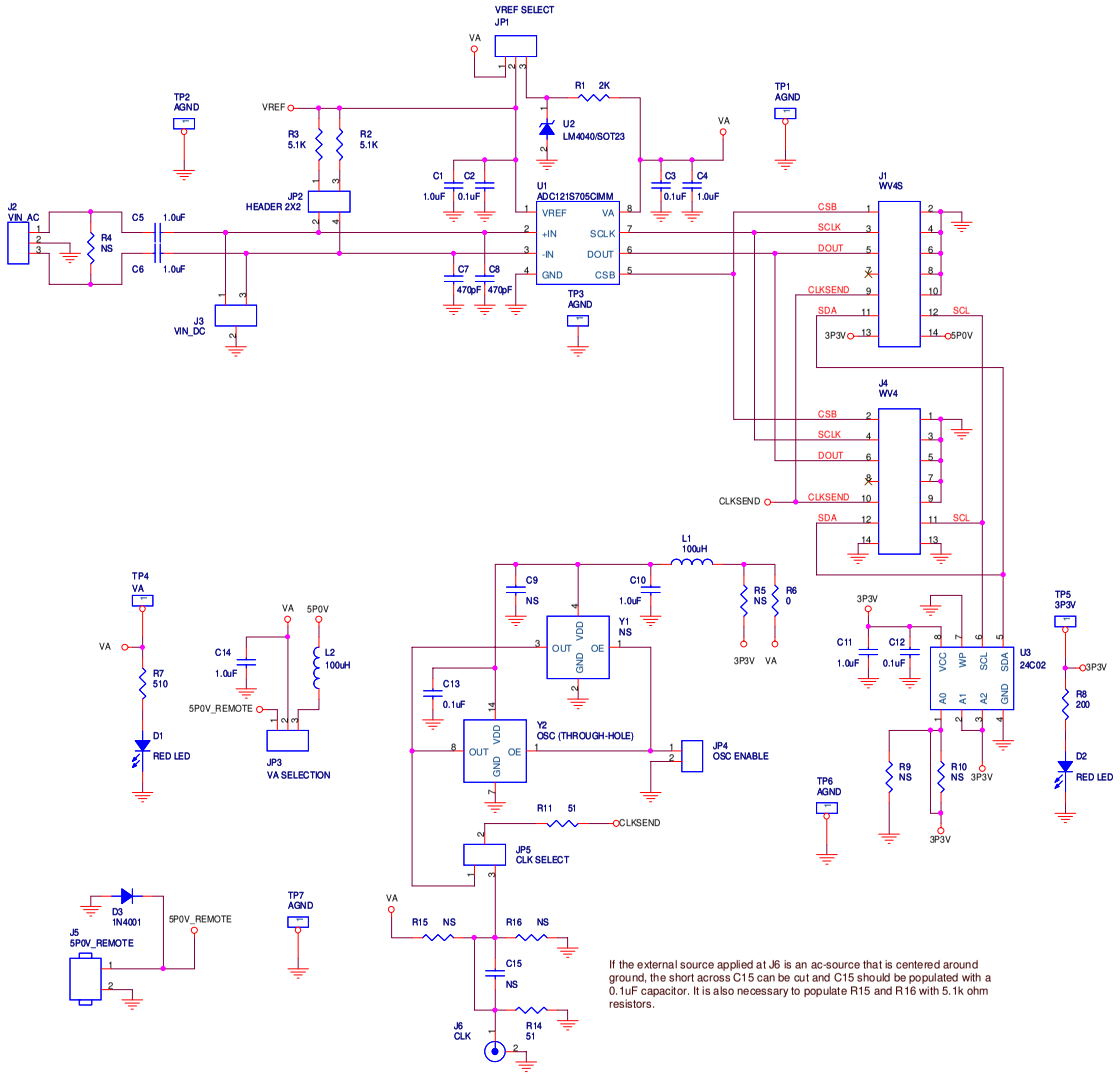
TP1: AGND	Ground. Located at the bottom right area of the board.
TP2: AGND	Ground. Located at the center of the board.
TP3: AGND	Ground. Located at the top left area of the board.
TP4: VA	VA test point. Located at the center of the board.
TP5: 3P3V	3.3V test point. Located at the middle right area of the board.
TP6: AGND	Ground. Located at the top right corner of the board.
TP7: AGND	Ground. Located in the middle right area of the board.

Connectors on the ADC121S705 Evaluation Board

J1: WV4S	14 pin dual row right angle male header: Connects to WV4.1 board.
J2: VIN_AC	Three pin male header: Differential AC input.
J3: VIN_DC	Three pin male header: Differential DC input.
J4: WV4	14 pin dual row male header: Connects to WV4.0 board.
J5: 5P0V_REMOTE	Terminal Block: Power connector for 5P0V.
J6: CLK_IN	BNC Connector: External clock input.

Selection Jumpers on the ADC121S705 Evaluation Board (Refer to Table 1 in Section 4.0 for configuration details)

JP1: VREF SELECT	Selects reference source for VREF.
JP2: VBIAS	Provides DC bias for analog inputs.
JP3: VA Selection	Selects source of voltage for VA.
JP4: OSC ENABLE	Not required for OSC provided with evaluation board.
JP5: CLK_SELECT	Selects clock source (on-board oscillator or external source).



If the external source applied at J6 is an ac-source that is centered around ground, the short across C15 can be cut and C15 should be populated with a 0.1uF capacitor. It is also necessary to populate R15 and R16 with 5.1k ohm resistors.

Title	ADC121S705 Evaluation Board	
Size C	Document Number 670012728-100A	Rev 1.0
Date: Tuesday, November 29, 2005	Sheet 1 of 1	

ADC121S705 Evaluation Board Revised: Thursday, January 17, 2007

870012728-100A Revision: 1.0

Bill Of Materials

Item	Quantity	Reference	Description	Value	Rating	Pacakage	Critical	Source	Source Part #
1	7	C1,C4,C5,C6,C10,C11,C14	CAP	1.0uF	50V	sm/c_1206			
2	4	C2,C3,C12,C13	CAP	0.1uF	50V	sm/c_0805			
3	2	C8,C7	CAP	470pF	50V	sm/c_0805			
4	2	C15,C9	CAP	NS	50V	sm/c_0805			
5	2	D2,D1	LED	RED LED		sm/led_21		Digikey	516-1440-1-ND
6	1	D3	DIO	1N4001 or IN4003		DAX2/DO41		Digikey	1N4001GICT-ND
7	1	JP1	HEAD	VREF SELECT		header		Digikey	A26513-40-ND
8	1	JP2	HEAD	HEADER 2X2		header		Digikey	A26529-40-ND
9	1	JP3	HEAD	VA SELECTION		header		Digikey	A26513-40-ND
10	1	JP4	HEAD	OSC ENABLE		header		Digikey	A26513-40-ND
11	1	JP5	HEAD	CLK SELECT		header		Digikey	A26513-40-ND
12	1	J1	HEAD	WV4S		rt angle header		Digikey	S2200-07-ND
13	1	J2	HEAD	VIN_AC		header		Digikey	A26513-40-ND
14	1	J3	HEAD	VIN_DC		header		Digikey	A26513-40-ND
15	1	J4	HEAD	WV4		header		Digikey	A26529-40-ND
16	1	J5	TERM	5P0V_REMOTE		term_block		Digikey	ED1609-ND
17	1	J6	BNC	CLK		BNC		Digikey	ARF1177-ND
18	2	L1,L2	IND	100uH		sm/l_1210		Digikey	445-1155-1-ND
19	1	R1	RES	2K		sm/r_0805			
20	2	R3,R2	RES	5.1K		sm/r_0805			
21	6	R4,R5,R9,R10,R15,R16	RES	NS		sm/r_0805			
22	1	R6	RES	0		sm/r_0805			
23	1	R7	RES	510		sm/r_0805			
24	1	R8	RES	200		sm/r_0805			
25	2	R14,R11	RES	51		sm/r_0805			
26	5	TP1,TP2,TP3,TP6,TP7	TP	AGND		header		Digikey	A26513-40-ND
27	1	TP4	TP	VA		header		Digikey	A26513-40-ND
28	1	TP5	TP	3P3V		header		Digikey	A26513-40-ND
29	1	U1	IC	ADC121S705CIMM		MSOP8			
30	1	U2	REF	LM4040/SOT23		sm/SOT23		Digikey	LM4040DIM3-2.5CT-ND
31	1	U3	EEPROM	24C02		EEPROM			
32	1	Y2A	OSC	16.0MHz OSC		OSC			
33	1	Y2B	SOCK	SOCKET		OSC_socket		Digikey	A462-ND
34	1	PCB	PCB	ADC121S725		Eval Board		Adv Cir	121S725_r1
35	5	2-pin jumpers	SHUNT						
36	4	Rubber Feet	BUMP						

BY USING THIS PRODUCT, YOU ARE AGREEING TO BE BOUND BY THE TERMS AND CONDITIONS OF NATIONAL SEMICONDUCTOR'S END USER LICENSE AGREEMENT. DO NOT USE THIS PRODUCT UNTIL YOU HAVE READ AND AGREED TO THE TERMS AND CONDITIONS OF THAT AGREEMENT. IF YOU DO NOT AGREE WITH THEM, CONTACT THE VENDOR WITHIN TEN (10) DAYS OF RECEIPT FOR INSTRUCTIONS ON RETURN OF THE UNUSED PRODUCT FOR A REFUND OF THE PURCHASE PRICE PAID, IF ANY.

The ADC121S705 Evaluation Board is intended for product evaluation purposes only and is not intended for resale to end consumers, is not authorized for such use and is not designed for compliance with European EMC Directive 89/336/EEC, or for compliance with any other electromagnetic compatibility requirements.

National Semiconductor Corporation does not assume any responsibility for use of any circuitry or software supplied or described. No circuit patent licenses are implied.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation Americas Tel: 1-800-272-9959 Fax: 1-800-737-7018 Email: support@nsc.com	**National Semiconductor Europe** Fax: +49 (0) 1 80-530 85 86 Email: europe.support@nsc.com Deutsch Tel: +49 (0) 699508 6208 English Tel: +49 (0) 870 24 0 2171 French Tel: +49 (0) 141 91 8790	**National Semiconductor Asia Pacific Customer Response Group** Tel: 65-2544466 Fax: 65-2504466 Email:sea.support@nsc.com	**National Semiconductor Japan Ltd.** Tel: 81-3-5639-7560 Fax: 81-3-5639-7507
www.national.com			

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		
	TI E2E Community Home Page		e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265