

FEATURES

High Speed

- 50 MHz Unity Gain Stable Operation
- 300 V/ms Slew Rate
- 120 ns Settling Time

Drives Unlimited Capacitive Loads

Excellent Video Performance

- 0.04% Differential Gain @ 4.4 MHz
- 0.198 Differential Phase @ 4.4 MHz

Good DC Performance

- 2 mV max Input Offset Voltage
- 15 mV/8C Input Offset Voltage Drift
- Available in Tape and Reel in Accordance with EIA-481A Standard

Low Power

- Only 10 mA Total Supply Current for Both Amplifiers
- ± 5 V to ± 15 V Supplies

PRODUCT DESCRIPTION

The AD827 is a dual version of Analog Devices' industry-standard AD847 op amp. Like the AD847, it provides high speed, low power performance at low cost. The AD827 achieves a 300 V/ μ s slew rate and 50 MHz unity-gain bandwidth while consuming only 100 mW when operating from ± 5 volt power supplies. Performance is specified for operation using ± 5 V to ± 15 V power supplies.

The AD827 offers an open-loop gain of 3,500 V/V into 500 Ω loads. It also features a low input voltage noise of $15 \text{ nV}/\sqrt{\text{Hz}}$, and a low input offset voltage of 2 mV maximum. Common-mode rejection ratio is a minimum of 80 dB. Power supply rejection ratio is maintained at better than 20 dB with input frequencies as high as 1 MHz, thus minimizing noise feedthrough from switching power supplies.

The AD827 is also ideal for use in demanding video applications, driving coaxial cables with less than 0.04% differential gain and 0.19° differential phase errors for 643 mV p-p into a 75 Ω reverse terminated cable.

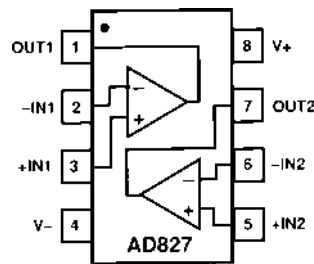
The AD827 is also useful in multichannel, high speed data conversion systems where its fast (120 ns to 0.1%) settling time is of importance. In such applications, the AD827 serves as an input buffer for 8-bit to 10-bit A/D converters and as an output amplifier for high speed D/A converters.

REV. C

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CONNECTION DIAGRAMS

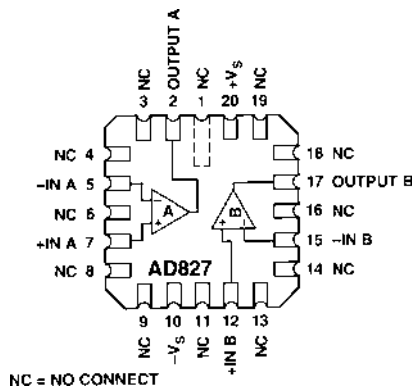
8-Lead Plastic (N) and Cerdip (Q) Packages



16-Lead Small Outline (R) Package



20-Lead LCC (E) Package



APPLICATION HIGHLIGHTS

1. Performance is fully specified for operation using ± 5 V to ± 15 V supplies.
2. A 0.04% differential gain and 0.19° differential phase error at the 4.4 MHz color subcarrier frequency, together with its low cost, make it ideal for many video applications.
3. The AD827 can drive unlimited capacitive loads, while its 30 mA output current allows 50 Ω and 75 Ω reverse-terminated loads to be driven.
4. The AD827's 50 MHz unity-gain bandwidth makes it an ideal candidate for multistage active filters.
5. The AD827 is available in 8-lead plastic mini-DIP and cerdip, 20-lead LCC, and 16-lead SOIC packages. Chips and MIL-STD-883B processing are also available.

AD827—SPECIFICATIONS (@ $T_A = +25^\circ\text{C}$, unless otherwise noted.)

Model	Conditions	V_S	AD827J			AD827A/S			Unit
			Min	Typ	Max	Min	Typ	Max	
DC PERFORMANCE									
Input Offset Voltage ¹	T_{MIN} to T_{MAX}	$\pm 5\text{ V}$	0.5	2		0.3	2	mV	
		$\pm 15\text{ V}$		3.5		4		mV	
Offset Voltage Drift	T_{MIN} to T_{MAX}	$\pm 5\text{ V}$ to $\pm 15\text{ V}$	15			15		$\mu\text{V}/^\circ\text{C}$	
		$\pm 5\text{ V}$ to $\pm 15\text{ V}$	3.3	7		3.3	7	μA	
Input Bias Current	T_{MIN} to T_{MAX}	$\pm 5\text{ V}$ to $\pm 15\text{ V}$		8.2			9.5	μA	
		$\pm 5\text{ V}$ to $\pm 15\text{ V}$	50	300		50	300	nA	
Input Offset Current	T_{MIN} to T_{MAX}	$\pm 5\text{ V}$ to $\pm 15\text{ V}$		400			400	nA	
		$\pm 5\text{ V}$ to $\pm 15\text{ V}$	0.5			0.5		$\text{nA}/^\circ\text{C}$	
Common-Mode Rejection Ratio	$V_{\text{CM}} = \pm 2.5\text{ V}$ $V_{\text{CM}} = \pm 12\text{ V}$ T_{MIN} to T_{MAX}	$\pm 5\text{ V}$	78	95		80	95	dB	
		$\pm 15\text{ V}$	78	95		80	95	dB	
		$\pm 5\text{ V}$ to $\pm 15\text{ V}$	75			75		dB	
Power Supply Rejection Ratio	T_{MIN} to T_{MAX}	$\pm 5\text{ V}$ to $\pm 15\text{ V}$	75	86		75	86	dB	
		$\pm 5\text{ V}$ to $\pm 15\text{ V}$	72			72		dB	
Open-Loop Gain	$V_O = \pm 2.5\text{ V}$ $R_{\text{LOAD}} = 500\ \Omega$ T_{MIN} to T_{MAX} $R_{\text{LOAD}} = 150\ \Omega$ $V_{\text{OUT}} = \pm 10\text{ V}$ $R_{\text{LOAD}} = 1\ \text{k}\Omega$ T_{MIN} to T_{MAX}	$\pm 5\text{ V}$							
		$\pm 5\text{ V}$	2	3.5		2	3.5	V/mV	
		$\pm 5\text{ V}$	1			1		V/mV	
		$\pm 15\text{ V}$		1.6			1.6	V/mV	
		$\pm 15\text{ V}$	3	5.5		3	5.5	V/mV	
		$\pm 15\text{ V}$	1.5			1.5		V/mV	
MATCHING CHARACTERISTICS									
Input Offset Voltage Crosstalk	$f = 5\text{ MHz}$	$\pm 5\text{ V}$		0.4			0.2	mV	
		$\pm 5\text{ V}$		85			85	dB	
DYNAMIC PERFORMANCE									
Unity-Gain Bandwidth		$\pm 5\text{ V}$		35			35	MHz	
		$\pm 15\text{ V}$		50			50	MHz	
Full Power Bandwidth ²	$V_O = 5\text{ V p-p}$, $R_{\text{LOAD}} = 500\ \Omega$ $V_O = 20\text{ V p-p}$, $R_{\text{LOAD}} = 1\ \text{k}\Omega$	$\pm 5\text{ V}$		12.7			12.7	MHz	
		$\pm 15\text{ V}$		4.7			4.7	MHz	
Slew Rate ³	$R_{\text{LOAD}} = 500\ \Omega$ $R_{\text{LOAD}} = 1\ \text{k}\Omega$	$\pm 5\text{ V}$		200			200	$\text{V}/\mu\text{s}$	
		$\pm 15\text{ V}$		300			300	$\text{V}/\mu\text{s}$	
Settling Time to 0.1%	$A_V = -1$ -2.5 V to $+2.5\text{ V}$ -5 V to $+5\text{ V}$	$\pm 5\text{ V}$		65			65	ns	
		$\pm 15\text{ V}$		120			120	ns	
Phase Margin	$C_{\text{LOAD}} = 10\ \text{pF}$ $R_{\text{LOAD}} = 1\ \text{k}\Omega$	$\pm 15\text{ V}$		50			50	Degrees	
		$\pm 15\text{ V}$		0.04			0.04	%	
Differential Gain Error	$f = 4.4\text{ MHz}$	$\pm 15\text{ V}$		0.19			0.19	Degrees	
Differential Phase Error	$f = 4.4\text{ MHz}$	$\pm 15\text{ V}$		15			15	$\text{nV}/\sqrt{\text{Hz}}$	
Input Voltage Noise	$f = 10\text{ kHz}$	$\pm 15\text{ V}$		1.5			1.5	$\text{pA}/\sqrt{\text{Hz}}$	
Input Current Noise	$f = 10\text{ kHz}$	$\pm 15\text{ V}$							
Input Common-Mode Voltage Range		$\pm 5\text{ V}$		+4.3			+4.3	V	
		$\pm 5\text{ V}$		-3.4			-3.4	V	
		$\pm 15\text{ V}$		+14.3			+14.3	V	
		$\pm 15\text{ V}$		-13.4			-13.4	V	
Output Voltage Swing	$R_{\text{LOAD}} = 500\ \Omega$ $R_{\text{LOAD}} = 150\ \Omega$ $R_{\text{LOAD}} = 1\ \text{k}\Omega$ $R_{\text{LOAD}} = 500\ \Omega$	$\pm 5\text{ V}$	3.0	3.6		3.0	3.6	$\pm\text{V}$	
		$\pm 5\text{ V}$	2.5	3.0		2.5	3.0	$\pm\text{V}$	
		$\pm 15\text{ V}$	12	13.3		12	13.3	$\pm\text{V}$	
		$\pm 15\text{ V}$	10	12.2		10	12.2	$\pm\text{V}$	
Short-Circuit Current Limit		$\pm 5\text{ V}$ to $\pm 15\text{ V}$		32			32	mA	
INPUT CHARACTERISTICS									
Input Resistance				300			300	$\text{k}\Omega$	
Input Capacitance				1.5			1.5	pF	

Model	Conditions	V _S	AD827J			AD827A/S			Unit
			Min	Typ	Max	Min	Typ	Max	
OUTPUT RESISTANCE	Open Loop		15			15			Ω
POWER SUPPLY									
Operating Range		±5 V	±4.5		±18	±4.5		±18	V
Quiescent Current	T _{MIN} to T _{MAX}			10	13		10	13	mA
		±15 V			16			16.5/17.5	mA
	T _{MIN} to T _{MAX}			10.5	13.5		10.5	13.5	mA
					16.5			17/18	mA
TRANSISTOR COUNT			92			92			

NOTES

¹ Offset voltage for the AD827 is guaranteed after power is applied and the device is fully warmed up. All other specifications are measured using high speed test equipment, approximately 1 second after power is applied.

² Full Power Bandwidth = Slew Rate/2 π V_{PEAK}.

³ Gain = +1, rising edge.

All min and max specifications are guaranteed.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS¹

Supply Voltage ±18 V

Internal Power Dissipation²

 Plastic (N) Package (Derate at 10 mW/°C) 1.5 W

 Cerdip (Q) Package (Derate at 8.7 mW/°C) 1.3 W

 Small Outline (R) Package (Derate at 10 mW/°C) ... 1.5 W

 LCC (E) Package (Derate at 6.7 mW/°C) 1.0 W

Input Common-Mode Voltage ±V_S

Differential Input Voltage 6 V

Output Short Circuit Duration³ Indefinite

Storage Temperature Range (N, R) -65°C to +125°C

Storage Temperature Range (Q) -65°C to +150°C

Operating Temperature Range

 AD827J 0°C to 70°C

 AD827A -40°C to +85°C

 AD827S -55°C to +125°C

Lead Temperature Range

 (Soldering to 60 sec) 300°C

NOTES

¹ Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

² Maximum internal power dissipation is specified so that T_J does not exceed 175°C at an ambient temperature of 25°C.

Thermal Characteristics:

MiniDIP: θ_{JA} = 100°C/W; θ_{JC} = 33°C/W

Cerdip: θ_{JA} = 110°C/W; θ_{JC} = 30°C/W

16-Lead Small Outline Package: θ_{JA} = 100°C/W

20-Lead LCC: θ_{JA} = 150°C/W; θ_{JC} = 35°C/W

³ Indefinite short circuit duration is only permissible as long as the absolute maximum power rating is not exceeded.

ORDERING GUIDE

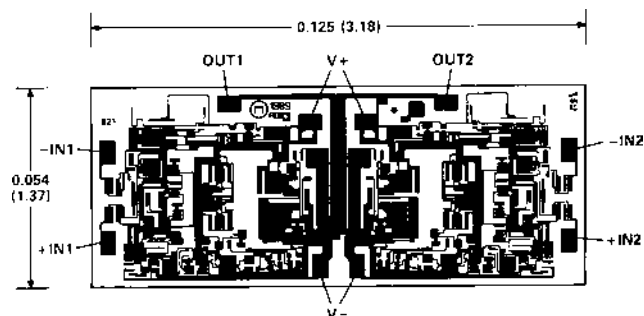
Model	Temperature Range	Package Description	Package Option
AD827JN	0°C to +70°C	8-Lead Plastic DIP	N-8
AD827JR	0°C to +70°C	16-Lead Plastic SO	R-16
AD827AQ	-40°C to +85°C	8-Lead Cerdip	Q-8
AD827SQ	-55°C to +125°C	8-Lead Cerdip	Q-8
AD827SQ/883B	-55°C to +125°C	8-Lead Cerdip	Q-8
5962-9211701MPA	-55°C to +125°C	8-Lead Cerdip	Q-8
AD827SE/883B	-55°C to +125°C	20-Lead LCC	E-20A
5962-9211701M2A	-55°C to +125°C	20-Lead LCC	E-20A
AD827JR-REEL	0°C to +70°C	Tape & Reel	
AD827JChips	0°C to +70°C	Die	
AD827SChips	-55°C to +125°C	Die	

METALLIZATION PHOTOGRAPH

Contact factory for latest dimensions.

Dimensions shown in inches and (mm).

Substrate is connected to V+.



AD827—Typical Performance Characteristics (@ +25°C & ±15 V, unless otherwise noted)

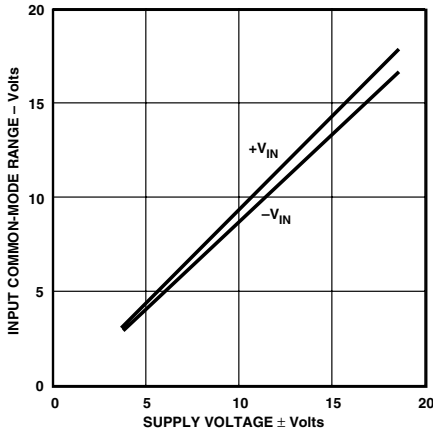


Figure 1. Input Common-Mode Range vs. Supply Voltage

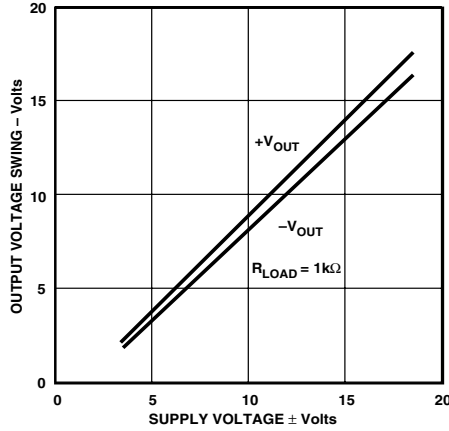


Figure 2. Output Voltage Swing vs. Supply Voltage

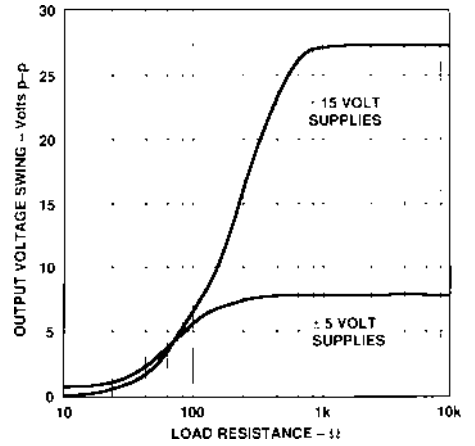


Figure 3. Output Voltage Swing vs. Load Resistance

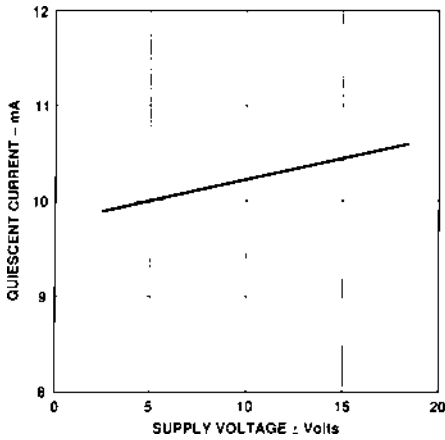


Figure 4. Quiescent Current vs. Supply Voltage



Figure 5. Input Bias Current vs. Temperature

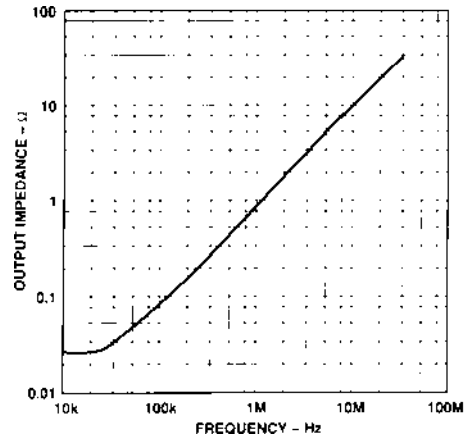


Figure 6. Closed-Loop Output Impedance vs. Frequency, Gain = +1

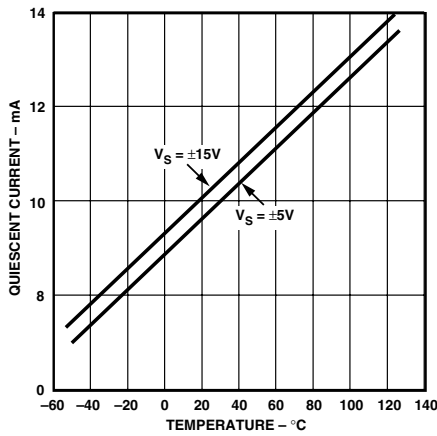


Figure 7. Quiescent Current vs. Temperature



Figure 8. Short-Circuit Current Limit vs. Temperature

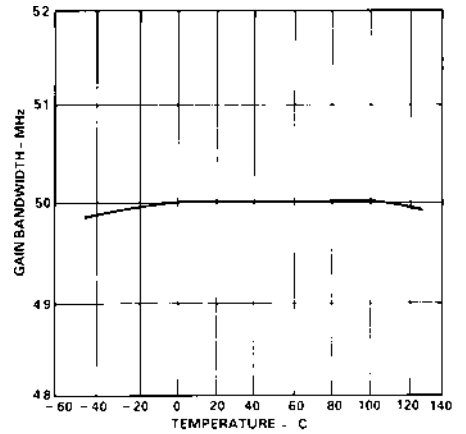


Figure 9. Gain Bandwidth vs. Temperature



Figure 10. Open-Loop Gain and Phase Margin vs. Frequency

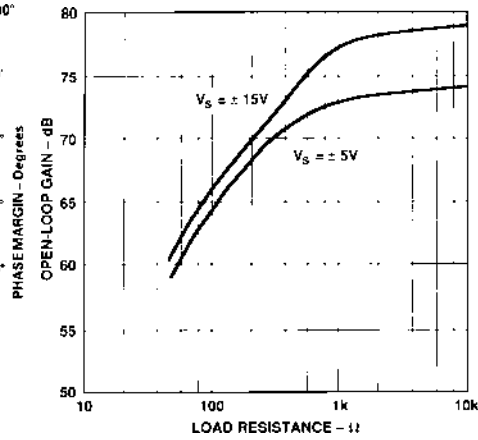


Figure 11. Open-Loop Gain vs. Load Resistance



Figure 12. Power Supply Rejection Ratio vs. Frequency



Figure 13. Common-Mode Rejection Ratio vs. Frequency

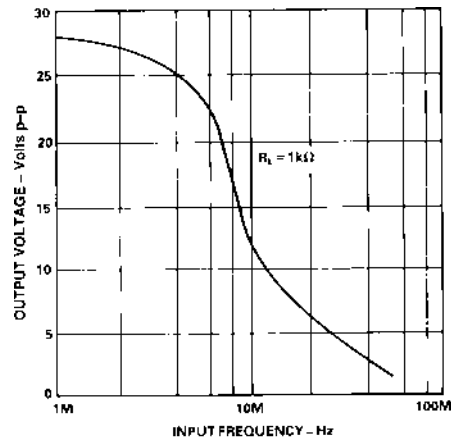


Figure 14. Large Signal Frequency Response



Figure 15. Output Swing and Error vs. Settling Time

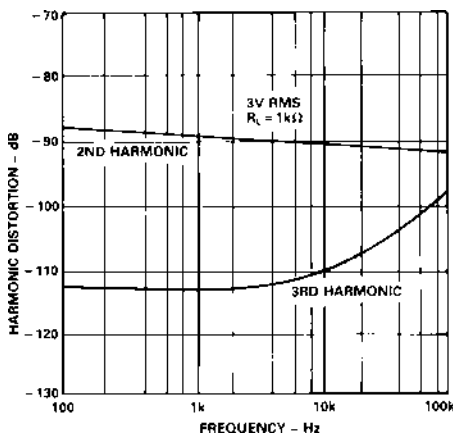


Figure 16. Harmonic Distortion vs. Frequency

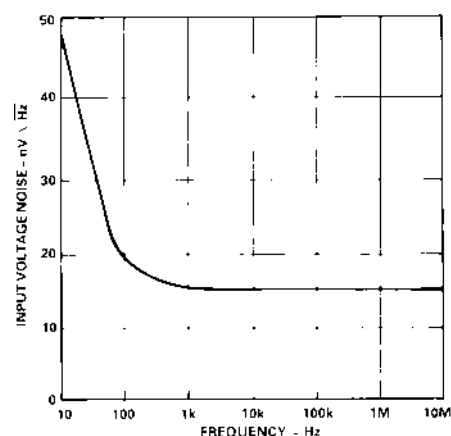


Figure 17. Input Voltage Noise Spectral Density

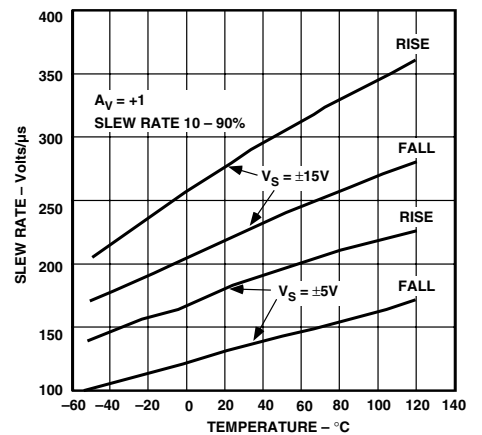


Figure 18. Slew Rate vs. Temperature

AD827

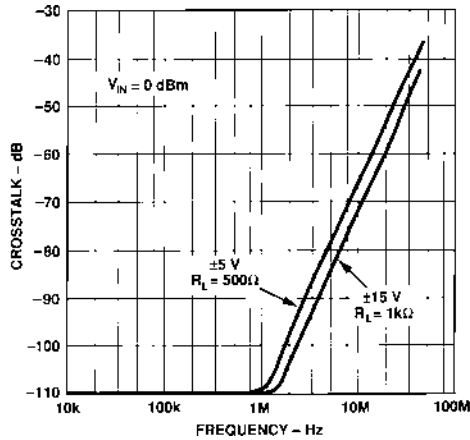
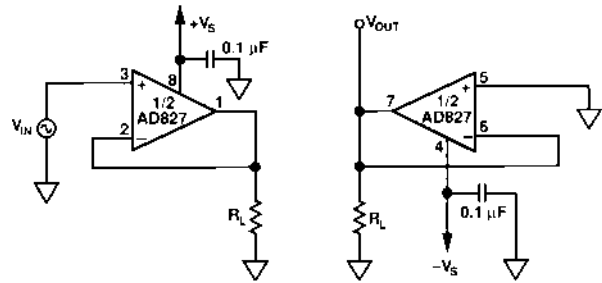


Figure 19. Crosstalk vs. Frequency



$R_L = 500\Omega$ FOR $\pm V_S = 5V$, $1k\Omega$ FOR $\pm V_S = 15V$
USE GROUND PLANE
PINOUT SHOWN IS FOR MINIDIP PACKAGE

Figure 20. Crosstalk Test Circuit

INPUT PROTECTION PRECAUTIONS

An input resistor (resistor R_{IN} of Figure 21a) is recommended in circuits where the input common-mode voltage to the AD827 may exceed (on a transient basis) the positive supply voltage. This resistor provides protection for the input transistors by limiting the maximum current that can be forced into their bases.

For high performance circuits, it is recommended that a second resistor (R_B in Figures 21a and 22a) be used to reduce bias-current errors by matching the impedance at each input. This resistor reduces the error caused by offset voltages by more than an order of magnitude.

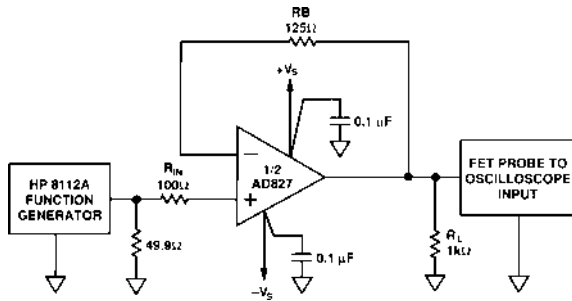


Figure 21a. Follower Connection

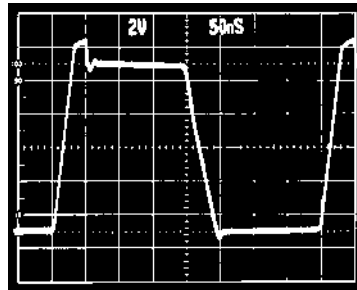


Figure 21b. Follower Large Signal Pulse Response

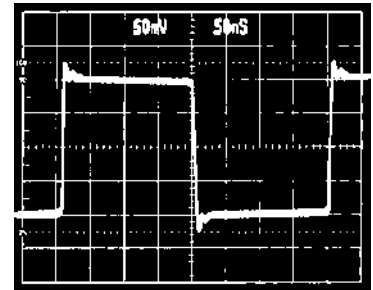


Figure 21c. Follower Small Signal Pulse Response

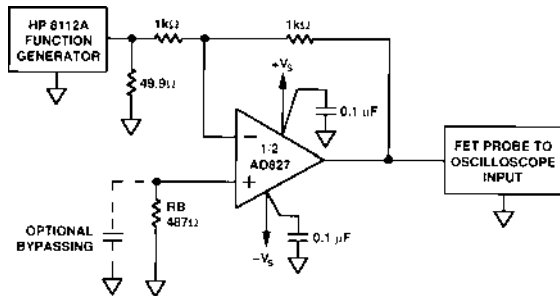


Figure 22a. Inverter Connection

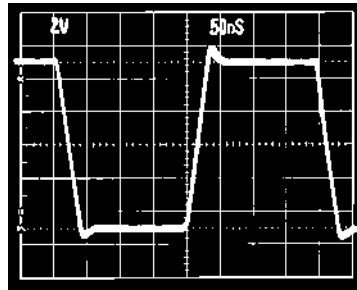


Figure 22b. Inverter Large Signal Pulse Response

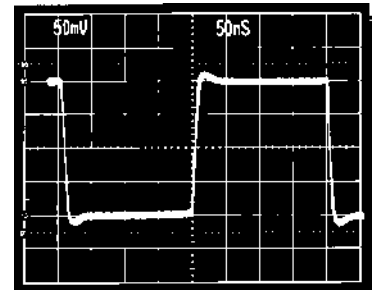


Figure 22c. Inverter Small Signal Pulse Response

AD827

A TWO-CHIP VOLTAGE-CONTROLLED AMPLIFIER (VCA) WITH EXPONENTIAL RESPONSE

Voltage-controlled amplifiers are often used as building blocks in automatic gain control systems. Figure 25 shows a two-chip VCA built using the AD827 and the AD539, a dual, current-output multiplier. As configured, the circuit has its two

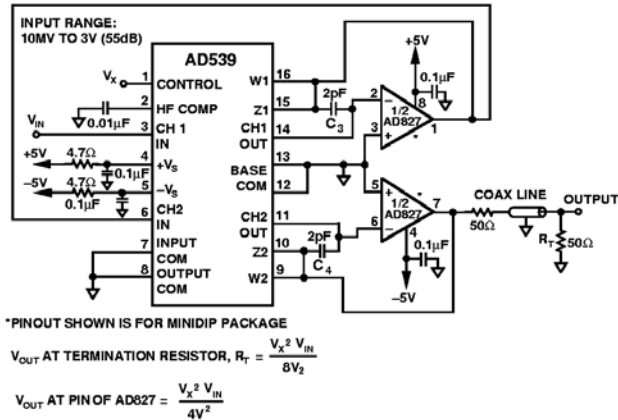


Figure 25. A Wide Range Voltage-Controlled Amplifier Circuit

multipliers connected in series. They could also be placed in parallel with an increase in bandwidth and a reduction in gain. The gain of the circuit is controlled by V_x , which can range from 0 to 3 V dc. Measurements show that this circuit easily supplies 2 V p-p into a 100 Ω load while operating from ± 5 V supplies. The overall bandwidth of the circuit is approximately 7 MHz with 0.5 dB of peaking.

Each half of the AD827 serves as an I/V converter and converts the output current of one of the two multipliers in the AD539 into an output voltage. Each of the AD539's two multipliers contains two internal 6 k Ω feedback resistors; one is connected

between the CH1 output and Z1, the other between the CH1 output and W1. Likewise, in the CH2 multiplier, one of the feedback resistors is connected between CH2 and Z2 and the other is connected between CH2 and W2. In Figure 25, Z1 and W1 are tied together, as are Z2 and W2, providing a 3 k Ω feedback resistor for the op amp. The 2 pF capacitors connected between the AD539's W1 and CH1 and W2 and CH2 pins are in parallel with the feedback resistors and thus reduce peaking in the VCA's frequency response. Increasing the values of C3 and C4 can further reduce the peaking at the expense of reduced bandwidth. The 1.25 mA full-scale output current of the AD539 and the 3 k Ω feedback resistor set the full-scale output voltage of each multiplier at 3.25 V p-p.

Current limiting in the AD827 (typically 30 mA) limits the output voltage in this application to about 3 V p-p across a 100 Ω load. Driving a 50 Ω reverse-terminated load divides this value by two, limiting the maximum signal delivered to a 50 Ω load to about 1.5 V p-p, which suffices for video signal levels. The dynamic range of this circuit is approximately 55 dB and is primarily limited by feedthrough at low input levels and by the maximum output voltage at high levels.

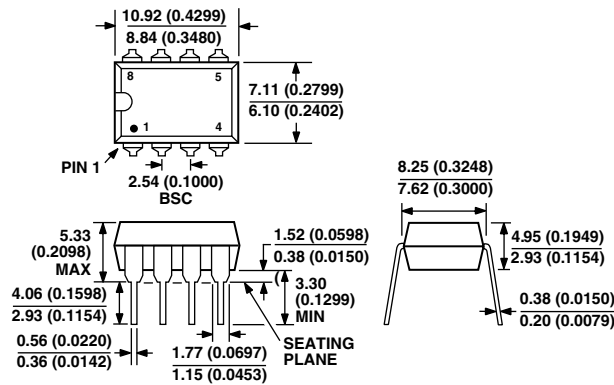
Guidelines for Grounding and Bypassing

When designing practical high frequency circuits using the AD827, some special precautions are in order. Both short interconnection leads and a large ground plane are needed whenever possible to provide low resistance, low inductance circuit paths. One should remember to minimize the effects of capacitive coupling between circuits. Furthermore, IC sockets should be avoided. Feedback resistors should be of a low enough value that the time constant formed with stray circuit capacitances at the amplifier summing junction will not limit circuit performance. As a rule of thumb, use feedback resistor values that are less than 5 k Ω . If a larger resistor value is necessary, a small (<10 pF) feedback capacitor in parallel with the feedback resistor may be used. The use of 0.1 μ F ceramic disc capacitors is recommended for bypassing the op amp's power supply leads.

OUTLINE DIMENSIONS

8-Lead Plastic Dual-in-Line Package [PDIP]
(N-8)

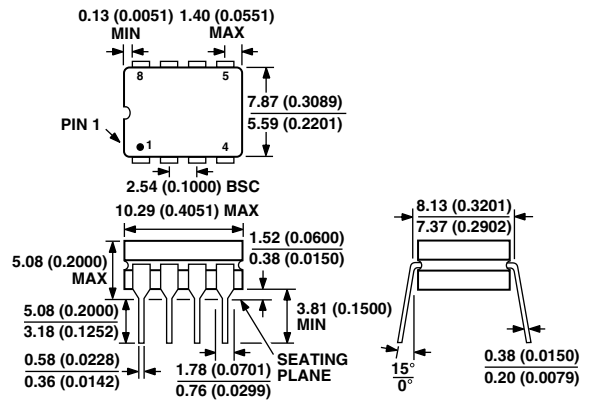
Dimensions shown in millimeters and (inches)



CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Ceramic DIP-Glass Hermetic Seal Package [CERDIP]
(Q-8)

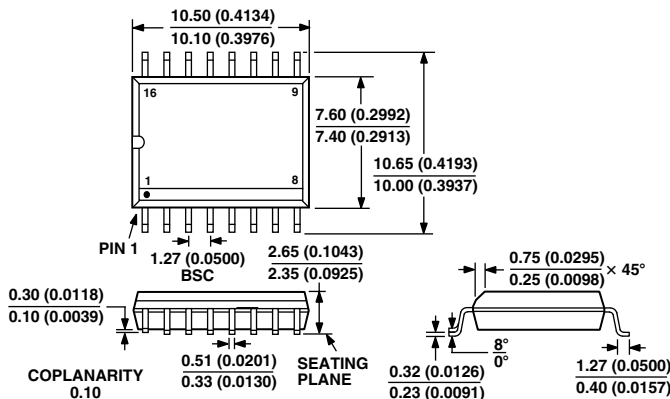
Dimensions shown in millimeters and (inches)



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16-Lead Standard Small Outline Package [SOIC]
Wide Body
(R-16)

Dimensions shown in millimeters and (inches)

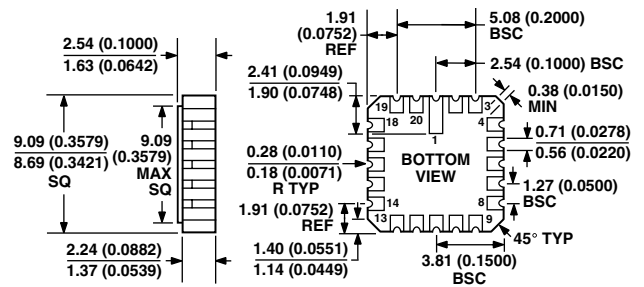


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COMPLIANT TO JEDEC STANDARDS MS-013AA

20-Terminal Ceramic Leadless Chip Carrier [LCC]
(E-20A)

Dimensions shown in millimeters and (inches)



CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

AD827

Revision History

Location	Page
8/02—Data Sheet changed from REV. B to REV. C.	
Updated Outline Dimensions	9

