ON Semiconductor

Is Now



To learn more about onsemi™, please visit our website at www.onsemi.com

onsemi and ONSEMI. and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries. onsemi owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of onsemi product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. onsemi reserves the right to make changes at any time to any products or information herein is provided "as-is" and onsemi makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using onsemi products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by onsemi. "Typical" parameters which may be provided in onsemi data sheets and/ or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. onsemi does not convey any license under any of its intellectual property rights nor the rights of others. onsemi products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use onsemi products for any such unintended or unauthorized application,



ON Semiconductor®

FDB070AN06A0-F085 N-Channel PowerTrench® MOSFET 60V, 80A, $7m\Omega$

Features

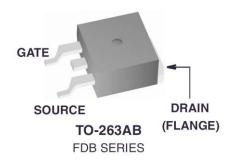
- $r_{DS(ON)} = 6.1 \text{m}\Omega$ (Typ.), $V_{GS} = 10 \text{V}$, $I_D = 80 \text{A}$
- $Q_{g(tot)} = 51nC (Typ.), V_{GS} = 10V$
- Low Miller Charge
- Low Q_{RR} Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)
- Qualified to AEC Q101
- RoHS Compliant

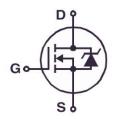
Formerly developmental type 82567



Applications

- Motor / Body Load Control
- ABS Systems
- Pow ertrain Management
- Injection Systems
- DC-DC converters and Off-line UPS
- Distributed Pow er Architectures and VRMs
- Primary Switch for 12V and 24V systems





Ordering Information

Device	Output Voltage	Marking	Package	Shipping
FDB070AN06A0-F085	TBD	FDB070AN06A0	TO-263AB	Tape and Reel

Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Ratings	Unit
V _{DSS}	Drain to Source Voltage	60	V
V _{GS}	Gate to Source Voltage	±20	V
Ι _D	Drain Current Continuous ($T_c < 97^{\circ}C$, $V_{GS} = 10V$)	80	А
U	Continuous ($T_A = 25$ °C, $V_{GS} = 10$ V, $R_{\theta JA} = 43$ °C/W)	15	Α
	Pulsed	Figure 4	Α
E _{AS}	Single Pulse Avalanche Energy (1)	190	mJ
P₀	Powerdissipation	175	W
P D	Derate above 25°C	1.17	W/°C
T _J , T _{STG}	Operating and Storage Temperature	-55 to 175	°C

Thermal Characteristics

R _{eJC}	Thermal Resistance Junction to Case TO-220,TO-263	0.86	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-220,TO-263 (2)	62	°C/W
$R_{ heta JA}$	Thermal Resistance Junction to Ambient TO-263, 1in ² copper pad area	43	°C/W

Notes:

- 1. Starting $T_J = 25 \,^{\circ}\text{C}$, $L = 93 \,\mu\text{H}$, $I_{AS} = 64A$.
- Pulse width = 100s.

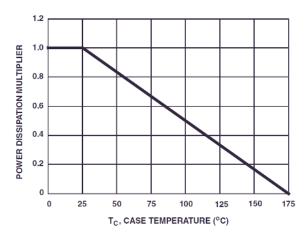
This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry.

All ON Semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted

Symbol	Parameter	Test Conditions		Min.	Тур.	Max.	Units
Off Characterist	ics	•		•			
B _{VDSS}	Drain to Source Breakdown Voltage	$I_D=250~\mu A,V_{GS}$	= 0 V	60			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 50 V				1	
		$V_{GS} = 0 V$	T _C = 150 °C			250	μΑ
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}$				±100	nA
On Characterist	ics	•				<u> </u>	
$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$		2		4	V
	 	I _D = 80A, V _{GS} = 10V			0.0061	0.007	
r _{DS(ON)}	Drain to Source On Resistance	$I_D = 80A, V_{GS} = 1$	0V,				Ω
		T _J = 175°C			0.0127	0.015	
Dynamic Charac	teristics						
C_{ISS}	Input Capacitance	V 05V V	0.1/		3000		pF
Coss	Output Capacitance	$V_{DS} = 25V, V_{GS} = 0 V,$ F = 1 MHz			510		pF
C _{RSS}	Reverse Transfer Capacitance				230		pF
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0V \text{ to } 10V$			51	66	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0V \text{ to } 2V$	$V_{DD} = 30 \text{ V}$		5.4	7	nC
Q_gs	Gate to Source Gate Charge		I _D = 80 A		17		nC
Q_{gs2}	Gate Charge Threshold to Plateau	1	$I_g = 1.0 \text{ mA}$		11.6		nC
Q_{gd}	Gate to Drain "Miller" Charge	1			16		nC
Switching Chara	acteristics (V _{GS} = 10 V)	•					
t _{ON}	Turn-On Time					256	ns
T _{d(ON)}	Turn-On Delay Time	1			12		ns
t _r	Rise Time	$V_{DD} = 30 \text{ V}, I_D = 80 \text{ A}$ $V_{GS} = 10 \text{ V}, R_{GS} = 5.6 \Omega$			159		ns
$T_{d(OFF)}$	Turn-Off Delay Time				27		ns
t _f	Fall Time	1			35		ns
t _{OFF}	Turn-Off Time	1				93	ns
Orain-Source Di	ode Characteristics						
V_{SD}	Source to Drain Diade Voltage	I _{SD} = 80 A				1.25	V
	Source to Drain Diode Voltage	I _{SD} = 40 A				1.0	V
t _{rr}	Reverse Recovery Time	$I_{SD} = 75 \text{ A}, dI_{SD}/dt = 100 \text{ A}/\mu\text{s}$				67	ns
Q_{RR}	Reverse Recovered Charge	$I_{SD} = 75 \text{ A}, dI_{SD}/dt = 100 \text{ A}/\mu\text{s}$				80	nC

Typical Characteristics T_C = 25°C unless otherwise noted



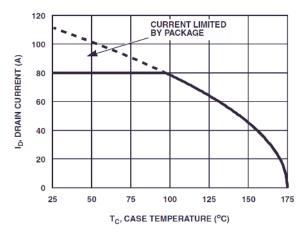


Figure 1. Normalized Power Dissipation vs Ambient Temperature

Figure 2. Maximum Continuous Drain Current vs Case Temperature

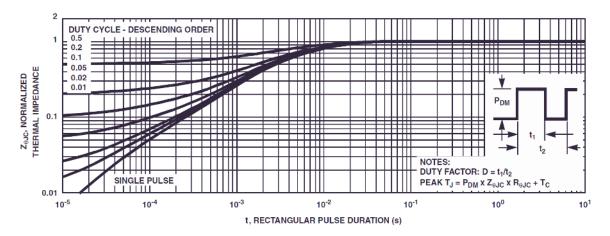


Figure 3. Normalized Maximum Transient Thermal Impedance

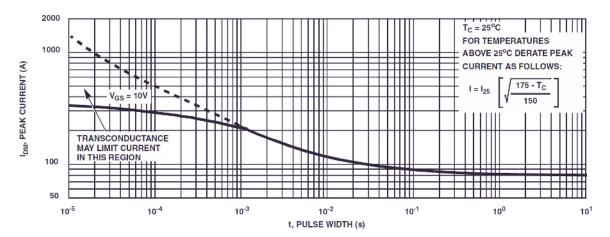


Figure 4. Peak Current Capability

Typical Characteristics T_C = 25°C unless otherwise noted

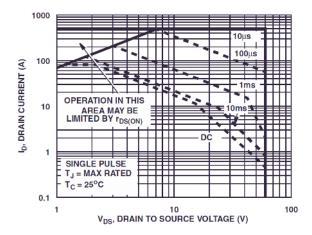
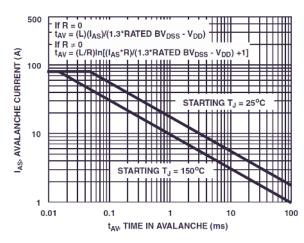


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to ON Semiconductor Application Notes AN7514 and AN7515

Capability

Figure 6.

Unclamped Inductive Switching

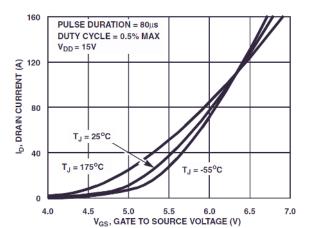


Figure 7. Transfer Characteristics

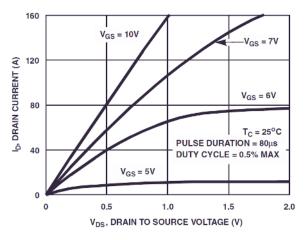


Figure 8. Saturation Characteristics

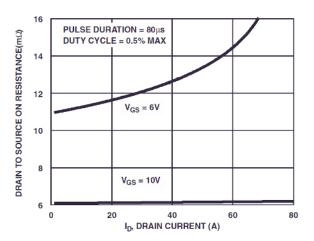


Figure 9. Drain to Source On Resistance vs Drain Current

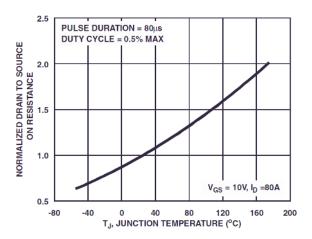
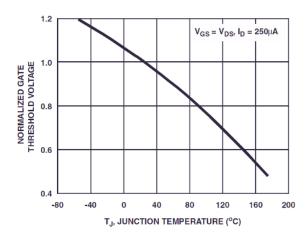


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

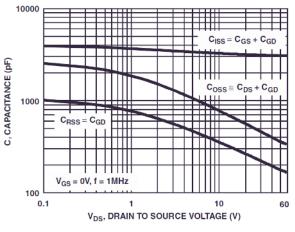
Typical Characteristics T_C = 25°C unless otherwise noted



1.10 I_D = 250µA I 1.05 I

Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature



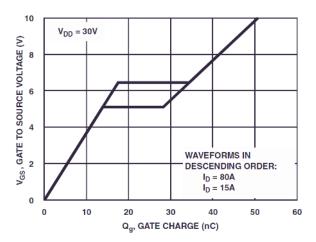


Figure 13. Capacitance vs Drain to Source Voltage

Figure 14. Gate Charge Waveforms for Constant Gate Current

Test Circuits and Waveforms

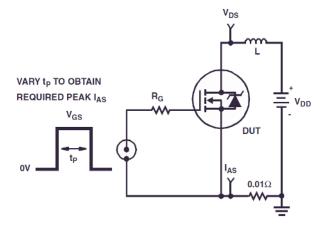


Figure 15. Unclamped Energy Test Circuit

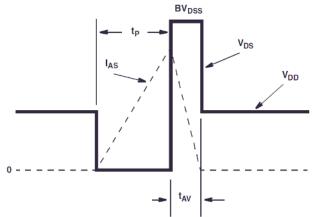


Figure 16. Unclamped Energy Waveforms

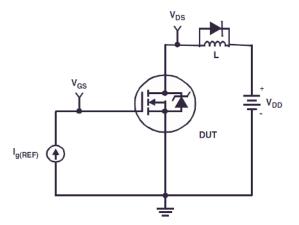


Figure 17. Gate Charge Test Circuit

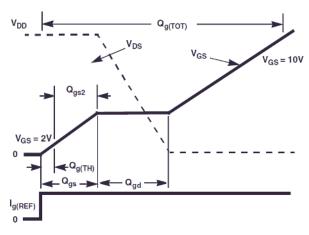


Figure 18. Gate Charge Waveforms

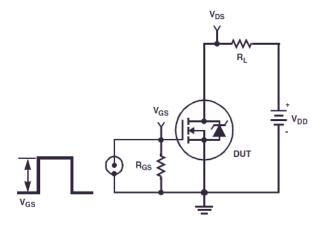


Figure 19. Switching Time Test Circuit

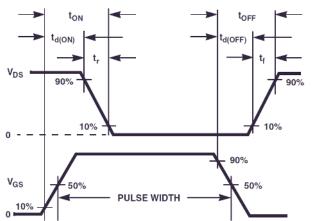


Figure 20. Switching Time Waveforms

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM} , and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM} , in an application. Therefore the application's ambient temperature, T_A (°C), and thermal resistance $R_{\theta JA}$ (°C/W) must be reviewed to

ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \tag{EQ. 1}$$

In using surface mount devices such as the TO-263 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

- Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
- The number of copper layers and the thickness of the board.
- 3. The use of external heat sinks.
- 4. The use of thermal vias.
- 5. Air flow and board orientation.
- For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

ON Semiconductor provides thermal information to assist the designer's preliminary application evaluation. Figure 21 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the ON Semiconductor device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2 or 3. Equation 2 is used for copper area defined in inches square and equation 3 is for area in centimeters square. The area, in square inches or square centimeters is the top copper area including the gate and source pads.

$$R_{\Theta JA} = 26.51 + \frac{19.84}{(0.262 + Area)}$$
 (EQ. 2)

Area in Inches Squared

$$R_{\Theta JA} = 26.51 + \frac{128}{(1.69 + Area)}$$
 (EQ. 3)

Area in Centimeters Squared

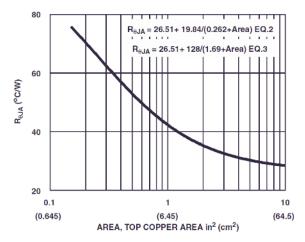


Figure 21. Thermal Resistance vs Mounting Pad Area

PSPICE Electrical Model .SUBCKT FDB070AN06A0 2 1 3; rev March 2003 Ca 12 8 1.5e-9 Cb 15 14 1.5e-9 Cin 68 2.9e-9 LDRAIN **DPLCAP** DRAIN Dbody 7 5 Dbody MOD Dbreak 5 11 DbreakMOD RLDRAIN Dplcap 10 5 DplcapMOD RSI C1 DBREAK 51 Ebreak 11 7 17 18 62 5 51 **ESLC** 11 Eds 14 8 5 8 1 Egs 13 8 6 8 1 50 Esg 6 10 68 1 **T** DBODY RDRAIN <u>6</u> 8 EBREAK Ev thres 6 21 19 8 1 **ESG** Ev temp 20 6 18 22 1 **EVTHRES** (<u>19</u>) **─** MWEAK **LGATE EVTEMP** It 8 17 1 RGATE GATE 18 22 ■MMED 20 Lgate 1 9 4.8e-9 **←**MSTRO RLGATE Ldrain 25 1.0e-9 LSOURCE Lsource 3 7 3e-9 CIN SOURCE RLgate 1 9 48 **RSOURCE** RLSOURCE RLdrain 2 5 10 S2A RLsource 3 7 3 **RBREAK** 14 13 Mmed 16 6 8 8 MmedMOD **≨**RVTEMP Mstro 16 6 8 8 MstroMOD a S2B СВ 19 Mweak 16 21 8 8 MweakMOD CA IT VBAT Rbreak 17 18 RbreakMOD 1 8 <u>5</u> 8 EGS **EDS** Rdrain 50 16 RdrainMOD 1.3e-3 Rgate 9 20 2.7 RSLC1 5 51 RSLCMOD 1e-6 **RVTHRES** RSLC2 5 50 1e3 Rsource 87 RsourceMOD 3.1e-3 Rvthres 22 8 RvthresMOD 1 Rvtemp 18 19 RvtempMOD 1 S1a 6 12 13 8 S1AMOD S1b 13 12 13 8 S1BMOD S2a 6 15 14 13 S2AMOD S2b 13 15 14 13 S2BMOD Vbat 22 19 DC 1 ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*250),10))} .MODEL Dbody MOD D (IS=7.6E-12 N=1.04 RS=2.2e-3 TRS1=2.7e-3 TRS2=2e-7 + CJO=1.6e-9 M=0.55 TT=5e-12 XTI=3.9) .MODEL DbreakMOD D (RS=8e-1 TRS1=5e-4 TRS2=-8.9e-6) .MODEL DplcapMOD D (CJO=1.05e-9 IS=1e-30 N=10 M=0.45) .MODEL MmedMOD NMOS (VTO=3.7 KP=10 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=2.7) .MODEL MstroMOD NMOS (VTO=4.7 KP=100 IS=1e-30 N=10 TOX=1 L=1u W=1u) .MODEL MweakMOD NMOS (VTO=3.01 KP=0.03 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=27 RS=0.1) .MODEL RbreakMOD RES (TC1=7.1e-4 TC2=-5.5e-7) .MODEL RdrainMOD RES (TC1=1.7e-2 TC2=4e-5) .MODEL RSLCMOD RES (TC1=3e-3 TC2=1e-5) .MODEL RsourceMOD RES (TC1=1e-3 TC2=1e-6) .MODEL RvthresMOD RES (TC1=-5.2e-3 TC2=-1.5e-5) .MODEL RytempMOD RES (TC1=-3e-3 TC2=1.3e-6) .MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4 VOFF=-2)

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2 VOFF=-4)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1.5 VOFF=0.5)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=0.5 VOFF=-1.5)

.ENDS

SABER Electrical Model rev March 2003 template FDB070AN06A0 n2.n1.n3 electrical n2,n1,n3 variiscl $dp..model\ dbody\ mod = (isl=7.6e-12,nl=1.04,rs=2.2e-3,trs1=2.7e-3,trs2=2e-7,cjo=1.6e-9,m=0.55,tt=5e-12,xti=3.9)$ dp..model dbreakmod = (rs=8e-1,trs1=5e-4,trs2=-8.9e-6) dp..model dplcapmod = (cjo=1.05e-9,isl=10e-30,nl=10,m=0.45) m..model mmedmod = $(type=_n, vto=3.7, kp=10, is=1e-30, tox=1)$ m..model mstrongmod = $(ty pe=_n, v to=4.7, kp=100, is=1e-30, tox=1)$ $m..model mweakmod = (ty pe=_n, v to=3.01, kp=0.03, is=1e-30, tox=1, rs=0.1)$ sw_vcsp..models1amod = (ron=1e-5,roff=0.1,von=-4,voff=-2) $sw_v csp..model s1bmod = (ron=1e-5, roff=0.1, von=-2, voff=-4)$ sw_v csp..model s2amod = (ron=1e-5,roff=0.1,v on=-1.5,v off=0.5) $sw_vcsp..model s2bmod = (ron=1e-5, roff=0.1, von=0.5, voff=-1.5)$ c.ca n12 n8 = 1.5e-9c.cb n15 n14 = 1.5e-9LDRAIN DPLCAP c.cin n6 n8 = 2.9e-910 RLDRAIN dp.dbody n7 n5 = model=dbody mod RSLC1 dp.dbreak n5 n11 = model=dbreakmod RSLC2[₹] dp.dplcap n10 n5 = model=dplcapmod ISCL DBREAK 3 spe.ebreak n11 n7 n17 n18 = 62 spe.eds n14 n8 n5 n8 = 1 RDRAIN 8 ESG spe.egs n13 n8 n6 n8 = 1 DBODY **EVTHRES** spe.esg n6 n10 n6 n8 = 1 MWEAK EVTEME LGATE spe.ev thres n6 n21 n19 n8 = 1 **RGATE** EBREA spe.ev temp n20 n6 n18 n22 = 1 MMED 20 i.it n8 n17 = 1 LSOURCE CIN SOURCE I.lgate n1 n9 = 4.8e-9~~ RSOURCE RLSOURCE I.Idrain n2 n5 = 1.0e-9I.Isource n3 n7 = 3e-9RBREAK res.rlgate n1 n9 = 48 RVTEMP S2B res.rldrain n2 n5 = 10 CB 19 res.rlsource n3 n7 = 3 IT VBAT EGS m.mmed n16 n6 n8 n8 = model=mmedmod, I=1u, m.mstrong n16 n6 n8 n8 = model=mstrongmod, **RVTHRES** l=1u, w=1u m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u res.rbreak n17 n18 = 1, tc1=7.1e-4,tc2=-5.5e-7 res.rdrain n50 n16 = 1.3e-3, tc1=1.7e-2,tc2=4e-5 res.rgate n9 n20 = 2.7 res.rslc1 n5 n51 = 1e-6, tc1=3e-3,tc2=1e-5 res.rslc2 n5 n50 = 1e3res.rsource n8 n7 = 3.1e-3, tc1=1e-3,tc2=1e-6 res.rvthres n22 n8 = 1, tc1=-5.2e-3,tc2=-1.5e-5 res.rv temp n18 n19 = 1, tc1=-3e-3,tc2=1.3e-6sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod sw_v csp.s1b n13 n12 n13 n8 = model=s1bmod sw_v csp.s2a n6 n15 n14 n13 = model=s2amod sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod v.vbat n22 n19 = dc=1 equations { i (n51->n50) +=iscl iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/250))** 10))}

PSPICE Thermal Model

REV 23 March 2003

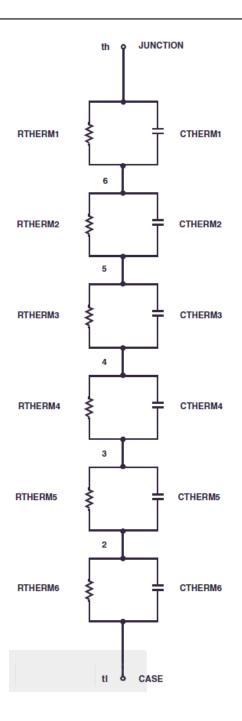
FDB070AN06A0T

CTHERM1 TH 6 3.5e-3 CTHERM2 6 5 1.7e-2 CTHERM3 5 4 1.8e-2 CTHERM4 4 3 1.9e-2 CTHERM5 3 2 4.7e-2 CTHERM6 2 TL 7e-2 RTHERM1 TH 6 2e-2 RTHERM2 6 5 7e-2 RTHERM3 5 4 1e-1 RTHERM4 4 3 1.5e-1 RTHERM5 3 2 1.6e-1 RTHERM5 2 TL 1.85e-1

SABER Thermal Model

SABER thermal model FDB070AN06A0T template thermal_model th tI thermal_c th, tI $\{$ ctherm.ctherm1 th 6 =3.5e-3 ctherm.ctherm2 6 5 =1.7e-2 ctherm.ctherm3 5 4 =1.8e-2 ctherm.ctherm4 4 3 =1.9e-2 ctherm.ctherm5 3 2 =4.7e-2 ctherm.ctherm6 2 tI =7e-2 rtherm.rtherm1 th 6 =2e-2 rtherm.rtherm2 6 5 =7e-2 rtherm.rtherm3 5 4 =1e-1 rtherm.rtherm4 4 3 =1.5e-1 rtherm.rtherm5 3 2 =1.6e-1

rtherm.rtherm6 2 tl =1.85e-1



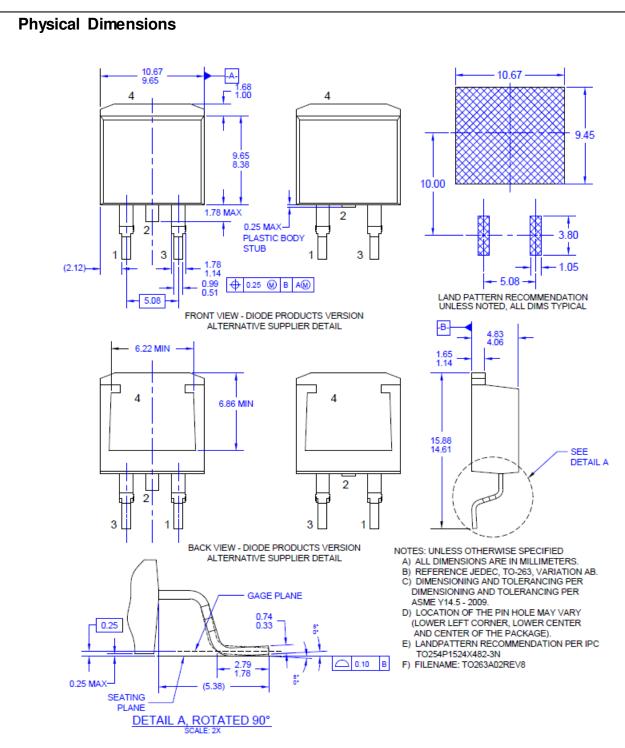


Figure 22. TO-263 2L (D2PAK), 4.445 x 10.16 x 15.24mm, TAPE REEL

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications using ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdicton or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsi

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor 19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA **Phone**: 303-675-2175 or 800-344-3860 Toll Free USA/Canada Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada

Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada.

Europe, Middle East and Africa Technical Support: Phone: 421 33 790 2910

Japan Customer Focus Center Phone: 81-3-5817-1050 ON Semic on ductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative