

TinyLogic HST 2-Input AND Gate

NC7ST08

Description

The NC7ST08 is a single 2-Input high performance CMOS AND Gate, with TTL-compatible inputs. Advanced Silicon Gate CMOS fabrication assures high speed and low power circuit operation. ESD protection diodes inherently guard both inputs and output with respect to the V_{CC} and GND rails. High gain circuitry offers high noise immunity and reduced sensitivity to input edge rate. The TTL-compatible inputs facilitate TTL to NMOS / CMOS interfacing. Device performance is similar to MM74HCT but with 1/2 the output current drive of HC / HCT.

Features

- Space Saving SOT23-5, SC-74A and SC-88A 5-Lead Package
- Ultra Small MicroPak™ Leadless Package
- High Speed: t_{PD} = 6 ns (Typ), V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C
- Low Quiescent Power: I_{CC} < 1 μA Typ, V_{CC} = 5.5 V
- Balanced Output Drive: 2 mA I_{OL}, -2 mA I_{OH}
- TTL-compatible Inputs
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

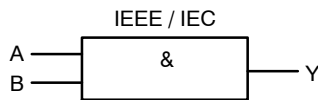
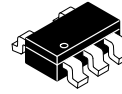
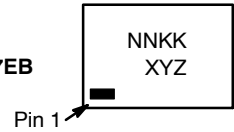


Figure 1. Logic Symbol

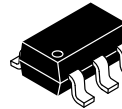
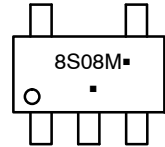
MARKING DIAGRAMS



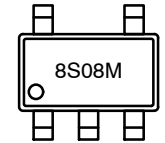
SIP6
CASE 127EB



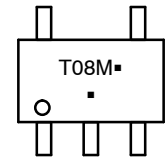
SC-74A
CASE 318BQ



SOT23-5
CASE 527AH



SC-88A
CASE 419A-02



NN, 8S08, T08 = Specific Device Code
KK = 2-Digit Lot Run Traceability Code
XY = 2-Digit Date Code Format
Z = Assembly Plant Code
M = Date Code*

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 4 of this data sheet.

NC7ST08

Pin Configurations

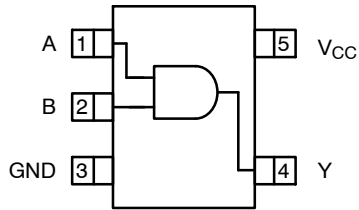


Figure 2. SOT23-5, SC-88A and SC-74A (Top View)

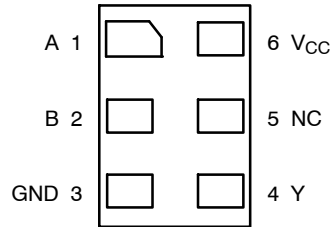


Figure 3. MicroPak (Top Through View)

PIN DESCRIPTION

| Pin Names | Description |
|-----------|-------------|
| A, B | Inputs |
| Y | Output |
| NC | No Connect |

FUNCTION TABLE (Y = AB)

| Inputs | | Output |
|--------|---|--------|
| A | B | Y |
| L | L | L |
| L | H | L |
| H | L | L |
| H | H | H |

H = HIGH Logic Level
L = LOW Logic Level

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Min | Max | Unit | |
|-----------------------|--|------------------------|----------------|--------------------|----|
| V_{CC} | Supply Voltage | -0.5 | 6.5 | V | |
| I_{IK} | DC Input Diode Current | $V_{IN} < 0\text{ V}$ | - | -20 | mA |
| | | $V_{IN} > V_{CC}$ | - | +20 | |
| V_{IN} | DC Input Voltage | -0.5 | $V_{CC} + 0.5$ | V | |
| I_{OK} | DC Output Diode Current | $V_{OUT} < 0\text{ V}$ | - | -20 | mA |
| | | $V_{OUT} > V_{CC}$ | - | +20 | |
| V_{OUT} | Output Voltage | -0.5 | $V_{CC} + 0.5$ | V | |
| I_{OUT} | DC Output Source or Sink Current | - | ± 12.5 | mA | |
| I_{CC} or I_{GND} | DC V_{CC} or Ground Current per Supply Pin | - | ± 25 | mA | |
| T_{STG} | Storage Temperature | -65 | +150 | $^{\circ}\text{C}$ | |
| T_J | Junction Temperature | - | +150 | $^{\circ}\text{C}$ | |
| T_L | Lead Temperature (Soldering, 10 Seconds) | - | +260 | $^{\circ}\text{C}$ | |
| P_D | Power Dissipation in Still Air | SC-74A / SOT23-5 | - | 390 | mW |
| | | SC-88A | - | 332 | |
| | | MicroPak-6 | - | 812 | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

NC7ST08

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---------------------------------|--------------------------|-------------------------|-----|-----------------|------|
| V _{CC} | Supply Voltage | | 4.5 | 5.5 | V |
| V _{IN} | Input Voltage | | 0 | V _{CC} | V |
| V _{OUT} | Output Voltage | | 0 | V _{CC} | V |
| T _A | Operating Temperature | | -40 | +85 | °C |
| t _r , t _f | Input Rise and Fall Time | V _{CC} = 5.0 V | 0 | 10 | ns/V |
| θ _{JA} | Thermal Resistance | SC-74A / SOT23-5 | - | 320 | °C/W |
| | | SC-88A | - | 377 | |
| | | MicroPak-6 | - | 154 | |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

- Unused inputs must be held HIGH or LOW. They may not float.

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = +25°C | | | T _A = -40 to +85°C | | Unit |
|------------------|---------------------------|---------------------|--|------------------------|-------------|-------------|-------------------------------|-------------|------|
| | | | | Min | Typ | Max | Min | Max | |
| V _{IH} | HIGH Level Input Voltage | 4.5 – 5.5 | | 2.0 | - | - | 2.0 | - | V |
| V _{IL} | LOW Level Input Voltage | 4.5 – 5.5 | | - | - | 0.8 | - | 0.8 | V |
| V _{OH} | HIGH Level Output Voltage | 4.5 4.5 | I _{OH} = -20 μA I _{OH} = -2 mA V _{IN} = V _{IH} | 4.4 4.18 | 4.5 4.35 | - | 4.4 4.13 | - | V |
| V _{OL} | LOW Level Output Voltage | 4.5 4.5 | I _{OL} = 20 μA I _{OL} = 2 mA V _{IN} = V _{IL} | - | 0 0.10 | 0.1 0.26 | - | 0.1 0.33 | V |
| I _{IN} | Input Leakage Current | 5.5 | 0 ≤ V _{IN} ≤ 5.5 V | - | - | ±0.1 | - | ±1.0 | μA |
| I _{CC} | Quiescent Supply Current | 5.5 | V _{IN} = V _{CC} or GND | - | - | 1.0 | - | 10.0 | μA |
| I _{CCT} | I _{CC} per Input | 5.5 | One Input V _{IN} = 0.5 V or 2.4 V, Other Input V _{CC} or GND | - | - | 2.0 | - | 2.9 | mA |

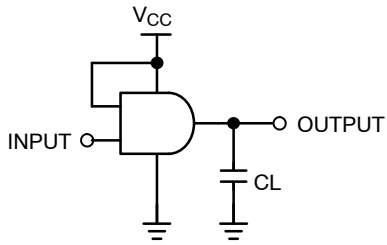
AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = +25°C | | | T _A = -40 to +85°C | | Unit |
|-------------------------------------|--|---------------------|------------------------|------------------------|-----|-----|-------------------------------|-----|------|
| | | | | Min | Typ | Max | Min | Max | |
| t _{PLH} , t _{PHL} | Propagation Delay (Figure 4, 6) | 5.0 | C _L = 15 pF | - | 4 | 12 | - | - | ns |
| | | | | - | 6 | 17 | - | - | |
| | | 4.5 | C _L = 50 pF | - | 6 | 16 | - | 20 | |
| | | | | - | 12 | 27 | - | 31 | |
| | | 5.5 | | - | 5 | 14 | - | 18 | |
| | | | | - | 11 | 26 | - | 30 | |
| t _{TLH} , t _{THL} | Output Transition Time (Figure 4, 6) | 5.0 | C _L = 15 pF | - | 4 | 10 | - | - | ns |
| | | 4.5 | C _L = 50 pF | - | 11 | 25 | - | 31 | |
| | | 5.5 | | - | 10 | 21 | - | 26 | |
| C _{IN} | Input Capacitance | Open | | - | - | 10 | - | - | pF |
| C _{PD} | Power Dissipation Capacitance (Figure 5) | 5.0 | (Note 2) | - | 6 | - | - | - | pF |

- C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current. Current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 5) C_{PD} is related to I_{CCD} dynamic operating current by the expression: I_{CCD} = (C_{PD}) (V_{CC}) (f_{IN}) + (I_{CCstatic}).

NC7ST08

AC Loading and Waveforms



C_L includes load and stray capacitance
Input PRR = 1.0 MHz, $t_W = 500$ ns

Figure 4. AC Test Circuit

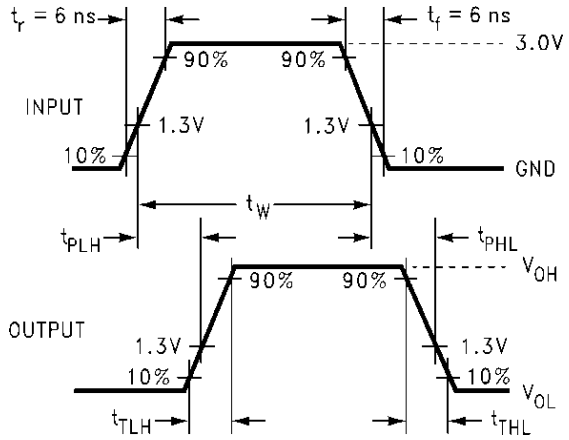
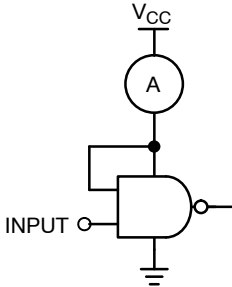


Figure 6. AC Waveforms



Input = AC Waveform;
PRR = Variable; Duty Cycle = 50%.

Figure 5. I_{CCD} Test Circuit

DEVICE ORDERING INFORMATION

| Device | Top Mark | Packages | Shipping [†] |
|-------------------|----------|----------------|-----------------------|
| NC7ST08M5X | 8S08 | SC-74A | 3000 / Tape & Reel |
| NC7ST08M5X-L22090 | 8S08 | SOT23-5 | 3000 / Tape & Reel |
| NC7ST08P5X | T08 | SC-88A | 3000 / Tape & Reel |
| NC7ST08P5X-L22057 | T08 | SC-88A | 3000 / Tape & Reel |
| NC7ST08L6X | NN | SIP6, MicroPak | 5000 / Tape & Reel |
| NC7ST08L6X-L22175 | NN | SIP6, MicroPak | 5000 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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MECHANICAL CASE OUTLINE

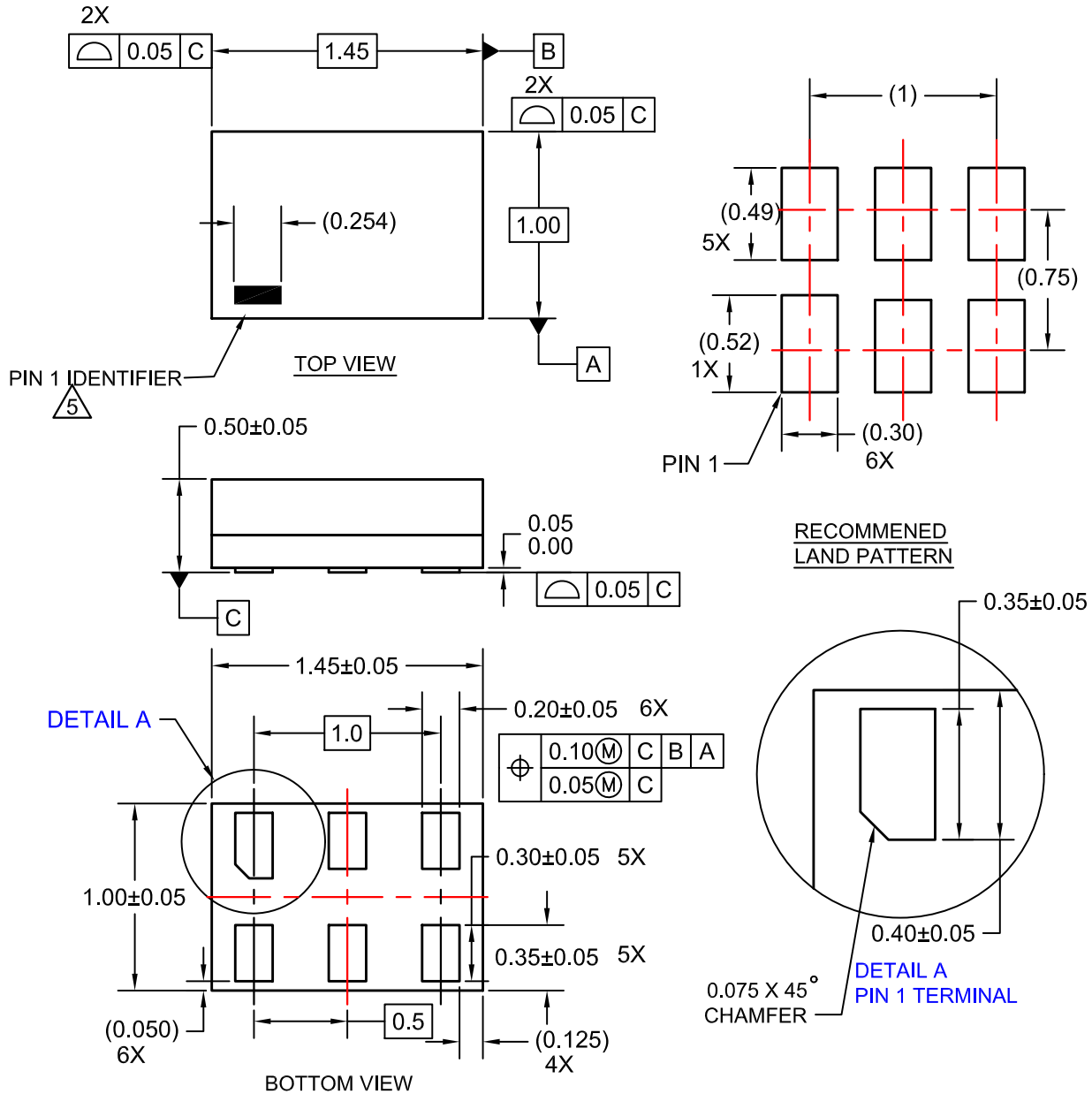
PACKAGE DIMENSIONS

ON Semiconductor®



SIP6 1.45X1.0
CASE 127EB
ISSUE O

DATE 31 AUG 2016



NOTES:

1. CONFORMS TO JEDEC STANDARD MO-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-2009
4. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

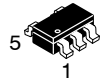
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| DESCRIPTION: | SIP6 1.45X1.0 | PAGE 1 OF 1 |

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

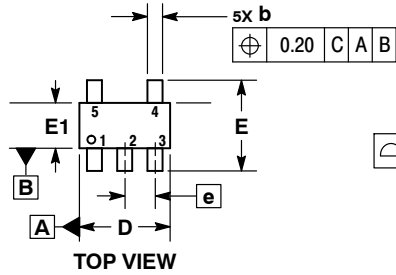
ON Semiconductor®



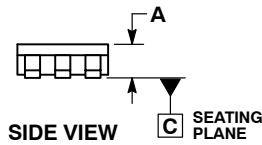
SCALE 2:1

SC-74A CASE 318BQ ISSUE B

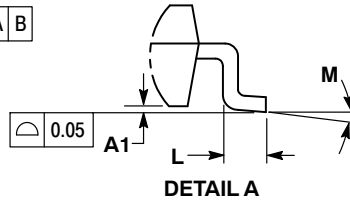
DATE 18 JAN 2018



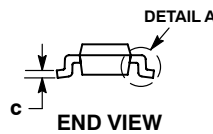
TOP VIEW



SIDE VIEW



DETAIL A



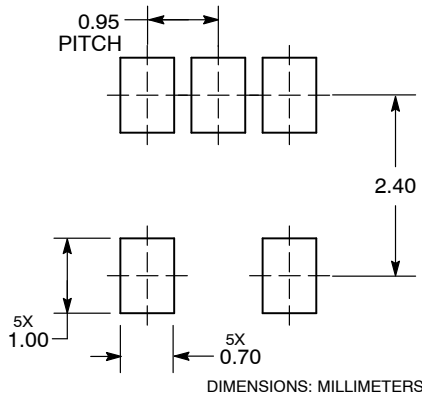
END VIEW

NOTES:

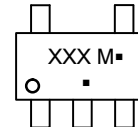
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2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.90 | 1.10 |
| A1 | 0.01 | 0.10 |
| b | 0.25 | 0.50 |
| c | 0.10 | 0.26 |
| D | 2.85 | 3.15 |
| E | 2.50 | 3.00 |
| E1 | 1.35 | 1.65 |
| e | 0.95 BSC | |
| L | 0.20 | 0.60 |
| M | 0° | 10° |

RECOMMENDED SOLDERING FOOTPRINT*



GENERIC MARKING DIAGRAM*



- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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| DESCRIPTION: | SC-74A | PAGE 1 OF 1 |

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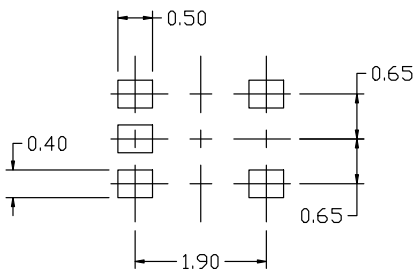
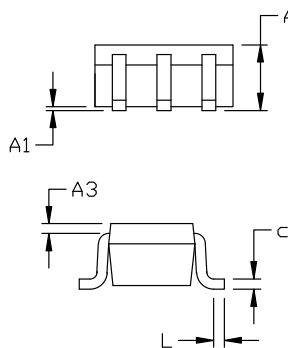
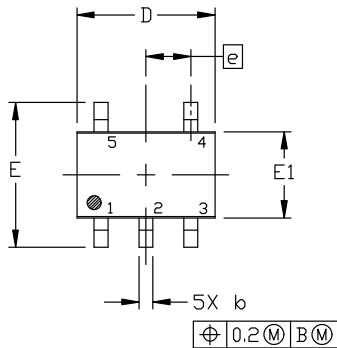
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 2:1

SC-88A (SC-70-5/SOT-353) CASE 419A-02 ISSUE M

DATE 11 APR 2023



RECOMMENDED MOUNTING FOOTPRINT

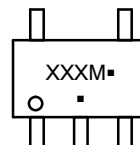
* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

| DIM | MILLIMETERS | | |
|-----|-------------|------|------|
| | MIN. | NOM. | MAX. |
| A | 0.80 | 0.95 | 1.10 |
| A1 | --- | --- | 0.10 |
| A3 | 0.20 REF | | |
| b | 0.10 | 0.20 | 0.30 |
| c | 0.10 | --- | 0.25 |
| D | 1.80 | 2.00 | 2.20 |
| E | 2.00 | 2.10 | 2.20 |
| E1 | 1.15 | 1.25 | 1.35 |
| e | 0.65 BSC | | |
| L | 0.10 | 0.15 | 0.30 |

GENERIC MARKING DIAGRAM*



*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

XXX = Specific Device Code

M = Date Code

▪ = Pb-Free Package

(Note: Microdot may be in either location)

STYLE 1:

1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:

1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:

1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:

1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:

1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:

1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:

1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:

1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:

1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

| | | |
|-------------------------|---------------------------------|---|
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| DESCRIPTION: | SC-88A (SC-70-5/SOT-353) | PAGE 1 OF 1 |

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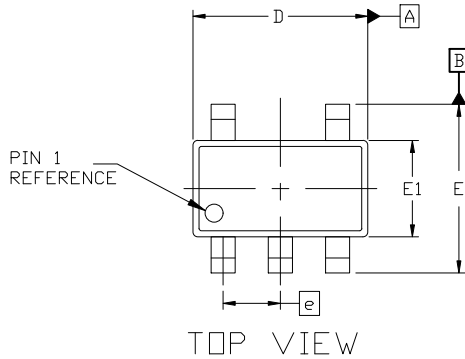
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

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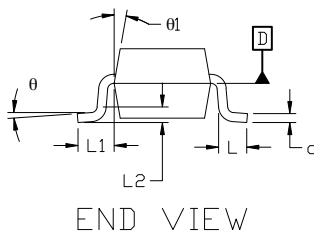
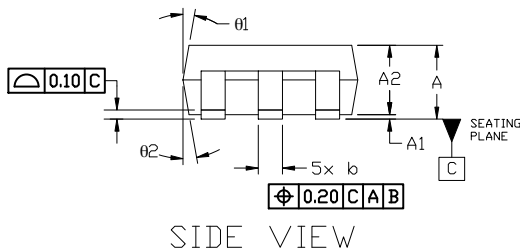
SOT-23, 5 Lead CASE 527AH ISSUE A

DATE 09 JUN 2021



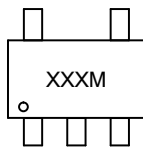
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1989A
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM D.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL NOT BE LESS THAN 0.07mm.



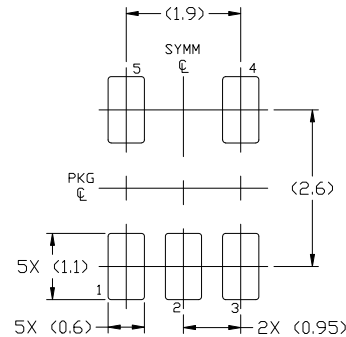
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|--------|-------------|------|------|
| | MIN. | NOM. | MAX. |
| A | 0.90 | — | 1.45 |
| A1 | 0.00 | — | 0.15 |
| A2 | 0.90 | 1.15 | 1.30 |
| b | 0.30 | — | 0.50 |
| c | 0.08 | — | 0.22 |
| D | 2.90 BSC | | |
| E | 2.80 BSC | | |
| E1 | 1.60 BSC | | |
| e | 0.95 BSC | | |
| L | 0.30 | 0.45 | 0.60 |
| L1 | 0.60 REF | | |
| L2 | 0.25 REF | | |
| theta | 0° | 4° | 8° |
| theta1 | 0° | 10° | 15° |
| theta2 | 0° | 10° | 15° |

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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| DESCRIPTION: | SOT-23, 5 LEAD | PAGE 1 OF 1 |

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