

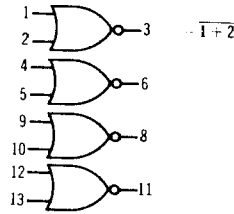
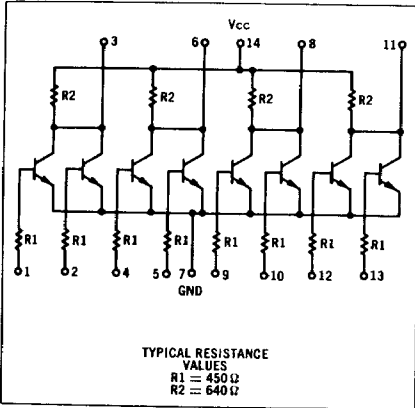
QUAD 2-INPUT GATES

MRTL MC900/800 series

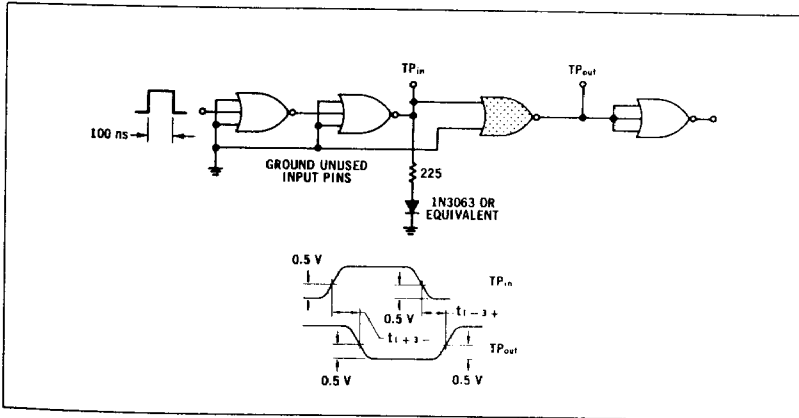
**MC924 • MC824** 

Available in TO-86 Flat Package, Add "F" Suffix.

This gate element consists of four 2-input positive logic NOR gate circuits in a single package. The gate circuits may be used independently, or connected together to form flip-flops or non-inverting gates.



SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



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**ELECTRICAL CHARACTERISTICS**

Test procedures are shown for one gate only. Other gates are tested in the same manner.

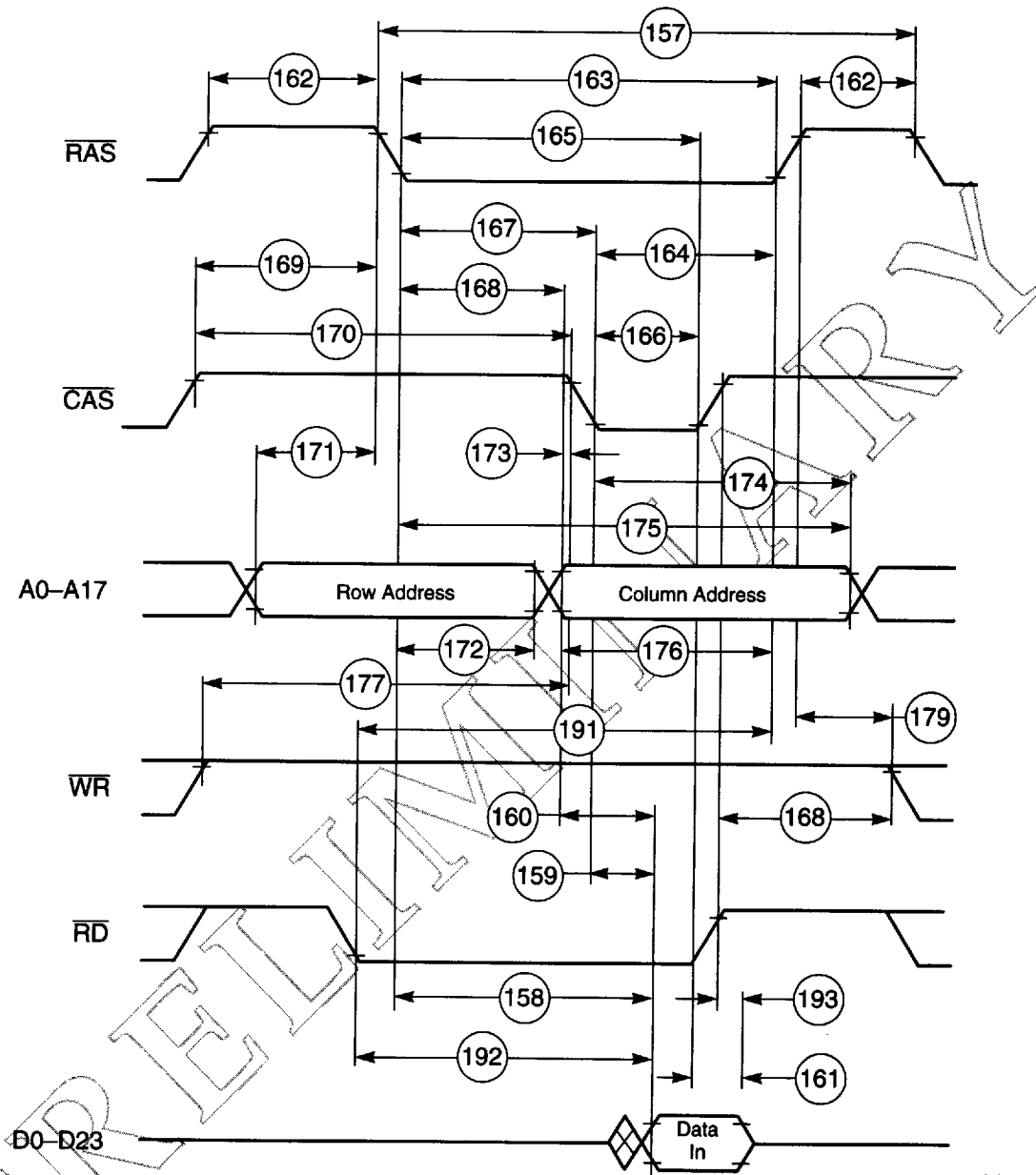
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE VALUES											
			@Test Temperature						TEST VOLTAGE					
			-55°C		+25°C		+100°C		APPLIED TO PINS LISTED BELOW:		TEST VOLTAGE		TEST VOLTAGE	
			V <sub>in</sub>	V <sub>on</sub>	V <sub>off</sub>	V <sub>out</sub>	V <sub>in</sub>	V <sub>on</sub>	V <sub>off</sub>	V <sub>out</sub>	V <sub>in</sub>	V <sub>on</sub>	V <sub>off</sub>	V <sub>out</sub>
			1.014	1.014	1.50	0.710	1.50	0.710	1.50	0.710	3.00	3.00	3.00	3.00
			0.844	0.813	1.50	0.565	1.50	0.320	3.00	3.00	3.00	3.00	3.00	3.00
			0.844	0.844	1.50	0.574	1.50	0.370	3.00	3.00	3.00	3.00	3.00	3.00
			0.844	0.844	1.50	0.554	1.50	0.370	3.00	3.00	3.00	3.00	3.00	3.00
			0.710	0.710	1.50	0.370	1.50	0.370	3.00	3.00	3.00	3.00	3.00	3.00
			0.710	0.710	1.50	0.370	1.50	0.370	3.00	3.00	3.00	3.00	3.00	3.00
			0.710	0.710	1.50	0.370	1.50	0.370	3.00	3.00	3.00	3.00	3.00	3.00

Characteristic	Symbol	Pin Under Test	TEST LIMITS											
			MC924				MC824				TEST VOLTAGE			
			-55°C		+25°C		+125°C		+100°C		APPLIED TO PINS LISTED BELOW:		TEST VOLTAGE	
			Min	Max	Min	Max	Min	Max	Min	Max	V <sub>in</sub>	V <sub>on</sub>	V <sub>off</sub>	V <sub>out</sub>
Input Current	I <sub>in</sub>	1, 2	-	485	435	-	470	450	-	450	1	-	2	14
			-	485	435	-	470	450	-	450	2	-	1	14
Output Current	I <sub>A5</sub>	3	2.47	-	2.54	-	2.35	-	2.38	-	3	-	-	14
Output Leakage Current	I <sub>CEX</sub>	3	-	100	218	-	235	225	-	225	-	-	-	7
Output Voltage	V <sub>out</sub>	3	-	710	300	-	330	400	-	400	-	-	-	14
			-	710	300	-	320	370	-	370	-	-	-	14
Saturation Voltage	V <sub>CE(sat)</sub>	3	-	200	210	-	280	260	-	260	-	-	-	14
			-	200	210	-	280	260	-	260	-	-	-	14
Switching Time	t	1-3, 1-3+	-	-	-	-	-	-	-	-	Pulse In	Pulse Out	-	2.7
			-	-	-	-	-	-	-	-	1	3	-	1.7
			-	-	-	-	-	-	-	-	1	3	-	2.7
			-	-	-	-	-	-	-	-	1	3	-	2.7

Ground inputs of gates not under test. Other pins not listed are left open.

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Figure 2-18 DRAM Out-of-Page Read Access

Preliminary Data