



# Am29841/Am29843

## High Performance Bus Interface Latches

### DISTINCTIVE CHARACTERISTICS

- High speed parallel latches
  - Noninverting transparent  $t_{PD} = 5.25$  ns typ
  - Inverting transparent  $t_{PD} = 6.0$  ns typ
- Buffered common latch enable, clear and preset input
- Three-state outputs glitch free during power-up and down
- Outputs have Schottky clamp to ground
- 48 mA Commercial  $I_{OL}$
- Low input/output capacitance
  - 6 pF inputs (typical)
  - 8 pF outputs (typical)
- $I_{OH}$  specified 2.0 V and 2.4 V
- 24-pin 0.3" space saving package
- Fully TTL compatible inputs and outputs
- IMOX™ high performance IMplanted QXide isolated process

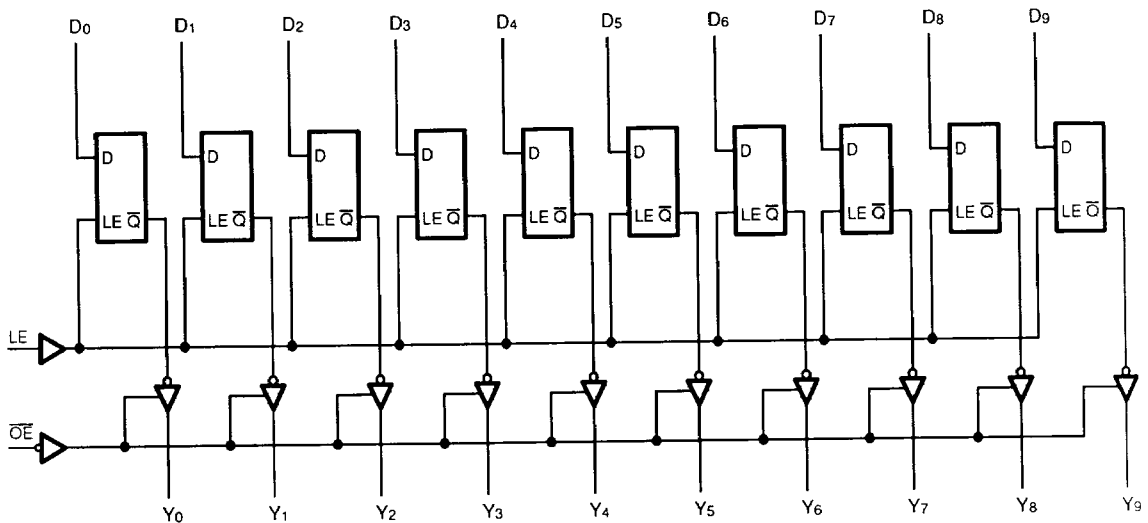
### GENERAL DESCRIPTION

The Am29841/843 bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The Am29841 is a buffered, 10-bit wide version of the popular '373 function. The Am29843 is a 9-bit wide buffered latch with Preset ( $\overline{PRE}$ ) and Clear ( $\overline{CLR}$ ) – ideal for parity bus interfacing in high performance systems.

All of the Am29800 high performance interface family is designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs are Schottky diode inputs, and all outputs are designed for low capacitance bus loading in the high impedance state.

### BLOCK DIAGRAMS

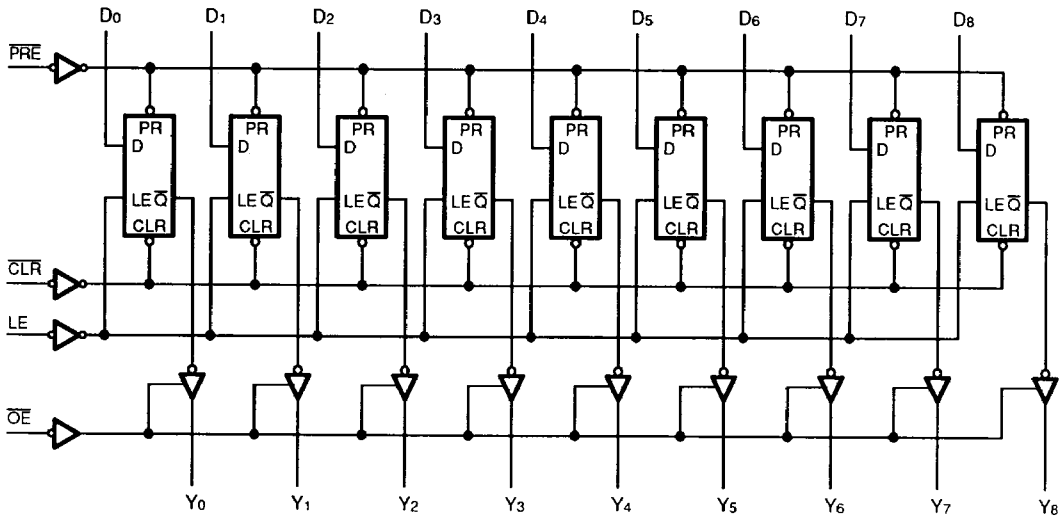
#### Am29841



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**BLOCK DIAGRAMS (Continued)**

**Am29843**

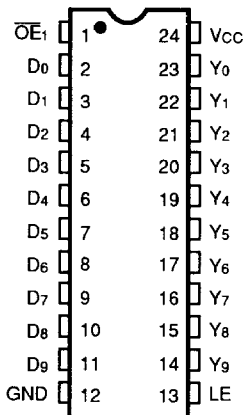


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**CONNECTION DIAGRAMS**  
Top View

**Am29841**

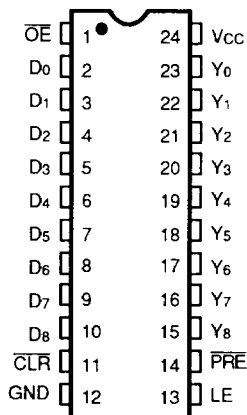
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**Am29843**

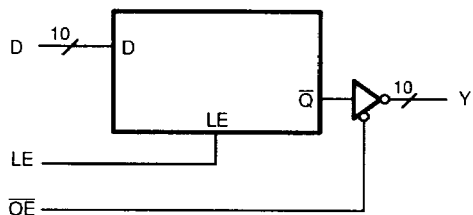
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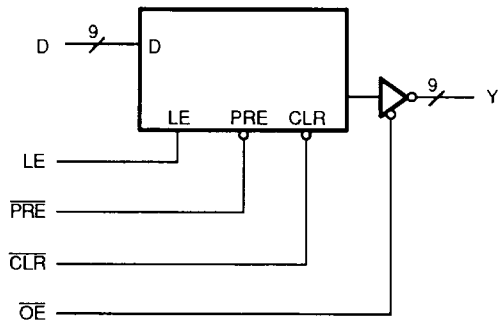
**LOGIC SYMBOLS**

**Am29841**  
**10-Bit Latch**



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**Am29843**  
**9-Bit Latch**



01972-006A

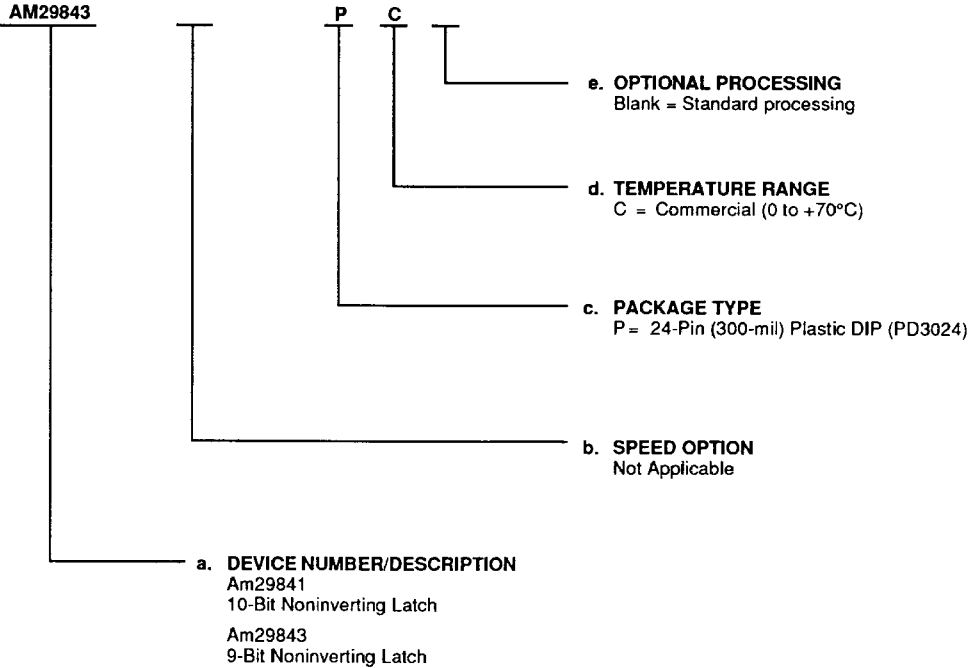
## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing

AM29841  
AM29843



Valid Combinations	
AM29841	PC
AM29843	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

**PIN DESCRIPTION**

**CLR**

When  $\overline{\text{CLR}}$  is LOW, the outputs are LOW if  $\overline{\text{OE}}$  is LOW.  
When  $\overline{\text{CLR}}$  is HIGH, data can be entered into the latch.

**D<sub>i</sub>**

The latch data inputs.

**LE**

The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.

**Y<sub>i</sub>**

The 3-state latch outputs.

**$\overline{\text{OE}}$**

The output enable control. When  $\overline{\text{OE}}$  is LOW, the outputs are enabled. When  $\overline{\text{OE}}$  is HIGH, the outputs Y<sub>i</sub> are in the high-impedance (off) state.

**$\overline{\text{PRE}}$**

Preset line. When  $\overline{\text{PRE}}$  is LOW, the outputs are HIGH if  $\overline{\text{OE}}$  is LOW. Preset overrides  $\overline{\text{CLR}}$ .

**FUNCTION TABLES**

**Am29841**

Inputs			Internal	Outputs	Function
$\overline{\text{OE}}$	LE	D <sub>i</sub>	$\overline{\text{Q}}_i$	Y <sub>i</sub>	
H	X	X	X	Z	Hi-Z
H	H	L	H	Z	Hi-Z
H	H	H	L	Z	Hi-Z
H	L	X	NC	Z	Latched (Hi-Z)
L	H	L	H	L	Transparent
L	H	H	L	H	Transparent
L	L	X	NC	NC	Latched

**Am29843**

Inputs				Internal	Outputs	Function	
$\overline{\text{CLR}}$	$\overline{\text{PRE}}$	$\overline{\text{OE}}$	LE	D <sub>i</sub>	$\overline{\text{Q}}_i$		Y <sub>i</sub>
H	H	H	X	X	X	Z	Hi-Z
H	H	H	H	L	H	Z	Hi-Z
H	H	H	H	H	L	Z	Hi-Z
H	H	H	L	X	NC	Z	Latched (Hi-Z)
H	H	L	H	L	H	L	Transparent
H	H	L	H	H	L	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	L	H	Preset
L	H	L	X	X	H	L	Clear
L	L	L	X	X	L	H	Preset
L	H	H	L	X	L	Z	Latched (Hi-Z)
H	L	H	L	X	L	Z	Latched (Hi-Z)

- H = HIGH
- L = LOW
- X = Don't Care
- NC = No Change
- Z = High Impedance

**ABSOLUTE MAXIMUM RATINGS**

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential Continuous	-0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	-0.5 V to +5.5 V
DC Input Voltage	-0.5 V to +5.5 V
DC Output Current, Into Outputs	100 mA
DC Input Current	-30 mA to +5.0 mA

**OPERATING RANGES****Commercial (C) Devices**

Ambient Temperature (T <sub>A</sub> )	0°C to +70°C
Supply Voltage (V <sub>CC</sub> )	5.0 V ± 10% - 4.5 V to 5.5 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*





**DC CHARACTERISTICS over operating ranges unless otherwise specified**

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = 4.5 V V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -15 mA I <sub>OH</sub> = -24 mA	2.4 2.0	V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = 4.5 V V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 48 mA	0.5	V
V <sub>IH</sub>	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0		V
V <sub>IL</sub>	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		0.8	V
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA		-1.2	V
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.4 V		-1.0	mA
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 2.7 V		50	μA
I <sub>I</sub>	Input HIGH Current	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V		1.0	mA
I <sub>OZ</sub>	Output Off-State (Hi-Z) Output Current	V <sub>CC</sub> = 5.5 V	V <sub>O</sub> = 0.4 V V <sub>O</sub> = 2.4 V	-50 50	μA
I <sub>SC</sub>	Output Short Circuit Current (Note 1)	V <sub>CC</sub> = 5.5 V		-75 -250	mA
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = 5.5 V Outputs Open	Over Temperature Range +70°C	120 110	mA

**Note:**

1. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

**SWITCHING CHARACTERISTICS** ( $T_A = +25^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V}$ )

Parameter Symbol	Parameter Description		Test Conditions (Note 1)	Min.	Typ.	Max.	Unit
t <sub>PLH</sub>	Data (D <sub>i</sub> ) to Output Y <sub>i</sub> (LE = HIGH)		C <sub>L</sub> = 50 pF	3.5	5.7	8	ns
t <sub>PHL</sub>				3.5	6.2	8	ns
t <sub>PLH</sub>			C <sub>L</sub> = 300 pF		10	13	ns
t <sub>PHL</sub>					10	13	ns
t <sub>s</sub>	Data to LE Setup Time		C <sub>L</sub> = 50 pF	2.0	-0.2		ns
t <sub>H</sub>	Data to LE Hold Time			2.5	0.7		ns
t <sub>PLH</sub>	Latch Enable (LE) to Y <sub>i</sub>		C <sub>L</sub> = 50 pF		8	10.5	ns
t <sub>PHL</sub>					7.5	10	ns
t <sub>PLH</sub>			C <sub>L</sub> = 300 pF			15	ns
t <sub>PHL</sub>						15	ns
t <sub>PLH</sub>	Propagation Delay, Preset to Y <sub>i</sub>		C <sub>L</sub> = 50 pF		6.5	9	ns
t <sub>s</sub>	Preset Recovery ( $\overline{\text{PRE}}$  ) Time				7.3	12	ns
t <sub>PHL</sub>	Propagation Delay, Clear to Y <sub>i</sub>				15	18	ns
t <sub>s</sub>	Clear Recovery ( $\overline{\text{CLR}}$  ) Time				7.8	12	ns
t <sub>PWH</sub>	LE Pulse Width	HIGH	C <sub>L</sub> = 50 pF	4	2.5		ns
t <sub>PWL</sub>	Preset Pulse Width	LOW		5			ns
t <sub>PWL</sub>	Clear Pulse Width	LOW		6			ns
t <sub>ZH</sub>	Output Enable Time $\overline{\text{OE}}$  to Y <sub>i</sub>		C <sub>L</sub> = 300 pF			17	ns
t <sub>ZL</sub>						21	ns
t <sub>ZH</sub>			C <sub>L</sub> = 50 pF		7.3	12	ns
t <sub>ZL</sub>					9.7	12	ns
t <sub>HZ</sub>	Output Disable Time $\overline{\text{OE}}$  to Y <sub>i</sub>		C <sub>L</sub> = 50 pF		10.4	14	ns
t <sub>LZ</sub>					4.7	11	ns
t <sub>HZ</sub>			C <sub>L</sub> = 5 pF (Note 2)		3.4	8	ns
t <sub>LZ</sub>					3.8	8	ns

**Notes:**

1. See test circuit and waveforms (Chapter 2).
2. Not tested.

**SWITCHING CHARACTERISTICS** over operating ranges unless otherwise specified

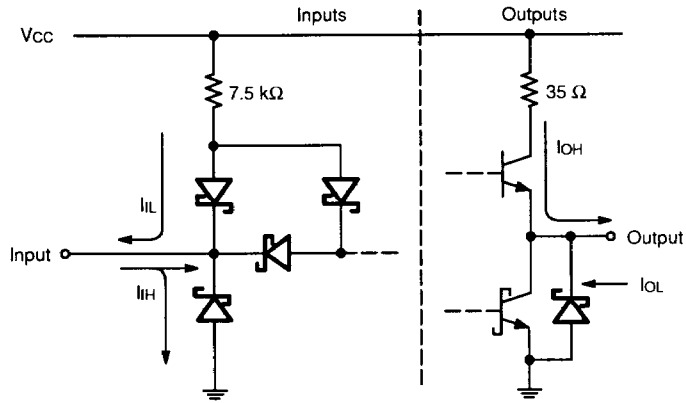
Parameter Symbol	Parameter Description		Test Conditions (Note 1)	Min.	Max.	Unit	
t <sub>PLH</sub>	Data (D <sub>i</sub> ) to Output Y <sub>i</sub> (LE = HIGH)		C <sub>L</sub> = 50 pF	3.5	9.5	ns	
t <sub>PHL</sub>				3.5	9.5	ns	
t <sub>PLH</sub>			C <sub>L</sub> = 300 pF			12.5	ns
t <sub>PHL</sub>						13	ns
t <sub>s</sub>	Data to LE Setup Time		C <sub>L</sub> = 50 pF	2.5		ns	
t <sub>h</sub>	Data to LE Hold Time			2.5		ns	
t <sub>PLH</sub>	Latch Enable (LE) to Y <sub>i</sub>		C <sub>L</sub> = 50 pF		12	ns	
t <sub>PHL</sub>					12	ns	
t <sub>PLH</sub>			C <sub>L</sub> = 300 pF			16	ns
t <sub>PHL</sub>						16	ns
t <sub>PLH</sub>	Propagation Delay, Preset to Y <sub>i</sub>		C <sub>L</sub> = 50 pF		12	ns	
t <sub>s</sub>	Preset Recovery ( $\overline{\text{PRE}}_{\text{f}}$ ) Time				14	ns	
t <sub>PHL</sub>	Propagation Delay, Clear to Y <sub>i</sub>				21	ns	
t <sub>s</sub>	Clear Recovery ( $\overline{\text{CLR}}_{\text{f}}$ ) Time				14	ns	
t <sub>PWH</sub>	LE Pulse Width	HIGH	C <sub>L</sub> = 50 pF	6		ns	
t <sub>PWL</sub>	Preset Pulse Width	LOW		8		ns	
t <sub>PWL</sub>	Clear Pulse Width	LOW		8		ns	
t <sub>ZH</sub>	Output Enable Time $\overline{\text{OE}}_{\text{f}}$ to Y <sub>i</sub>		C <sub>L</sub> = 300 pF		20	ns	
t <sub>ZL</sub>					23	ns	
t <sub>ZH</sub>			C <sub>L</sub> = 50 pF			14	ns
t <sub>ZL</sub>						14	ns
t <sub>HZ</sub>	Output Disable Time $\overline{\text{OE}}_{\text{f}}$ to Y <sub>i</sub>		C <sub>L</sub> = 50 pF		15	ns	
t <sub>LZ</sub>					12	ns	
t <sub>HZ</sub>			C <sub>L</sub> = 5 pF			9	ns
t <sub>LZ</sub>						9	ns

**Note:**

1. See test circuit and waveforms (Chapter 2).



**INPUT/OUTPUT CURRENT INTERFACE CONDITIONS**

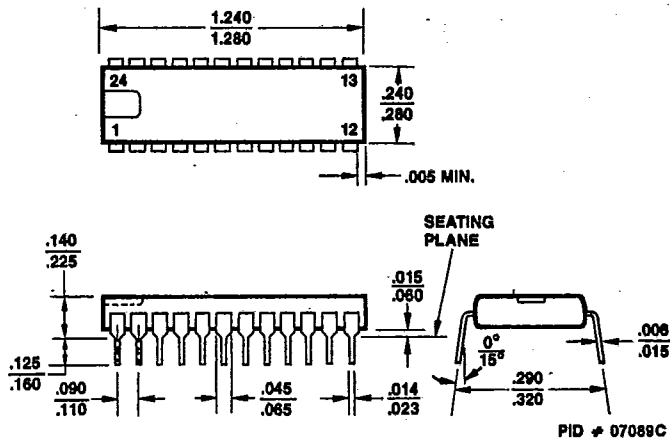


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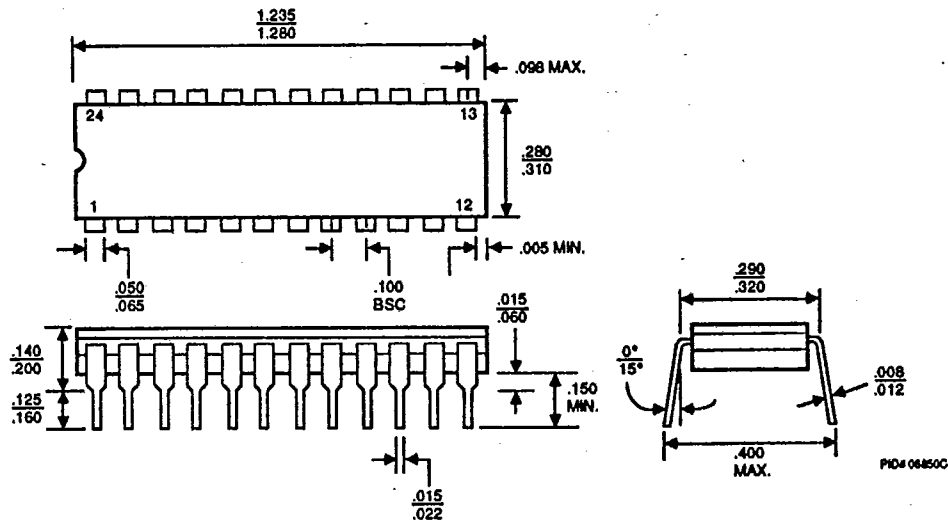
PACKAGE OUTLINES\*

T-90-20

PD3024



CD3024

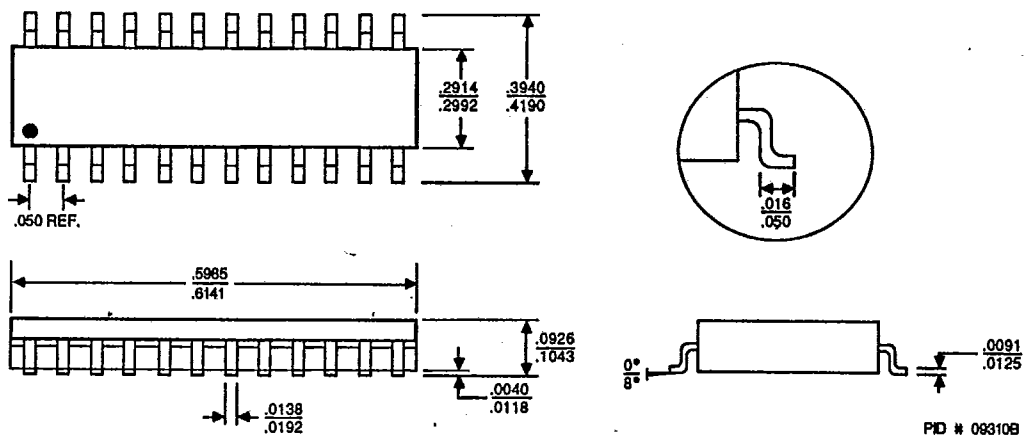


\*For reference only.

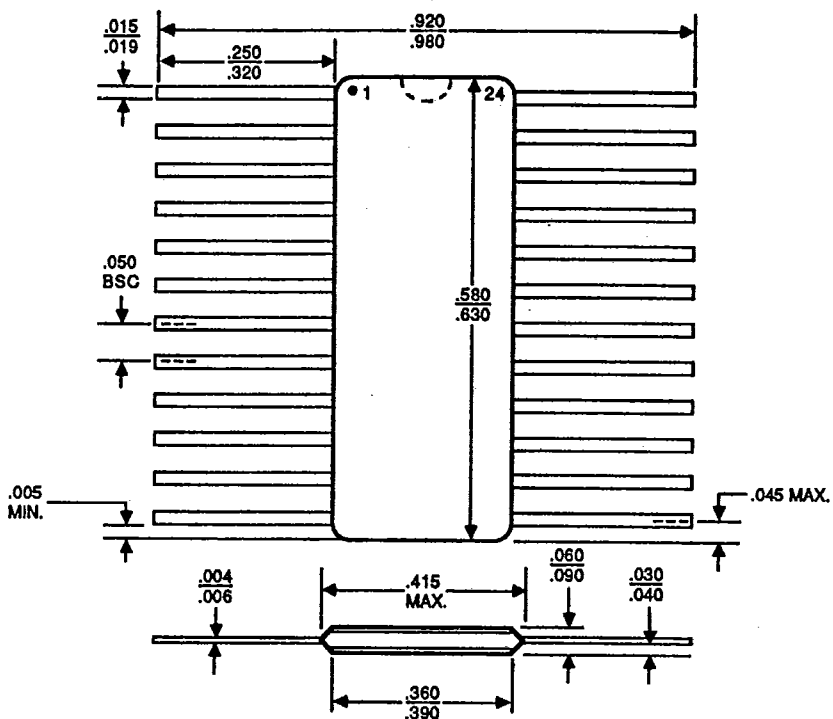
PACKAGE OUTLINES (Cont'd.)

T-90-20

SO 024



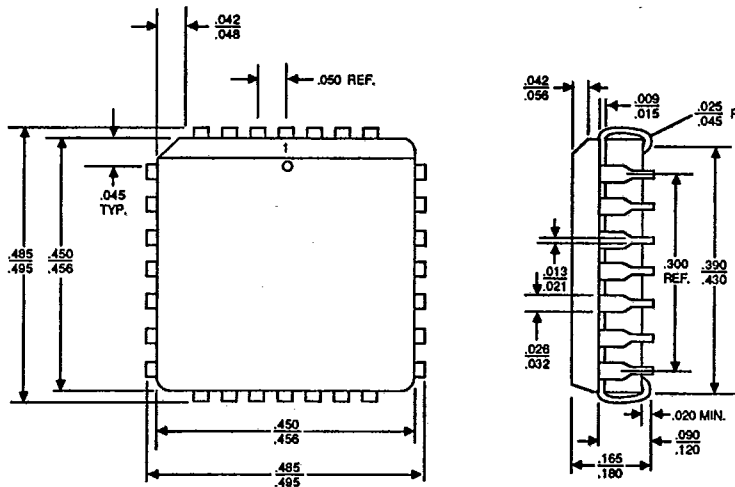
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PACKAGE OUTLINES (Cont'd.)

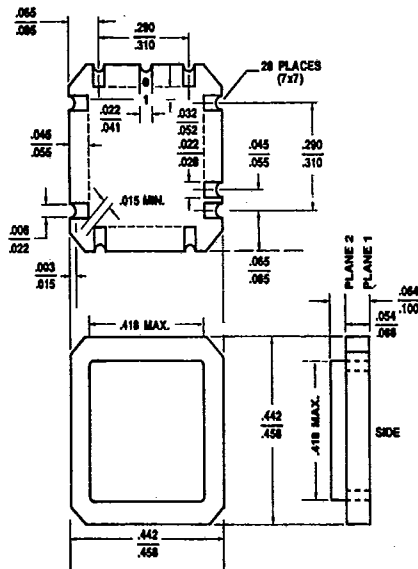
T-90-20

PL 028



PID # 06751E

CL 028



PID # 06595D

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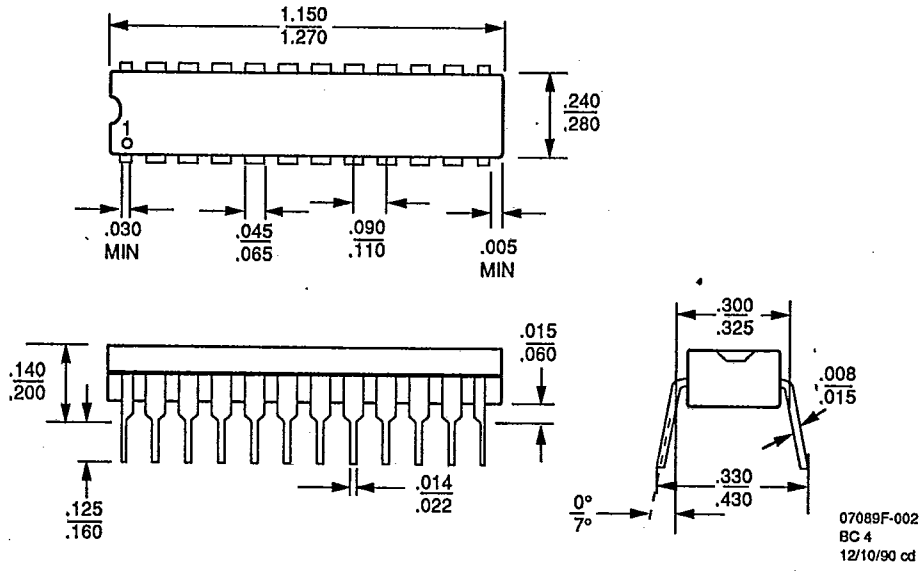


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**PD3024**  
**24-Pin 300-mil Plastic SKINNYDIP**

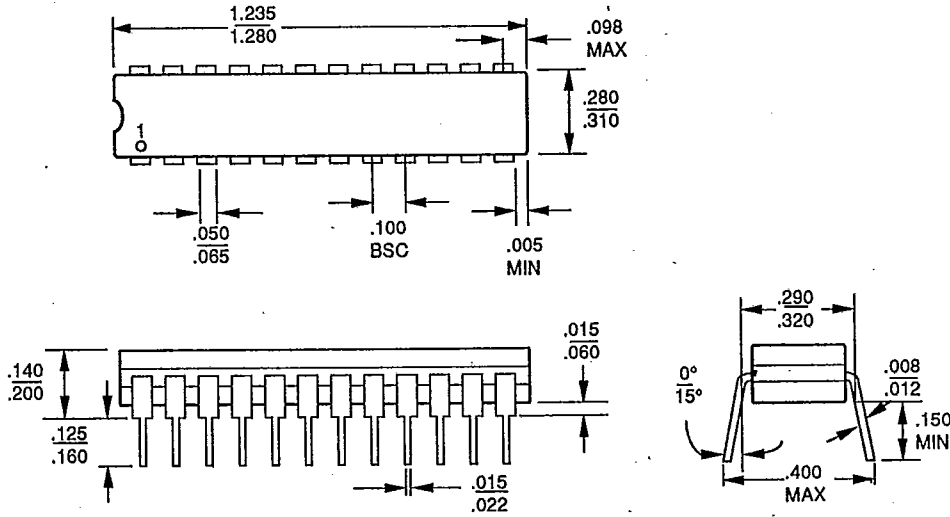
T-90-20



**Note:**  
For reference only. All dimensions measured in inches. BSC is an ANSI standard for Basic Space Centering.

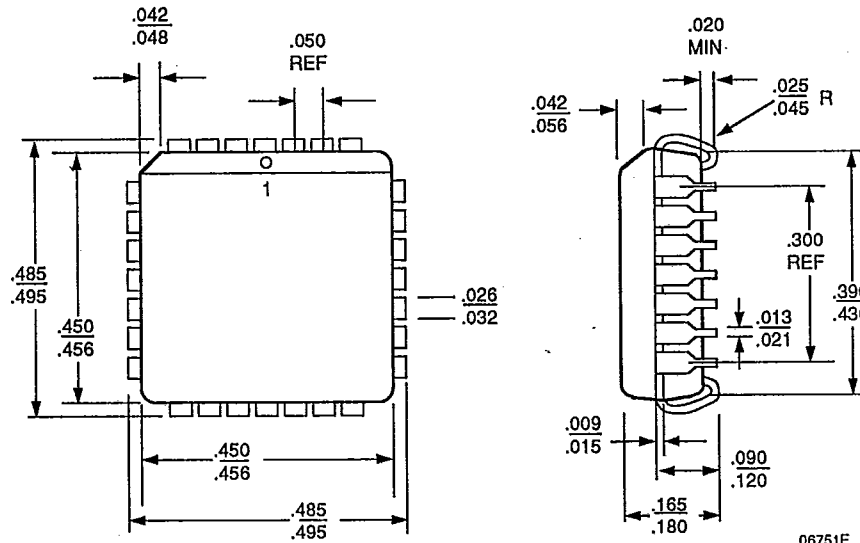
T-90-20

**CD3024**  
**24-Pin 300-mil Ceramic SKINNYDIP**



06850C

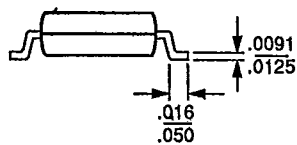
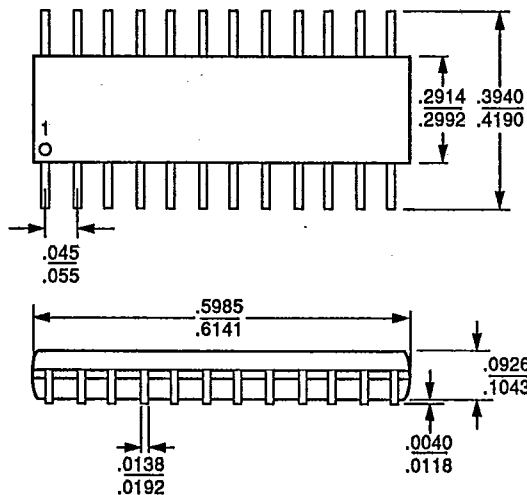
**PL 028**  
**28-Pin Plastic Leaded Chip Carrier**



06751E

**SO 024**  
**24-Pin Plastic Small Outline Package**

T-90-20



09310B