CDB5560-2

50 kSps, 24-bit ΔΣ ADC Evaluation Board

Features

- Single Analog Input Channel to the CS5560 ADC
- Pre-configured to require a minimum number of external connections to your data acquisition system.
- All functionality accessible through the connector interface and board-level options.
- On-board 4.096 V Reference
- Pre-configured for Master mode SPI™ communication to a data capture system.

General Description

The CDB5560-2 is a versatile tool designed for evaluating the functionality and performance of the CS5560 ADC (Analog-to-Digital Converter). The SPI serial port on the CDB5560-2 evaluation board is configured in Master mode and will start transmitting data after power-up upon reset. This evaluation board is designed to connect to your data capture system or will interface to the CapturePlus II data acquisition system available from Cirrus Logic.

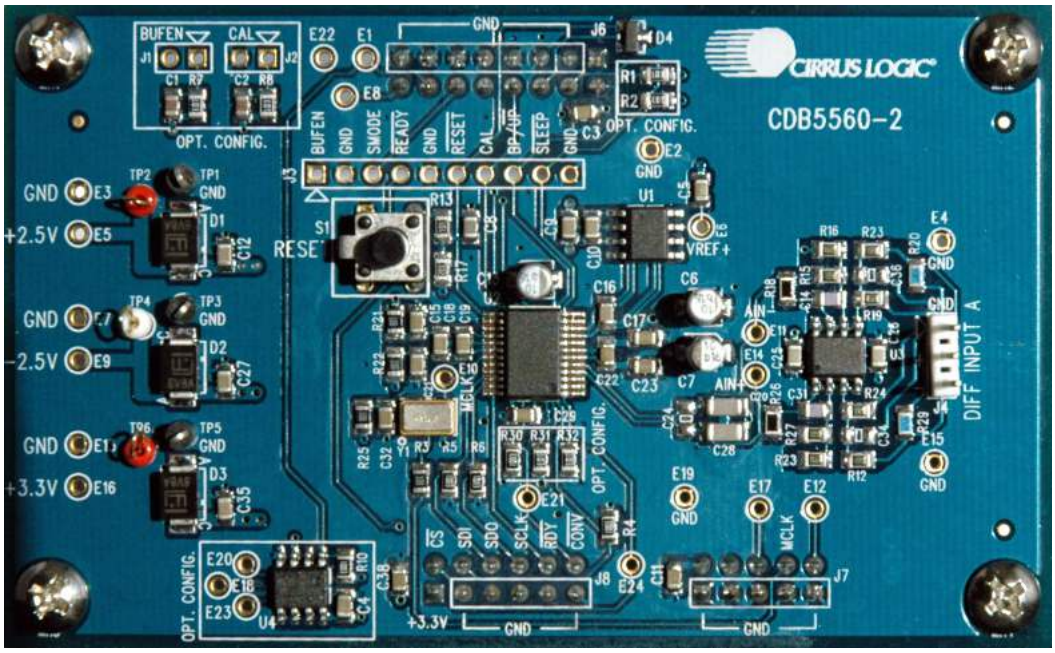
The CS5560 delta-sigma ADC produces fully settled conversions to full specified accuracy at 50 kSps. .

All evaluation board functionality for evaluating the CS5560 ADC is accessed through the connector interface and board-level options.

Schematics in PADS™ PowerLogic™ format are available for download at:
http://www.cirrus.com/en/products/pro/detail/P1120.html.

ORDERING INFORMATION

CDB5560-2	Evaluation Board



Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative. To find the one nearest to you go to www.cirrus.com

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1. INTRODUCTION

The CDB5560-2 evaluation board is a platform for evaluating the CS5560 ADC performance. The evaluation board is designed to connect to the SPI serial port of a processor or data capture system or will interface directly to the CapturePlus II data acquisition system available from Cirrus Logic. The CapturePlus II data acquisition system is a powerful integrated hardware/software tool designed to fully exercise the CDB5560-2 and other Cirrus Logic evaluation boards.

The CDB5560-2 evaluation board is designed to simplify the hardware setup required to evaluate the CS5560. Interfacing the CDB5560-2 evaluation board to a user-supplied data capture system can be as simple as connecting the SPI port and using the CDB5560-2 default hardware configuration. In this configuration simply press the Reset switch on the CDB5560-2 and it will automatically begin transmitting data to the data capture system.

All evaluation board functionality for evaluating the CS5560 ADC is accessed through the connector interface and board-level options.

The CS5560 delta-sigma ADC produces fully settled conversions to full specified accuracy at 50 kSps.

For detailed information on the CS5560 ADC, please reference data sheet DS713 at www.cirrus.com.

1.1 Overview

The CDB5560-2 evaluation board has both analog and digital circuit sections. The analog section consists of the CS5560 ADC, an analog input signal buffer that conditions the signal into the ADC, and a precision 4.096 V reference. The digital section consists of board operation configuration control signals, reset circuitry, an SPI™ serial port, a jumper connection for initiating ADC calibration, and an EEPROM for evaluation board identification.

The evaluation board operates from +2.5V, -2.5V, +3.3V and communicates through an SPI™ serial port.

Figure 1 illustrates the CDB5560-2 block diagram.

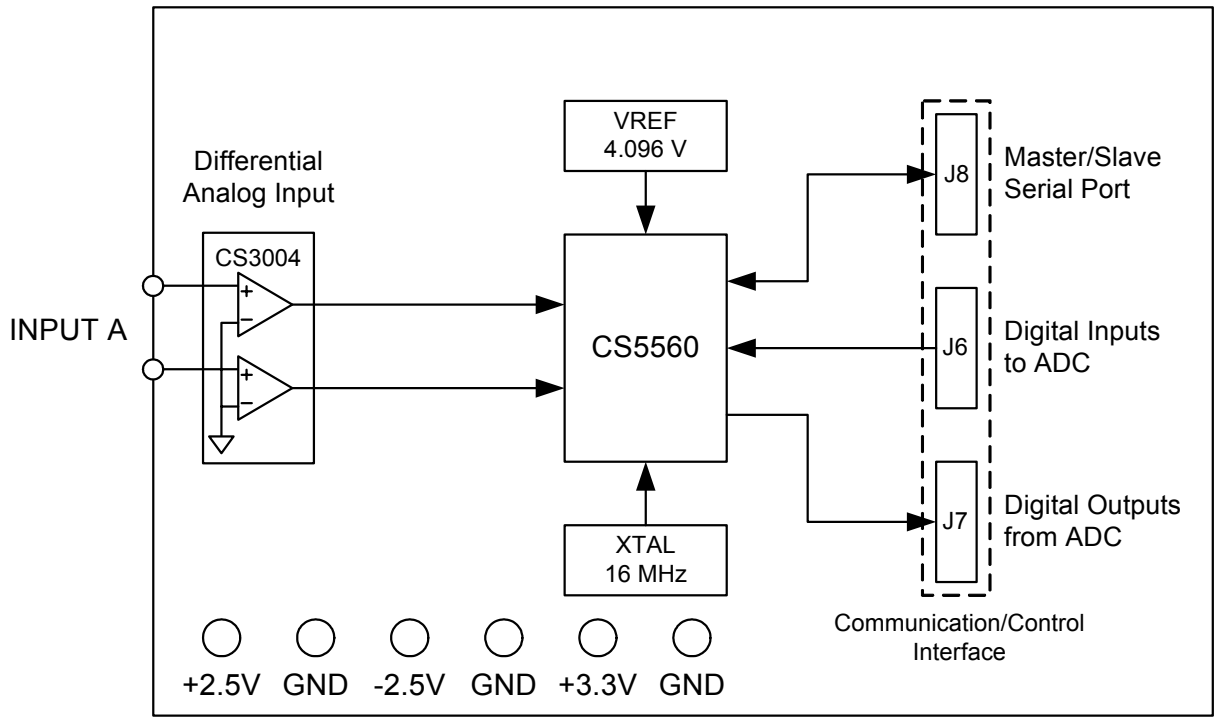
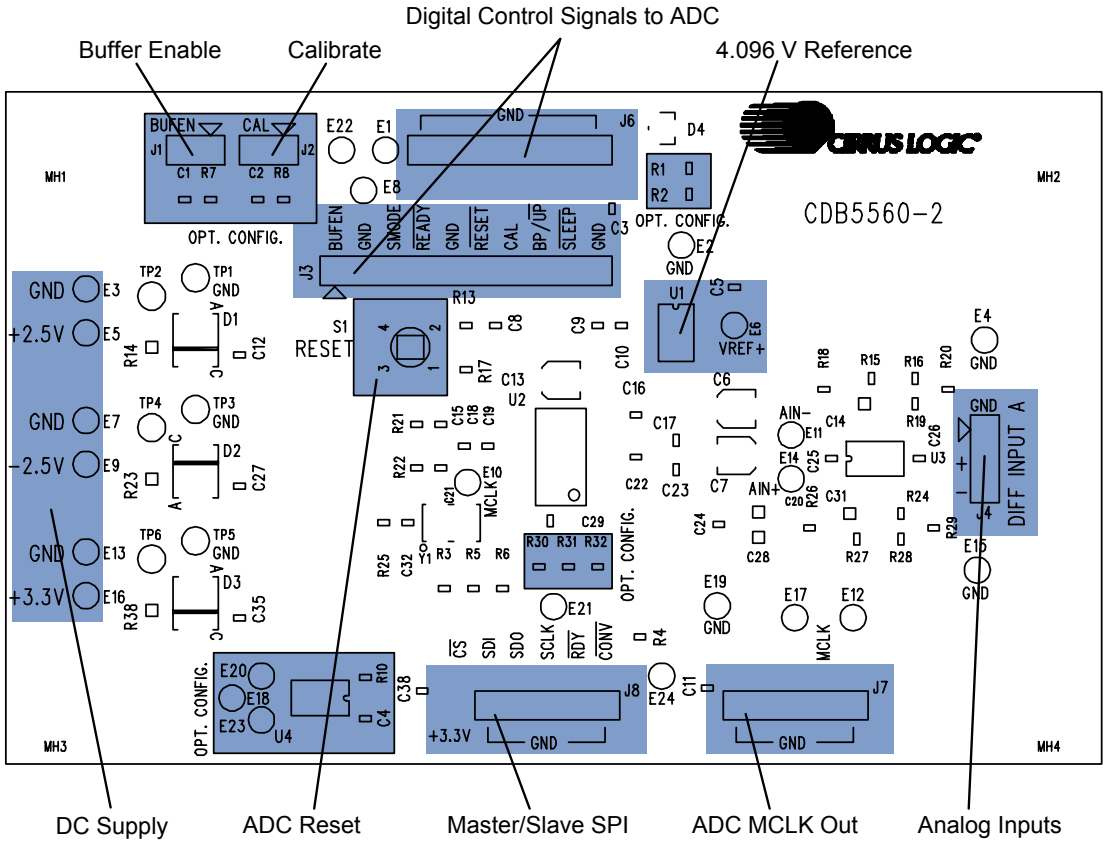


Figure 1. CDB5560-2 Block Diagram

2. QUICK START



NOTE: Shaded boxes marked with "OPT. CONFIG." are not necessary for operation in an end user product.

Figure 2. CDB5560-2 Board Layout

The CDB5560-2 evaluation board is designed to interface with a data acquisition system. To connect and configure the CDB5560-2 perform the following initialization procedure:

1. Verify that the power supplies are off.
2. Connect the power supplies to the CDB5560-2 as shown in Table 1 on page 7.
3. Verify that the power is off to the analog input signal & control signal sources.
4. Connect the analog input signal source to the evaluation board per Table 2 on page 7. .
5. Configure the CDB5560-2 by connecting the control signal sources to the evaluation board as shown in Table 3 on page 9. Apply logic-level inputs as required to override the resistor pull-ups/pull-downs.
6. Make connections to the SPI™ serial port connector as shown in Table 4 on page 9. The CS5560 ADC serial port is configured by default to operate in the SSC (Synchronous Self Clocking) mode. Refer to the CS5560 data sheet for more information on serial communication modes and signal timing.
7. Turn on the power supplies to the evaluation board.
8. Apply power to the signal source.
9. Press the Reset switch on the evaluation board.
10. The CS5560 ADC's SPI™ serial port should now be communicating data.

3. HARDWARE DESCRIPTION

3.1 Absolute Maximum Ratings

Observe the following limits to ensure the CDB5560-2 component ratings are not exceeded.

- **CS5560**
  - The absolute maximum supply voltage that can be applied to the +3.3V power supply connection is +3.6V.
  - The absolute maximum power supply voltage that can be applied between pins VL and V1- is 6.1 V.
- **CS3004**
  - The absolute maximum power supply voltage that can be applied between the +2.5V and -2.5V power supply connections is +5.5V.

3.2 Power Supply

Power supply connections and requirements are specified in Table 1. below.

Table 1. Power Supply Connections

Power Supply Requirement	Power Supply Connection	Associated Ground Return	Associated Test Points
+2.5 V DC, ±5%, <50 mA	E5	E3	TP2, TP1 (GND)
-2.5 V DC, ±5%, <50 mA	E9	E7	TP4, TP3 (GND)
+3.3 V DC, ±5%, <50 mA	E16	E13	TP6, TP5 (GND)

Important: It is recommended that all power supplies be isolated from utility ground to prevent the introduction of a ground loop. One ground connection may already exist through the serial port connection to utility ground. Using the Cirrus Logic CapturePlus II system simplifies making connections to the CDB5560-2 by providing electrical isolation between the two.

Using twisted/shielded wire will reduce electrical noise induced onto the power supply cables.

Power supplies are to be adequately regulated and sufficiently low noise to meet the application requirements.

3.3 Analog Section

3.3.1 Analog Input Buffers

The analog input signal connections to the input buffers are made at the INPUT A connector, as specified in Table 2.

Table 2. Analog Input Connection

Channel	Analog Input Connection	Differential Input Signal Voltage Range	Impedance
INPUT A	J4	-4.096 V to +4.096 V	50 Ohms

There is one analog input channel on the evaluation board. The analog input channel consists of two low-noise amplifiers configured as unity gain non-inverting buffers. The buffers utilize a Cirrus Logic CS3004 precision, low-noise, low-voltage, dual op-amp These op-amps enable both the inputs and outputs of the analog input buffer to operate virtually rail to rail. The channel input impedance is 50 Ohms.

For detailed information on the CS3004 precision industrial op-amps, please reference data sheet DS719 at www.cirrus.com.

The theoretical input frequency range of the CS5560 is from DC to the Nyquist frequency of 25 kHz. The analog input buffer amplifiers are configured for a cutoff frequency of 16.8 kHz to band-limit noise into the ADC. Changing the cutoff frequency will change the noise bandwidth accordingly.

3.3.2 ADC Reset

The CS5560 ADC makes use of an externally generated power-on reset. Therefore, after power is applied to the ADC, the reset pin must be driven low then released. Pressing the Reset button generates a reset cycle. A reset cycle can be generated at any time during ADC operation. The ADC $\overline{\text{RST}}$ pin (active low) is held inactive through a pull-up resistor.

3.3.3 Voltage Reference

The voltage reference IC provided generates a 4.096 V precision reference.

3.3.4 ADC Reference Frequency

The reference frequency for the CS5560 ADC is provided by a 16.000 MHz oscillator.

3.4 Digital Section

3.4.1 Hardware Configuration

The CDB5560-2 evaluation board hardware comes pre-configured so the only connection required between it and a data acquisition system is the serial port connection.

The hardware setup is reconfigurable through the hardware control interface connectors. Configure the evaluation board by setting the appropriate control line to the appropriate logic level.

Table 3. Hardware Configuration Signals

Function	Default Level	Label	Connector	Test Point
Analog Input Buffers	Buffers = Enabled (High)	BUFEN	J1	J3, Pin1
Serial Port Mode	Sync. Self Clock = Enabled (High)	SMODE	J6, Pin 12	J3, Pin 3
Data Ready Flag	Data Ready When Set (Low)	$\overline{\text{RDY}}$	J8, Pin 10	J3, Pin 4
Reset	Reset = Inactive (High)	$\overline{\text{RST}}$	J6, Pin 6; S1	J3, Pin 6
Self Calibration Mode	Calibration = Inactive (Low)	CAL	J6, Pin 8; J2	J3, Pin 7
Bipolar / Unipolar Mode	Bipolar = Enabled (High)	BP / $\overline{\text{UP}}$	J6, Pin 2	J3, Pin 8
Sleep Mode	Sleep = Inactive (High)	$\overline{\text{SLEEP}}$	J6, Pin 4	J3, Pin 9
Serial Port Communication	Chip Select = Enabled (Low)	$\overline{\text{CS}}$	J8, Pin 2	E23
Data Conversion Mode	Continuous Conversion = Active (Low)	$\overline{\text{CONV}}$	J8, Pin 12	E21

3.4.2 SPI™ Serial Port Communications

The CS5560 ADC communications port features an SPI™ serial port. It can be configured for SSC mode (Master) or SEC mode (Slave) mode as shown in Table 4. Test points are provided to monitor serial communications.

Connections to the serial interface are made according to the following table.

Table 4. Serial Interface Connections

Function	Label	Connector	Test Point
Chip Select	$\overline{\text{CS}}$	J8, Pin 2	E23
Serial Data Input	SDI	J8, Pin 4	E24
Serial Data Output	SDO	J8, Pin 6	E25
Serial Clock	SCLK	J8, Pin 8	E26

APPENDIX A. MAXIMIZING THE PERFORMANCE OF THE CS5560

A.1 PCB Layout Considerations

- Keep the signal path short between the CS5560 ADC input capacitors C20, C28 and the ADC input pins to minimize trace inductance.
- Power supply noise is a major design consideration and the power supplies need adequate bypassing and bulk capacitance.
- When operating the ADC from +2.5 V and -2.5 V split supplies, place the power supply & buffer amplifier bypass capacitor ground connections close together.
- Keep all ground connections on each differential buffer amplifier as close to the device as possible to avoid introducing differential noise through high-impedance connections.
- Keep trace lengths short between the ADC and the voltage reference IC negative supply pins.
- Route the oscillator output away from analog circuitry.
- Use a solid ground plane in the PCB layout.
- Provide adequate separation between analog and digital signals.
- To minimize distortion within the analog signal path, consider using components with smaller voltage dependencies.
- Minimize ADC digital output edge transition current loading.

A.2 Hardware Considerations

At a system level, use shielded cable for interconnects. Keep interconnect cable lengths as short as possible. Route analog and digital signals connecting to the PCB away from each other.

APPENDIX B. BILL OF MATERIALS

Item	Cirrus P/N	Rev	Description	Qty	Reference Designator	MFG	MFG P/N	Notes
1	001-03713-Z1	A	CAP 1000pF ±10% 50V X7R NPb 0805	2	C1 C2	KEMET	C0805C102K5RAC	
2	001-04345-Z1	A	CAP 0.1uF ±10% 50V X7R NPb 0805	22	C3 C4 C5 C9 C10 C11 C12 C15 C16 C17 C18 C19 C21 C22 C23 C25 C26 C27 C29 C32 C35 C38	KEMET	C0805C104K5RAC	
3	012-00012-Z1	A	CAP 10uF ±20% 16V ELEC NPb CASE A	3	C6 C7 C13	PANASONIC	EEE1CS100SR	
4	001-03987-Z1	A	CAP 4700pF ±10% 50V X7R NPb 0805	1	C8	KEMET	C0805C472K5RAC	
5	001-02976-Z1	A	CAP 47pF ±10% 50V C0G NPb 0805	2	C14 C31	KEMET	C0805C470K5GAC	
6	001-06472-Z1	A	CAP 4700pF ±5% 50V C0G NPb 1206	2	C20 C28	KEMET	C1206C472J5GAC	
7	001-03710-Z1	A	CAP 1000pF ±5% 50V C0G NPb 0805	0	C24	KEMET	C0805C102J5GAC	NO POP
8	001-10036-Z1	A	CAP 2200pF ±5% 50V C0G NPb 0805	0	C34 C36	KEMET	C0805C222J5GAC	NO POP
9	070-00111-Z1	A	DIODE TR 6.8V 600W NPb DO-214AA	3	D1 D2 D3	LITTELFUSE	P6SMBJ6.8A	
10	070-00010-Z1	A	DIODE SCHTKY BAR 30V 0.2A NPb SOT23	1	D4	PHILIPS	BAT54	
11	000-00025-Z1	A	NO POP 040 PAD 064 NPb TH	0	E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 E11 E12 E13 E14 E15 E16 E17 E18 E19 E20 E21 E22 E23 E24	NO POP	NP-PAD-040	NO POP
12	115-00052-Z1	A	HDR 2x1 ML .1"CTR 093 GLD NPb	0	J1 J2	SAMTEC	TSW-102-26-G-S	NO POP
13	115-00217-Z1	A	HDR 10X1 FML .1" 093 GLD NPb TH	0	J3	SAMTEC	SSW-110-01-G-S	NO POP
14	115-00202-Z1	A	HDR 3X1 ML .1" PCH .062BD NPb TH	1	J4	MOLEX	22-66-2030	
15	115-00239-Z1	A	HDR 8X2 093BD FML .1" .331" NPb TH	1	J6	SAMTEC	SSW-108-01-G-D	
16	115-00238-Z1	A	HDR 5X2 093BD FML .1" .331" NPb TH	1	J7	SAMTEC	SSW-105-01-G-D	
17	115-00241-Z1	A	HDR 6X2 093BD FML .1" .331" NPb TH	1	J8	SAMTEC	SSW-106-01-G-D	
18	304-00012-Z1	A	SPCR STANDOFF NYL HEX750/4-40TH NPb	4	MH1 MH2 MH3 MH4	KEYSTONE	1902D	REQUIRES SCREW 4-40X1X4" PH NYLON, 300-00002-Z1
19	021-00435-Z1	A	RES 10k OHM 1/8W ±5% NPb 0805 FILM	6	R1 R2 R7 R8 R31 R32	DALE	CRCW080510K0JNEA	
20	021-00363-Z1	A	RES 10 OHM 1/8W ±5% NPb 0805 FILM	4	R3 R21 R22 R25	DALE	CRCW080510R0JNEA	
21	020-02044-Z1	A	RES 100k OHM 1/8W ±1% NPb 0805 FILM	5	R4 R5 R6 R10 R30	DALE	CRCW0805100KFKEA	
22	020-01895-Z1	A	RES 4.99k OHM 1/8W ±1% NPb 0805 FLM	8	R12 R15 R16 R19 R23 R24 R27 R28	DALE	CRCW08054K99FKEA	
23	021-00387-Z1	A	RES 100 OHM 1/8W ±5% NPb 0805 FILM	1	R13	DALE	CRCW0805100RJNEA	
24	021-00423-Z1	A	RES 3.3k OHM 1/8W ±5% NPb 0805 FIL	1	R17	DALE	CRCW08053K300JNEA	
25	023-00002-Z1	A	RES 49.9 OHM 1/10W ±.5% NPb 0805 TN	2	R18 R26	SUSUMU	RR1220Q-49R9-D-M	
26	020-01667-Z1	A	RES 49.9 OHM 1/8W ±1% NPb 0805 FILM	2	R20 R29	DALE	CRCW080549R9FKEA	
27	120-00057-Z1	A	SWT SPST 130G 0/1 7mm TACT ESD NPb	1	S1	ITT INDUSTRIES	PTS645TL70	INSTALL AFTER WASH PROCESS
28	110-00045-Z1	A	CON TEST PT .1"CTR TIN PLAT NPb BLK	3	TP1 TP3 TP5	KEYSTONE	5001	
29	110-00024-Z1	A	CON TEST PT .1" TIN PLT RED NPb TH	2	TP2 TP6	KEYSTONE	5000	
30	110-00025-Z1	A	CON TEST PT .1" TIN PLATE WHT NPb	1	TP4	KEYSTONE	5002	
31	060-00351-Z1	A	IC LNR PREC VREF 4.096Vout NPb SO8	1	U1	MAXIM	MAX6126AASA41+	
32	065-00212-Z1	A0	IC CRUS ADC 1CH 24BIT NPb SSOP24	1	U2	CIRRUS LOGIC	CS5560-ISZ/A0	
33	065-00219-Z1	A0	IC CRUS PREC DL LO-V AMP NPb SOIC8	1	U3	CIRRUS LOGIC	CS3004-FSZ/A0	
34	062-00064-Z1	A	IC PGM SPI EEPROM 8kX8 2MHz NPb SO8	1	U4	MICROCHIP	25LC640-I/SN	
35	102-00097-Z1	A	OSC 16MHz 50ppm 3.3V NPb SMD 3x5	1	Y1	ABRACON	ASFL1-16.000MHZ-EC-T	
36	603-00278-Z1	C	ASSY DWG PWA CDB5560-2-Z NPb	REF		CIRRUS LOGIC	603-00278-Z1	
37	240-00278-Z1	C	PCB CDB5560-2-Z NPb	1		CIRRUS LOGIC	240-00278-Z1	
38	600-00278-Z1	C	SCHEM CDB5560-2-Z NPb	REF		CIRRUS LOGIC	600-00278-Z1	
39	300-00002-Z1	A	SCREW 4-40X1/4" PH NYLON NPb	4	XMH1 XMH2 XMH3 XMH4	BUILDING FASTENERS	NY PMS 440 0025 PH	

APPENDIX C. SCHEMATICS

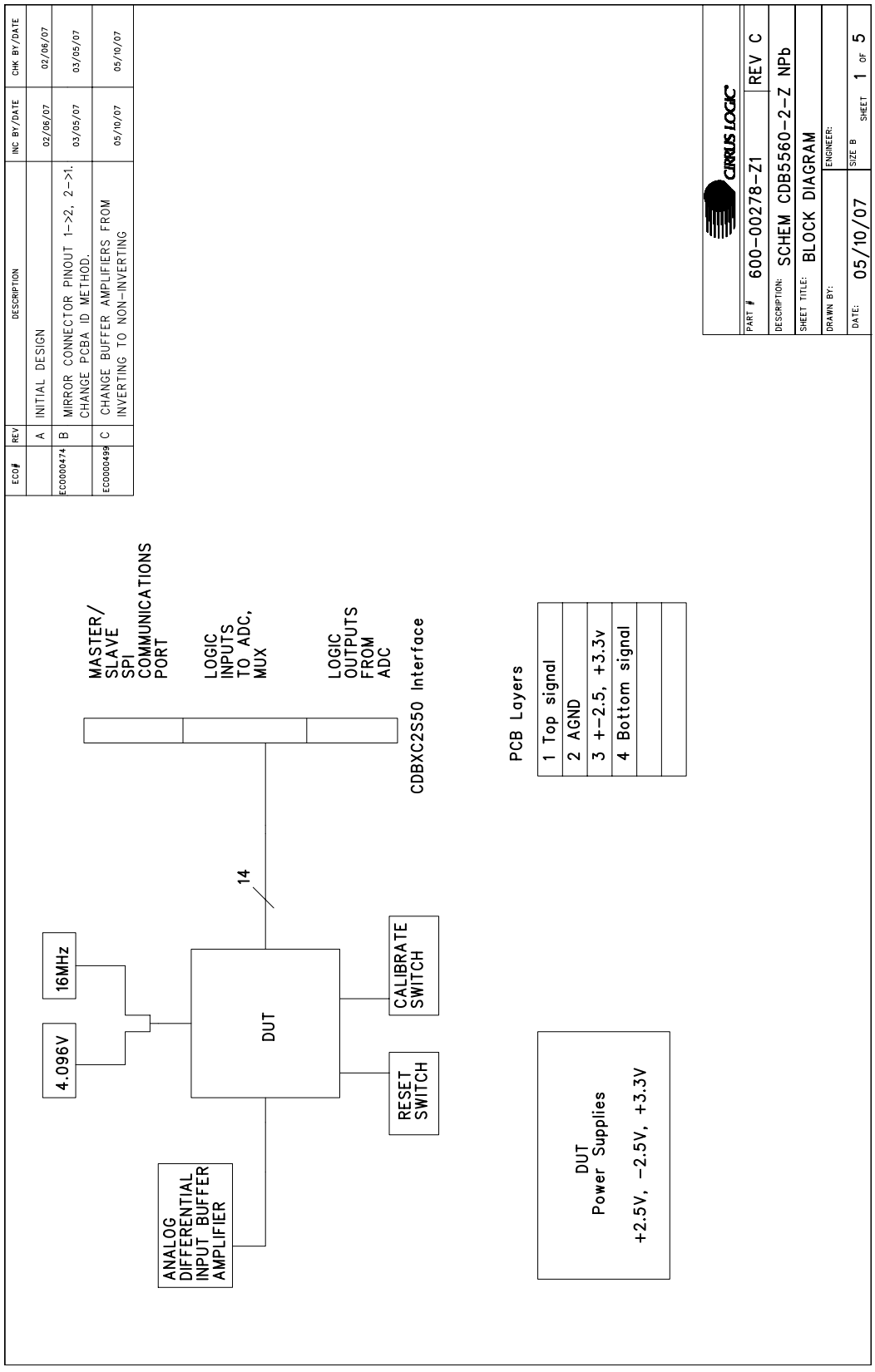


Figure 3. Schematic - Block Diagram

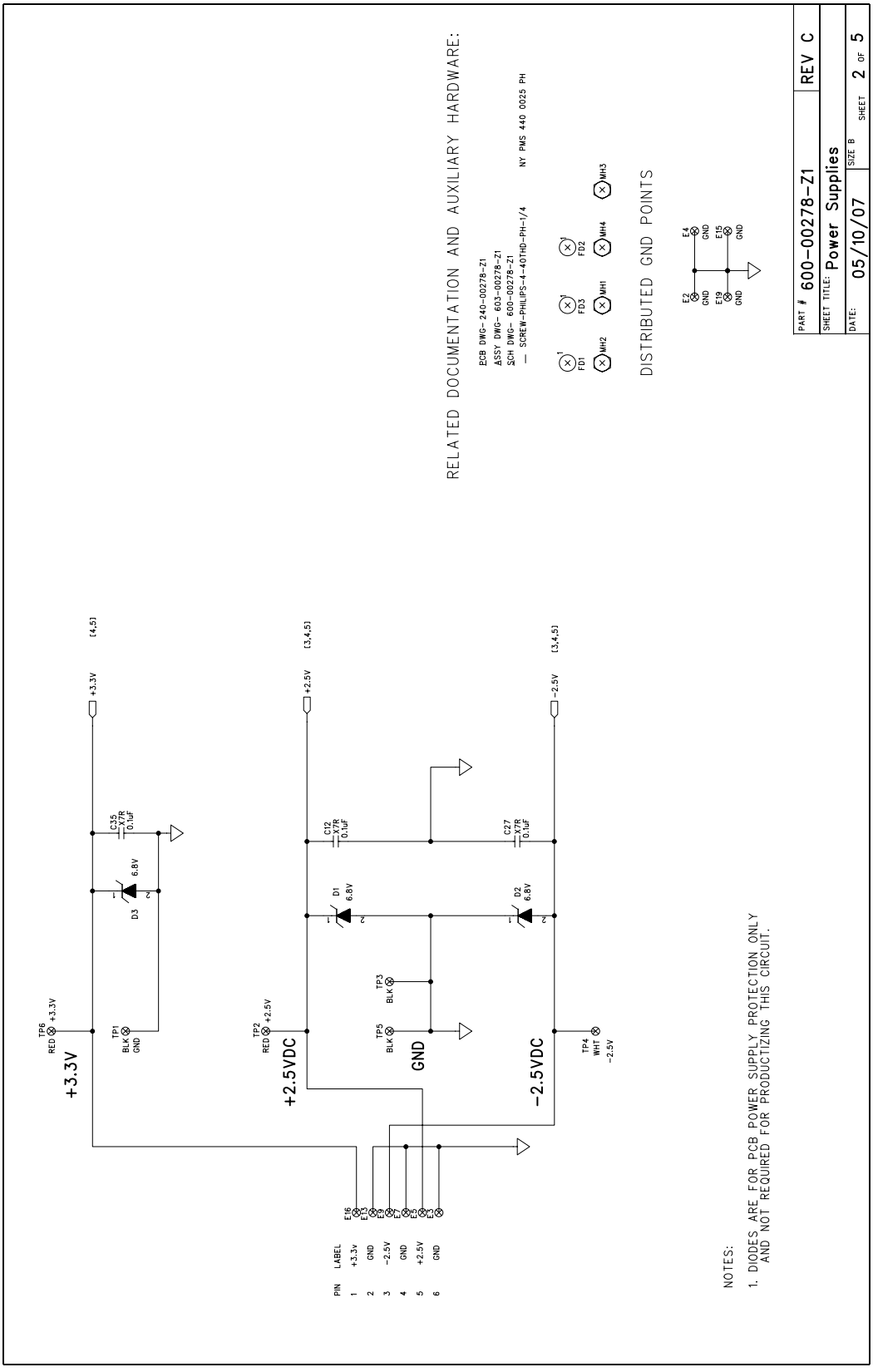


Figure 4. Schematic - Power Supplies

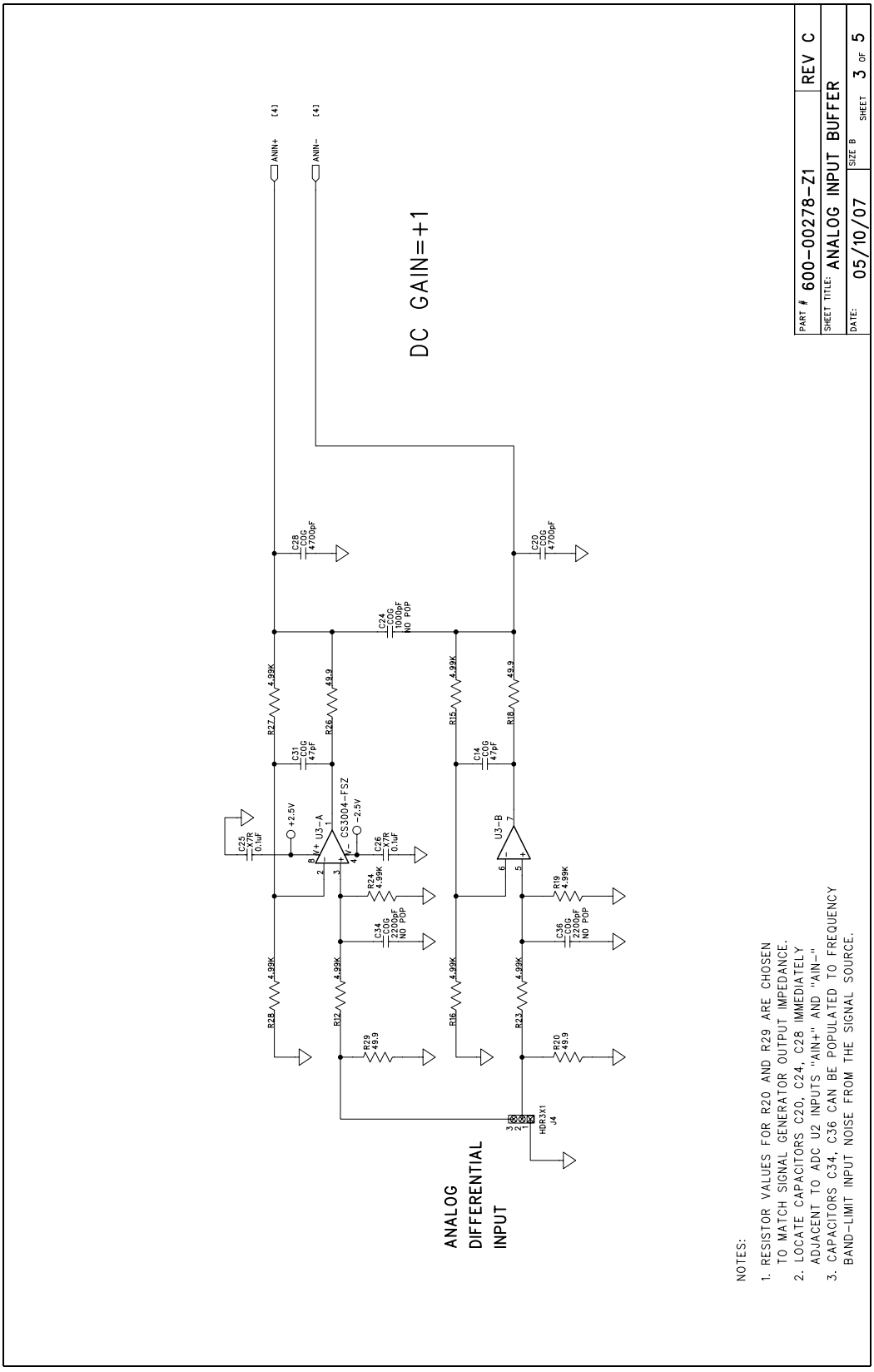


Figure 5. Schematic - Input Buffers and Multiplexer

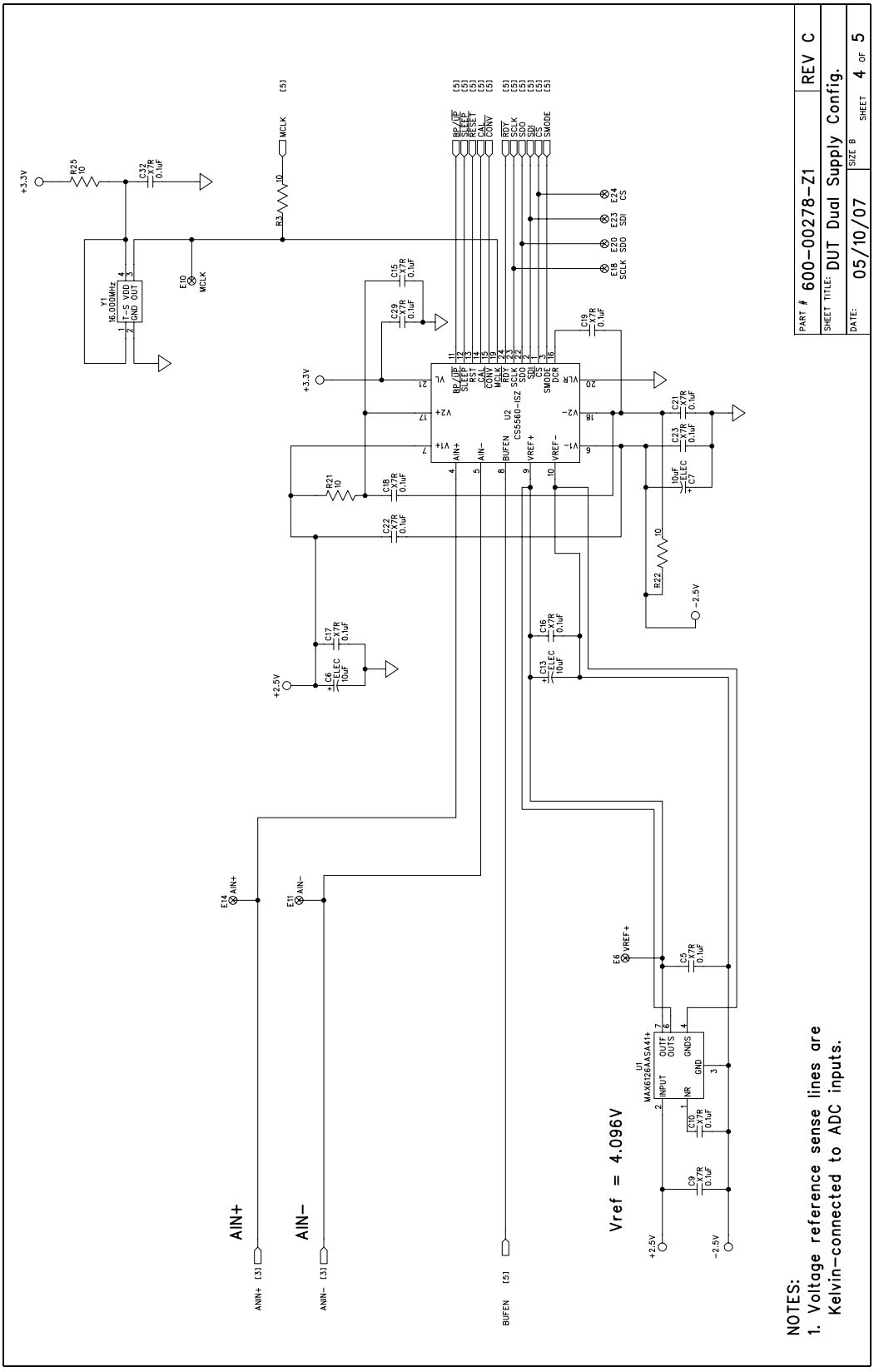


Figure 6. Schematic - CS5560

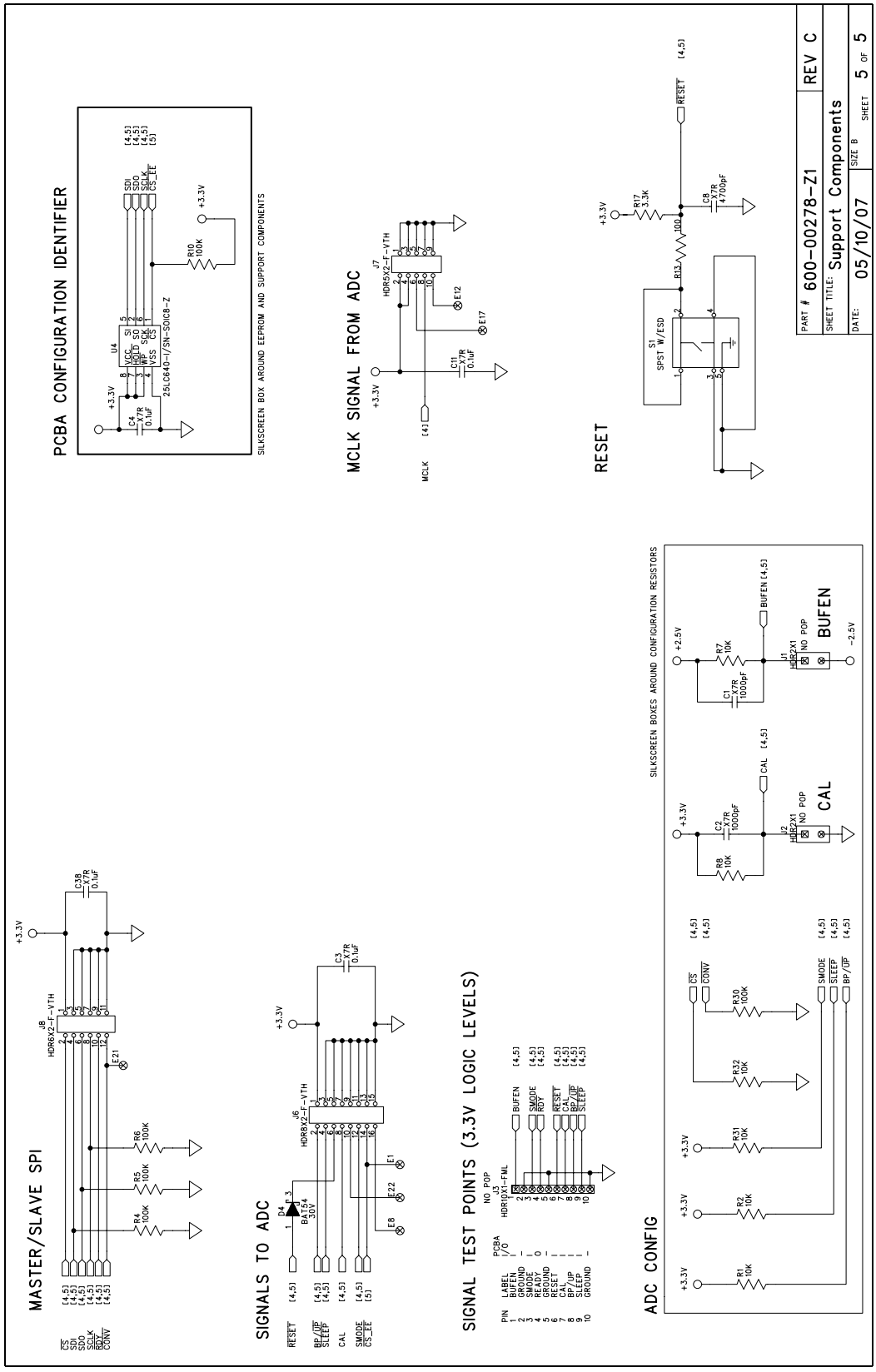


Figure 7. Schematic - Configuration & Misc.

APPENDIX D. LAYER PLOTS

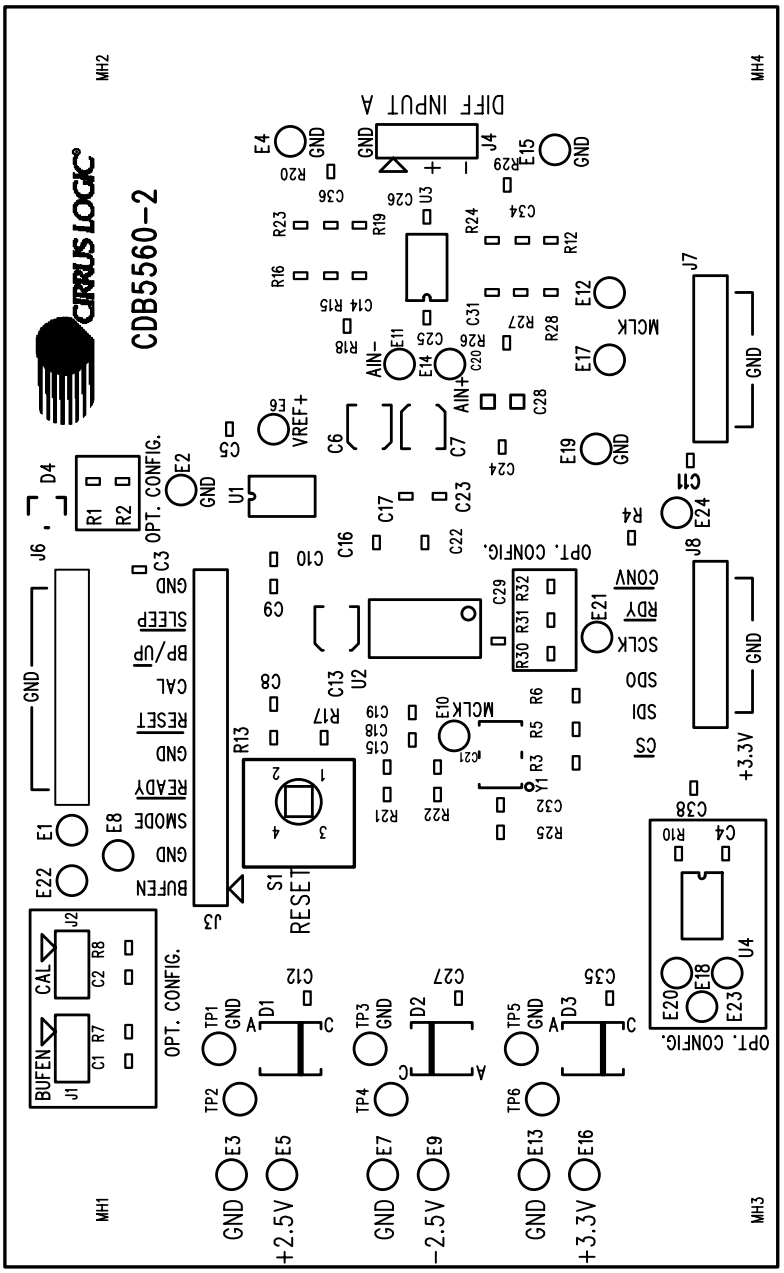
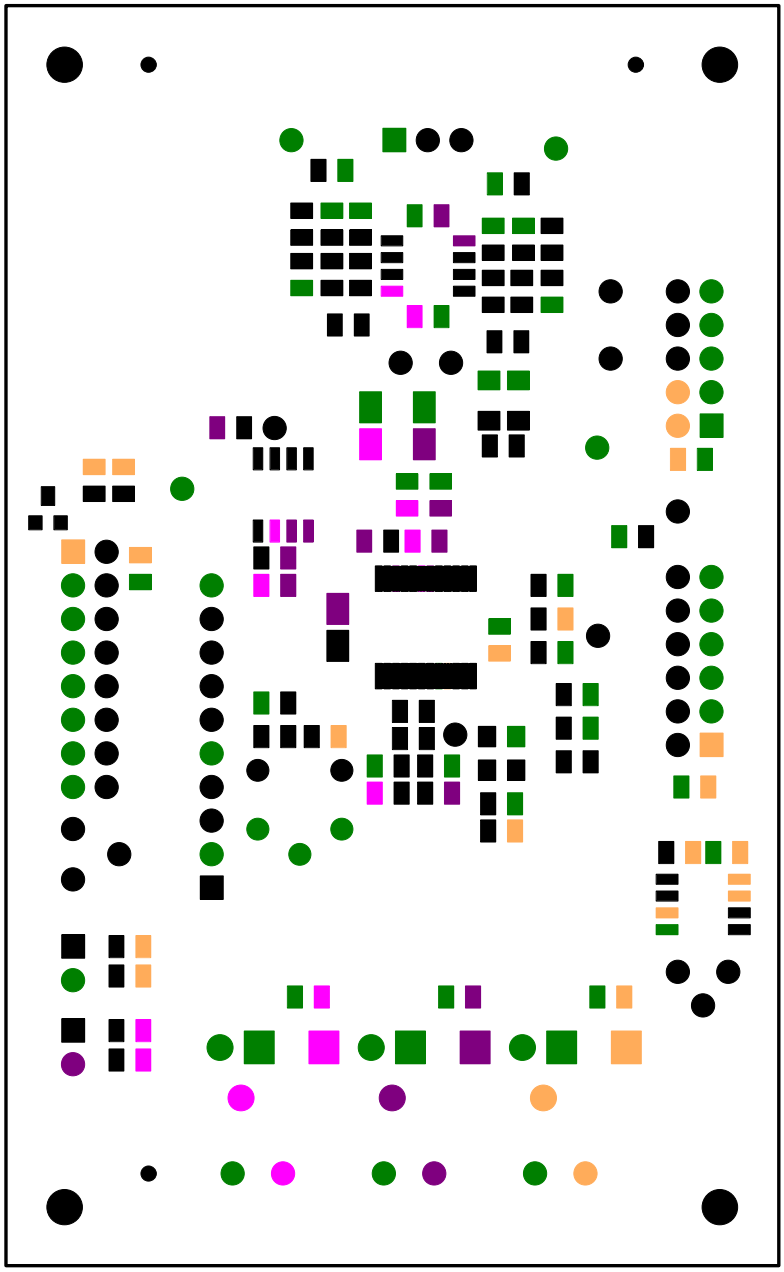


Figure 8. Top Silkscreen



CIRRUS LOGIC 240-00278-Z1 REV C

SOLDERMASK TOP

Figure 9. Top Solder Mask

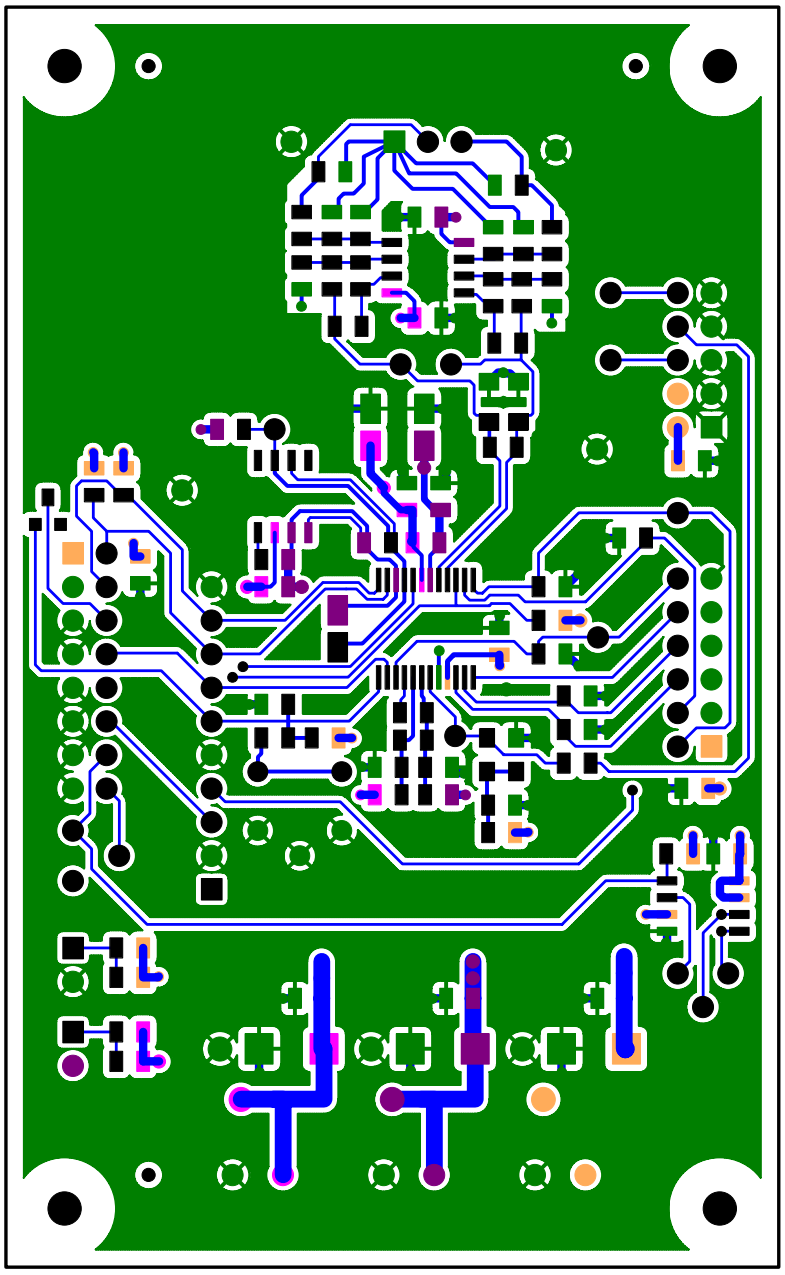


Figure 10. Top Routing

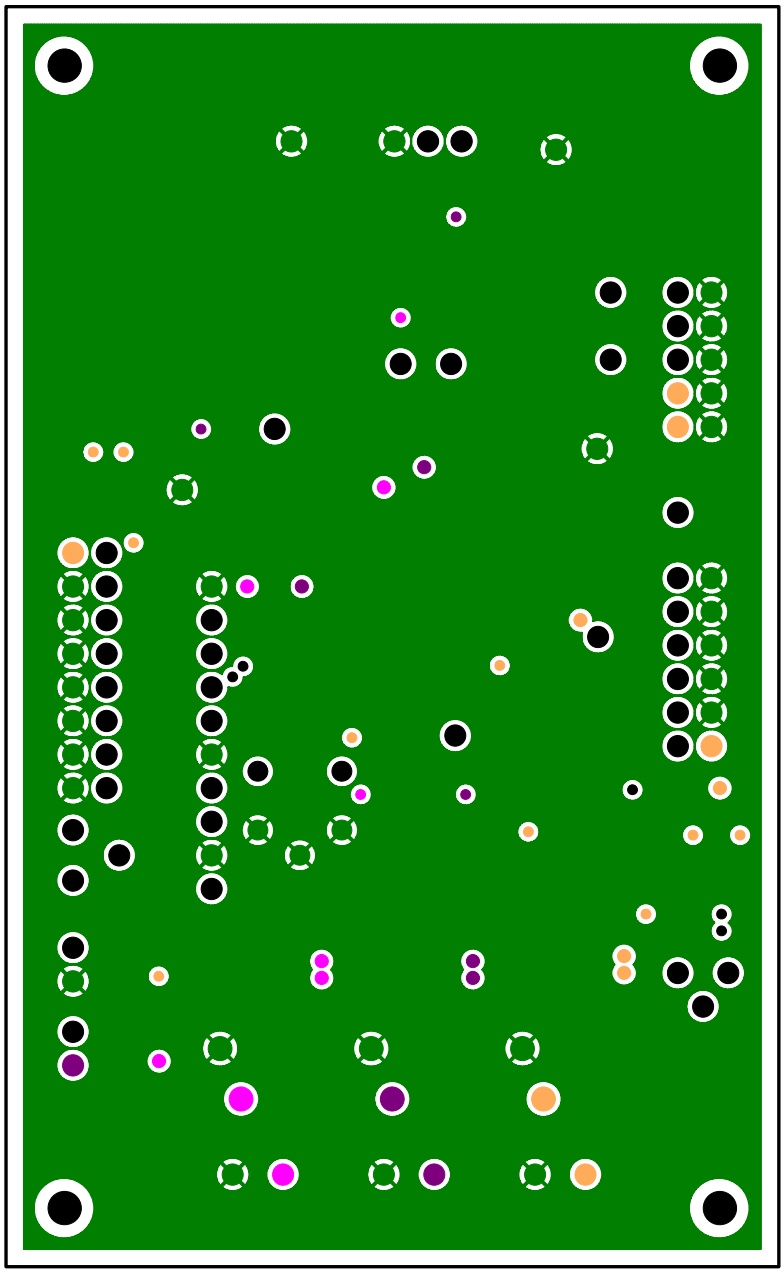


Figure 11. Ground Plane

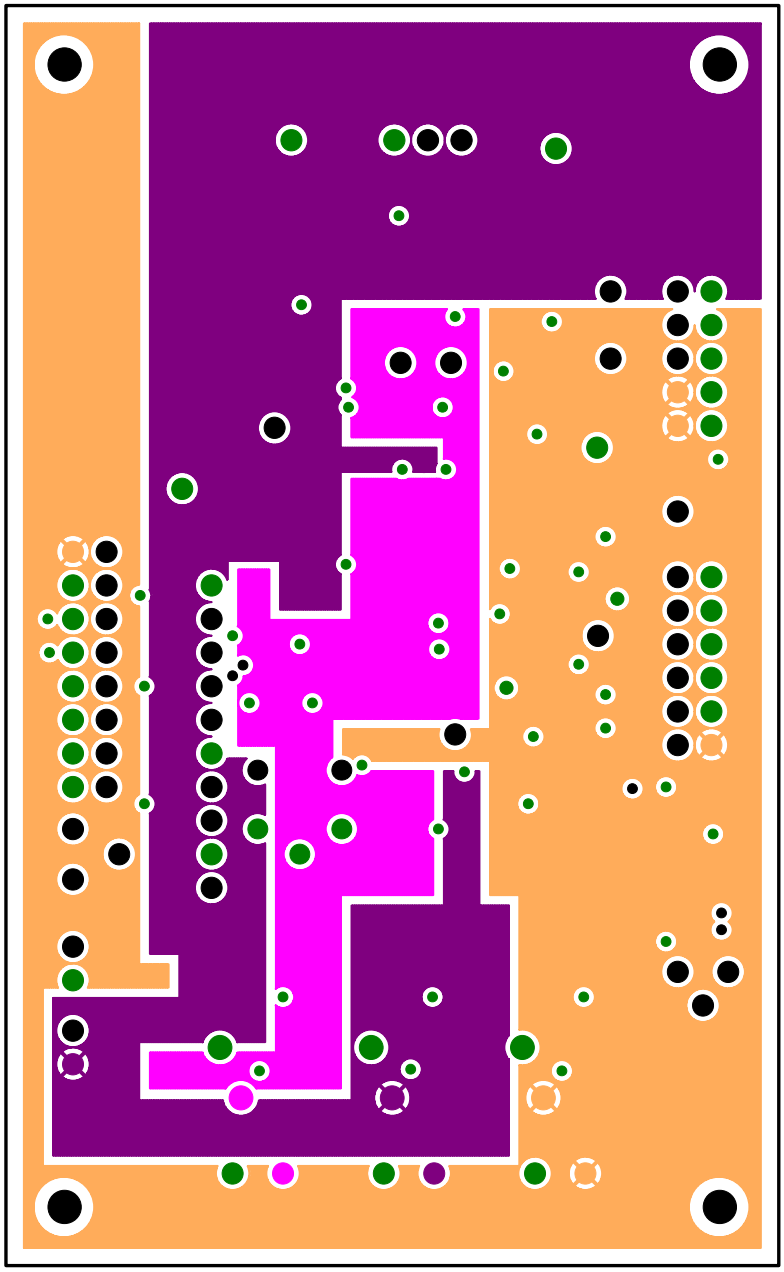


Figure 12. Power Plane

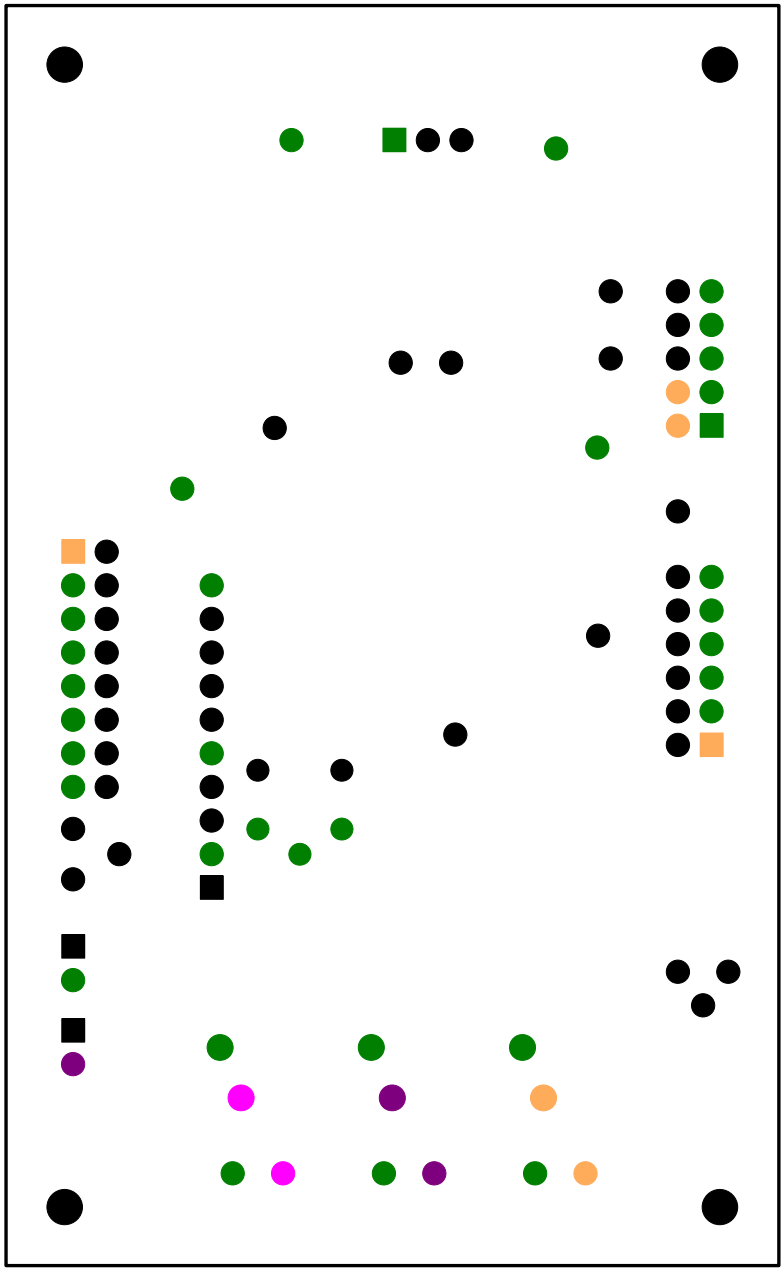


Figure 13. Bottom Solder Mask

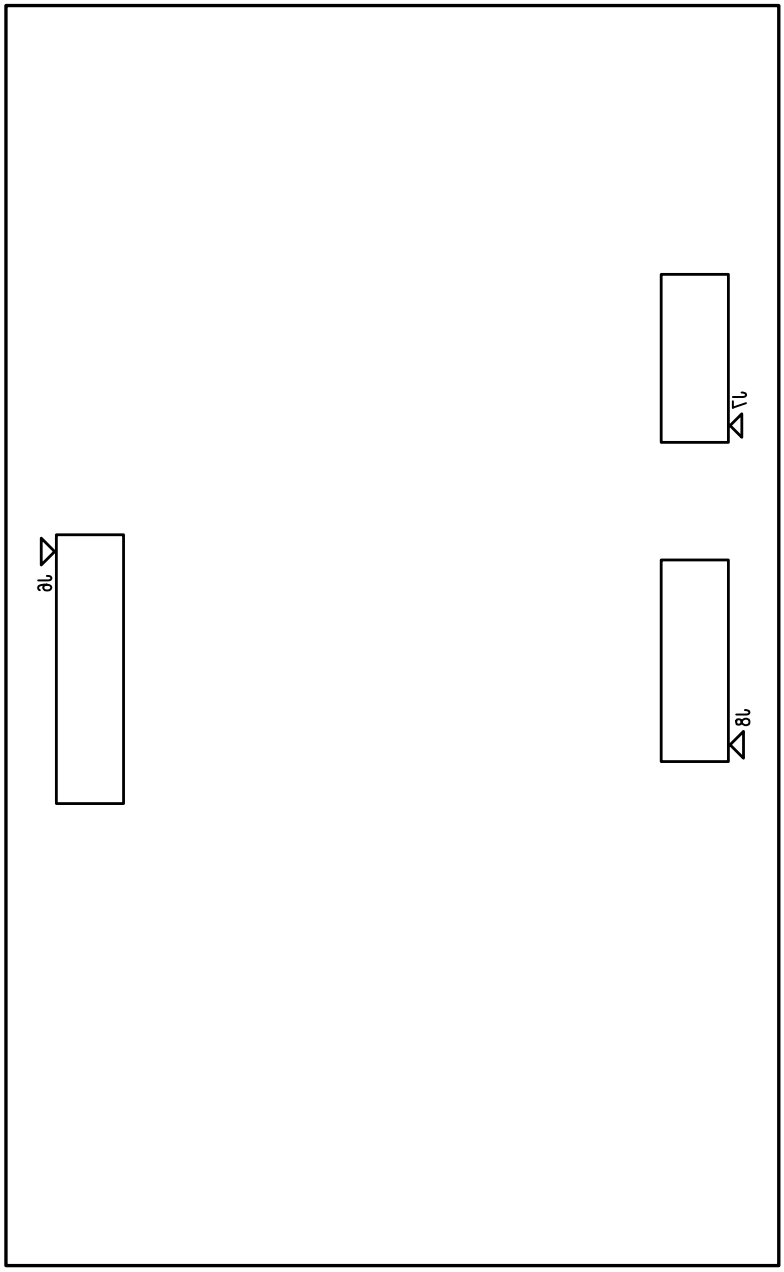


Figure 14. Bottom Silkscreen

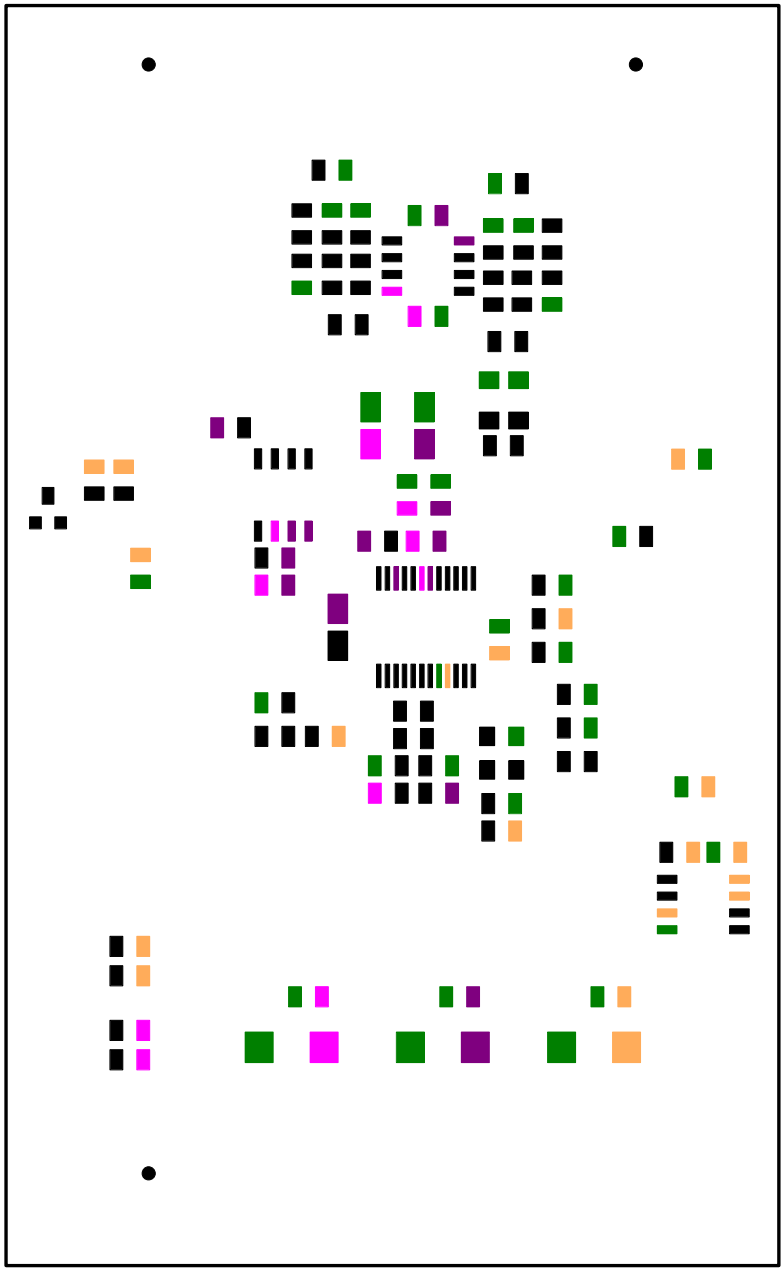


Figure 15. Top Solder Paste Mask

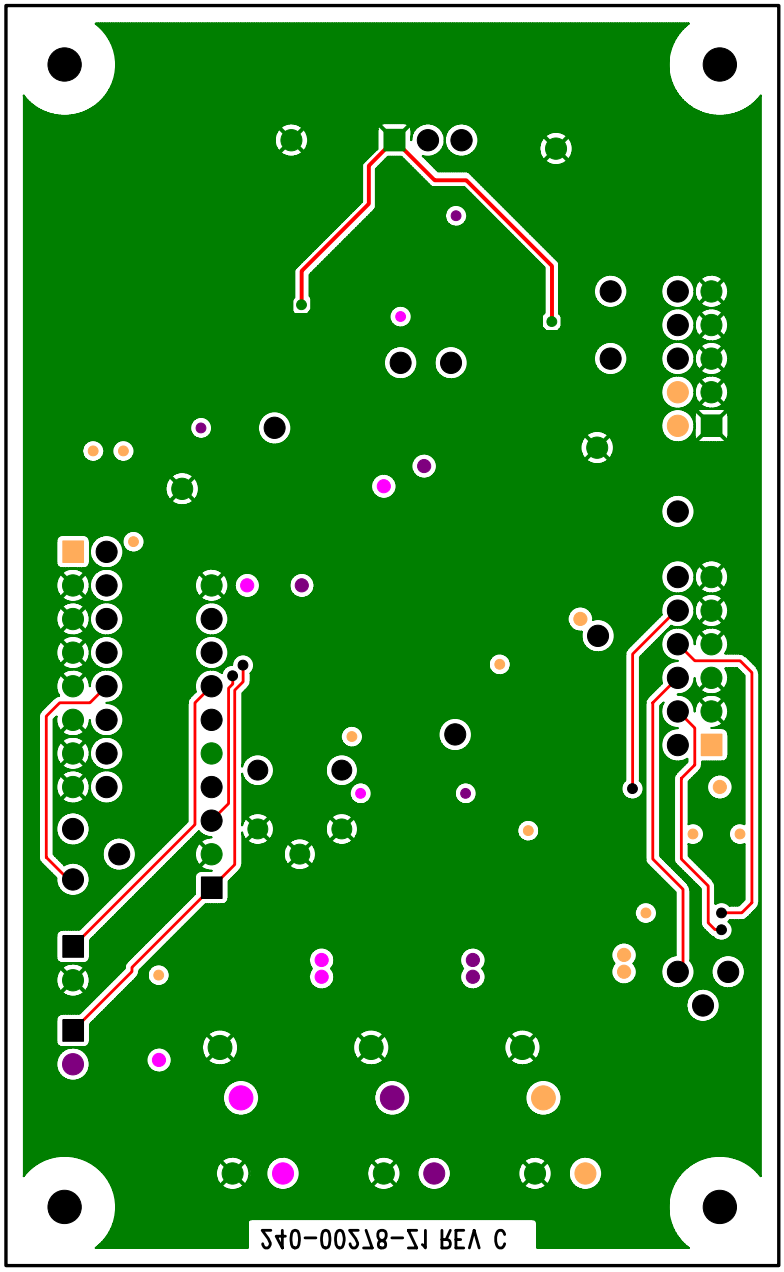


Figure 16. Bottom Routing

REVISION HISTORY

Revision	Date	Changes
DB1	APR 2007	Initial Release.
DB2	SEP 2007	Updated schematics, gerber plots to reflect rev C assembly, non-inverting buffers. Added photo of board.