

## MAX13256

# 36V H-Bridge Transformer Driver for Isolated Supplies

### General Description

The MAX13256 H-bridge transformer driver provides a simple solution for making isolated power supplies up to 10W. The device drives a transformer's primary coil with up to 300mA of current from a wide 8V to 36V DC supply. The transformer's secondary-to-primary winding ratio defines the output voltage, allowing selection of virtually any isolated output voltage.

The device features adjustable current limiting, allowing indirect limiting of secondary-side load currents. The current limit of the MAX13256 is set by an external resistor. A  $\overline{\text{FAULT}}$  output asserts when the device detects an overtemperature or overcurrent condition. In addition, the device features a low-power mode to reduce the overall supply current to 0.65mA (typ) when the driver is not in use.

The device can be operated using the internal oscillator or driven by an external clock to synchronize multiple MAX13256 devices and precisely set the switching frequency. Internal circuitry guarantees a fixed 50% duty cycle to prevent DC current flow through the transformer, regardless of which clock source is used.

The device is available in a small 10-pin (3mm x 3mm) TDFN package and is specified over the -40°C to +125°C automotive temperature range.

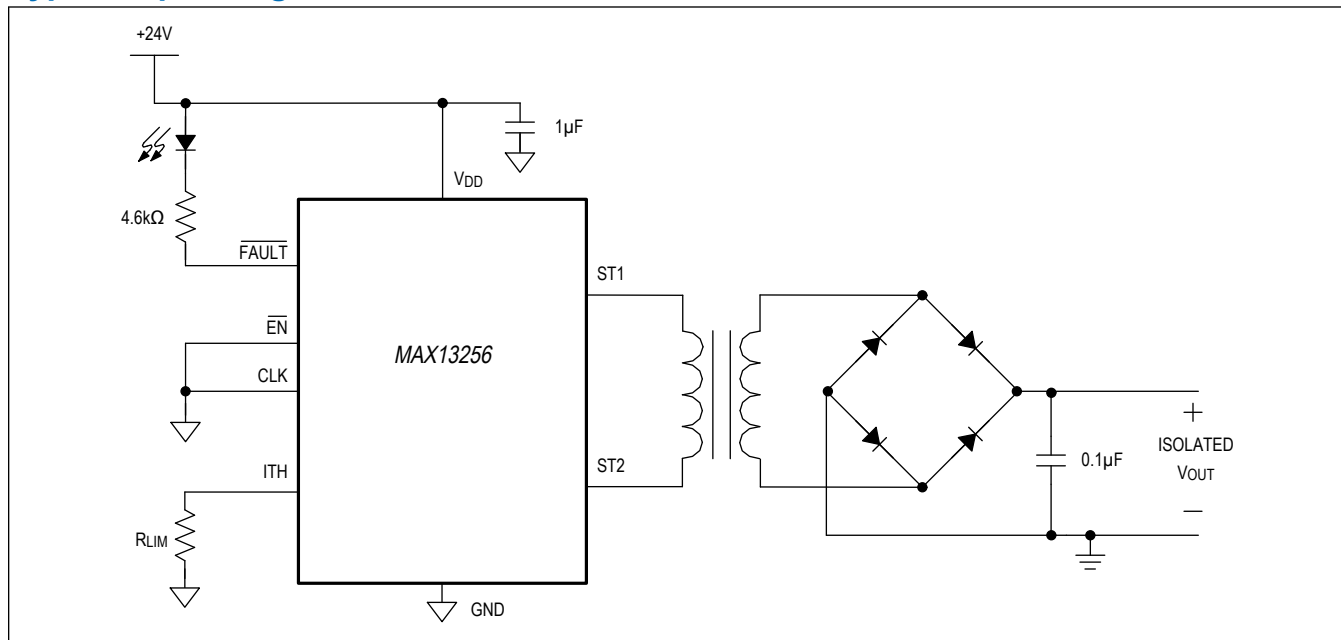
### Applications

- Power Meters
- Isolated Fieldbus Interfaces
- 24V PLC Supply Isolation
- Medical Equipment
- Motor Controls

### Benefits and Features

- Simple, Flexible Design
  - 8V to 36V Supply Range
  - Up to 90% Efficiency
  - Provides Up to 10W to the Transformer
  - Undervoltage Lockout
  - 2.5V to 5V Compatible Logic Interface
  - Internal or External Clock Source
  - Adjustable Overcurrent Threshold
- Integrated System Protection
  - Fault Detection and Indication
  - Overcurrent Limiting
  - Overtemperature Protection
- Saves Space on Board
  - Small 10-Pin TDFN Package (3mm x 3mm)

Typical Operating Circuit



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**TABLE OF CONTENTS**


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|   |    |
|---|----|
| General Description . . . . .                                       | 1  |
| Applications . . . . .  | 1  |
| Benefits and Features . . . . .                                     | 1  |
| Typical Operating Circuit . . . . .                                 | 2  |
| Absolute Maximum Ratings . . . . .                                  | 7  |
| Package Information . . . . .                                       | 7  |
| 10 TDFN-EP . . . . .  | 7  |
| Electrical Characteristics . . . . .                                | 7  |
| Typical Operating Characteristics . . . . .                         | 10 |
| Pin Configuration . . . . .   | 12 |
| MAX13256 . . . . .  | 12 |
| Pin Description . . . . .   | 12 |
| Functional Diagram . . . . .  | 13 |
| MAX13256 . . . . .  | 13 |
| Detailed Description . . . . .                                      | 14 |
| Isolated Power Supply . . . . .                                     | 14 |
| Clock Source . . . . .  | 14 |
| Internal Oscillator Mode . . . . .                                  | 14 |
| External Clock Mode . . . . .                                       | 14 |
| Watchdog . . . . .  | 14 |
| Transients on ST1/ST2 During $t_{DEAD}$ . . . . .                   | 14 |
| Disable Mode . . . . .  | 14 |
| Power-Up and Undervoltage Lockout . . . . .                         | 14 |
| Overcurrent Limiting . . . . .                                      | 15 |
| FAULT Output . . . . .  | 15 |
| Thermal Shutdown . . . . .  | 15 |
| Applications Information . . . . .                                  | 17 |
| Snubber . . . . .   | 17 |
| Power Dissipation . . . . .   | 17 |
| High-Temperature Operation . . . . .                                | 17 |
| Hot Insertion . . . . .   | 17 |
| Output-Ripple Filtering . . . . .                                   | 17 |
| Power-Supply Decoupling . . . . .                                   | 17 |
| Output-Voltage Regulation . . . . .                                 | 17 |
| Isolated DAC/ADC Interface for Industrial Process Control . . . . . | 18 |
| Isolated RS-485/RS-232 Data Interfaces . . . . .                    | 20 |
| PCB Layout Guidelines . . . . .                                     | 20 |
| Exposed Pad . . . . .   | 20 |
| Component Selection . . . . .                                       | 21 |

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**TABLE OF CONTENTS (CONTINUED)**

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|  |    |
|--|----|
| Transformer Selection .....                      | 21 |
| Low-Voltage Operation .....                      | 21 |
| Diode Selection .....                            | 22 |
| Capacitor Selection .....                        | 22 |
| Input Bypass Capacitor .....                     | 22 |
| Output Filter Capacitor .....                    | 22 |
| Suggested External Component Manufacturers ..... | 22 |
| Ordering Information .....                       | 22 |
| Revision History .....                           | 23 |

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**LIST OF FIGURES**

---

|   |    |
|---|----|
| Figure 1. Test Circuits (A and B) and Timing Diagram (C) for Rise, Fall, and Dead Times . . . . . | 9  |
| Figure 2. Timing Diagram for Current Limiting . . . . .   | 9  |
| Figure 3. Secondary-Side Rectification Topologies . . . . .                                       | 16 |
| Figure 4. Output Snubber . . . . .  | 16 |
| Figure 5. Output Ripple Filtering . . . . .   | 16 |
| Figure 6. +24V to Isolated, Regulated +3.3V . . . . .   | 18 |
| Figure 7. +24V to Isolated, Regulated +12V . . . . .  | 18 |
| Figure 8. +24V to Isolated, Regulated $\pm 15V$ . . . . .   | 19 |
| Figure 9. Isolated Power Supply for Industrial Control Applications . . . . .                     | 20 |

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**LIST OF TABLES**

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Table 1. Component Manufacturers ..... 22

## Absolute Maximum Ratings

|  |                                   |  |                 |
|--|-----------------------------------|--|-----------------|
| (Voltages referenced to GND.)                          |                                   | TDFN (Single-Layer Board) (derate 18.5mW/°C above +70°C) | 1481.5mW        |
| V <sub>DD</sub> , FAULT                                | -0.3V to +40V                     | Operating Temperature Range                              | -40°C to +125°C |
| ST1, ST2   | -0.3V to (V <sub>DD</sub> + 0.3V) | Junction Temperature                                     | +150°C          |
| CLK, ITH, EN   | -0.3V to +6V                      | Storage Temperature Range                                | -65°C to +150°C |
| FAULT Continuous Current                               | ±50mA                             | Lead Temperature (soldering, 10s)                        | +300°C          |
| ST1, ST2 Continuous Current                            | ±850mA                            | Soldering Temperature (reflow)                           | +260°C          |
| Continuous Power Dissipation (T <sub>A</sub> = +70°C)  |                                   |  |                 |
| TDFN (Four-Layer Board) (derate 24.4mW/°C above +70°C) | 1951.2mW                          |  |                 |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Package Information

### 10 TDFN-EP

|  |                         |
|--|-------------------------|
| Package Code   | T1033+1                 |
| Outline Number   | <a href="#">21-0137</a> |
| Land Pattern Number                                    | <a href="#">90-0003</a> |
| <b>Thermal Resistance, Single Layer Board:</b>         |                         |
| Junction-to-Ambient (θ <sub>JA</sub> )                 | 54°C/W                  |
| Junction-to-Case Thermal Resistance (θ <sub>JC</sub> ) | 9°C/W                   |
| <b>Thermal Resistance, Four Layer Board:</b>           |                         |
| Junction-to-Ambient (θ <sub>JA</sub> )                 | 41°C/W                  |
| Junction-to-Case Thermal Resistance (θ <sub>JC</sub> ) | 9°C/W                   |

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

## Electrical Characteristics

(V<sub>DD</sub> = 8V to 36V, V<sub>EN</sub> = 0V, T<sub>A</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) ([Note 1](#))

| PARAMETER                      | SYMBOL            | CONDITIONS   | MIN | TYP  | MAX | UNITS |
|--------------------------------|-------------------|--|-----|------|-----|-------|
| <b>DC CHARACTERISTICS</b>      |                   |  |     |      |     |       |
| Supply Voltage Range           | V <sub>DD</sub>   | <a href="#">(Note 2)</a>   | 8   |      | 36  | V     |
| Supply Current                 | I <sub>DD</sub>   | V <sub>EN</sub> = 0V, V <sub>CLK</sub> = 0V, R <sub>LIM</sub> = 1000Ω, ST1/ST2 not connected |     | 6    | 9   | mA    |
| Disable Supply Current         | I <sub>DIS</sub>  | V <sub>EN</sub> = 3.3V, V <sub>CLK</sub> = 0V  |     | 0.65 | 1.1 | mA    |
| Driver Output Resistance       | R <sub>OH</sub>   | ST1 = ST2 = high, I <sub>ST1</sub> , I <sub>ST2</sub> = +300mA, R <sub>LIM</sub> = 1000Ω     |     | 1    | 1.5 | Ω     |
|                                | R <sub>OL</sub>   | ST1 = ST2 = low, I <sub>ST1</sub> , I <sub>ST2</sub> = -300mA, R <sub>LIM</sub> = 1000Ω      |     | 0.6  | 1.0 |       |
| Undervoltage-Lockout Threshold | V <sub>UVLO</sub> | V <sub>DD</sub> rising   | 5.9 | 6.3  | 6.9 | V     |

**Electrical Characteristics (continued)**(V<sub>DD</sub> = 8V to 36V, V<sub>EN</sub> = 0V, T<sub>A</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) ([Note 1](#))

| PARAMETER                                 | SYMBOL                 | CONDITIONS  | MIN  | TYP  | MAX  | UNITS |
|---|------------------------|---|------|------|------|-------|
| Undervoltage-Lockout Threshold Hysteresis | V <sub>UVLO_HYST</sub> |   |      | 300  |      | mV    |
| ST1, ST2 Current Limit                    | I <sub>LIM</sub>       | R <sub>LIM</sub> = 1000Ω  | 500  | 650  | 800  | mA    |
|   |                        | R <sub>LIM</sub> = 3010Ω  | 165  | 215  | 265  |       |
| ST1, ST2 Leakage Current                  | I <sub>LKG</sub>       | V <sub>EN</sub> = 3.3V, V <sub>CLK</sub> = 0V, V <sub>ST1</sub> = V <sub>ST2</sub> = 0V or (V <sub>DD</sub> - 1V) | -1   |      | +1   | μA    |
| <b>LOGIC SIGNALS (CLK, EN, FAULT)</b>     |                        |   |      |      |      |       |
| Input Logic-High Voltage                  | V <sub>IH</sub>        |   | 2    |      |      | V     |
| Input Logic-Low Voltage                   | V <sub>IL</sub>        |   |      |      | 0.8  | V     |
| Input Leakage Current                     | I <sub>IL</sub>        | V <sub>CLK</sub> = V <sub>EN</sub> = 5.5V or 0V   | -1   |      | +1   | μA    |
| FAULT Output Logic-Low Voltage            | V <sub>OL</sub>        | I <sub>FAULT</sub> = 10mA   |      |      | 1    | V     |
| FAULT Leakage Current                     | I <sub>LKGF</sub>      | V <sub>FAULT</sub> = 36V, FAULT deasserted  |      |      | 10   | μA    |
| <b>AC CHARACTERISTICS</b>                 |                        |   |      |      |      |       |
| Switching Frequency                       | f <sub>SW</sub>        | V <sub>CLK</sub> = 0V, measured at ST1/ST2 outputs  | 255  | 425  | 700  | kHz   |
| CLK Input Frequency                       | f <sub>EXT</sub>       | External clocking   | 200  |      | 2000 | kHz   |
| ST1/ST2 Duty Cycle                        | D <sub>TC</sub>        | Internal or external clocking   | 49   | 50   | 51   | %     |
| ST1/ST2 Rise Time                         | t <sub>RISE</sub>      | ST1/ ST2 = 20% to 80% of V <sub>DD</sub> , R <sub>L</sub> = 1kΩ, C <sub>L</sub> = 50pF, <a href="#">Figure 1</a>  |      |      | 100  | ns    |
| ST1/ST2 Fall Time                         | t <sub>FALL</sub>      | ST1/ST2 = 80% to 20% of V <sub>DD</sub> , R <sub>L</sub> = 1kΩ, C <sub>L</sub> = 50pF, <a href="#">Figure 1</a>   |      |      | 100  | ns    |
| Crossover Dead Time                       | t <sub>DEAD</sub>      | R <sub>L</sub> = 200Ω, <a href="#">Figure 1</a>   |      | 30   |      | ns    |
| Watchdog Timeout                          | t <sub>WDOG</sub>      | ( <a href="#">Note 3</a> )  | 20   | 32   | 55   | μs    |
| Current-Limit Blanking Time               | t <sub>BLANK</sub>     | <a href="#">Figure 2</a>  | 0.73 | 1.2  | 2.0  | ms    |
| Current-Limit Autoretry Time              | t <sub>RETRY</sub>     | <a href="#">Figure 2</a>  | 23.4 | 38.4 | 64.0 | ms    |
| <b>PROTECTION</b>                         |                        |   |      |      |      |       |
| Thermal-Shutdown Threshold                | T <sub>SHDN</sub>      |   |      | +160 |      | °C    |
| Thermal-Shutdown Hysteresis               | T <sub>SHDN_HYS</sub>  |   |      | 10   |      | °C    |

**Note 1:** All units are production tested at T<sub>A</sub> = +25°C. Specifications over temperature are guaranteed by design.**Note 2:** If V<sub>DD</sub> is greater than 27V, see the [Snubber](#) section.**Note 3:** See the [Watchdog](#) section.



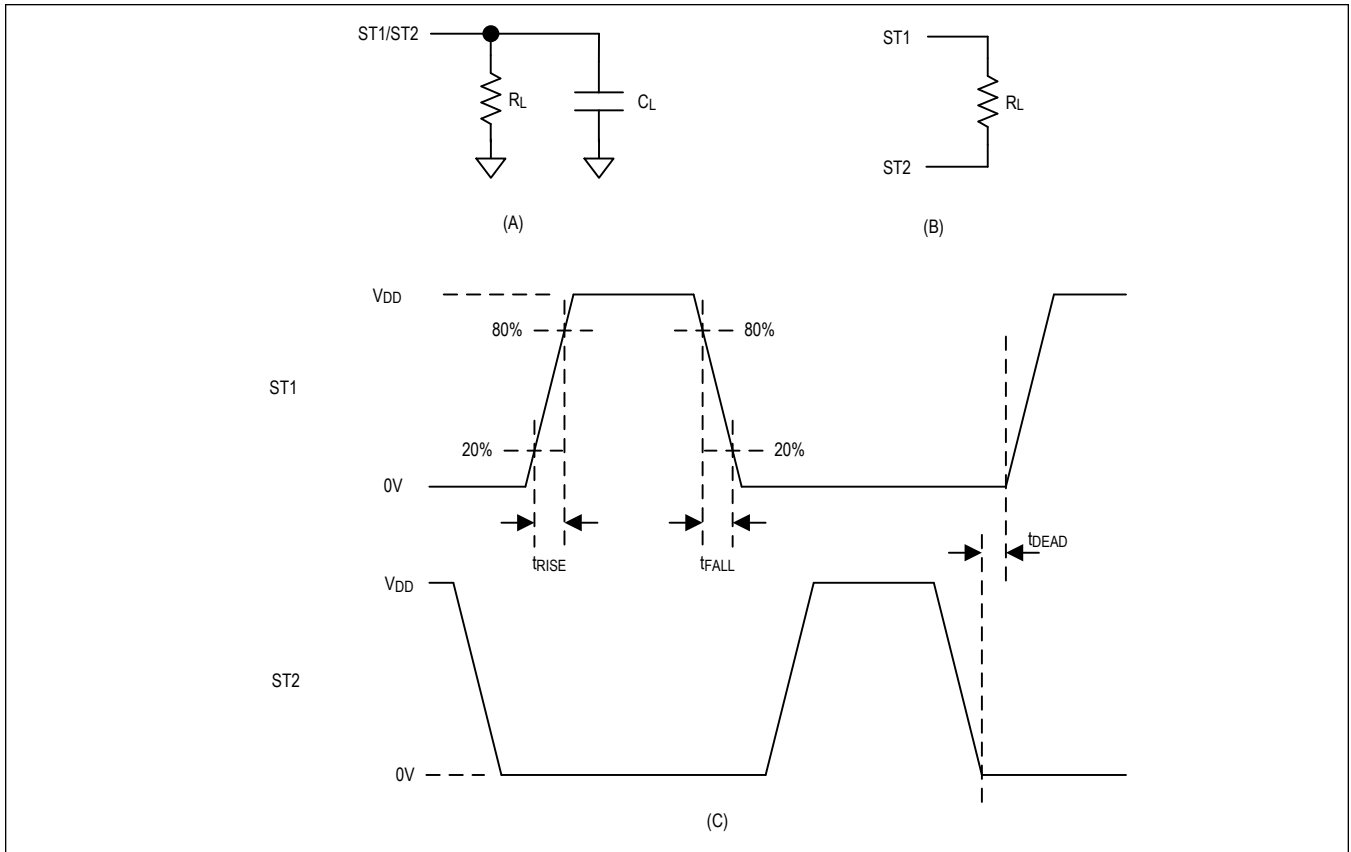


Figure 1. Test Circuits (A and B) and Timing Diagram (C) for Rise, Fall, and Dead Times

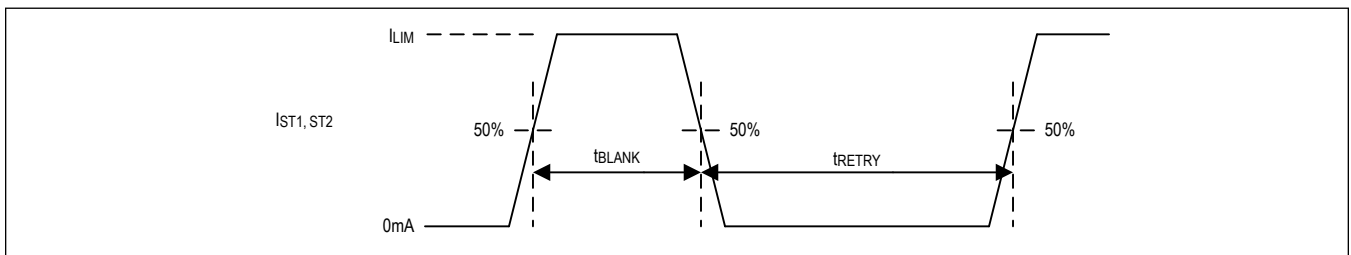
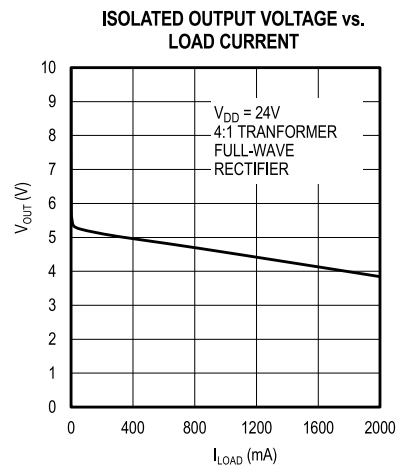
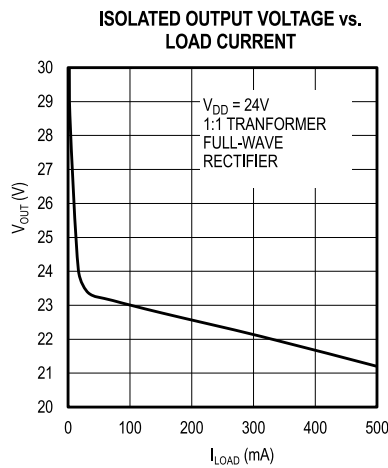
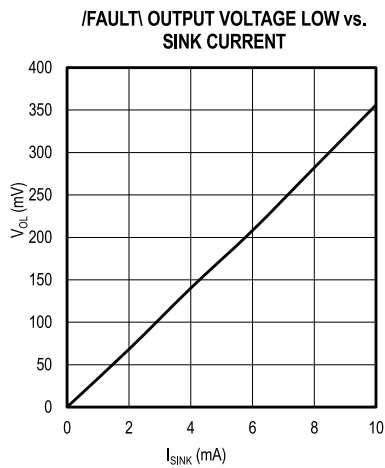
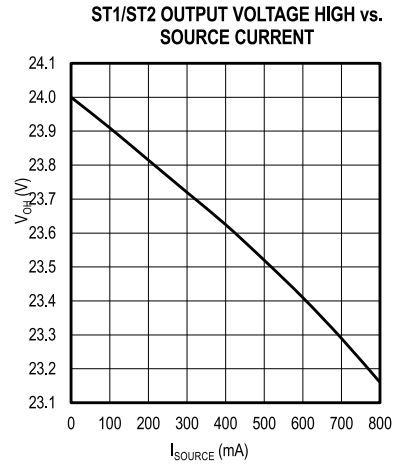
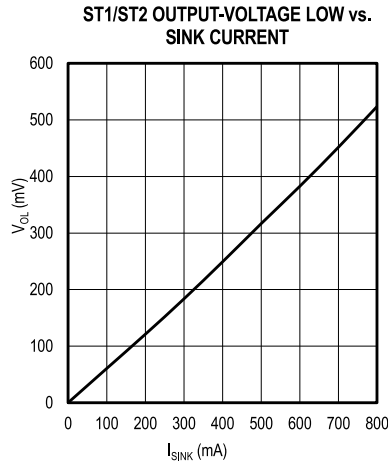
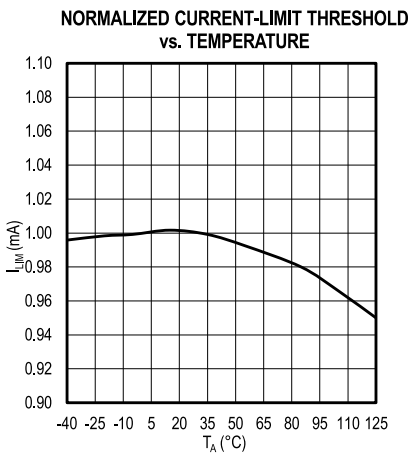
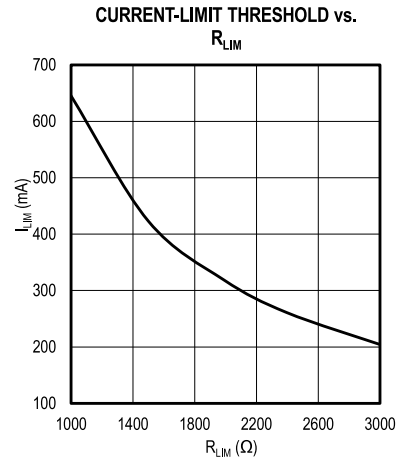
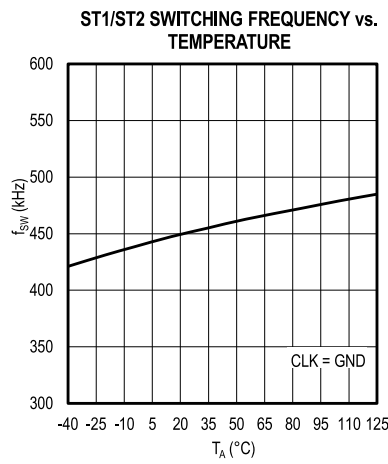
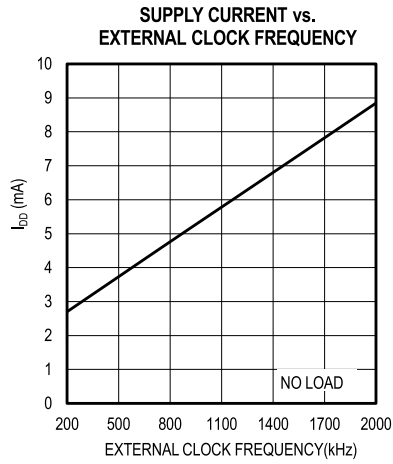


Figure 2. Timing Diagram for Current Limiting

Typical Operating Characteristics

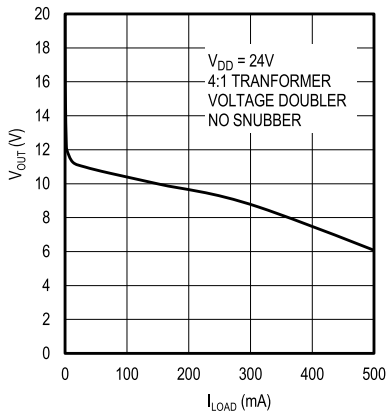
( $V_{DD} = 24V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



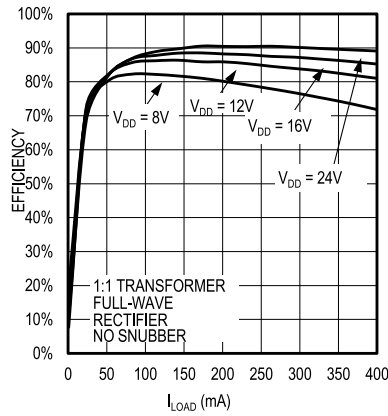
Typical Operating Characteristics (continued)

( $V_{DD} = 24V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

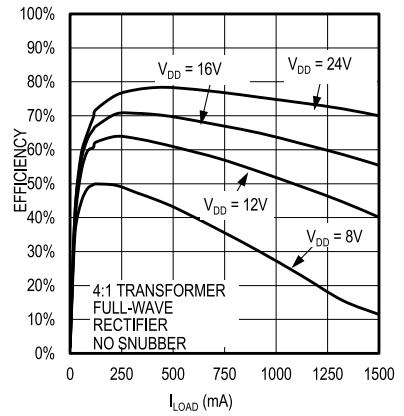
ISOLATED OUTPUT VOLTAGE vs. LOAD CURRENT



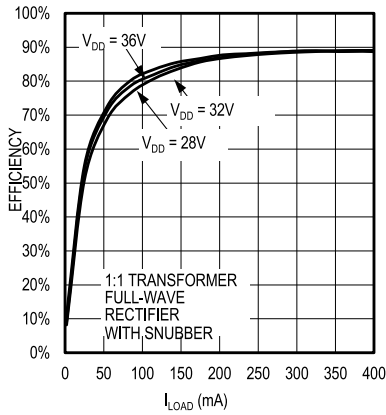
EFFICIENCY vs. LOAD CURRENT



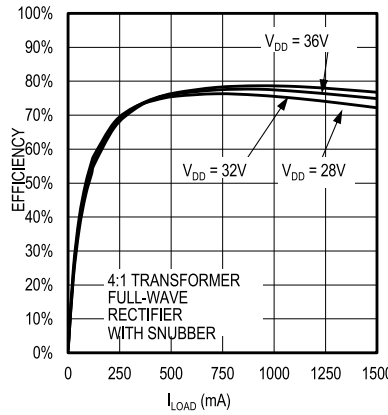
EFFICIENCY vs. LOAD CURRENT



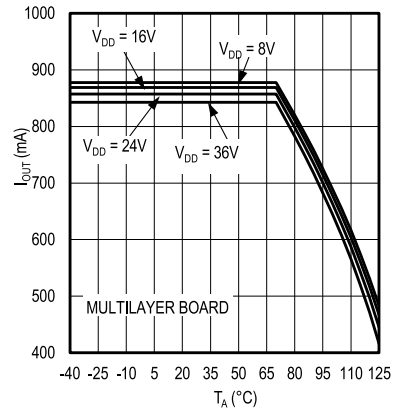
EFFICIENCY vs. LOAD CURRENT



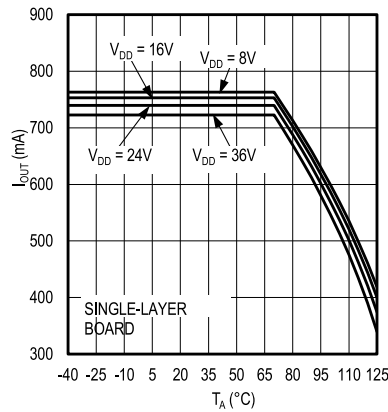
EFFICIENCY vs. LOAD CURRENT



MAXIMUM OUTPUT CURRENT vs. TEMPERATURE

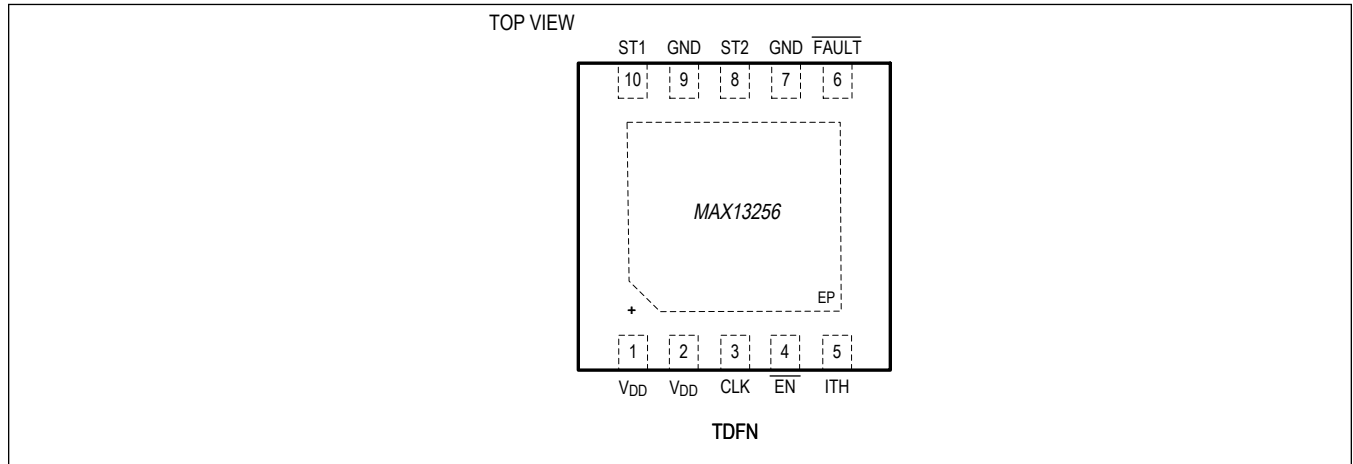


MAXIMUM OUTPUT CURRENT vs. TEMPERATURE



Pin Configuration

MAX13256

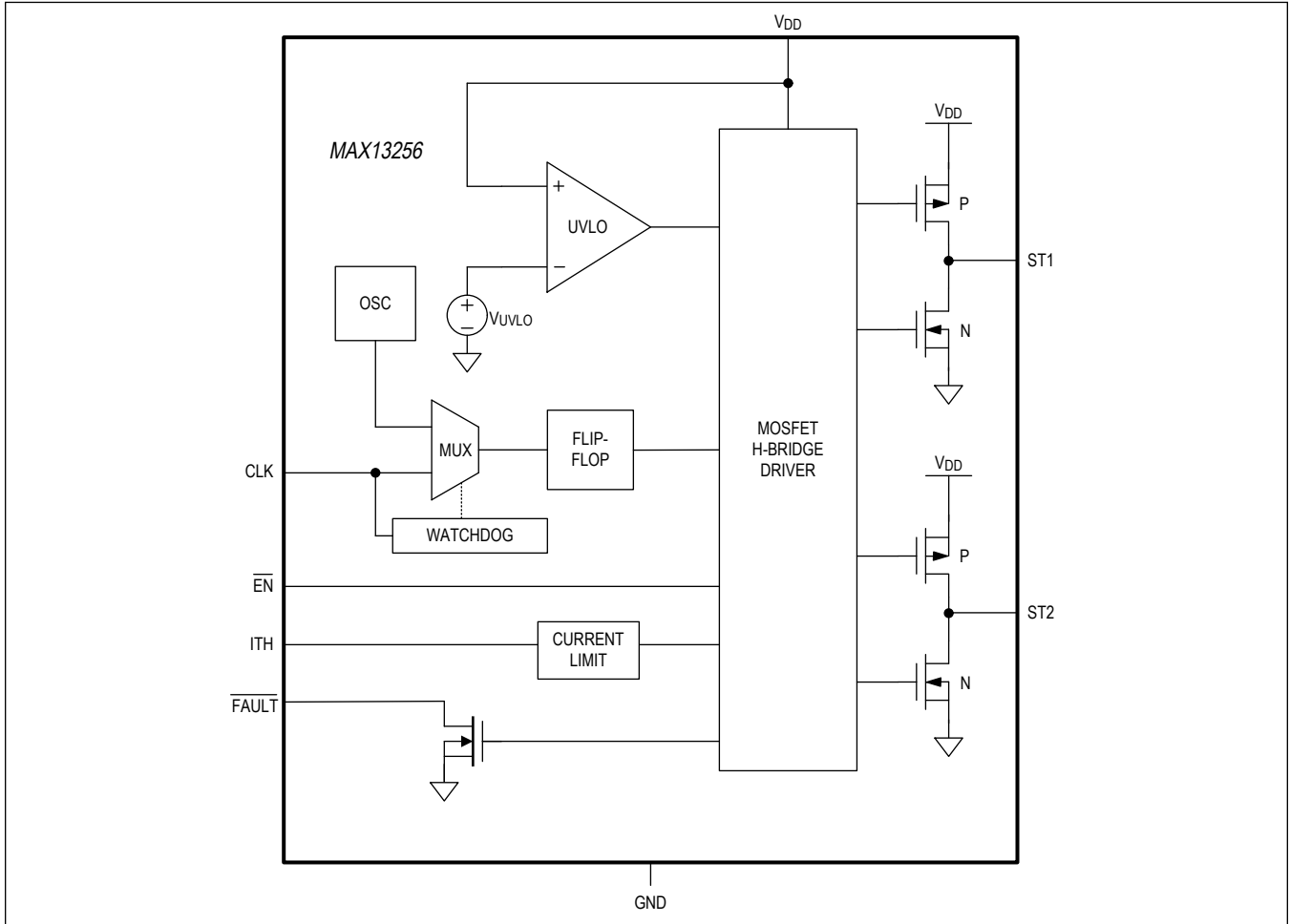


Pin Description

| PIN  | NAME                      | FUNCTION  |
|------|---------------------------|---|
| 1, 2 | V <sub>DD</sub>           | Power Supply. Bypass V <sub>DD</sub> to ground with a 1μF capacitor as close as possible to the device.   |
| 3    | CLK                       | Clock Input. Connect CLK to GND to enable internal clocking. Apply a clock signal to CLK to enable external clocking.   |
| 4    | $\overline{\text{EN}}$    | Enable Input. Drive $\overline{\text{EN}}$ low to enable the device. Drive $\overline{\text{EN}}$ high to disable the device.   |
| 5    | ITH                       | Overcurrent Threshold Adjustment Input. Connect a resistor (R <sub>LIM</sub> ) from ITH to GND to set the overcurrent threshold for the ST1 and ST2 outputs. Do not exceed 10pF of capacitance to GND on ITH. |
| 6    | $\overline{\text{FAULT}}$ | Fault Open-Drain Output. The fault open-drain transistor turns on when there is either an overtemperature or overcurrent condition.   |
| 7, 9 | GND                       | Ground  |
| 8    | ST2                       | Transformer Drive Output 2  |
| 10   | ST1                       | Transformer Drive Output 1  |
| -    | EP                        | Exposed Pad. Internally connected to GND. Connect EP to a large ground plane to maximize thermal performance; not intended as an electrical connection point.   |

Functional Diagram

MAX13256



## Detailed Description

The MAX13256 is an integrated primary-side controller and H-bridge driver for isolated power-supply circuits. The device contains an on-board oscillator, protection circuitry, and internal MOSFETs to provide up to 300mA of current to the primary winding of a transformer. The device can be operated using the internal oscillator or driven by an external clock to synchronize multiple MAX13256 devices and control EMI behavior. Regardless of the clock source being used, an internal flip-flop stage guarantees a fixed 50% duty cycle to prevent DC current flow in the transformer as long as the period of the clock is constant.

The device operates from a wide single-supply voltage of 8V to 36V, and includes undervoltage lockout for controlled startup. The device features break-before-make switching to prevent cross conduction of the H-bridge MOSFETs. An external resistor sets an overcurrent limit, allowing primary-side limiting of load currents on the transformer's secondary side. Thermal-shutdown circuitry provides additional protection against excessive power dissipation.

## Isolated Power Supply

The MAX13256 allows a versatile range of secondary-side rectification circuits (see [Figure 3](#)). The primary-to-secondary transformer winding ratio can be chosen to adjust the isolated output voltage. The device delivers up to 300mA of current to the transformer with a supply up to +36V.

The MAX13256 provides the advantages of the H-bridge converter topology, including multiple isolated outputs, step-up/step-down or inverted output, relaxed filtering requirements, and low output ripple.

## Clock Source

Either the internal oscillator or an external clock provides the switching signal for the MAX13256. Connect CLK to ground to select the internal oscillator. Provide a clock signal to CLK to automatically select external clocking.

## Internal Oscillator Mode

The MAX13256 includes an internal oscillator that drives the H-bridge when a watchdog timeout is detected on CLK. The outputs switch at 425kHz (typ) with a guaranteed 50% duty cycle in the internal oscillator mode.

## External Clock Mode

The MAX13256 provides an external clock mode. When an external clock source is applied to CLK, the external clock drives the H-bridge. An internal flip-flop divides the external clock by two in order to generate a switching signal with a guaranteed 50% duty cycle. As a result, the device outputs switch at one-half of the external clock frequency. The device switches on the rising edge of the external clock signal.

## Watchdog

A stalled clock could cause excessive DC current to flow through the primary winding of the transformer. The MAX13256 features an internal watchdog circuit to prevent damage from this condition. The internal oscillator provides the switching signal to the H-bridge whenever the period between edges on CLK exceeds the watchdog timeout period of 20 $\mu$ s (min).

## Transients on ST1/ST2 During $t_{DEAD}$

When the MAX13256 switches, there is a period of time when both ST1 and ST2 are high impedance to ensure that there are no shoot-through currents in the H-bridge. During this dead time, the voltage at these pins may temporarily exceed the absolute maximum ratings due to the inductive load presented by the transformer. This transient voltage will not damage the device.

## Disable Mode

The MAX13256 provides a disable mode to reduce current consumption. The ST1 and ST2 outputs are high impedance in disable mode.

## Power-Up and Undervoltage Lockout

The MAX13256 provides an undervoltage-lockout feature to both ensure a controlled power-up state and prevent

operation before the oscillator has stabilized. On power-up and during normal operation if the supply voltage drops below  $V_{UVLO}$ , the undervoltage-lockout circuit forces the device into disable mode. The ST1 and ST2 outputs are high impedance in disable mode.

### Overcurrent Limiting

The MAX13256 limits the ST1/ST2 output current. Connect an external resistor ( $R_{LIM}$ ) to ITH to set the current limit. When the current reaches the limit for longer than the blanking time of 1.2ms (typ), the drivers are disabled and  $\overline{FAULT}$  is asserted low. The drivers are reenabled after the autoretry time of 38.4ms (typ). If a continuous fault condition is present, the duty cycle of the fault current is approximately 3%.

To set the current-limit threshold, use the following equation:

$$R_{LIM}(k\Omega) = \frac{650}{I_{LIM}(mA)}$$

where  $I_{LIM}$  is the desired current threshold in the range of  $215mA < I_{LIM} < 650mA$  (typ). For example, a 1k $\Omega$  resistor sets the current limit to 650mA. Use a 1% resistor for  $R_{LIM}$  for increased accuracy.

Ensure that the overcurrent threshold is set to at least twice the expected maximum operating current. For an expected maximum operating current of 300mA, set the  $I_{LIM}$  to 650mA. For an expected operating current of 100mA, set the  $I_{LIM}$  to 215mA.

### $\overline{FAULT}$ Output

The  $\overline{FAULT}$  output is asserted low whenever the device is disabled due to a fault condition.  $\overline{FAULT}$  is automatically deasserted when the device is enabled after the autoretry time following an overcurrent fault, resulting in  $\overline{FAULT}$  toggling during a continuous overcurrent condition.  $\overline{FAULT}$  is asserted for the entire duration of an over-temperature fault.  $\overline{FAULT}$  is an open-drain output.

### Thermal Shutdown

The MAX13256 is protected from overtemperature damage by a thermal-shutdown circuit. When the junction temperature ( $T_J$ ) exceeds +160°C, the device is disabled and  $\overline{FAULT}$  is asserted low.  $\overline{FAULT}$  stays low for the duration of an overtemperature fault. The device resumes normal operation when  $T_J$  falls below +150°C.

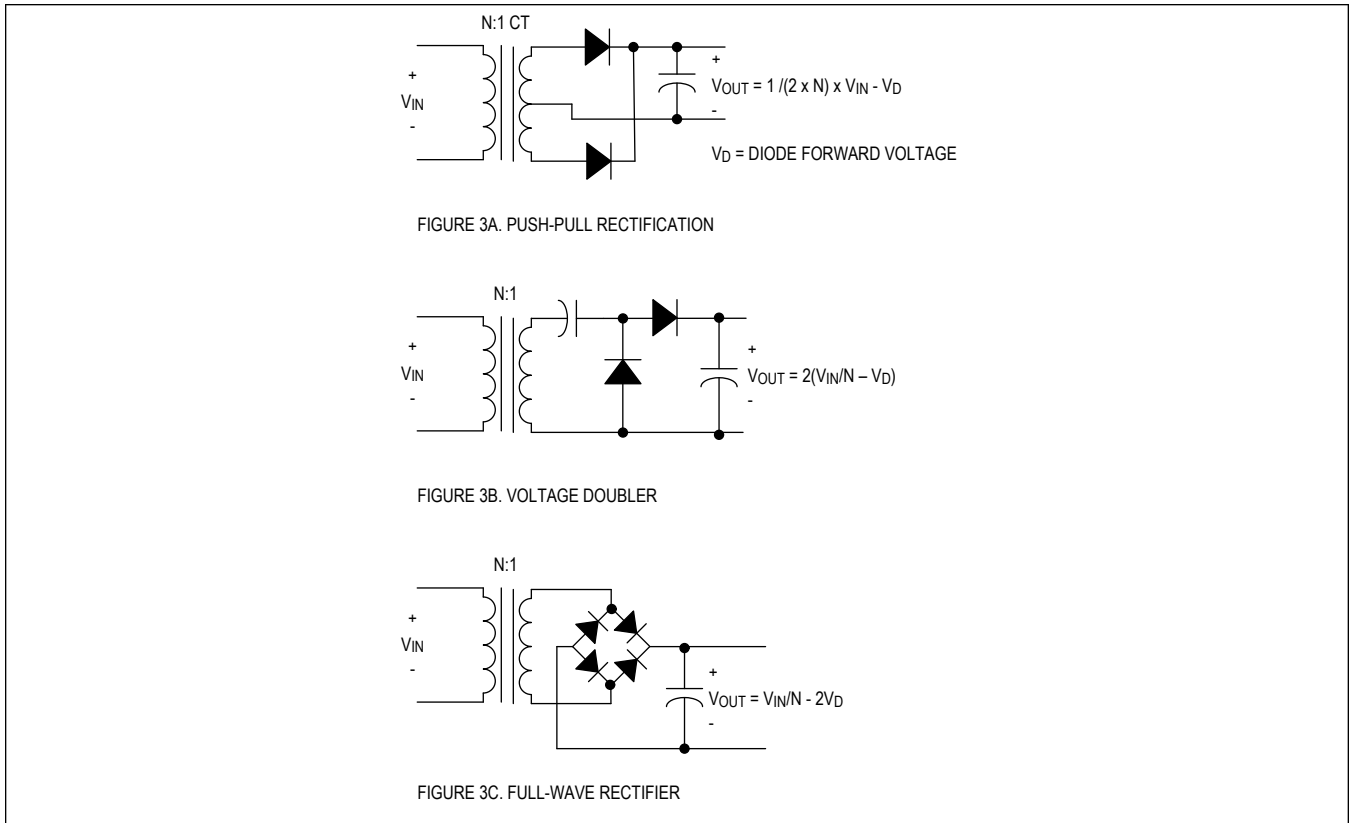


Figure 3. Secondary-Side Rectification Topologies

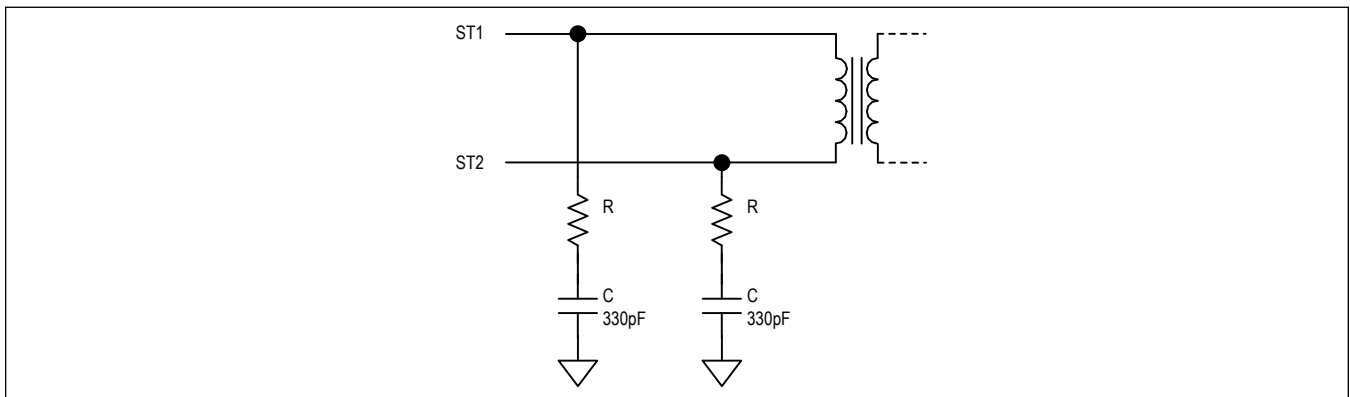


Figure 4. Output Snubber

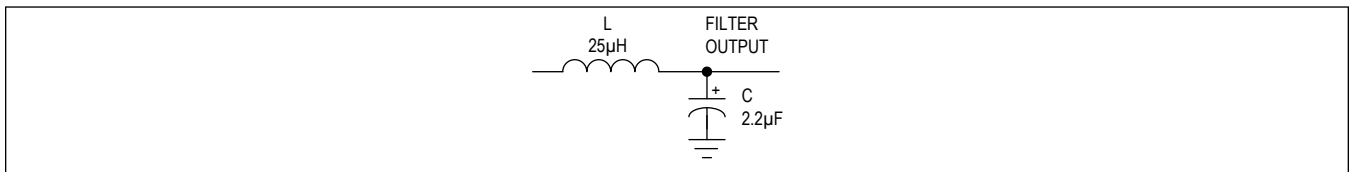


Figure 5. Output Ripple Filtering



## Applications Information

### Snubber

For  $V_{DD}$  greater than 27V, use a simple RC snubber circuit on ST1 and ST2 to ensure that the peak voltage is less than 40V during switching ([Figure 4](#)). Recommended values for the snubber are  $R = 91\Omega$  and  $C = 330\text{pF}$ .

### Power Dissipation

The power dissipation of the device is approximated by:

$$P_D = (R_{OHL} \times I_{PRI}^2) + (I_{DD} \times V_{DD})$$

where  $R_{OHL}$  is the combined high-side and low-side on-resistance of the internal FET drivers, and  $I_{PRI}$  is the load current flowing through ST1 and ST2.

### High-Temperature Operation

When the MAX13256 is operated under high ambient temperatures, the power dissipated in the package can raise the junction temperature close to thermal shutdown. Under such temperature conditions, the power dissipation should be held low enough so that that junction temperature observes a factor of safety margin. The maximum junction temperature should be held below +140°C. Use the package's thermal resistances to calculate the junction temperature. Alternatively use the Maximum Output Current vs. Temperature curves shown in the [Typical Operating Characteristics](#) section to determine the maximum ST1/ST2 load currents.

### Hot Insertion

If the MAX13256 is inserted into a live backplane, it is possible to damage the device. Damage is caused by overshoot on  $V_{DD}$  exceeding the absolute maximum rating. Limit the transient input voltage to the MAX13256 with an external protection device.

### Output-Ripple Filtering

Output-voltage ripple can be reduced with a lowpass LC filter (see [Figure 5](#)). The component values shown give a cutoff frequency of 21.5kHz by the equation:

$$f_{3dB} = \frac{1}{2\pi\sqrt{LC}}$$

Use an inductor with low DC resistance and sufficient saturation current rating to minimize filter power dissipation.

### Power-Supply Decoupling

Bypass  $V_{DD}$  to ground with a 1 $\mu\text{F}$  ceramic capacitor as close as possible to the device.

### Output-Voltage Regulation

For many applications, the unregulated output of the MAX13256 meets the output-voltage tolerances. This configuration represents the highest efficiency possible with the device.

For applications requiring a regulated output voltage, Maxim provides several solutions. In the following examples, assume a tolerance of  $\pm 10\%$  for the input voltage.

When the load currents on the transformer's secondary side are low, the output voltage can strongly increase. If operation under low load currents is expected, output-voltage limiting should be used to keep the voltage within the tolerance range of the subsequent circuitry. If the minimum output load current is less than approximately 5mA, connect a zener diode from the output node to ground as shown in [Figure 6](#) to limit the output voltage to a safe value.

#### Example 1: +24V to Isolated, Regulated +3.3V

In [Figure 6](#), the MAX13256 feeds approximately +4.4V to the input of an LDO through a TGMR-502V6LF 4:1 transformer and 4-diode bridge rectifier (see [Figure 3](#)). From this, a MAX604 LDO produces a regulated +3.3V output at up to 500mA.

#### Example 2: +24V to Isolated, Regulated +12V

In the circuit of [Figure 7](#), the MAX13256 feeds approximately +14.2V through a 1.5:1 transformer and a 4-diode bridge rectifier (see [Figure 3](#)). From this, a MAX1659 LDO produces a regulated +12V output at up to 350mA.

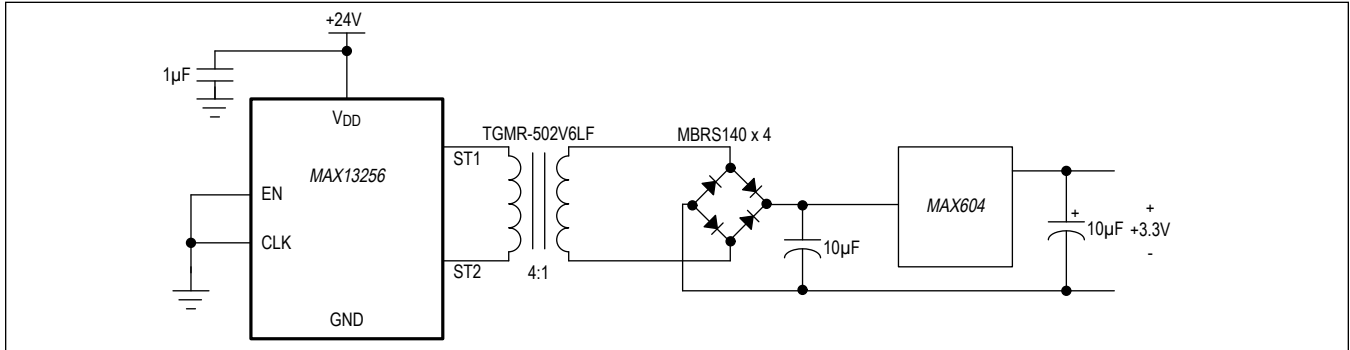


Figure 6. +24V to Isolated, Regulated +3.3V

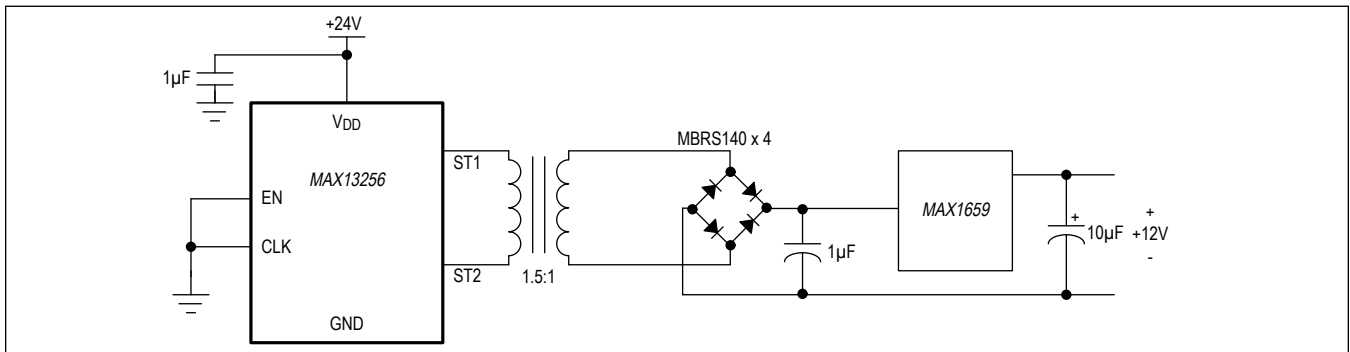


Figure 7. +24V to Isolated, Regulated +12V

### Example 3: +24V to Isolated, Regulated $\pm 15V$

In [Figure 8](#), the MAX13256 is used with a 1:1.5 center tapped transformer and a 4-diode bridge rectifier network (see [Figure 3](#)) to supply  $\pm 17.1V$  to a MAX8719 LDO and a 7915 LDO. The circuit produces regulated  $\pm 15V$  outputs at up to 100mA.

### Isolated DAC/ADC Interface for Industrial Process Control

The MAX13256 provides isolated power for data converters in industrial process control applications (see [Figure 9](#)). The 300mA output current capability allows for multiple data converters operating across an isolation barrier. The power output capability also supports circuitry for signal conditioning and multiplexing.

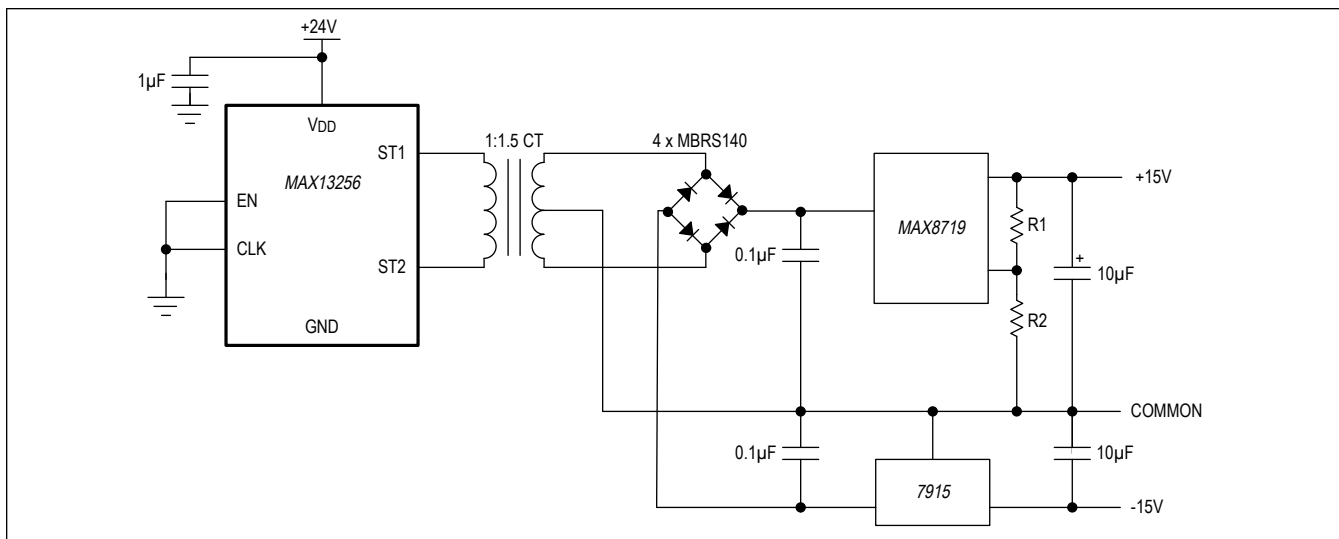


Figure 8. +24V to Isolated, Regulated ±15V

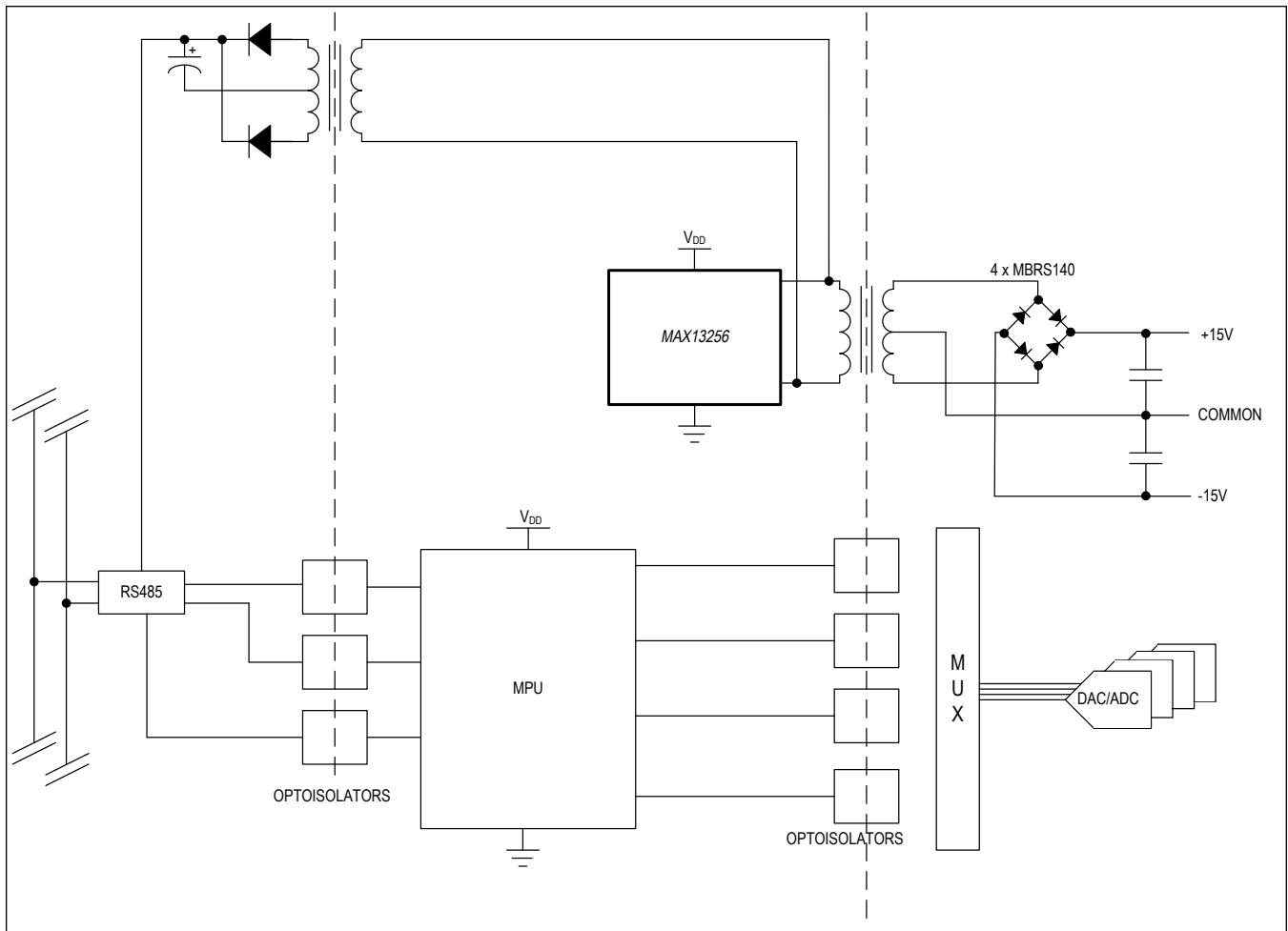


Figure 9. Isolated Power Supply for Industrial Control Applications

### Isolated RS-485/RS-232 Data Interfaces

The MAX13256 provides power for multiple transceivers in isolated RS-485/RS-232 data interface applications. The 300mA output current capability of the MAX13256 allows multiple RS-485/RS-232 transceivers to operate simultaneously.

### PCB Layout Guidelines

As with all power-supply circuits, careful PCB layout is important to achieve low switching losses and stable operation. For thermal performance, connect the exposed pad to a solid copper ground plane.

The traces from ST1 and ST2 to the transformer must be low resistance and inductance paths. Place the transformer as close as possible to the MAX13256 using short, wide traces.

When the device is operating with the internal oscillator, it is possible for high-frequency switching components on ST1 and ST2 to couple into the CLK circuitry through PCB parasitic capacitance. This capacitive coupling can induce duty-cycle errors in the oscillator, resulting in a DC current through the transformer. To ensure proper operation, ensure that CLK has a solid ground connection.

### Exposed Pad

Ensure that the exposed pad has a solid connection to the ground plane for best thermal performance. Failure to provide

a low thermal impedance path to the ground plane results in excessive junction temperatures when delivering maximum output power.

## Component Selection

### Transformer Selection

Transformer selection for the MAX13256 can be simplified by the use of a design metric, the ET product. The ET product relates the maximum allowable magnetic flux density in a transformer core to the voltage across a winding and switching period. Inductor magnetizing current in the primary winding changes linearly with time during the switching period of the device. Transformer manufacturers specify a minimum ET product for each transformer. The transformer's ET product must be larger than:

$$ET = V_{DD}/(2 \times f_{SW})$$

where  $f_{SW}$  is the minimum switching frequency of the ST1/ST2 outputs (255kHz (min)) when the internal oscillator is used or one-half of the clock frequency when an external clock source is used.

Choose a transformer with sufficient ET product in the primary winding to ensure that the transformer does not saturate during operation. Saturation of the magnetic core results in significantly reduced inductance of the primary, and therefore a large increase in current flow. This can cause the current limit to be reached even when the load is not high.

For example, when the internal oscillator is used to drive the H-bridge, the required transformer ET product for an application with  $V_{DD(max)} = 36V$  is  $70.6V\mu s$ . An application with  $V_{DD(max)} = 8.8V$  has a transformer ET product requirement of  $17.3V\mu s$ .

In addition to the constraint on ET product, choose a transformer with a low DC-winding resistance. Power dissipation of the transformer due to the copper loss is approximated as:

$$P_{D\_TX} = I_{LOAD}^2 \times (R_{PRI}/N^2 + R_{SEC})$$

where  $R_{PRI}$  is the DC winding resistance of the primary, and  $R_{SEC}$  is the DC winding resistance of the secondary. In most cases, an optimum is reached when  $R_{SEC} = R_{PRI}/N^2$ . For this condition, the power dissipation is equal for the primary and secondary windings.

As with all power-supply designs, it is important to optimize efficiency. In designs incorporating small transformers, the possibility of thermal runaway makes low transformer efficiencies problematic. Transformer losses produce a temperature rise that reduces the efficiency of the transformer. The lower efficiency, in turn, produces an even larger temperature rise.

To ensure that the transformer meets these requirements under all operating conditions, the design should focus on the worst-case conditions. The most stringent demands on ET product arise for minimum input voltage, switching frequency, and maximum temperature and load current. Additionally, the worst-case values for transformer and rectifier losses should be considered.

The primary should be a single winding; however, the secondary can be center-tapped, depending on the desired rectifier topology. In most applications, the phasing between primary and secondary windings is not significant. Half-wave rectification architectures are possible with the MAX13256; however, these are discouraged. If a net DC current results due to an imbalanced load, the average magnetic flux in the core is increased. This reduces the effective ET product and can lead to saturation of the transformer core.

Transformers for use with the device are typically wound on a high-permeability magnetic core. To minimize radiated electromagnetic emissions, select a toroid, pot core, E/I/U core, or equivalent.

### Low-Voltage Operation

The MAX13256 can be operated from an +8V supply by decreasing the turns ratio of the transformer, or by designing a voltage doubler circuit as shown in [Figure 3](#).

Optimum performance at +8V is obtained with fewer turns on the primary winding since the ET product requirement is lower than for a +24V supply. However, any of the transformers for use with a +24V supply can operate properly with a +8V supply. For a given power level, the transformer currents are higher with a +8V supply than with a +24V supply. Therefore, the DC resistance of the transformer windings has a larger impact on the circuit efficiency.

### Diode Selection

The high switching speed of the MAX13256 necessitates high-speed rectifiers. Ordinary silicon signal diodes such as 1N914 or 1N4148 can be used for low-output current levels (less than 50mA). But at higher output current levels, their reverse recovery times might degrade efficiency. At higher output currents, select low forward-voltage Schottky diodes to improve efficiency. Ensure that the average forward current rating for the rectifier diodes exceeds the maximum load current of the circuit. For surface-mount applications, Schottky diodes such as the BAT54, MBRS140, and MBR340 are recommended.

### Capacitor Selection

#### Input Bypass Capacitor

Bypass the supply pin to GND with a 1 $\mu$ F ceramic capacitor as close as possible to the device. The equivalent series resistance (ESR) of the input capacitors is not as critical as for the output filter capacitors. Typically ceramic X7R capacitors are adequate.

#### Output Filter Capacitor

In most applications, the actual capacitance rating of the output filter capacitors is less critical than the capacitor's ESR. In applications sensitive to output-voltage ripple, the output filter capacitor must have low ESR. For optimal performance, the capacitance should meet or exceed the specified value over the entire operating temperature range. Capacitor ESR typically rises at low temperatures; however, OS-CON capacitors can be used at temperatures below 0°C to help reduce output-voltage ripple in sensitive applications. In applications where low output-voltage ripple is not critical, standard ceramic 0.1 $\mu$ F capacitors are sufficient.

### Suggested External Component Manufacturers

**Table 1. Component Manufacturers**

| MANUFACTURER          | COMPONENT    | WEBSITE  |
|-----------------------|--------------|--|
| Central Semiconductor | Diodes       | <a href="http://www.centrasemi.com">www.centrasemi.com</a>           |
| Halo Electronics      | Transformers | <a href="http://www.haloelectronics.com">www.haloelectronics.com</a> |
| Kemet                 | Capacitors   | <a href="http://www.kemet.com">www.kemet.com</a>                     |
| Sanyo                 | Capacitors   | <a href="http://www.sanyo.com">www.sanyo.com</a>                     |
| Taiyo Yuden           | Capacitors   | <a href="http://www.t-yuden.com">www.t-yuden.com</a>                 |
| TDK                   | Capacitors   | <a href="http://www.component.tdk.com">www.component.tdk.com</a>     |

### Ordering Information

| PART         | TEMP RANGE      | PIN-PACKAGE |
|--------------|-----------------|-------------|
| MAX13256ATB+ | -40°C to +125°C | 10 TDFN-EP* |

+Denotes a lead(Pb)-free/RoHS-compliant package.

\*EP = Exposed Pad

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION  | PAGES CHANGED |
|-----------------|---------------|--|---------------|
| 0               | 6/11          | Initial release  | —             |
| 1               | 8/11          | Added Note 4 to Watchdog Timeout section in the <i>Electrical Characteristics</i> table, updated text and formula in <i>Overcurrent Limiting</i> section | 3, 9          |
| 2               | 9/21          | Updated ST1, ST2 Leakage Current test conditions in the <i>Electrical Characteristics</i> table  | 4             |