M08888-11

High Performance RGB Driver for DLP/LCD/LCoS Projectors

Rev V4

Features

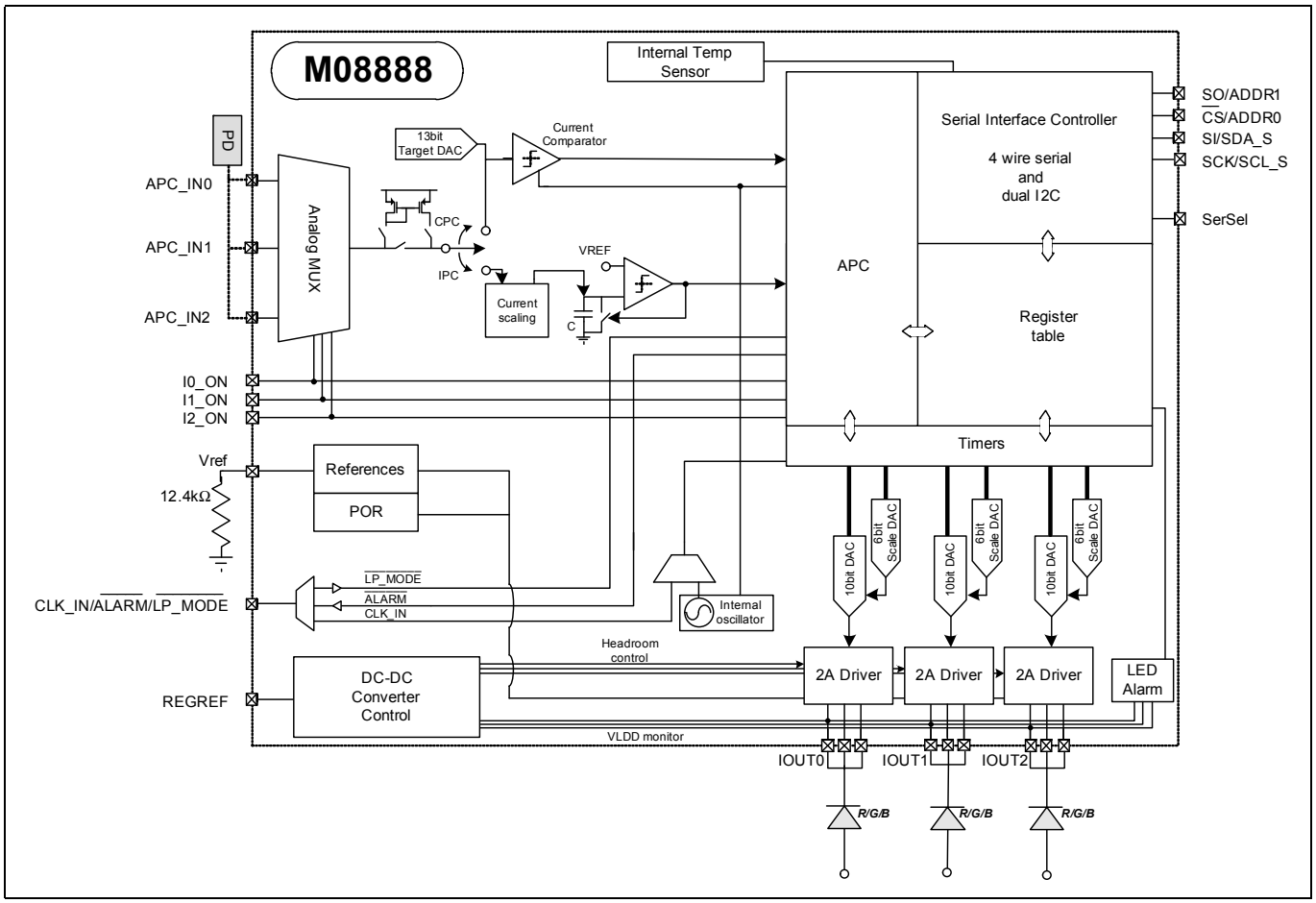
- Three 2A common anode LED/laser drivers
- Integrated 12.5 Msps 10-bit current DACs with 6-bit programmable full scale
- Real-time continuous and integrating optical power control
- DC-DC control circuitry
- Safety circuitry
- High speed 4 wire interface or I^2C

Applications

- DLP/LCD/LCoS Projector Systems
- Backlight illumination

The M08888 is a high efficiency integrated triple channel 2A LED/laser driver for LCD/LCoS/DLP projection displays. It features automatic optical power control for consistent white balance across temperature variation and light source aging. The M08888 allows for the control of an external DC-DC converter to generate optimal light sources supply and improve overall system efficiency. An internal junction temperature monitor is also available. The part can be programmed via I^2C or high speed 4-wire SPI interface.

M08888 Block Diagram



Ordering Information

Part Number	Package	Operating Temperature
M08888G-11 *	28 pin, 4.5 mm x 4.5 mm QFN	-40 °C to +85 °C
M08888-11EVM	Evaluation board with M08888-11	-40 °C to +85 °C
* The letter "G" designator in the part number indicates that the device is RoHS-compliant.		

Revision History

Revision	Level	Date	Description
V4	Release	July 2015	Updated register references.
E (V3)	Release	September 2011	Updated Ordering Information
D (V2)	Release	August 2011	Add operating specifications at Tc=120°C in Tables 1-5, 1-6 and 1-8. Change pin24 from *DIS* to *GND*.
C (V1)	Release	June 2011	Update Product Specifications, Functional Descriptions and Register Descriptions
B (V1P)	Preliminary	October 2010	Update Product Specifications, Functional Description and Register Descriptions. Swapped pinout of *ADDR0* (pin 19) and *ADDR1* (pin 18).
A (V1A)	Advance	June 2010	Initial

Conventions

Throughout this document, pins will be identified with italics (example *IOUT1*) while x or X means 0,1,2 to indicate the different channels.

1.0 Product Specification

1.1 Absolute Maximum Ratings

These are the absolute maximum ratings at or beyond which the IC can be expected to fail or be damaged. Reliable operation at these extremes for any length of time is not implied.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
DV_{DD}, ALV_{DD}	1.8 V Digital and Analog Voltage at pins *DVDD* and *ALVDD*	1.98	V
DHV_{DD}, AHV_{DD}	3.3 V Digital and Analog Voltage at pins *DVDD* and *ALVDD*	3.63	V
IOUT0, IOUT1, IOUT2	Output pins for driving LED/Laser - maximum voltage	5.5	V
T_{JCTN}	Junction Temperature	-40 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
SERSEL	Serial data format select input	-0.4 to 3.63	V
APC_IN0, APC_IN1, APC_IN2	RGB Photodiode Feedback Input Voltage	-0.4 to ALV_{DD} + 0.4	V
I_{APC_IN0}, I_{APC_IN1}, I_{APC_IN2}	RGB Photodiode Feedback Input Current	-0.5 to 4	mA
I_VREF	Current into Reference Voltage Pin	-0.12 to +0.12	mA
I0_ON, I1_ON, I2_ON	Enable LED/Laser output	-0.4 to 3.63	V
CLK_IN, $\overline{CS}$, SI, SCLK, SO	SPI inputs and output	-0.4 to 3.63	V
SCLK_S, SDA_S	I^2C interface	-0.4 to 3.63	V
REGREF	External DC-DC converter control signal	-0.4 to DV_{DD} +0.4	V
I_REGREF	Current into or out of *REGREF*	-0.12 to +0.12	mA

1.2 DC Characteristics

Min and Max values: Tc= -40 °C to 85 °C, DV_{DD}=1.8 V+/-5%, ALV_{DD}=1.8 V+/-5%, DHV_{DD}=3.3 V+/-5%, AHV_{DD} =3.3 V+/-5% unless otherwise noted. **Typical values:** Tc=25 °C, DV_{DD}=1.8 V, ALV_{DD}=1.8 V, DHV_{DD} =3.3 V, AHV_{DD} =3.3 V unless otherwise noted.

Table 1-2. DC Characteristics

Symbol	PARAMETER	CONDITIONS	Min	Typ	Max	Units
DV_{DD}	1.8 V supply for digital circuitry		1.71	1.8	1.89	V
ALV_{DD}	1.8 V supply for analog circuitry		1.71	1.8	1.89	V
DHV_{DD}	3.3 V supply for digital circuitry		3.13	3.3	3.47	V
AHV_{DD}	3.3 V supply for analog circuitry		3.13	3.3	3.47	V
I_{LVDD}	1.8 V Supply Current (DV_{DD} and ALV_{DD})[1, 2]	Open Loop	—	18.5	21.5	mA
		Closed Loop (IPC)	—	8.5	11	
		Closed Loop (CPC)	—	22	30	
I_{HVDD}	3.3 V (DHV_{DD} and AHV_{DD})[1] Standby Current - 3.3 V	Open Loop	—	7.5	13	mA
		Closed Loop (IPC) additional to open loop current	—	—	0.05	
		Closed Loop (CPC)	—	2.5	3.2	
LV_{POR}	1.8 V SET Threshold 1.8 V RESET Threshold	For positive going supply For negative going supply	—	1.5 1.4	—	V
HV_{POR}	3.3 V SET Threshold 3.3 V RESET Threshold	For positive going supply For negative going supply	—	2.72 2.62	—	V
Tc	Case Temp.	Measured on top of M08888 case	-40	—	85	°C

NOTES:

1. Excludes serial interface (SPI/I^2C) current and LED current
2. I_{LVDD} will be increase by 0.5% of the *I**x**_OUT* current when *I**x**_OUT* is active. For the specified values inputs are toggling at 1 kHz at 50% of maximum *I**x**_OUT* current.

1.3 APC Input Characteristics (register 4Ah[4]=1b)

Min and Max values: Tc= -40 °C to 85 °C, DV_{DD}=1.8 V+/-5%, ALV_{DD}=1.8 V+/-5%, DHV_{DD}=3.3 V+/-5%, AHV_{DD} =3.3 V+/-5% unless otherwise noted. **Typical values:** Tc=25 °C, DV_{DD}, ALV_{DD}=1.8 V, AHV_{DD} =3.3 V

Table 1-3. APC Input Characteristics (photodiode cathode connected to pin APC_INX and photodiode anode connected to ground)

Parameter	Conditions	Minimum	Typical	Maximum	Units
Full scale input	*APC_IN0,1,2*	3.1	3.25	3.4	mA
PD capacitance[1]	*APC_IN0,1,2*	—	—	80	pF
Input bias	*APC_IN0,1,2*	—	1.8	—	V
Maximum input voltage		—	—	1.89	V

NOTES:

1. Care should be taken in routing of each PD input so that total capacitance on the pin including routing does not exceed 80 pF

1.4 APC Input Characteristics (register 4Ah[4]=0b)

Min and Max values: Tc= -40 °C to 85 °C, DV_{DD}=1.8 V+/-5%, ALV_{DD}=1.8 V+/-5%, DHV_{DD}=3.3 V+/-5%, AHV_{DD} =3.3 V+/-5% unless otherwise noted. **Typical values:** Tc=25 °C, DV_{DD}, ALV_{DD}=1.8 V, AHV_{DD} =3.3 V

Table 1-4. APC Input Characteristics (Current Sink Input)

Parameter	Conditions	Minimum	Typical	Maximum	Units
Full scale input	*APC_IN0,1,2*[2]	3.1	3.25	3.4	mA
PD capacitance[1]	*APC_IN0,1,2*[2]	—	—	300	pF
Min Input bias	*APC_IN0,1,2*[2]	—	0.6		V
Maximum input voltage		—	—	1.89	V

NOTES:

1. Care should be taken in routing of each PD input so that total capacitance on the pin including routing does not exceed 300 pF
2. Only a single channel can be used (broadband monitor photodetector). If multiple channel are used accuracy is not guaranteed.

1.5 CPC Target DAC

Min and Max values: Tc= -40 °C to 85 °C, DV_{DD}=1.8 V+/-5%, ALV_{DD}=1.8 V+/-5%, DHV_{DD}=3.3 V+/-5%, AHV_{DD} =3.3 V+/-5% unless otherwise noted. **Typical values:** Tc=25 °C, DV_{DD}, ALV_{DD}=1.8 V, AHV_{DD} =3.3 V

Table 1-5. CPC Target DAC

Parameter	Conditions	Minimum	Typical	Maximum	Units
Resolution		—	13	—	bits
Conversion rate		—	30	—	Msps
Full scale monitor photodetector current		—	3.25	3.4	mA
Step size		—	350	515	nA
CPC Control Loop Accuracy[1]		-6	—	6	%

NOTES:

1. At Tc= 120 °C control loop accuracy is +/-7%

1.6 Integrating Power Control

Min and Max values: Tc= -40 °C to 85 °C, DV_{DD}=1.8 V+/-5%, ALV_{DD}=1.8 V+/-5%, DHV_{DD}=3.3 V+/-5%, AHV_{DD} =3.3 V+/-5% unless otherwise noted. **Typical values:** Tc=25 °C, DV_{DD}, ALV_{DD}=1.8 V, AHV_{DD} =3.3 V

Table 1-6. Integrating Power Control

Parameter	Conditions	Minimum	Typical	Maximum	Units
Resolution		—	10	—	bits
Count variation	Part to part	-35		+35	%
Stability[2]	For targets > 200 µA and register 0x0B=50h	-11	—	+11	%

NOTES:

1. This will correspond to a total power (LED/MPD current?) variation: monotonicity will still be guaranteed by the architecture
2. Variation of integration target over supply and temperature. At Tc= 120 °C accuracy is +/-14%

1.7 LED Drivers

Min and Max values: Tc= -40 °C to 85 °C, DV_{DD}=1.8 V+/-5%, ALV_{DD}=1.8 V+/-5%, DHV_{DD}=3.3 V+/-5%, AHV_{DD} =3.3 V+/-5% unless otherwise noted. **Typical values:** Tc=25 °C, DV_{DD}, ALV_{DD}=1.8 V, AHV_{DD} =3.3 V

Table 1-7. LED Drivers

Parameter	Conditions	Minimum	Typical	Maximum	Units
Headroom required[1]	At 2A full scale	—	—	0.3	V
Maximum allowable voltage headroom[2]		—	—	5.5	V
Rise/fall time[3]	20-80% Into 1 Ω electrical output, no snubber network	—	—	200	ns

NOTES:

1. Required headroom scales with output current, maximum output current requires maximum headroom (see Section 2.3).
2. To prevent damage at output pins do not exceed this voltage. Also verify power sequencing and power dissipation.
3. Guaranteed by design

Table 1-8. Output Current DACs

Parameter	Conditions	Minimum	Typical	Maximum	Units
Resolution		—	10	—	bits
Conversion rate		—	12.5	—	Msps
Full scale *IOUTX*	Referred to the current output	—	2	—	A
IOUTX absolute accuracy	Referred to the current output[1]	-8	—	8	%

NOTES:

1. For driver headroom > specified in Table 1-7. Measured at 1000 mA. At Tc= 120 °C accuracy is -8% to +10%

Table 1-9. Scale DACs

Parameter	Conditions	Minimum	Typical	Maximum	Units
Resolution		—	6	—	bits
Minimum scale value	Referred to the current output, equivalent to code 000000b	180	200	220	mA
Maximum scale value	Referred to the current output, equivalent to code 111111b	1.775	2	2.2	A
Scale step	Referred to the current output	25	28.6	31	mA

1.8 DC-DC Converters Reference Generators

Min and Max values: Tc= -40 °C to 85 °C, DV_{DD}=1.8 V+/-5%, ALV_{DD}=1.8 V+/-5%, DHV_{DD}=3.3 V+/-5%, AHV_{DD} =3.3 V+/-5% unless otherwise noted. **Typical values:** Tc=25 °C, DV_{DD}, ALV_{DD}=1.8 V, AHV_{DD} =3.3 V

Table 1-10. DC-DC Converters Reference Generators

Parameter	Conditions	Minimum	Typical	Maximum	Units
Voltage compliance		0.5	1.2	1.3 V	V
DAC resolution		—	9	—	bits
DAC DNL		-1.3	—	1.3	LSB
DAC full scale	(regref_setup[1]=0b)	—	100	110	µA
DAC full scale	(regref_setup[1]=1b)	—	200	220	µA
DC-DC Converter Headroom Error	Configured as per Table 2-4 using a Texas Instruments TPS63020 DC-DC converter and decimation set to 64.	-20	—	+20	mV

1.9 Internal Temperature Sensor

Typical values: Tc=-40 °C to 100 °C, DV_{DD}, ALV_{DD}=1.8 V, AHV_{DD} =3.3 V

Table 1-11. Internal Temperature Sensor

Parameter	Conditions	Minimum	Typical	Maximum	Units
Range		—	-40 to 125	—	°C
Temperature step		—	0.65	—	°C
Absolute accuracy[1]		-10	—	+10	°C

NOTES:

1. After system calibration at room temperature (one point calibration).

1.10 Light Sources Alarm

Min and Max values: Tc= -40 °C to 85 °C, DV_{DD}=1.8 V+/-5%, ALV_{DD}=1.8 V+/-5%, DHV_{DD}=3.3 V+/-5%, AHV_{DD} =3.3 V+/-5% unless otherwise noted. **Typical values:** Tc=25 °C, DV_{DD}, ALV_{DD}=1.8 V, AHV_{DD} =3.3 V

Table 1-12. Light Sources Alarm

Parameter	Conditions	Minimum	Typical	Maximum	Units
Light sensor alarm thresholds[1]		50	—	200	mV
Threshold accuracy		—	+/-15	—	mV
Alarm response time		—	5	—	µs

NOTES:

1. Threshold can be programmed through register alarm_setup0/1 to 50 mV, 100 mV, 150 mV, 200 mV.

1.11 CMOS Pins Characteristics

Min and Max values: Tc= -40 °C to 85 °C, DV_{DD}=1.8 V+/-5%, ALV_{DD}=1.8 V+/-5%, DHV_{DD}=3.3 V+/-5%, AHV_{DD} =3.3 V+/-5% unless otherwise noted. **Typical values:** Tc=25 °C, DV_{DD}, ALV_{DD}=1.8 V, AHV_{DD} = +3.3 V

Table 1-13. CMOS Pins Characteristics

Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IH}[1]		0.65 DV_{DD}	—	3.63	V
V_{IL}		0	—	0.35 DV_{DD}	V
V_{OH}		DV_{DD}-0.4	—	DV_{DD}	V
V_{0L}		0	—	0.4	V
Rise/fall time[2]	Maximum load of 5 pF. SPI mode	—	3	—	ns

NOTES:

1. Digital pins are 3.3 V (+/-10%) tolerant
2. In I^2C mode, rise/fall time depends on load and pull up resistor.

1.12 Slave I²C Timing Specifications[1,2]

Min and Max values: Tc= -40 °C to 85 °C, DV_{DD}=1.8 V+/-5%, ALV_{DD}=1.8 V+/-5%, DHV_{DD}=3.3 V+/-5%, AHV_{DD} =3.3 V+/-5% unless otherwise noted. **Typical values:** Tc=25 °C, DV_{DD}, ALV_{DD}=1.8 V, AHV_{DD} =3.3 V

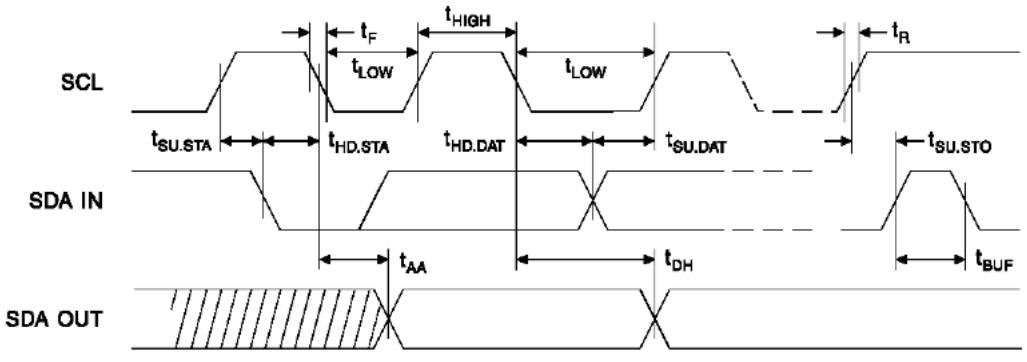
Table 1-14. Slave I²C Timing Specifications[1,2]

Parameter	Symbol (refer to figure below)	Minimum	Typical	Maximum	Units
Clock Frequency, SCL_M	f_{SCL_MASTER}	—	—	3.4	MHz
Clock Pulse Width Low	t_{LOW}	160	—	—	ns
Clock Pulse Width High	t_{HIGH}	60	—	—	ns
Clock Low to Data Out Valid	t_{AA}	0	—	70	ns
Start Hold Time	t_{HDSTA}	160	—	—	ns
Start Set-up Time	t_{SUSTA}	160	—	—	ns
Data In Hold Time	t_{HDDAT}	0	—	—	ns
Data In Set-up Time	t_{SUDAT}	10	—	—	ns
Outputs (*SDA_M, SCL_M, SDA_S* and *SCL_S*) internal pull-up resistor value [3]	$R_{PULL-UP}$	—	250	—	kΩ
Stop Set-up Time	t_{SUSTO}	160	—	—	ns
Data Out Hold Time	t_{DH}	5	—	—	ns

NOTES:

1. Guaranteed by design and characterization.
2. Specified at recommended operating conditions.
3. 4.7 kΩ should be added externally.

Figure 1-1. Slave I²C Timing



1.13 High Speed Serial Interface Timing Specifications

Min and Max values: Tc= -40 °C to 85 °C, DV_{DD}=1.8 V+/-5%, ALV_{DD}=1.8 V+/-5%, DHV_{DD}=3.3 V+/-5%, AHV_{DD} =3.3 V+/-5% unless otherwise noted. **Typical values:** Ta=25 °C, DV_{DD}, ALV_{DD}=1.8 V, AHV_{DD} =3.3 V

Table 1-15. High speed serial interface timing specifications

Parameter	Symbol (refer to figure below)	Minimum	Typical	Maximum	Units
Clock Frequency	fclk=1/Tclk	—	—	3.4	MHz
Data in to clk hold time	Tdh	160	—	—	ns
Data in to clk set-up time	Tds	60	—	—	ns
Enable to clk set up time	Tcs	0	—	70	ns
Enable to clk hold time	Tch	160	—	—	ns
Read data output valid following rising edge of SCLK	Tdd	160	—	—	ns
SCLK duty cycle		45	—	55	%

NOTES:

1. Maximum output capacitance of 30 pF.

Figure 1-2. Serial Interface Sequential Write

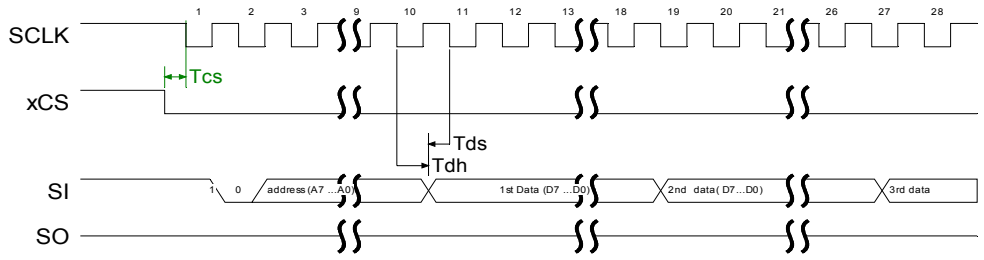


Figure 1-3. Serial Interface Random Write

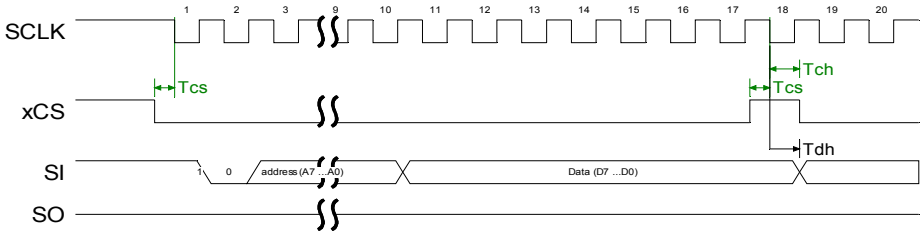


Figure 1-4. Serial Interface Sequential Read

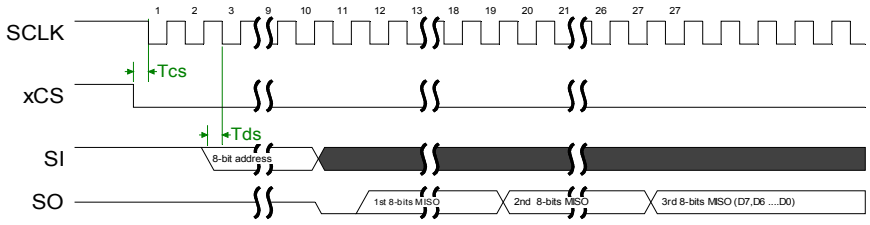
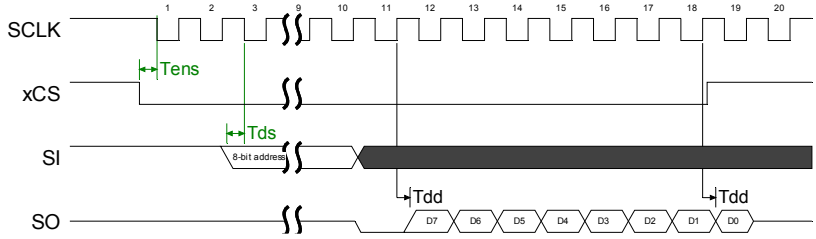


Figure 1-5. Serial Interface Random Read



1.14 M08888 Pinout

The M08888 is packaged in a 4.5 x 4.5 mm 28-pin QFN package with 0.5 mm pin pitch.

Figure 1-6. M08888 Pinout

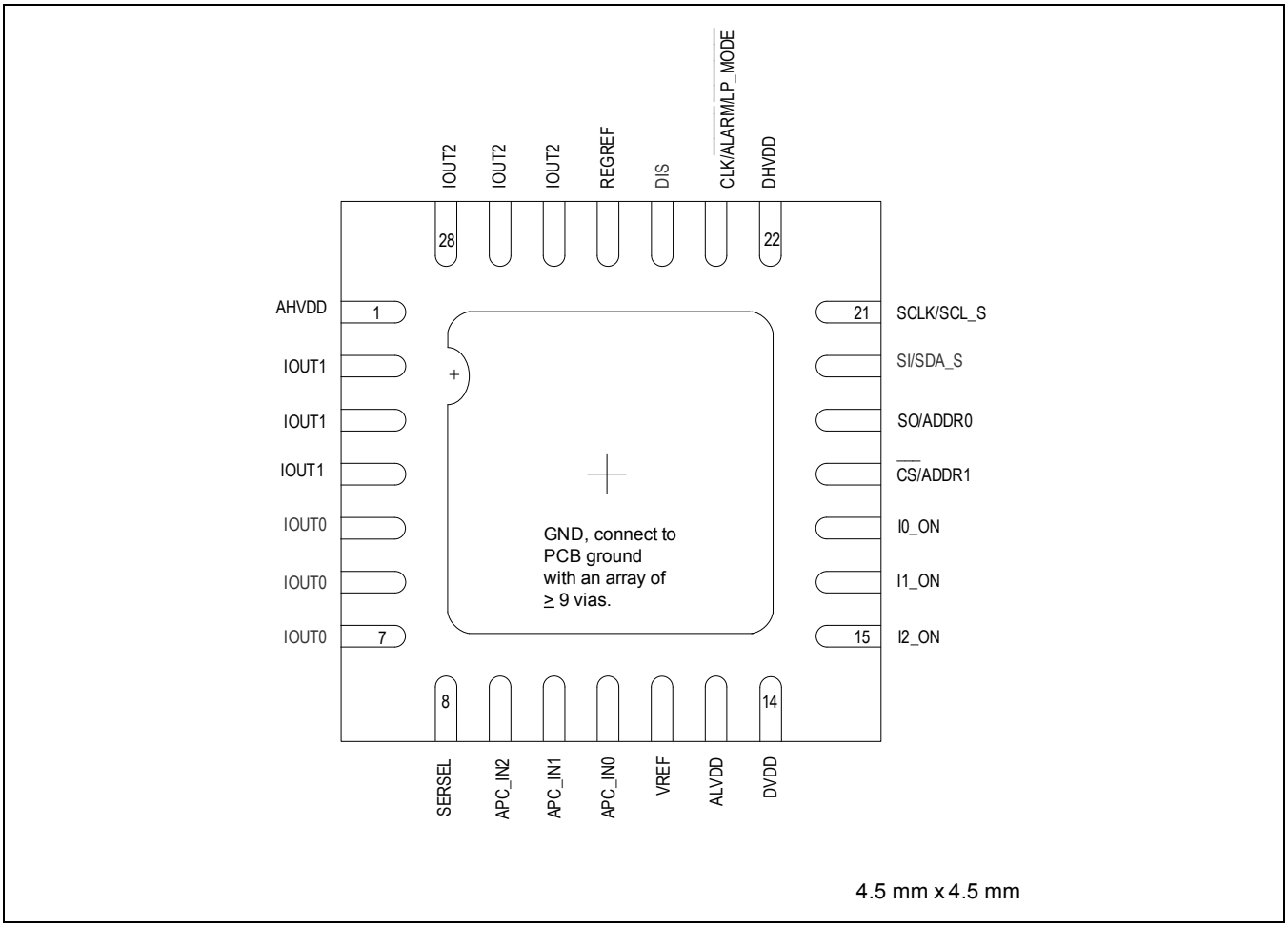


Table 1-16. Pin List and Descriptions

Pins	Name	Type	Function
1	*AHVDD*	Supply	3.3 V analog supply
2, 3, 4	*IOUT1*	Analog	Channel 1 output
5, 6, 7	*IOUT0*	Analog	Channel 0 output
8	*SerSEL*	CMOS (w/ pulldown)	Serial interface select (L=I^2C,H=SPI)
9, 10, 11	*APC_IN*	Analog	Monitor PD inputs (assignable)
12	*VREF*	Analog	Current reference generator
13	*ALVDD*	Supply	1.8 V analog supply
14	*DVDD*	Supply	1.8 V digital supply
15	*I2_ON*	CMOS (w/ pulldown)	Turns on driver 2
16	*I1_ON*	CMOS (w/ pulldown)	Turns on driver 1
17	*I0_ON*	CMOS (w/ pulldown)	Turns on driver 0
18	$\overline{CS}$/*ADDR0*	Open Drain (w/ pull-up)	Serial enable/I^2C address0
19	*SO/ADDR1*	Open Drain (w/ pull-up)	Serial data out/I^2C address1
20	*SI/SDA_S*	Open Drain (w/ pull-up)	Serial data in/I^2C data slave
21	*SCLK/SCL_S*	Open Drain (w/ pull-up)	Serial clock/I^2C clock slave
22	*DHVDD*	Supply	3.3 V digital supply
23	*CLK_IN/*$\overline{ALARM}$/$\overline{LP\_MODE}$	CMOS (w/ pulldown)	CLK_IN pin or $\overline{ALARM}$ or $\overline{LP\_MODE}$ pin
24	*DIS*	CMOS	Disable Pin
25	*REGREF*	Analog	DC-DC converter control voltage
26, 27, 28	*IOUT2*	Analog	Channel 2 output
	GND	Supply	Ground

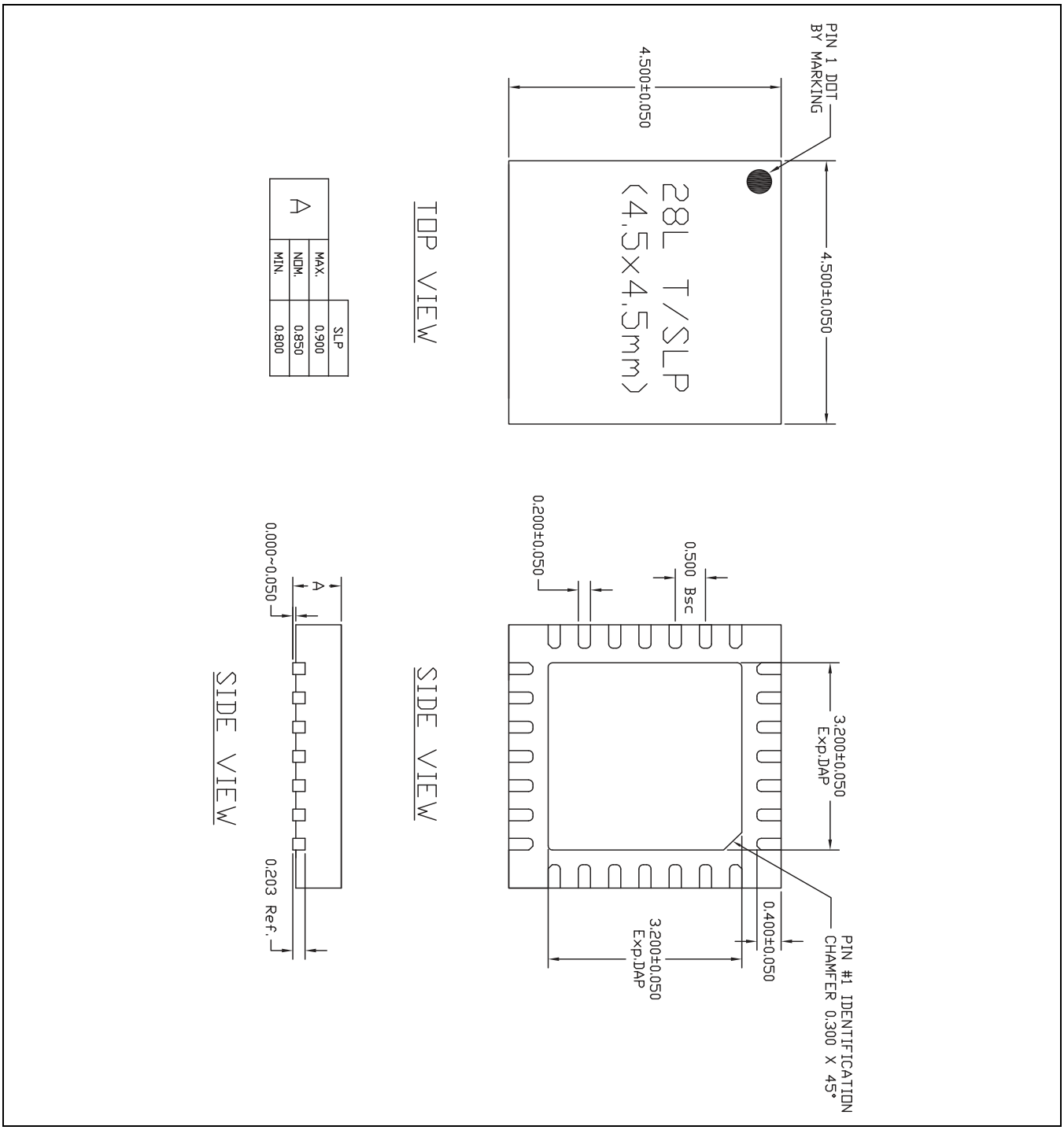
NOTES:

PD means pulled down, PU means pulled up.

4.7 µF + 100nF should be used on each of the M08888 supply.

1.15 Package Information

Figure 1-7. Package Information



2.0 Functional Description

The M08888 is a highly integrated LED/laser driver for LCD/LCoS/DLP projection display applications. It provides control and monitoring of up to three LEDs/lasers, a temperature sensor and control of external DC-DC converters for optimal laser/led supply voltage.

Each Laser/LED output consists of a 10 bit DAC which controls a high efficiency driver. If the desired maximum current is less than 2A the output resolution can by improved by a 6 bit independent scaling DAC.

The output stages require only 300 mV of headroom between the M08888 output and the Laser/LED cathode when driving 2 amperes. The headroom requirement can be scaled proportionally lower for lower currents.

The M08888 also incorporates safety and alarm features and a temperature monitor with 8 bit resolution.

The M08888 internal registers are loaded from an external micro controller through a slave I^2C interface or a 4-wire high speed interface. The host micro controller can monitor the temperature sensor and read back the analog to digital converter outputs and status registers using either serial interface.

2.1 Operating Modes

The M08888 can operate in 3 different optical power control modes. The power control modes are open loop (OL) and 2 automatic power control (APC) modes: continuous power control (CPC) and integrating power control (IPC).

Different output channels can have different operating modes. Some channels may be configured as Open Loop and some channels may be configured to use APC (either CPC or IPC).

Open Loop mode is the simplest mode of operation and the Laser/LED current is set by writing the desired current to the output DAC.

The 2 automatic power control modes (APC) use monitor photodiode feedback to accurately adjust the Laser/LED output power to make the current from a photodiode match a target current. With APC control temperature compensation of the Laser/LED is automatic and color balance is simplified.

The user can select the polarity of the monitor photodetector if an APC mode is selected. By default the M08888 accepts a current source monitor photodetector (MPD) tied to the positive supply. It is possible to accept current sink MPD by selecting ipc_setup[4]=1b.

Configuration of the M08888 timer settings and pin 23 configuration will also affect optical power control.

2.1.1 Open Loop Output Control

In open loop mode the current for each Laser/LED is stored in register (iout**x**[9:0]). The M08888 will shift the contents of iout**x**[9:0] and iout**x**_scale[5:0] registers to the output DAC when pin ***Ix**_ON* goes high and the output will then sink the programmed current through the Laser/LED.

By changing the scale setting iout**x**_scale the full 10 bits of settability can be retained even for low Laser/LED currents. The scale can be changed on a frame by frame basis but when iout**x**_scale is changed the rise time of the output stage will be significantly slower during the first *I**x**_ON* period in which the change in the scale is made. The rise time will return to its normal value in subsequent *I**x**_ON* periods if the scale is not changed.

The M08888 includes timers that can be used to delay, pulse width modulate or clock the Open Loop output signal. See Section 2.4 for a description of how to use these features.

When pin 23 operates in $\overline{LP\_MODE}$ (input_ctrl[6:5]=10b) the scale value of each channel can be different for the different pin 23 states. These scales are set in iout**x**_scale[5:0] (pin 23=H) and iout**x**_scale_LP[5:0] (pin 23=L).

Table 2-1. Basic Register Configuration for Open Loop Control (when REGREF is not controlling a DC-DC Converter)

Name	Address	Recommend Setting	Description
out_ctrl**x**	0x05[7],0x06[7], 0x07[7]	1b	Set outputs to Open Loop Control if Regref is not used to control a DC-DC converter at this output.
pd_fe	0x0A[0]	1b	Power down photodiode amplifier (if all channels are under open loop control)
iout**x**_msb	0x10[1:0], 0x14[1:0], 0x18[1:0]	xxb	Two most significant bits of output current setting
iout**x**_lsb	0x11, 0x15,0x19	xxh	Eight least significant bits of output current setting
iout**x**_scale	0x12, 0x16, 0x1A	11xxxxxb	Set the scaling of the output currents
iout**x**_scale_lp	0x13, 0x17, 0x1B	11xxxxxb	Set the scaling of the output currents in Low Power mode
apc0_ch apc1_ch apc2_ch	0x34[1:0] 0x34[3:2] 0x34[5:4]	11b	Disable APC input for selected channel

2.1.2 Automatic Power Control

Automatic power control (APC) can keep the laser/led power constant and the color balanced by comparing the monitor photodetector (RGB color sensor) currents to target values programmed into the 13-bit target DACs.

At power-up the APC can be enabled/disabled independently for each channel by setting apc_ctrl0[5:0]=11. For channels with disabled APC the laser/led currents are controlled through the serial interface using bits iout**x**[9:0].

It is possible to freeze the APC loop for each channel by using apc**x**_freeze[0]. In this case the M08888 will stop updating the *IOUT**x*** currents independently of the state of *I**x**_ON* pins.The photodiode (RGB sensor) target values are programmed via the serial interface in registers target2[12:0], target1[12:0] and target0[12:0] respectively for *IOUT2, IOUT1* and *IOUT0*. When the corresponding color is turned on as signaled by the transition of *I0_ON*, *I1_ON* or *I2_ON* from low to high the LED/Laser drive currents are automatically adjusted up or down to always make the photodetector current (RGB sensor current) match the target current.

If desired, these target currents can be adjusted on a frame by frame basis to optimize contrast and save battery power depending on the brightness required for a particular frame.

The target values are stored in registers target2[12:0], target1[12:0] and target0[12:0] respectively for *IOUT2*, IOUT1 and IOUT0 before the corresponding color is turned on by the transition of *I2_ON*, *I1_ON* or *I0_ON* from low to high. This allows for the control of the LED/laser power in real time on a frame by frame basis.

When one of the ***Ix**_ON* signals is enabled (low to high transition), the target DAC value for that input is activated and the incoming monitor photodetector current is selected by the analog multiplexer from *APC_IN0*, *APC_IN1* or *APC_IN2*. The monitor photodetector input is assigned to an output using apc_ctrl[5:0].

Each Laser/LED can have its own photodetector or all the Lasers/LEDs can share a single broadband photodetector. For example, if a single broadband photodetector is used and connected to APC_IN0 all the apc_ctrl0[5:0] should be set to 00b. It should be noted that the index in the APC registers does not refer to the input channel but to the Laser/LED output channel. If the monitor photodetector feedback for IOUT2 is tied to APC_IN0 then apc_ctrl[5:4]=00 and the settings for the monitor photodetector should be programmed in the APC registers with index 2.

If more then one laser is turned on (2 or 3 of I0_ON, I1_ON or I2_ON are high at the same time) the M08888 freezes the update of the APC loop for as long as more then one of the ***Ix**_ON* signals are high. This prevents the APC loop from using incorrect photodetector information in case a single photodetector is used. In the case of multiple ***Ix**_ON* simultaneously the optical power tracked and adjusted is that of the channel corresponding to the last***Ix**_ON* transitioning high. It should be noted that 2 or more low to high transitions of any of the *I0_ON*, *I1_ON* or *I2_ON* within 500 ns of each other would violate internal timing and will result in unpredictable operation. Care should be taken to prevent damage to the part when multiple lasers are enabled. The power dissipation of the M08888 should be kept below the level that, when multiplied by the thermal resistance of the package in the system and added to the maximum ambient temperature, does not exceed 125 °C.

The maximum photodiode current supported by the M08888 is 3.25 mA. The full scale value of the target DAC is 3.25 mA with a resolution of 13 bits (390 nA step size). As an example, if the maximum current from the photodiode is 200 µA then the possible target values are up to 512 decimal (200 µA/390 nA). In this example the maximum target value for target**x**[12:0] would be 200h.

Readback of the output current DAC of each channel is possible by strobing the DACs using strbalarm_ctrl[1] and reading registers rb_iout**x**[9:0]

When pin 23 is set to $\overline{LP\_MODE}$ (input_ctrl[6:5]=10b) the target power value will be controlled by the state of pin 23. When pin 23 is high the Laser/LED current will be adjusted until the monitor photodiode current matches the target in register target**x**[12:0] and when pin 23 is low the Laser/LED current will be adjusted until the monitor photodiode current matches the target in register target**x** _LP[12:0].

The M08888 is capable of accepting also current sink type monitor photodetector typical of LCOS panels. This can be done by setting register ipc_setup[4]=1b. When sink MPD is selected the mirror ratio can be selected between 1:1 and 4:1 by setting bit ipc_setup[5].

The MPD can have a maximum capacitance of up to 300 pF however in this case the M08888 will operate only with a single broadband photodetector.

2.1.2.1 Continuous Power Control

In continuous power control (CPC) mode, the M08888 continuously compares the monitor photodetector current to a target value and makes monitor photodiode current match the target value by adjusting the current in the laser/LED. For example, if the monitor photodetector current is below the target then the Laser/LED current is increased. The sign of this operation can be inverted using input_ctrl[4] (but it should not be changed unless it is certain that there is an inversion in the monitor photodiode signal).

The CPC loop is designed to settle to the desired output power in less than 50 µs. To achieve optimal settling time, the CPC loop must be adjusted to the laser/monitor photodetector characteristics. This is done using the settings in apc**x**_ctrl0, apc**x**_ctrl1 and apc**x**_ctrl2.

To further reduce the settling time the user can program the initial current from which the CPC loop will start. This can be 0, the value programmed in iout**x**[9:0] register or the value to which the CPC had converged during the previous frame. The selection of the initial current is done using register iturnon**x**[1:0] (apc**x**_ctrl1[3:2]). Starting from the previously determined value will substantially accelerate settling time since it is likely that it will be starting at the proper level.

It is possible to “freeze” the APC loop for each channel by using apc**x**_ctrl0[0]. When apc**x**_ctrl0[0]=1b the M08888 will stop updating the *IOUT**x*** currents irregardless of the state of *I**x**_ON* pins. It is possible also to delay operation the CPC loop immediately following the light source turn-on. This will allow the DC-DC converter to settle to the proper voltage before the APC starts adjusting the current. The CPC delay time can be programmed using register apc**x**_ctrl0[2:1].

Table 2-2. Basic Register Configuration for CPC Control

Name	Address	Recommend Setting	Description
out_ctrl**x**	0x05[7],0x06[7], 0x07[7]	1b	Set output to Closed Loop Control
loop select apc0_ch apc1_ch apc2_ch	0x34[6] 0x34[1:0] 0x34[3:2] 0x34[5:4]	1b xxb	Select CPC loop control Select which photodiode (RGB sensor) input will control which output. Setting depends on hardware connection to photodiode(s) and which channels will use APC control. See Register description for details.
target**x**_msb target**x**_lsb	0x35, 0x37, 0x39 0x36, 0x38, 0x3A	000x xxxxb xxh	Set the target at desired level. The LED drive current will be adjusted up or down until the photodiode current is equal to the target current for the channels that are controlled by CPC.
apc0_ctrl2 apc1_ctrl2 apc2_ctrl2	0x47 0x44 0x41	xxh	Set the length in clock counts of the initial, mid and min step intervals. Set the delay for the clock divider. The decimation factor and clock divider will also affect interval lengths.
apc0_ctrl1 apc1_ctrl1 apc2_ctrl1	0x48 0x45 0x42	xxh	Set the step size of the change in LED drive current for the initial and mid intervals. Set the initial LED current to be 0 mA, the ending value of the previous I_on period or the value set in iout**x** register. Set the clock divider.
apc0_ctrl0 apc1_ctrl0 apc2_ctrl0	0x49 0x46 0x43	xxx00xx0b	Set the decimation factor (mid and min count changes will occur at rate divided by the decimation factor). Set the WAIT states (APC will not change LED current during WAIT states).

2.1.2.2 Integral Power Control

Integral power control (IPC) can be enabled by setting registers apc_ctrl[6]=0b.

The working principle of integral power control is to mimic the behavior of the human eye which integrates the optical power over the frame period. This is achieved in the M08888 by charging a capacitor with the monitor photodetector current.

When ***Ix_ON*** goes high the M08888 will drive the Laser/LED with a current defined by register iout**x**[9:0]. The monitor photodiode current will charge an internal capacitor until its voltage matches an internal reference voltage (~0.8 V) at which time a counter is incremented and the capacitor is discharged. The monitor photodiode current continues to charge the capacitor and increment the counter until the count matches the target set by the user in registers target**x**[9:0]. Once the counter reaches the value set by the user the M08888 stops driving the Laser/LED. By adjusting the count higher or lower the brightness of a frame can be adjusted. The target counter has 10bits and the M08888 can distinguish between 1024 different power levels. The target registers are the same of the CPC target registers but the resolution in IPC mode is limited to 10 bits instead of 13 bits.

In order to maximize the dynamic range and be able to utilize the entire 10bits the user must select the proper mirroring ratios for the monitor photodetector current (ipd**x**_sel[4:0]), the charging current (ich**x**_sel[4:0]) and the value of the capacitance (cap**x**_sel[3:0]). The settings of these bits will depend on the frame (or subframe) duration and on the monitor photodetector current.

If it is desired to typically have the LED on for 1/2 the frame time then the registers should be configured such that:

$$1/2 \times FR/512 = 0.8\ V \times Cch / Ich$$

where FR is the frame or subframe rate, Cch is the charging capacitors selected through cap**x**_sel[3:0], and Ich is the resulting charging current obtained by multiplying the monitor photodetector current by the ipd**x**_sel[4:0] and by the ich**x**_sel[4:0] mirroring ratios. The factor of 512 is length of the 10 bit range.

$$Cch = 25\ pF + N \times 2.5\ pF$$ where N is the setting of cap**x**_sel[3:0].

$$Ich = (I_{MPD} / ipdx\_sel[4:0]) \times ichx\_sel[4:0]$$ where I_{MPD} is the monitor photodiode current

Example: Assume that the monitor photodiode current is 150 µA when the LED is on at the desired amplitude, the ***Ix_ON*** time is 1 ms and it is desired that the LED be on approximately 50% of this time. The mirroring ratio should be set to the 200 µA range ich**x**_sel[4:0] = 00001b, choose a Cch = 25 pF with ich**x**_sel[4:0] = 00000b (any other value is also OK but using the default value means this register never needs to be written), choose a mirroring ratio such that the Cch can be charged to 0.8 V several hundred times in 0.5 ms. (if it is desired that it be charged ~250 times in 0.5 ms then:

0.5 ms/250 =0.8 V x 25 pF /((150 µA / 200 µA) x ich**x**_sel[4:0])
0.002 ms = 26.67e-12 / ich**x**_sel[4:0]
ich**x**_sel[4:0] = 2.667e-5 / 2 which is between 10 µA and 20 µA so set ich**x**_sel[4:0] =00001b

As in CPC mode, when pin23 operates in $\overline{LP\_MODE}$ (input_ctrl[6:5]=10b) the target power value can be changed by toggling pin23. When pin 23 is high the Laser/LED current will be on until the monitor photodiode count matches the target in register target**x**[9:0] and when pin 23 is low the Laser/LED current will be on until the monitor photodiode count matches the target**x** _LP[9:0].

The monitor photodiode input can be changed from sinking to sourcing at ipc_setup[4] and an additional scaling factor of 4:1 is available at ipc_setup[5].

Table 2-3. Basic Register Configuration for IPC Control

Name	Address	Recommend Setting	Description
ipc_setup[4]	0x4Ah[4]	0b or 1b	M08888 sinks MPD current (1b) or sources MPD current (0b)
out_ctrl**x**	0x05[7],0x06[7], 0x07[7]	1b	Set output to Closed Loop Control
loop select	0x34[6]	0b	Select IPC loop control
apc0_ch apc1_ch apc2_ch	0x34[1:0] 0x34[3:2] 0x34[5:4]	xxb	Select which photodiode (RGB sensor) input will control which output. Setting depends on hardware connection to photodiode(s) and which channels will use APC control. See Register description for details.
target**x**_msb target**x**_lsb	0x35, 0x37, 0x39 0x36, 0x38, 0x3A	000xxxxxb xxh	Set the target to the desired count. The LED drive current set in the iout**x** register will be on until the current from the ich**x** current mirror charges the capacitor set at ipc**x**_ctrl2[3:0] to 0.8 V the number of times set in this target register (the capacitor at pc**x**_ctrl2[3:0] is discharged every time the 0.8 V comparator is tripped and recharging begins again until the target count is reached).
iout**x**_msb	0x10[1:0], 0x14[1:0], 0x18[1:0]	xxb	Two most significant bits of output current setting
iout**x**_lsb	0x11, 0x15,0x19	xxh	Eight least significant bits of output current setting
iout**x**_scale	0x12, 0x16, 0x1A	11xxxxxb	Set the scaling of the output currents
ipd**x**_sel	0x4C[4:0] 0x4F[4:0] 0x52[4:0]	x xxxxb	Select a setting that is greater than the peak current expected from the monitor photodiode. Choosing a lower amplitude setting will give more resolution/accuracy in setting the IPC target.
ich**x**_sel	0x4D[4:0] 0x50[4:0] 0x53[4:0]	x xxxxb	Select a current range that can charge the IPC capacitor several hundred (but <511) times during the *I**x**_ON* time.

2.2 Outputs

2.2.1 LASER/LED Current DACs

The M08888 includes three monotonic DACs which generate the currents for the three LED output drivers.

The three DACs have a maximum range from 0 to 2A, a resolution of 10 bits and a maximum update rate of 12.5 MSPS. The output rise time will be limited by the M08888 output current driver unless a single DC-DC converter is used for more than one Laser/LED, in which case the DC-DC converter settling time and overall supply loop behavior may determine the output rise time.

The full scale of each output DAC can be programmed through the iout**x**_scale[5:0] bits independently for each channel. The scale DAC changes the full scale of each output current DAC from a minimum of 200 mA to a maximum of 2A in steps of 28.57 mA. At power-up the scale DACs are set at maximum scale (2A).

2.2.2 Output Current Drivers

The integrated output current drivers deliver the DAC currents to the Lasers/LEDs.

Each Laser/LED driver output (*IOUT**x***) is controlled by the corresponding ON signal (*I**x**_ON*) and the PWM and MPG setting as described later. Rise/fall time of the driver is typically 200 ns into a resistive electrical load connected to a stable supply voltage. If a DC-DC converter is employed the response time of the current output may also depend on the response time of the DC-DC converter and the series resistance of the light sources. The rise and fall time is specified for any transition of the iout**x**[9:0] registers for a constant iout**x**_scale[5:0] code.

The drivers require a worst case headroom of 300 mV. The headroom is proportionally lower at lower drive currents.

The M08888 typical driver headroom follows the following equation:

VLDD = 150 mΩ x IOUT

The voltage at the laser driver output should never exceed 5.5 V. An external resistor should be used between the laser/LED cathode and ground to provide a small leakage current into the light source allowing the voltage at the *IOUT**x*** to be reduced from the anode voltage by the laser/LED voltage drop. The value of the resistor should be chosen such that the current flowing is enough to create a voltage drop on the laser while keeping the laser current far below threshold or, in the case of LEDs, low enough so as to not cause light pollution in the system.

2.2.3 Recommended Snubbing Network at *IOUTx* Pins

A snubbing network of 1 µF in series with 1.5 Ω should be placed in parallel with the LED/Laser at each *IOUT**x*** pin. The inductance in series with the LED/Laser should be less than 500 nH.

2.3 Controlling the Output Voltage to Optimize Power Consumption

The system power dissipation will be dominated by the Laser/LED current and the bias voltage of the Laser/LED. For each ampere of Laser/LED current, each 100 mV of excess Laser/LED bias voltage results in 100 mW of wasted power.

The M08888 minimizes the voltage drop on the output stage and optimizes overall power dissipation by adjusting the anode voltage of the light sources through the external DC-DC converter. Given the expected maximum current for a particular LED/laser on a channel, the user can program the headroom required for each channel based on the equations above (Section 2.2.2) to optimize system power. Whether or not the M08888 controls the DC-DC converter output voltage the required headroom of the M08888 outputs must be maintained when the corresponding *I**x**_ON* is high (see Section 2.2.2).

2.3.1 Control of External DC-DC Converters with the M08888

An external DC-DC converter is controlled by the M08888 by connecting pin *REGREF* to the DC-DC converter feedback pin.

Typical register settings to allow control of an external DC-DC converter are shown below.

Table 2-4. Basic Register Configuration for Controlling an External DC-DC Control

Name	Address	Recommended Setting	Description
selfcal_hr	0x00[4]	1b	Power-up REGREF circuitry
opmode_ctrl1	0x01[7]	1b	Set DC-DC output to minimum when all *Ix_ON* are low
out_ctrlx	0x05, 0x06, 0x07	8Ch	Recommended Configuration
regref_setup	0x24	00h	Set REGREF operating mode
regref2_ctrl1	0x27	FFh	Set the headroom at *IOUT2* to 310 mV and the decimation factor to 2048. Lower headroom values can be used depending on the maximum *IOUT2* output current. See section 2.2.2
regref2_ctrl0	0x28	44h	Set the DAC update rate and the starting value at *IOUT2*.
regref1_ctrl1	0x2B	FFh	Set the headroom at *IOUT1* to 310 mV and the decimation factor to 2048. Lower headroom values can be used depending on the maximum *IOUT1* output current. See section 2.2.2
regref1_ctrl0	0x2C	44h	Set the DAC update rate and the starting value at *IOUT1*.
regref0_ctrl1	0x2F	FFh	Set the headroom at *IOUT0* to 310 mV and the decimation factor to 2048. Lower headroom values can be used depending on the maximum *IOUT0* output current. See section 2.2.2
regref0_ctrl0	0x30	44h	Set the DAC update rate and the starting value at *IOUT0*.

The M08888 DC-DC converter control circuitry uses a 9 bit DAC to set a feedback factor for the external DC-DC converter and adjust the anode voltage of the Laser/LEDs. The DAC is controlled by a digital filter with programmable update rate and decimation factor. The digital filter is fed by a comparator which increments or decrements the counter code depending on whether the headroom of the driver is higher or lower than the programmed headroom. The sign of this operation can be inverted through input_ctrl[3] (this bit should not be set unless it is known that the DC-DC converter feedback path is inverted from the usual polarity). The above operations are performed automatically by the M08888 and no interaction with the M08888 is required beyond initializing the register settings as described at the beginning of this section.

Once the LED is turned off the value of the DAC inputs are stored by the M08888. The next time this LED is active, the loop will automatically start from the stored DAC value. The initial value of the DAC code can be selected through regref**x**_ctrl0[3:2] to be either the previously determined value, 0 or the value written in register regref**x**_dac. The DAC codes for each channel can be read back by using the strobe bit (strbalarm_ctrl[1]) and registers rb_regrefdac**x**[8:0].

The headroom, decimation filter and update rate can be programmed independently for each channel using regref**x**_ctrl1[7:3], regref**x**_ctrl1[2:0] and regref**x**_ctrl0[7:5] respectively.

If more then one output is being turned on at the same time, the regref will control the DC-DC converter for the headroom of the last output turned on.

If CPC is used, the user should program the headroom for the highest expected output current.

If CPC control is used there may be interactions between the settling of the DC-DC converter and the digital control method. If the settling of the DC-DC converter is such that the initial headroom is less than what is required by the Laser/LED then this may cause the CPC loop to rail (adjust the Laser/LED current to 2A) and potentially damage

the Laser/LED when the voltage rises to a high enough voltage to allow unrestricted forward current conduction. The interaction of the DC-DC converter digital control method with the CPC should therefore be carefully evaluated to avoid damage to the LEDs. One way to minimize interaction between the voltage supply and the CPC control is to let the voltage supply settle before enabling CPC control of the Laser/LED current. The update of the output current in CPC mode can also be delayed using register apc**x**_ctrl0[2:1] to allow proper settling of the DC-DC converter before the operation of control loop starts.

The initial update of the IDAC which controls the LED/Laser supply headroom can be delayed through registers regref**x**_ctrl0[1:0] to allow the DC-DC converter to settle.

In the case of integrating power control mode the speed of the DC-DC converter settling is not important: the light source current will be equal to the programmed current if the headroom is higher or equal to the required and will be smaller if the headroom is less then the required headroom however this will not matter as long as the frame/ subframe time is long enough to guarantee that the integrated power over the time meets the target.

The monotonic DAC used for controlling external DC-DC converters has a full scale current of 100 µA and 9bits of resolution. The full scale can be increase by a factor of 2 to 200 µA by setting regref_setup[1]=1b.

If the *I**x**_ON* signals do not overlap and there is a significant amount of time (>10 µs) when *I**x**_ON*=L (blanking period), opmode_ctrl1[7] should be set to 1. In this case during the blanking period the DAC current is set to 0 and all the *IOUT**x*** signals are disconnected so that an external resistor divider network can be used to set the light sources anode voltage. The impedance level at *REGREF* pin, defined by R1//R2//input impedance of the DC-DC converter, should always be greater then 500 kΩ.

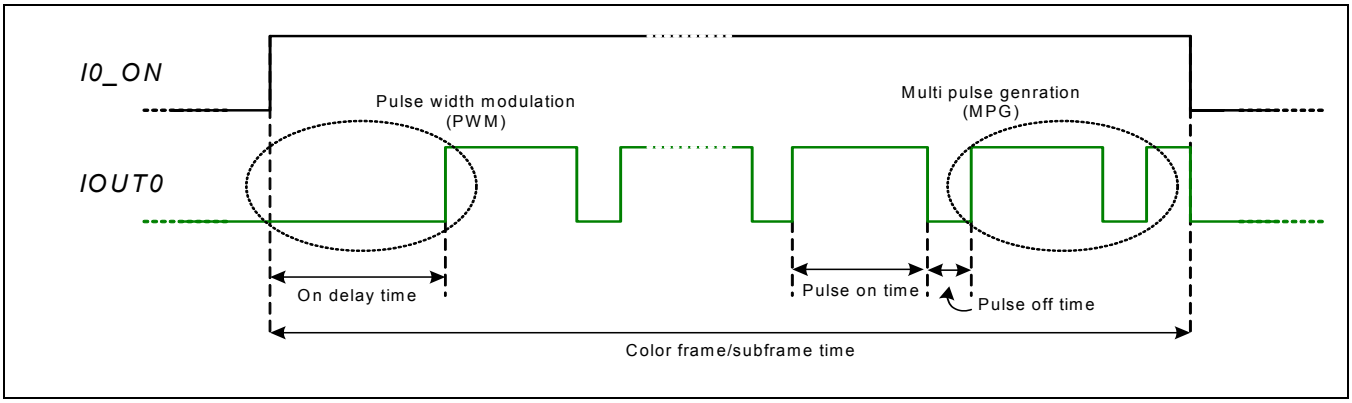
2.4 Timers

The M08888 features internal timers which allow an extra layer of control of the current by means of pulse width modulation (PWM) and multi pulse generation (MPG).

The clock source for the internal timer circuitry can be either the internal 25 MHz oscillator or an external clock fed through *CLK_IN* (pin 23).

With reference to the following diagram for channel 0 (*I0_ON, IOUT0*), PWM controls the “On delay time” while MPG adjusts independently both the “Pulse on time” and “Pulse off time”.

Figure 2-1. Example of PWM and MPG Timers



2.4.1 Pulse Width Modulation (PWM)

Activating pulse width modulation will allow the output current to be delayed with respect to the ***Ix**_ON* signal. This may be useful if a blanking period is needed to allow the LCD or DLP to settle or it may be useful to save power if a laser is used and the same optical output can be achieved with fewer coulombs if higher laser driver currents and shorter durations are used (the coulombs will be less with higher current and shorter duration if the laser threshold current is approximately the same with PWM activated at higher current as it is at lower current without PWM activated).

PWM works in all optical power control modes: Open Loop, CPC and IPC.

The PWM delay is implemented with a 10 bit counter that counts the clock cycles of an internal 25 MHz oscillator. At the rising edge of each ***Ix**_ON* the counter is decremented and the Laser/LED is turned on when the counter reaches 0. The laser is turned off as usual on the falling edge of the corresponding ***Ix**_ON* signal. The maximum delay achievable is ~41 µs (1023 times the 40 ns period of the internal oscillator). Additional delay can be achieved by using the M08888 programmable divider of the internal clock. The internal clock can be divided down by a factor of 1, 2, 4, 8, 16, 32, 64, and 128. This can be obtained by writing register clk_div_pwm[3:0]. The maximum delay is therefore equal to ~5.24msec.

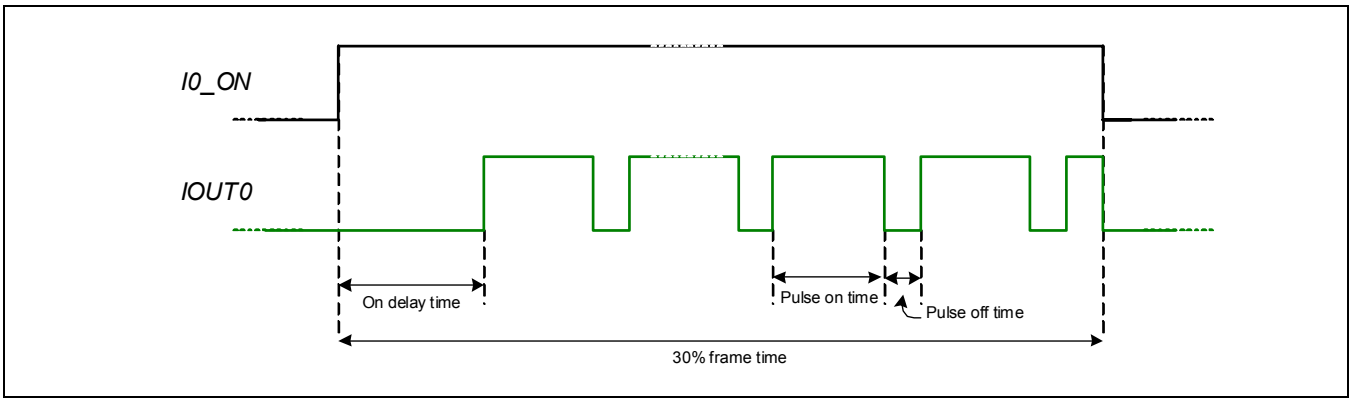
The values of the programmable counter are stored in register on_count**x**[9:0]. The rising edge of the ***Ix**_ON* signal strobes the corresponding on_count**x**[9:0] value into the M08888 in the same fashion as other output current settings such as registers target**x**[12:0] and iout**x**[9:0] registers. If the on_count register value is changed during the on time for that color the effect of the register change will be available during the next ***Ix**_ON* cycle.

If the on_count**x** is programmed to 000h the PWM feature is disabled for *IOUT**x***.

The internal ring oscillator clock will vary by as much as +/-15% over process, temperature and supply. If this accuracy is not acceptable then pin 23 can be defined to be a clock input and a more accurate external clock signal can be used. The PWM block is designed to operate with a maximum frequency of 25 MHz. The PWM generator will work at the speed of the signal at *CLK_IN* (pin 23) when the external clock is selected with register clk_ctrl[2:1].

2.4.2 Multi Pulse Generator (MPG)

Figure 2-2. Multi Pulse Generator Timing



A less than 100% duty cycle pulsed waveform can be programmed into the M08888 using the Multi-Pulse Generator (MPG).

The multi-pulse generator (MPG) operates in a similar manner of the PWM generator. For each of the Lasers/LED outputs, two 10bit counters specify the number of 25 MHz internal clock cycles during which the output is on and off. As with the PWM timer, the MPG timer can be controlled by an external clock signal at *CLK_IN* (pin 23).

The duty cycle of the pulsed waveform is resolved in 25 MHz clock periods or 40 ns steps. If both counters are loaded with the maximum value (1023) the waveform driving the output will be a clock of period ~81 µs.

The clock can be divided down to lower rates by programming register clk_div_mpg[3:0].

MPG works in all optical power control modes: Open Loop, CPC and IPC. However if IPC or CPC power control is employed, the minimum divider ratio at register clk_div_mpg[3:0] is 8. Care should be taken when MPG is used while controlling the DC-DC converter as the slow response time of the DC-DC converter to variation in the light source drop may create oscillation and instability. It is recommended that register opmode_ctrl0[5]=1 if analog control mode is used to control the DC-DC converter. In this setting the DC-DC converter feedback will not be driven while the LED current is off (pulse off time). To prevent the DC-DC converter from drifting away from the optimal headroom operating point external resistive feedback R1/R2 should be added as shown in figure 1-2. The effective resistance of R1/R2 should be 500 kΩ.

Because a 10 bit counter is used, the duty cycle resolution obtainable is 1/1023 or better then 0.1% assuming the highest count value is used for one of the counters. The duty cycle accuracy is inversely proportional to the maximum counter value.

The control for the *IOUT**x*** output on pulse is programmed in register pulse_on**x**[9:0]. The off pulse is programmed in pulse_off**x**[9:0].

The rising edge of the *I**x**_ON* signals strobe the corresponding pulse_on/off**x**[9:0] values into the M08888 timing controller. If the pulse_on/pulse_off register values are changed during the on time for that output the MPG setting will not be changed until the next *I**x**_ON* cycle.

If either the pulse_on or pulse_off for a channel is programmed to 000h then the MPG function is disabled for that channel.

2.5 Temperature Sensor

The M08888 features an internal temperature sensor which measures the internal junction temperature of the part. The information is converted by the ADC and can be read through the serial interface at temp[7:0] register.

The ambient temperature of the system can be calculated from the part junction temperature, the part power dissipation and the package thermal resistance (temperature measurements can vary dramatically at different locations within a system and measurements are dependent on mechanical factors such as PCB area, material and number of layers, airflow, heatsinking, etc.)

Absolute accuracy of the temperature sensor is +/-10 °C after calibration at room temperature. Its resolution is 8-bit or 0.65 °C over the range of -40 °C to 125 °C.

2.6 Safety

Using this driver for LEDs or Lasers in the manner described in this data sheet does not ensure that the resulting optical emissions comply with established standards such as IEC825. Designers must take the necessary precautions to ensure that eye safety and other applicable standards are met. Note that determining and

implementing the level of fault tolerance required by the applications that this part is going into is the responsibility of the projector designer and manufacturer since the application of this device cannot be controlled by MACOM.

A register alarm is available: the safety monitor block compares the output current of each Laser/LED with 3 thresholds (one for each of the lasers/LEDs) and an alarm is issued if the current is higher then the programmed thresholds. The digital thresholds can be programmed in the following registers: alarm_th**x**[7:0], these represent the MSB of the output current.

The alarm can be routed to the *CLK_IN* (pin 23) by setting input_ctrl[6:5]=00b. This signal can be used externally to shut down power to the lasers/LEDs or it can be read back from register alarm_ctrl[7:2] by the micro controller. It should be noticed that the alarm_ctrl[7:2] register is not self clearing: once an alarm has occurred, it must be cleared by the user by writing 1 to clear_alarm (strbalrm_ctrl[0]).

The M08888 can also be programmed (opmode_ctrl1[3]) for automatic shutdown if the programmed threshold is exceeded. In this case the output current for that output is automatically forced to 0 by forcing 0 to the DAC inputs. This feature can be disabled via registers.

When configured as $\overline{ALARM}$ pin 23 is an open collector and can operate in status mode and interrupt mode. This can be selected through opmode_ctrl0[3]. In status mode the alarm is provided directly to the pin. It should be noticed that in status mode the alarm may be issued only for the duration of one clock cycle of the internal high speed clock. Because of the high speed of the digital engine (12.5 MHz clock) a load which acts as a low pass filter will prevent this signal from being recognized by external circuitry. Excess capacitance and high impedances may act as low pass filters. In interrupt mode the M08888 will issue a positive going pulse on the alarm pin every time the internal alarm changes state. The width of the generated pulse can be programmed at opmode_ctrl0[2:0].

The output stage can also be disabled by the user via register, through bits opmode_ctrl1[1].

2.7 Alarm

The M08888 is capable of detecting an open or a short at the driver outputs and it will issue an alarm if a voltage lower then the programmed threshold is detected at the *IOUT**x*** outputs while the Laser/LED is not driven. Similarly, while the Laser/LED is driven, an alarm is issued if the voltage at *IOUT**x*** decreases below a preprogrammed threshold. This would indicate an open LED as the driver will force the *IOUT**x*** voltage to 0 if no LED is connected.

The LED alarms can be enabled and programmed independently for each channel using registers alarm_setup0[7:0] and alarm_setup1[3:0].

If pin23 is configured as $\overline{ALARM}$ the alarm is issued at that pin but the alarm can also be read back at alarm_iout[2:0]. Alarm _iout[2:0] is not self clearing.

To prevent false alarms caused by slow DC-DC converter settling the alarm signal can be delayed using alarm_set1[5:4].

2.8 Programmable Serial Interface

The M08888 will not begin operation until the internal registers of the M08888 are loaded and the start bit is set (0x61[0]=1b). It is not necessary to load values into a register if its default value is acceptable.

The M08888 can be configured to use a 4 wire high speed serial interface or I^2C. This can be achieved by connecting pin *SERSEL* high or low respectively.

When the part is configured to use I^2C, an external host µController can access the register and read-back ADC from the slave I^2C (SDA_S/SCL_S). The maximum SCL_S supported is 400 kHz. The slave address of the part can be programmed using *ADDR0/1* pin. The address of the M08888 will be set to 98h, 9Ah, 9Ch or 9Eh when writing from the M08888 and 99h, 9Bh, 9Dh or 9Fh when reading to the M08888 when *ADDR0/1* pin configured respectively to 00b, 01b, 10b or 11b.

4.7 kΩ pull up resistors should be used.

The 4 wire high speed interface (*SCLC/SI/SO/$\overline{CS}$*) supports up to 40 MHz serial clock speeds.

2.9 Power Sequencing

To obtain reliable operation from the M08888 the power-up and power-down sequencing described in the diagrams below must be followed.

Figure 2-3. Power-Up

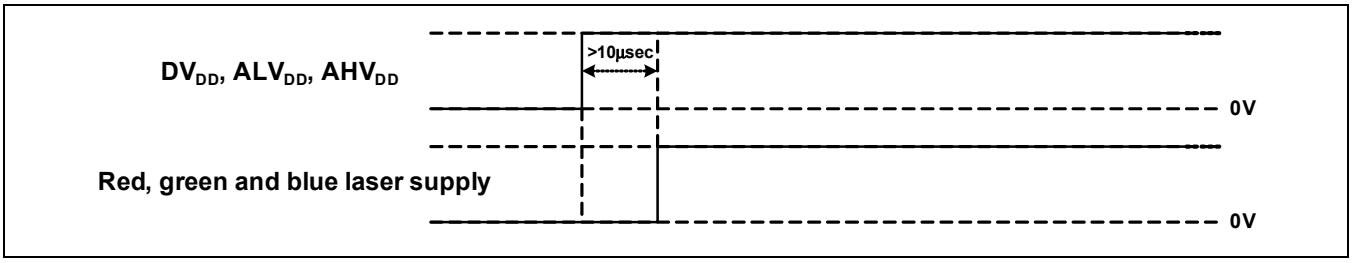
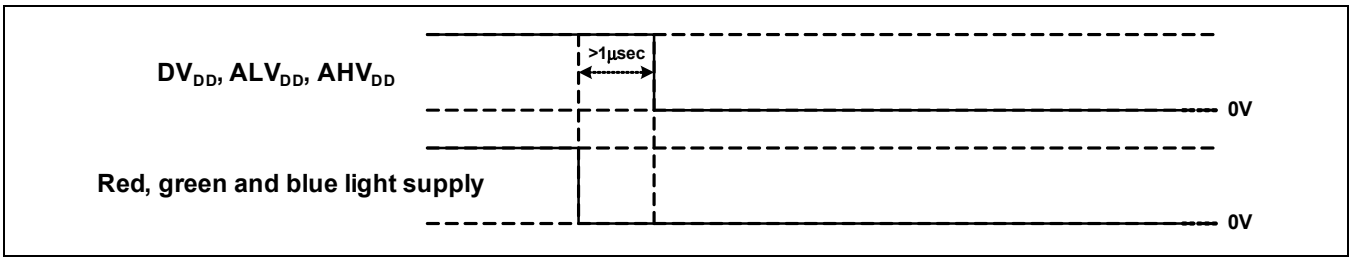


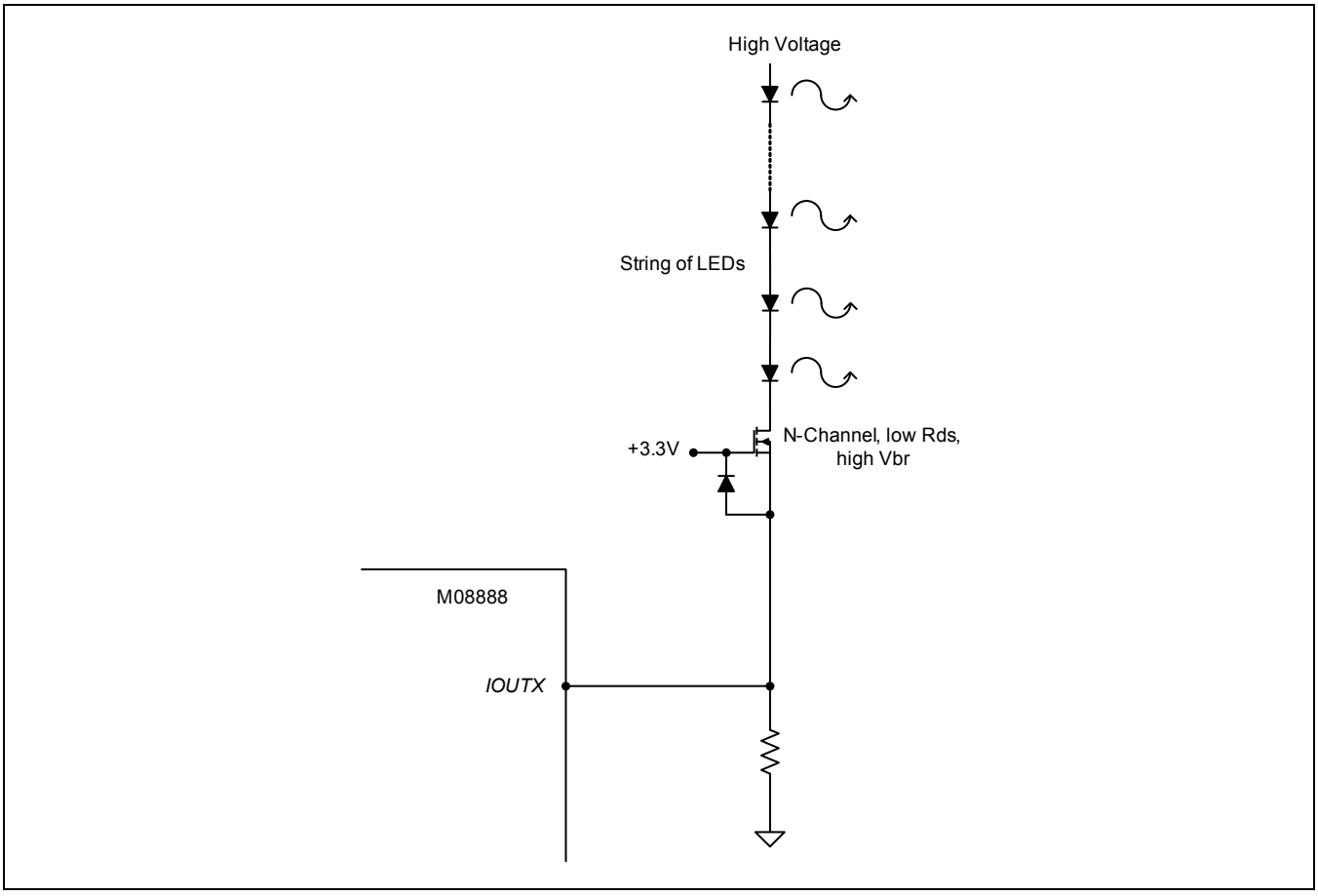
Figure 2-4. Power-Down



2.10 Driving a String of LEDs from a High Voltage Supply

An M08888 can be used to drive a string of LEDs as shown in Figure 2-5 below. The M08888 must be isolated from the high voltage by an NFET transistor. The NFET should have a breakdown voltage greater than the high voltage supply and should also have a very low on resistance at 2.5 V gate-source voltage. The Diodes Inc. DMN2075U is an example of a suitable 20 V NFET.

Figure 2-5. Driving a String of LEDs from a High Voltage Supply



2.11 Layout Considerations

The center pad of the package is the electrical ground and the heat sinking path for the M08888. The center pad should be connected to an internal ground plane through an array of 9 or more vias.

The accuracy of the internal DACs and the LED/laser drive amplitudes and timing depend on pin *VREF* being noise-free. The resistor at this pin should be close to the M08888 and the via to ground from the resistor should be nearby.

The external DC-DC converter will amplify any noise on the *REGREF* pin. Care should be taken in routing this pin so it is not parallel to the laser/LED drive signals or clock signals.

Decoupling capacitors should be on the same side of the PCB as the M08888 and close to the pin they are decoupling. Vias to ground and voltage supplies should not be shared by components or signals (crosstalk between signals will occur).

3.0 Registers

Table 3-1. M08888 Registers

Addr	Register name	d7	d6	d5	d4	d3	d2	d1	d0	Default	Type
General REGISTERS											
00h	**opmode_ctrl0**	parallel	pd_target DAC	regref_ mpg	selfcal_hr	alrm_ctrl<3:0>				01000000	R/W
		1. Enable parallel mode of operation 0: Normal mode of operation	Powers down target DAC: 1: powers down target DAC (Open loop control) 0: normal operation (APC Conrol)	1: disconnect regref control during mpg 0. do not disconnect refreg during mpg event	1: enable self-cal of output headroom for all channels (Recommended for control of external DC-DC converter) 0: disable self calibration	Controls the behavior of the $\overline{\text{Alarm}}$ 1xxx: Status mode 0000: Interrupt mode with 1 cycle pulse width (1cycle=20 ns) 0001: Interrupt mode with 2 cycle pulse width 0010: Interrupt mode with 4 cycle pulse width …. 0111: Interrupt mode with 128 cycle pulse width					
01h	**opmode_ctrl1**	regref_ blank	regref_edge	seq	RSVD	alarm_dis	RSVD	disable	RSVD	00000000	R/W
		1: When all *I**x**_ON* low disconnects *IOUT**x*** and sends 0 code to IDAC (controlled by rising edge) 0: Normal operation (01h[6] setting controls regref)	Switch regref output on: 1: *I**x**_ON* falling edge 0: *I**x**_ON* rising edge	Color sequence selector in case of falling edge: 1: 2-1-0 0: 2-0-1	RSVD	Disable output on alarm: 1: disable output current on alarm 0: do not disable	RSVD	Outputs disabled 1: *IOUT**x*** disabled 0: *IOUT**x*** enabled	RSVD		

Table 3-1. M08888 Registers

Addr	Register name	d7	d6	d5	d4	d3	d2	d1	d0	Default	Type
02h	**input_ctrl**	timer_clk	pin23_def[1:0]		RSVD	regref_pol	I2_ON_pol	I1_ON_pol	I0_ON_pol	00000000	R/W
		1: Use CLK_IN as clock for the timers (MPG/PWM) 0: Normal operation (timers use internal oscillator)	Configuration register for PIN23 11: RSVD 10: Pin 23 is $\overline{\text{LP\_MODE}}$ 01: Pin 23 is CLK_IN 00: Pin 23 is $\overline{\text{ALARM}}$		RSVD	Flip regref counter polarity 1b: Flip polarity 0b: normal polarity	Polarity of *I2_ON* 1: Flipped 0: Normal	Polarity of *I1_ON* 1: Flipped 0: Normal	Polarity of *I0_ON* 1: Flipped 0: Normal		
03h	**clk_ctrl**	clk_delay				RSVD	clkin_div[1:0]		duty_en	00000000	R/W
		Input clock programmable delay: 0000 = nodelay 0001 = 500nsec 0010 = 1000nsec … 1111 = 7500nsec				RSVD	Input clock divider: 00: 1 01: 2 10: 4 11: 3		1: enable duty cycle control 0: disable duty cycle control		
04h	**RSVD**	RSVD								00000000	R/W
		RSVD									
05h	**out_ctrl2**	feedON-Off_iout2	feedBias_iout2[1:0]		RSVD		BiasOnOf_iout2	pd_iout2[1:0]		10001100	R/W
		1: Closed loop *IOUT2* output current control 0: open loop output current control (Set to 1b in all cases if DC-DC converter is controlled by Regref for this output)	Set the bias level of the Regref2 loop: 11: 1.8 V 10: 600 mV 01: 500 mV 00: 400 mV (00 is recommended)		RSVD		Increases Regref2 bias current to inprove performance at low currents 1: Enabled 0: Disabled	Power down control 11: Regref2 always on regardless of ***Ix***_*ON* signal 10: Fast power down 01: Deep sleep when ***Ix***_*ON*=L 00: Deep sleep when ***Ix***_*ON*=L			

Table 3-1. M08888 Registers

Addr	Register name	d7	d6	d5	d4	d3	d2	d1	d0	Default	Type
06h	**out_ctrl1**	feedON-Off_iout1	feedBias_iout1[1:0]		RSVD		BiasOnOf_iout1	pd_iout1[1:0]		10001100	R/W
		1: Closed loop *IOUT1* output current control 0: open loop output current control (Set to 1b in all cases if DC-DC converter is controlled by Regref for this output)	Set the bias level of the Regref1 loop: 11: 1.8 V 10: 600 mV 01: 500 mV 00: 400 mV		RSVD		Increases Regref1 bias current to inprove performance at low currents 1: Enabled 0: Disabled	Power down control 11: Output stage always on regardless of ***I*x*_ON*** signal 10: Fast power down 01: Deep sleep when ***I*x*_ON***=L 00: Deep sleep when ***I*x*_ON***=L			
07h	**out_ctrl0**	feedON-Off_iout0	feedBias_iout0[1:0]		RSVD		BiasOnOf_iout0	pd_iout0[1:0]		10001100	R/W
		1: Closed loop *IOUT0* output current control 0: open loop output current control (Set to 1b in all cases if DC-DC converter is controlled by Regref for this output)	Set the bias level of the Regref0 loop: 11: 1.8 V 10: 600 mV 01: 500 mV 00: 400 mV		RSVD		Increases Regref0 bias current to inprove performance at low currents 1: Enabled 0: Disabled	Power down control 11: Output stage always on regardless of ***I*x*_ON*** signal 10: Fast power down 01: Deep sleep when ***I*x*_ON***=L 00: Deep sleep when ***I*x*_ON***=L			
08h	**tempsens_ctrl**	temptest_sel	pd_temp	temp_cal[3:0]				temp_gain[1:0]		01100000	R/W
			1: Powers down temp sensor 0: Temp sensor enabled	Temperature sensor offset calibration				Calibrate temp sensor gain			

Table 3-1. M08888 Registers

Addr	Register name	d7	d6	d5	d4	d3	d2	d1	d0	Default	Type
09h	**tia_ctrl**	cpd_comp	cf_ctrl	cz_ctrl		rz_ctrl		rf_ctrl		00100110	R/W
		Cpd compensation 1: 16 pF 0: 9 pF	Controls value of TIA Cf 1: 700fF 0: 500fF	Controls value of CZ: APC compensation control: 11: 14 pF 10: 10 pF 01: 8 pF 00: 4 pF		Controls value of Rz: APC compensation control: 1x: 2.5kOhms 01: 3.75kOhms 00: 5kOhms		Controls value of Rf: TIA gain control: 11: 20kOhms 10/01: 40kOhms 00: 60kOhms		tia_ctrl_d	
0Ah	**apc_fe_ctrl**	RSVD	Cpd_comp[1:0]	RSVD					pd_fe	00000001	R/W
		RSVD	Photodiode compensation for APC inputs	RSVD					APC photodiode amplifier power down 1: power down (no photodiode feedback or color sensor) 0: normal operation (APC Control)		
0Bh	**bandgap**	bg_set set to 0101b				RSVD				00000000	R/W
		RSVD									
0Ch	**alarm_setup0**	led_alrm_rc1	led_alarm_thres1		en_ledalarm1	led_alrm_rc0	led_alarm_thres0		en_ledalarm0	00010001	R/W
		LED alarm time constant 1: 5usec 0: 2usec	LED alarm threshold for channel 1 00: 200 mV 01: 150 mV 10: 100 mV 11: 50 mV		Power down LED alarm for channel 1 1: power down 0: enable	LED alarm time constant 1: 5usec 0: 2usec	LED alarm threshold for channel 0 00: 200 mV 01: 150 mV 10: 100 mV 11: 50 mV		Power down LED alarm for channel 0 1: power down 0: enable		

Table 3-1. M08888 Registers

Addr	Register name	d7	d6	d5	d4	d3	d2	d1	d0	Default	Type
0Dh	**alarm_setup1**	RSVD		turnon_alarm_delay		led_alrm_rc2	led_alarm_thres2		en_ledalarm2	00110001	R/W
		RSVD		Delay alarm after channel turn on 11: 50usec 10: 100usec 01: 200usec 00: 500usec		LED alarm time constant 1: 5usec 0: 2usec	LED alarm threshold for channel 2 00: 200 mV 01: 150 mV 10: 100 mV 11: 50 mV		Power down LED alarm for channel 2 1: power down 0: enable		
10h	**iout2_msb**	RSVD						iout2[9:8]		00000000	R/W
		RSVD						*IOUT2* MSBs			
11h	**iout2_lsb**	iout2[7:0]								00000000	R/W
		IOUT2 LSBs									
12h	**iout2_scale**	RSVD		iout2_scale[5:0]						00111111	R/W
		RSVD		Adjusts *IOUT2* full scale 63d = 2A … 28d = 1A … 1d = 228.27 0d = 200 mA							
13h	**iout2_scale_LP**	RSVD		iout2_scale[5:0]						00111111	R/W
		RSVD		Adjusts *IOUT2* full scale when $\overline{LP\_MODE}$ pin is low 63d = 2A … 1d = 228.27 0d = 200 mA							
14h	**iout1_msb**	RSVD						iout1[9:8]		00000000	R/W
		RSVD						*IOUT1* MSBs			
15h	**iout1_lsb**	iout1[7:0]								00000000	R/W
		IOUT1 LSBs									

Table 3-1. M08888 Registers

Addr	Register name	d7	d6	d5	d4	d3	d2	d1	d0	Default	Type
16h	**iout1_scale**	RSVD		iout1_scale[5:0]						00111111	R/W
		RSVD		Adjusts *IOUT1* full scale 63d = 2A … 28d = 1A … 1d = 228.27 0d = 200 mA							
17h	**iout1_scale_LP**	RSVD		iout1_scale[5:0]						00111111	R/W
		RSVD		Adjusts *IOUT1* full scale when $\overline{LP\_MODE}$ pin is low 63d = 2A … 1d = 228.27 0d = 200 mA							
18h	**iout0_msb**	RSVD						iout0[9:8]		00000000	R/W
		RSVD						*IOUT0* MSBs			
19h	**iout0_lsb**	iout0[7:0]								00000000	R/W
		IOUT0 LSBs									
1Ah	**iout0_scale**	RSVD		iout0_scale[5:0]						00111111	R/W
		RSVD		Adjusts *IOUT0* full scale 63d = 2A … 1d = 228.27 0d = 200 mA							
1Bh	**iout0_scale_LP**	RSVD		iout0_scale[5:0]						00111111	R/W
		RSVD		Adjusts *IOUT0* full scale when $\overline{LP\_MODE}$ pin is low 63d = 2A … 1d = 228.27 0d = 200 mA							
1Ch	**alarm_th2**	alarm_th2[7:0]								11111111	R/W
		Alarm threshold for *IOUT2* (output DAC MSB)									
1Dh	**alarm_th1**	alarm_th1[7:0]								11111111	R/W
		Alarm threshold for *IOUT1* (output DAC MSB)									
1Eh	**alarm_th0**	alarm_th0[7:0]								11111111	R/W
		Alarm threshold for *IOUT0* (output DAC MSB)									

Table 3-1. M08888 Registers

Addr	Register name	d7	d6	d5	d4	d3	d2	d1	d0	Default	Type
1Fh	**RSVD**	RSVD								00000000	R/W
		RSVD									
20h	**RSVD**	RSVD								00000000	R/W
		RSVD									
21h	**RSVD**	RSVD								00000000	R/W
		RSVD									
22h	**RSVD**	RSVD								00000000	R/W
		RSVD									
23h	**RSVD**	RSVD								00000000	R/W
		RSVD									
DC-DC converter Control REGISTERS											
24h	**regref_setup**	extr_ctrl	regref_ res2	regref_ res1	regref_mode	pd_dac	pd_digapc	idac_cur- rent	dig_RC	00011100	R/W
		1: Use exter- nal resistor for DC-DC converter control 0: Normal operation	1: Cut resis- tor in half 0: Normal resistor	1: Add 87 kΩ resistor in series to 13.7kOhms resistor 0: Normal resistor	DC-DC con- verter control mode 1: Analog con- trol 0: Digital con- trol	Must be set to 0b if an external DC-DC is being controlled: 1: DAC pow- ered down 0: Normal operation	Must be set to 0b if external DC-DC is being con- trolled: 1: Compar- ator and headroom reference powered down 0: Normal operation	1: Double full scale IDAC cur- rent to 200 µA 0: Normal operation (100 µA)	1: Add 1usec RC filter to *IOUT* voltage when in digi- tal control mode 0: Normal operation		
25h	**regref2_dac_MSB**	RSVD							regref2_dac[8]	00000000	R/W
		RSVD							REGREF DAC output for *IOUT2*, MSB		
26h	**regref2_dac**	regref2_dac[7:0]								00000000	R/W
		REGREF DAC output for *IOUT2*									

Table 3-1. M08888 Registers

Addr	Register name	d7	d6	d5	d4	d3	d2	d1	d0	Default	Type
27h	**regref2_ctrl1**	headroom2[4:0] (100 mV/Amp, 70 mV min)					regref2_dec[2:0]			00000000	R/W
		Controls headroom for *IOUT2* 00000: 0 mV 00001:10 mV 00010:20 mV 00011:30 mV …. 11111:310 mV (recommended)					Select decimation factor for *REGREF* digital loop: 000: 1 001: 2 010: 4 011: 32 100: 64 101: 256 110: 512 111: 2048 (recommended)				
28h	**regref2_ctrl0**	update_rate2[2:0]			RSVD	rregrefDAC2_init[1:0]		regref_wait2[1:0]		00000000	R/W
		DAC update rate (12.5 MHz clock cycles) 000: No updates 001: 8 010: 512 (recommended) 011: 1024 100: 2048 101: 4096 110: 8192 111: 16374 (equiv. to 1.31 ms)			RSVD	Initial value of DAC output for *IOUT2* 01b recommended 00: 0 01: previous value 10: value contained in regref2_dac[8:0] 11: 0		Wait states after I_ON before enabling counting (IDAC current is fixed to initial value - this is not impacted by PWM or MPG) 00: no wait 01: ~20usec 10: ~100usec 11: ~200usec			
29h	**regref1_dac_MSB**	RSVD							regref1_dac[8]	00000000	R/W
		RSVD							REGREF DAC output for *IOUT1*, MSB		
2Ah	**regref1_dac**	regref1_dac[7:0]								00000000	R/W
		REGREF DAC output for *IOUT1*									
2Bh	**regref1_ctrl1**	headroom1[4:0]					regref1_dec[2:0]			00000000	R/W
		Controls headroom for *IOUT1* 00000: 0 mV 00001:10 mV 00010:20 mV 00011:30 mV …. 11111:310 mV (recommended)					Select decimation factor for REGREF digital loop: 000: 1 001: 2 010: 4 011: 32 100: 64 101: 256 110: 512 111: 2048 (recommended)				

Table 3-1. M08888 Registers

Addr	Register name	d7	d6	d5	d4	d3	d2	d1	d0	Default	Type
2Ch	**regref1_ctrl0**	update_rate1[2:0]			RSVD	rregrefDAC1_init[1:0]		regref_wait1[1:0]		00000000	R/W
		DAC update rate (12.5 MHz clock cycles) 000: No updates 001: 8 010: 512 011: 1024 100: 2048 101: 4096 110: 8192 111: 16374 (equiv. to 1.31 ms)			RSVD	Initial value of DAC output for *IOUT1* 00: 0 01: previous value 10: value contained in regref1_dac[8:0] 11: 0		Wait states after I_ON before enabling counting (IDAC current is fixed to initial value - this is not impacted by PWM or MPG) 00: no wait 01: ~20usec 10: ~100usec 11: ~200usec			
2Dh	**regref0_dac_MSB**	RSVD							regref0_dac[8]	00000000	R/W
		RSVD							REGREF DAC output for *IOUT0*, MSB		
2Eh	**regref0_dac**	regref0_dac[7:0]								00000000	R/W
		REGREF DAC output for *IOUT0*									
2Fh	**regref0_ctrl1**	headroom0[4:0]						regref0_dec[2:0]		00000000	R/W
		Controls headroom for *IOUT0* 00000: 0 mV 00001:10 mV 00010:20 mV 00011:30 mV …. 11111:310 mV						Select decimation factor for REGREF digital loop: 000: 1 001: 2 010: 4 011: 32 100: 64 101: 256 110: 512 111: 2048 (recommended)			
30h	**regref0_ctrl0**	update_rate0[2:0]			RSVD	rregrefDAC0_init[1:0]		regref_wait0[1:0]		00000000	R/W
		DAC update rate (12.5 MHz clock cycles) 000: No updates 001: 8 010: 512 (recommended) 011: 1024 100: 2048 101: 4096 110: 8192 111: 16374 (equiv. to 1.31 ms)			RSVD	Initial value of DAC output for channel 0 01b recommended 00: 0 01: previous value 10: value contained in regref0_dac[8:0] 11: 0		Wait states after I_ON before enabling counting (IDAC current is fixed to initial value - this is not impacted by PWM or MPG) 00: no wait 01: ~20usec 10: ~100usec 11: ~200usec			

Table 3-1. M08888 Registers

Addr	Register name	d7	d6	d5	d4	d3	d2	d1	d0	Default	Type
31h	**alarm_idac2**	alarm_th2[7:0]								11111111	R/W
		Alarm threshold for *IOUT2* (output DAC MSB)									
32h	**alarm_idac1**	alarm_th1[7:0]								11111111	R/W
		Alarm threshold for *IOUT1* (output DAC MSB)									
33h	**alarm_idac0**	alarm_th0[7:0]								11111111	R/W
		Alarm threshold for *IOUT0* (output DAC MSB)									
	APC REGISTERS										
34h	**apc_ctrl**	apc_clk	loop_select	apc2_ch		apc1_ch		apc0_ch		01111111	R/W
		CPC clock 1: Use external clock input (CLK_IN) 0: use internal oscillator	Selects APC type: 1: CPC 0: IPC	Selects APC input for *IOUT2* 00: *APC_IN0* 01: *APC_IN1* 10: *APC_IN2* 11: disable APC		Selects APC input for *IOUT1* 00: *APC_IN0* 01: *APC_IN1* 10: *APC_IN2* 11: disable APC		Selects APC input for *IOUT0* 00: *APC_IN0* 01: *APC_IN1* 10: *APC_IN2* 11: disable APC			
35h	**target2_msb**	RSVD			target2[12:8]					00000000	R/W
		RSVD			MSB target DAC for gain of *IOUT2*						
36h	**target2_lsb**	target2[7:0]								00000000	R/W
		LSB target DAC for gain of *IOUT2*									
37h	**target1_msb**	RSVD			target1[12:8]					00000000	R/W
		RSVD			MSB target DAC for gain of *IOUT1*						
38h	**target1_lsb**	target1[7:0]								00000000	R/W
		LSB target DAC for gain of *IOUT1*									
39h	**target0_msb**	RSVD			target0[12:8]					00000000	R/W
		RSVD			MSB target DAC for gain of *IOUT0*						
3Ah	**target0_lsb**	target0[7:0]								00000000	R/W
		LSB target DAC for gain of *IOUT0*									
3Bh	**target2_msb_LP**	RSVD			target2_LP[12:8]					00000000	R/W
		RSVD			MSB target DAC for gain of *IOUT2* when $\overline{\text{LP\_MODE}}$=L						
3Ch	**target2_lsb_LP**	target2_LP[7:0]								00000000	R/W
		LSB target DAC for gain of *IOUT2* when $\overline{\text{LP\_MODE}}$=L									
3Dh	**target1_msb_LP**	RSVD			target1_LP[12:8]					00000000	R/W
		RSVD			MSB target DAC for gain of *IOUT1* when $\overline{\text{LP\_MODE}}$=L						
3Eh	**target1_lsb_LP**	target1_LP[7:0]								00000000	R/W
		LSB target DAC for gain of *IOUT1* when $\overline{\text{LP\_MODE}}$=L									

Table 3-1. M08888 Registers

Addr	Register name	d7	d6	d5	d4	d3	d2	d1	d0	Default	Type
3Fh	**target0_msb_LP**	RSVD			target0_LP[12:8]					00000000	R/W
		RSVD			MSB target DAC for gain of *IOUT0* when $\overline{\text{LP\_MODE}}$=L						
40h	**target0_lsb_LP**	target0_LP[7:0]								00000000	R/W
		LSB target DAC for gain of *IOUT0* when $\overline{\text{LP\_MODE}}$=L									
		CPC REGISTERS									
41h	**apc2_ctrl2**	Tck_init2[1:0]		Tck_mid2[1:0]		Tck_min2[1:0]		Tck_div2[1:0]		00000000	R/W
		Initial clock count for *IOUT2* 00: 0 01: 63 10: 127 11: 255		Mid clock count for *IOUT2* 00: 0 01: 31 10: 63 11: 127		Clock counts for *IOUT2* at min step 00: 0 01: 31 10: 63 11: 127		Clock counts to enable clock divider for *IOUT2* 00: 0 01: 63 10: 127 11: 255			
42h	**apc2_ctrl1**	Step_init2[1:0]		Step_mid2[1:0]		iturnon2		ck_div2[1:0]		00000000	R/W
		Initial step size in LSB of *IOUT2* 00: 1 01: 8 10: 16 11: 32		Mid step size in LSB of *IOUT2* 00: 1/2 of Step_init 01: 1/4 of Step_init 10: reserved 11: reserved		Initial value of *IOUT2* 00: 0 01: previous value 10: value contained in bit iout2[9:0] 11: 0		Clock divider for *IOUT2* 00: 1 01: 4 10: 8 11: 16			
43h	**apc2_ctrl0**	Dec2[2:0]			RSVD	line_mode2	cpc_wait2[1:0]		apc2_freeze	00000000	R/W
		Digital filter decimation factor for *IOUT2*: 000: 1 001: 2 010: 4 011: 8 100: 16 101: 32 110: 64 111: 128			RSVD	Line mode for *IOUT2* 1: OUT2 on only during CLK_IN=H 0: Ignore CLK_IN	Wait states before enabling APC (current is fixed to initial value) 00: no wait 01: ~20usec 10: ~100usec 11: ~200usec		1: freeze APC for *IOUT2* 0: normal operation		
44h	**apc1_ctrl2**	Tck_init1[1:0]		Tck_mid1[1:0]		Tck_min1[1:0]		Tck_div1[1:0]		00000000	R/W
		Initial clock count for *IOUT1* 00: 0 01: 63 10: 127 11: 255		Mid clock count for *IOUT1* 00: 0 01: 31 10: 63 11: 127		Clock counts for *IOUT1* at min step 00: 0 01: 31 10: 63 11: 127		Clock counts to enable clock divider for *IOUT1* 00: 0 01: 63 10: 127 11: 255			

Table 3-1. M08888 Registers

Addr	Register name	d7	d6	d5	d4	d3	d2	d1	d0	Default	Type
45h	**apc1_ctrl1**	Step_init1[1:0]		Step_mid1[1:0]		iturnon1		ck_div1[1:0]		00000000	R/W
		Initial step size in LSB of *IOUT1* 00: 1 01: 8 10: 16 11: 32		Mid step size in LSB of *IOUT1* 00: 1/2 of Step_init 01: 1/4 of Step_init 10: reserved 11: reserved		Initial value of *IOUT1* 00: 0 01: previous value 10: value contained in bit iout1[9:0] 11: 0		Clock divider for *IOUT1* 00: 1 01: 4 10: 8 11: 16			
46h	**apc1_ctrl0**	Dec1[2:0]			RSVD	line_mode1	cpc_wait1[1:0]		apc1_freeze	00000000	R/W
		Digital filter decimation factor for *IOUT1*: 000: 1 001: 2 010: 4 011: 8 100: 16 101: 32 110: 64 111: 128			RSVD	Line mode for *IOUT1* 1: OUT1 on only during CLK_IN=H 0: Ignore CLK_IN	Wait states before enabling APC (current is fixed to initial value) 00: no wait 01: ~20usec 10: ~100usec 11: ~200usec		1: freeze APC (both gain and offset) for *IOUT1* : normal operation		
47h	**apc0_ctrl2**	Tck_init0[1:0]		Tck_mid0[1:0]		Tck_min0[1:0]		Tck_div0[1:0]		00000000	R/W
		Initial clock count for *IOUT0* 00: 0 01: 63 10: 127 11: 255		Mid clock count for *IOUT0* 00: 0 01: 31 10: 63 11: 127		Clock counts for *IOUT0* at min step 00: 0 01: 31 10: 63 11: 127		Clock counts to enable clock divider for *IOUT0* 00: 0 01: 63 10: 127 11: 255			
48h	**apc0_ctrl1**	Step_init0[1:0]		Step_mid0[1:0]		iturnon0		ck_div0[1:0]		00000000	R/W
		Initial step size in LSB of *IOUT0* 00: 1 01: 8 10: 16 11: 32		Mid step size in LSB of *IOUT0* 00: 1/2 of Step_init 01: 1/4 of Step_init 10: reserved 11: reserved		Initial value of *IOUT0* 00: 0 01: previous value 10: value contained in bit *iout0*[9:0] 11: 0		Clock divider for *IOUT0* 00: 1 01: 4 10: 8 11: 16			

Table 3-1. M08888 Registers

Addr	Register name	d7	d6	d5	d4	d3	d2	d1	d0	Default	Type
49h	**apc0_ctrl0**	Dec0[2:0]			RSVD	line_mode0	cpc_wait0[1:0]		apc0_freeze	00000000	R/W
		Digital filter decimation factor for *IOUT0*: 000: 1 001: 2 010: 4 011: 8 100: 16 101: 32 110: 64 111: 128			RSVD	Line mode for *IOUT0* 1: OUT0 on only during CLK_IN=H 0: Ignore CLK_IN	Wait states before enabling APC (current is fixed to initial value) 00: no wait 01: ~20usec 10: ~100usec 11: ~200usec		1: freeze APC (both gain and offset) for *IOUT0* 0: normal operation		
		IPC REGISTERS									
4Ah	**ipc_setup**	pfet_test	RSVD	mirror ratio	source_sink	pd_pre-charge2	pd_pre-charge1	pd_pre-charge0	pre_chrg	00000000	
		1: Enable test mode for pfet mirror 0: Normal operation	RSVD	1: 1:1 mir-roring ratio 0: 4x mir-roring ratio	1: Current sinking MPD (pfet input stage) 0: Normal MPD	1: power down pre-charge for *APC_IN2* 0: Normal operation	1: power down pre-charge for *APC_IN1* 0: Normal operation	1: power down pre-charge for *APC_IN0* 0: Normal operation	1: always ON 0: Depends on channel being turned on		
4Bh	**ipc2_ctrl2**	RSVD	pd_comp	RSVD	pd_ihelp2	cap2_sel[3:0]				00000001	R/W
		RSVD	1: Power down com-parator 0: Normal operation	RSVD	Powers down 100 µA helper current : 1: Power down 0: Normal operation	IPC2 charging capacitor value selector 0000 := 25.0 pF 0001 := 27.5 pF 0010 := 30.0 pF .... 1111 := 62.5 pF					
4Ch	**ipc2_ctrl1**	RSVD			ipd2_sel[4:0]					00000000	R/W
		RSVD			Peak amplitude monitor photodetector 00000 = 100 µA 00001 = 200 µA .... 11111 = 3.2 mA						

Table 3-1. M08888 Registers

Addr	Register name	d7	d6	d5	d4	d3	d2	d1	d0	Default	Type
4Dh	**ipc2_ctrl0**	RSVD			ich2_sel[4:0]					00000000	R/W
		RSVD			Peak current into IPC2 charging capacitor 00000 = 10 µA 00001 = 20 µA …. 11111 = 320 µA						
4Eh	**ipc1_ctrl2**	RSVD	pd_comp	hs_sel	pd_ihelp1	cap1_sel[3:0]				00000001	R/W
		RSVD	1: Power down comparator 0: Normal operation	1:Increase comparator bias current by 66% 0: Normal operation	Powers down 100 µA helper current : 1: Power down 0: Normal operation	IPC1 charging capacitor value selector 0000 := 25.0 pF 0001 := 27.5 pF 0010 := 30.0 pF …… …… 1111 := 62.5 pF					
4Fh	**ipc1_ctrl1**	RSVD			ipd1_sel[4:0]					00000000	R/W
		RSVD			Peak amplitude monitor photodetector 00000 = 100 µA 00001 = 200 µA …. 11111 = 3.2 mA						
50h	**ipc1_ctrl0**	RSVD			ich1_sel[4:0]					00000000	R/W
		RSVD			Peak current into IPC1 charging capacitor 00000 = 10 µA 00001 = 20 µA …. 11111 = 320 µA						
51h	**ipc0_ctrl2**	RSVD	pd_comp	hs_sel	pd_ihelp0	cap0_sel[3:0]				00000001	R/W
		RSVD	1: Power down comparator 0: Normal operation	1:Increase comparator bias current by 66% 0: Normal operation	Powers down 100 µA helper current : 1: Power down 0: Normal operation	IPC0 charging capacitor value selector 0000 := 25.0 pF 0001 := 27.5 pF 0010 := 30.0 pF …… …… 1111 := 62.5 pF					

Table 3-1. M08888 Registers

Addr	Register name	d7	d6	d5	d4	d3	d2	d1	d0	Default	Type
52h	**ipc0_ctrl1**	RSVD			ipd0_sel[4:0]					00000000	R/W
		RSVD			Peak amplitude monitor photodetector 00000 = 100 µA 00001 = 200 µA …. 11111 = 3.2 mA						
53h	**ipc0_ctrl0**	RSVD			ich0_sel[4:0]					00000000	R/W
		RSVD			Peak current into IPC0 charging capacitor 00000 = 10 µA 00001 = 20 µA …. 11111 = 320 µA						
TIMER REGISTERS											
54h	**clk_div**	clk_div_pwm[3:0]				clk_div_mpg[3:0]				00000000	R/W
		PWM clock divider 0000 = 1 0001 = 2 0010 = 4 0011 = 8 0100 = 16 0101 = 32 0110 = 64 0111 = 128				MPG clock divider 0000 = 1 0001 = 2 0010 = 4 0011 = 8 0100 = 16 0101 = 32 0110 = 64 0111 = 128					
55h	**pwm_msb**	RSVD		on_count2[9:8]		on_count1[9:8]		on_count0[9:8]		00000000	R/W
		RSVD		PWM *IOUT2* (msb)		PWM *IOUT1* (msb)		PWM *IOUT0* (msb)			
56h	**pwm2**	on_count2[7:0]								00000000	R/W
		PWM on count for *IOUT2*									
57h	**pwm1**	on_count1[7:0]								00000000	R/W
		PWM on count for *IOUT1*									
58h	**pwm0**	on_count0[7:0]								00000000	R/W
		PWM on count for *IOUT0*									
59h	**mpg_off_msb**	RSVD		pulse_off2[9:8]		pulse_off1[9:8]		pulse_off0[9:8]		00000000	R/W
		RSVD		MPG off *IOUT2* (msb)		MPG off *IOUT1* (msb)		MPG off *IOUT0* (msb)			
5Ah	**mpg_off2**	pulse_off2[7:0]								00000000	R/W
		MPG pulse off for *IOUT2*									
5Bh	**mpg_off1**	pulse_off1[7:0]								00000000	R/W
		MPG pulse off for *IOUT1*									

Table 3-1. M08888 Registers

Addr	Register name	d7	d6	d5	d4	d3	d2	d1	d0	Default	Type
5Ch	**mpg_off0**	pulse_off0[7:0]								00000000	R/W
		MPG pulse off for *IOUT0*									
5Dh	**mpg_on_msb**	RSVD		pulse_on2[9:8]		pulse_on1[9:8]		pulse_on0[9:8]		00000000	R/W
		RSVD		MPG on *IOUT2* (msb)		MPG on *IOUT1* (msb)		MPG on *IOUT0* (msb)			
5Eh	**mpg_on2**	pulse_on2[7:0]								00000000	R/W
		MPG pulse on for *IOUT2*									
5Fh	**mpg_on1**	pulse_on1[7:0]								00000000	R/W
		MPG pulse on for *IOUT1*									
60h	**mpg_on0**	pulse_on0[7:0]								00000000	R/W
		MPG pulse on for *IOUT0*									
61h	**start_op**	RSVD							start_op	00h	R/W
		RSVD							1b: Start operation 0b: Not operational Note: M08888 will not be operational until 1b is written		
62h	**soft_reset**	Soft reset								00000000	R
		Writing AA causes a 16 refclk cycles to reset (self clear after reset)									
63h	**chip_id**	Revision identification:				Chip identification				00001100	R
		0000				1100					
64h	**temp**	temp[7:0]								00000000	R
		Temperature readback									
65h	**rb_iout2_msb**	RSVD						rb_iout2[9:8]		00000000	R
		RSVD						Readback *IOUT2* DAC MSB			
66h	**rb_iout2_lsb**	rb_iout2[7:0]								00000000	R
		Readback *IOUT2* DAC LSB									
67h	**rb_regrefdac2_MSB**	RSVD							rb_regrefdac2[8]	00000000	R
		RSVD							Readback of *IOUT2* DAC		
68h	**rb_regrefdac2**	rb_regrefdac2[7:0]								00000000	R
		Readback of *IOUT2* DAC.									
69h	**rb_iout1_msb**	RSVD						rb_iout1[9:8]		00000000	R
		RSVD						Readback *IOUT1* DAC MSB			

Table 3-1. M08888 Registers

Addr	Register name	d7	d6	d5	d4	d3	d2	d1	d0	Default	Type
6Ah	**rb_iout1_lsb**	rb_iout1[7:0]								00000000	R
		Readback *IOUT1* DAC LSB									
6Bh	**rb_regrefdac1_MSB**	RSVD							rb_regref-dac1[8]	00000000	R
		RSVD							Readback of *IOUT1* DAC		
6Ch	**rb_regrefdac1**	rb_regrefdac1[7:0]								00000000	R
		Readback of *IOUT1* DAC.									
6Dh	**rb_iout0_msb**	RSVD						rb_iout0[9:8]		00000000	R
		RSVD						Readback *IOUT0* DAC MSB			
6Eh	**rb_iout0_lsb**	rb_iout0[7:0]								00000000	R
		Readback *IOUT0* DAC LSB									
6Fh	**rb_regrefdac0_MSB**	RSVD							rb_regref-dac0[8]	00000000	R
		RSVD							Readback of *IOUT0* DAC		
70h	**rb_regrefdac0**	rb_regrefdac0[7:0]								00000000	R
		Readback of *IOUT0* DAC.									
71h	**alarm_ctrl**	alarm2	alarm1	alarm0	alarm_IDAC2	alarm_IDAC1	alarm_I-DAC0	N/A	N/A	00000000	R
		CPC alarm for *IOUT2*	Alarm for *IOUT1*	Alarm for *IOUT0*	Alarm for IDAC2	Alarm for IDAC1	Alarm for IDAC0	N/A	N/A		
72h	**alarm_iout**	IPC_over-shoot	RSVD				alarm_iout 2	alarm_iout 1	alarm_iout0	00000000	R
		Alarm for high MPD current	RSVD				Alarm for open or short on *IOUT2*	Alarm for open or short on *IOUT1*	Alarm for open or short on *IOUT0*		

Table 3-1. M08888 Registers

Addr	Register name	d7	d6	d5	d4	d3	d2	d1	d0	Default	Type
73h	**RSVD**	RSVD								00000000	R/W
		RSVD									
74h	**RSVD**	RSVD								00000000	R/W
		RSVD									

Table 3-1. M08888 Registers

Addr	Register name	d7	d6	d5	d4	d3	d2	d1	d0	Default	Type
75h	**strbalrm_ctrl**	RSVD			reg_spl_dis	RSVD		strb_iout	clear_alarm	00000000	R/W
		RSVD			Disables register sampling: 1: Disable register sampling (cannot read/write to any register except 68h) 0: Normal operation (all registers are accessible)	RSVD		1: strobes iout current before readback 0: Normal	1: Clear alam 0: Normal		
80h	**alarm_iout_mask**	alarm_iout_mask								11111111	R/W
		When 1 masks to 0 alarm bits in alarm_iout									